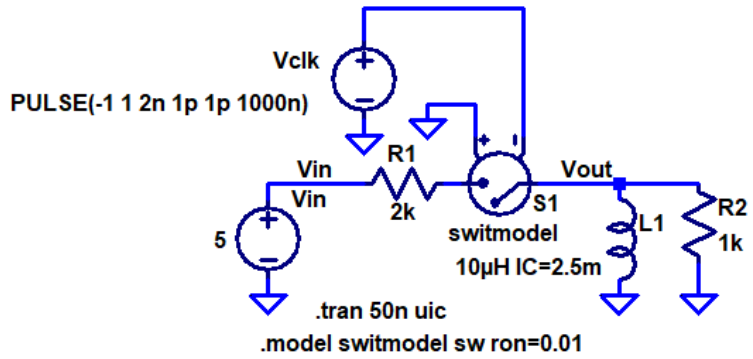
Practice Midterm Exam – EE 421 Digital Electronics and ECG 621 Digital IC Design
Fall – University of Nevada, Las Vegas

NAME: _____

Open book, closed notes.
Show your work for credit. When possible place boxes around your answers.

1. Plot the current through the inductor in the following circuit. (10 points)



2. What key binding is used to descend and edit a cell in Cadence? (5 points)

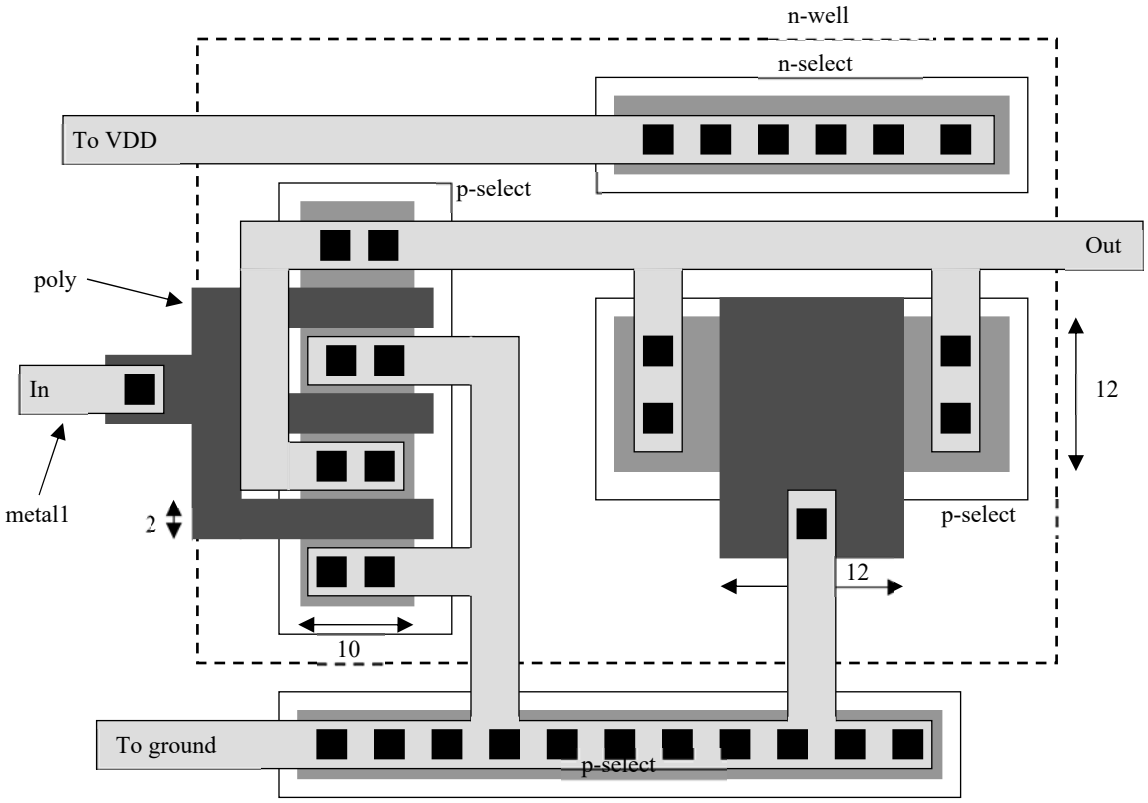
3. Estimate the delay through an n-well resistor having a sheet resistance of 1kohm/square and a zero-bias depletion capacitance of 100 fF/um^2. Assume the resistor is 100 um long and 2 um wide. (5 points)

4. Explain **in your own words** why depletion capacitance of a pn junction decreases with increasing reverse bias. Use a cross-sectional view of a pn junction showing the depletion region's width in your explanation. Also show a plot of the depletion capacitance against reverse bias. Do not use equations in your explanation. (15 points)

5. Work problem 3.5 on page 80. (10 points)

6. For problem 6.1 on page 162 determine the frequency when the AC component of the output voltage is 0.75 mV (3/4 of the input AC voltage). (20 points)

7. Sketch the corresponding schematic for the following layout. Make sure the body connections of the MOSFETs are clearly seen in your schematic. (15 points)



8. Sketch the layout of a 30k poly2 resistor in the C5 process using the hires layer assuming the sheet resistance is 1k/square. Make sure to label each of the layers in your layout. Sketch the cross-sectional view of your layout. Explain what the hires layer does during the fabrication process. (20 points)