UNIVERSITY OF NEVADA LAS VEGAS. DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

The Flyback Switching Power Supply

Design, Analysis and Implementation in the ONSEMI C5 Process

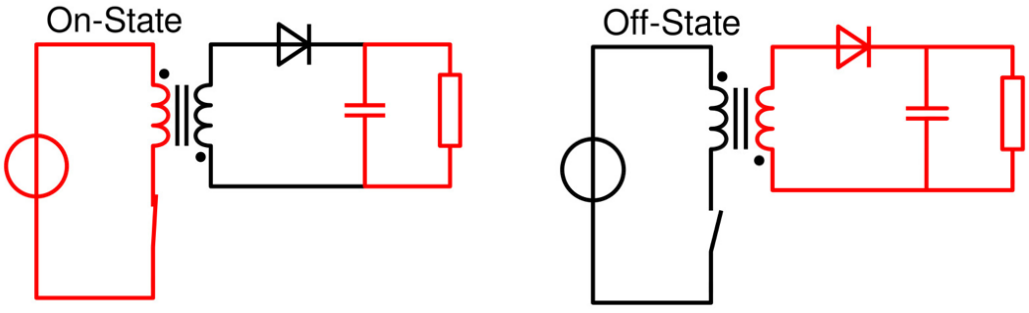
By Brian Wolak

1. Introduction / Theory of Operation

Since its development in the 30's and 40's the flyback power supply has been used in a vast array of charging applications from original vacuum tube power supplies to nearly all portable electronic devices in some form. This report will cover the basic operation, internal components, overall design and technical analysis through hand calculations and simulation modeling to provide a clear and concise device characterization.

The flyback power supply belongs to a family of devices known as mode switching power supplies. These devices operate by driving an off-chip transistor between the cutoff state and saturation state as quickly as possible. This transistor serves as the grounding device for the line voltage or wall power supply connection of the device. Voltage is sensed through a feedback loop and monitored by a comparative device to determine optimal switching and output demands. Once the switching signal is received the transistor rapidly switches modes hence the name "switching power supply" and the transistor enters saturation mode.

The flyback design differs from its other similarly transformer driven counterparts in that it also uses its transformer as an inductor to temporarily store magnetic energy. When in cutoff mode the transformer becomes separated from ground by the inactive transistor and begins storing electromagnetic energy to be immediately released upon transition to the saturation or charging mode. Again, once powered on, the transistor provides a ground to the transformer and the stored magnetic energy is released through the transformer to the output of the device. Below we can see the two modes associated with the on or "charging" state and the off or "sensing and storing" state.

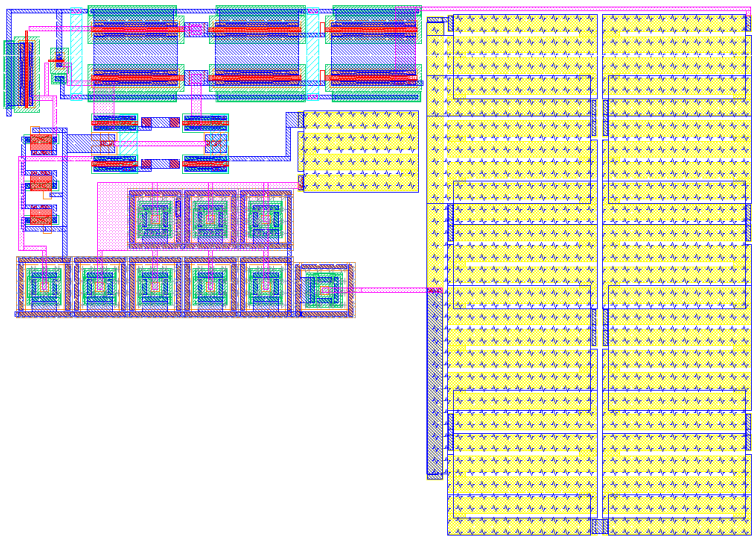


2. Description of Components

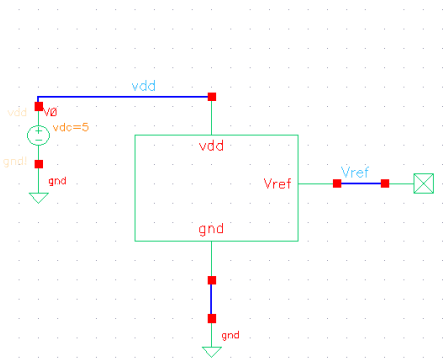
The flyback power supply operates with minimal components, but each component plays an integral part in the device's overall operation. Each component was designed independently using the C5 process and ran through strict design rule checks passing all DRC and LVS confirmations before being combined into the final circuit. This portion will cover the design of each component in the C5 process and their respective role in the device's operation as well as some of the important design considerations that must be evaluated with each.

The Bandgap Reference Supply

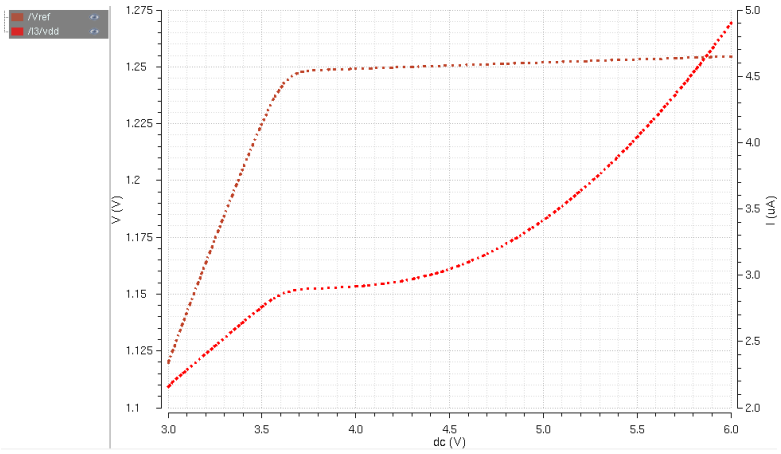
The heart of the flyback switching power supply begins in the bandgap reference circuit. This internal reference circuit serves as the 1.25V reference voltage that will be used in comparison to the output feedback voltage circuit. The bandgap circuit is designed to provide a constant 1.25V to the device's internal comparator circuit regardless of changes in temperature and VDD. Included below is a circuit design schematic, layout, as well as descriptive simulations showing proper operation of the bandgap circuit.



Bandgap Circuit Layout

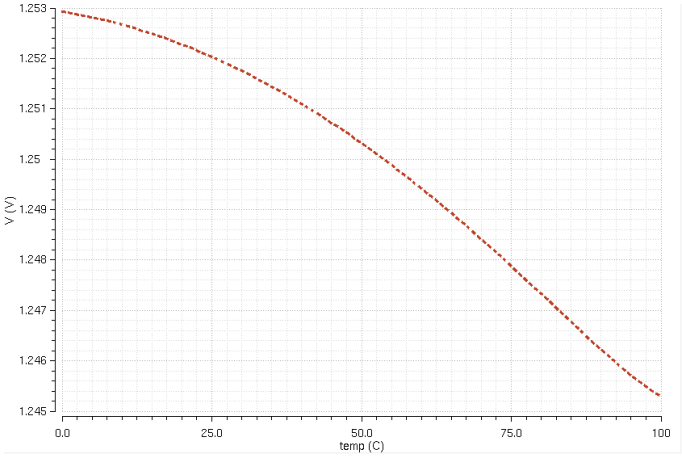


Bandgap Circuit Symbol



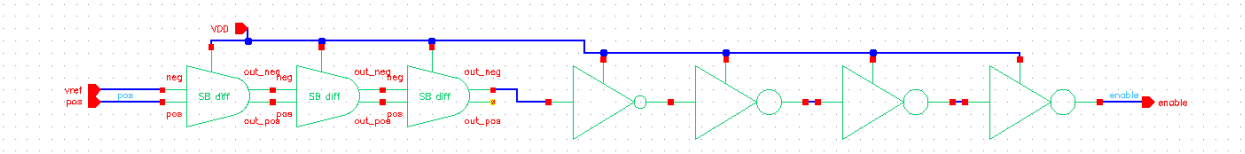
Bandgap Simulation #1: Plotting Change in VDD

In the simulation above we can see that as VDD voltage increases the 1.25V output of the bandgap circuit remains steady. In the simulation below we see that as temperature increases from 0^0 C to 100^0 C the bandgap circuit output only varies by 8mV making this reference supply very suitable for a wide range of applications.



Bandgap Simulation #2: Plotting Temperature Variance

The Comparator



Comparator Symbol

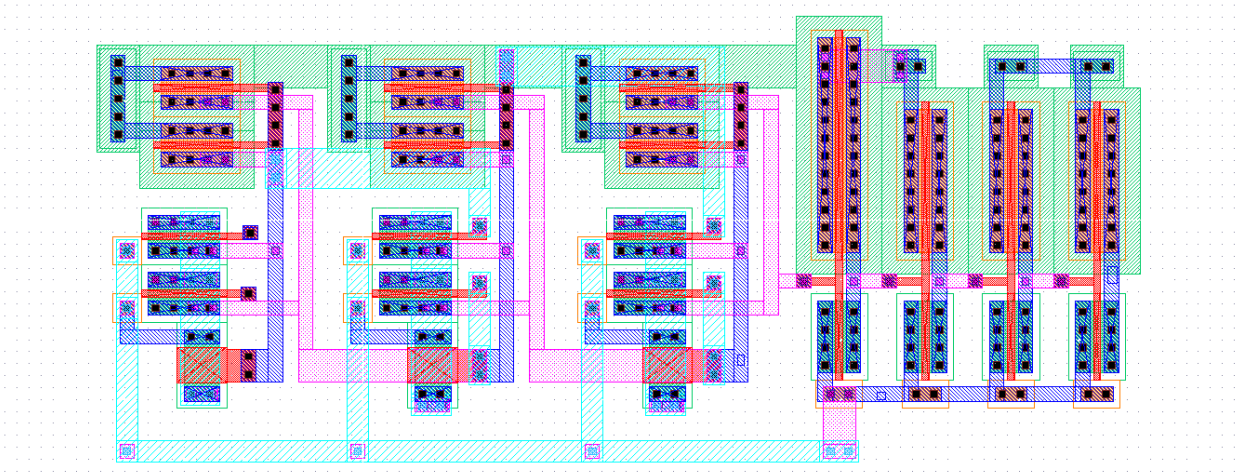
Moving on to the comparator circuit I will begin to set up concepts of logic into the design. The comparator is constructed by cascading three self-biasing differential amplifiers back-to-back. The differential amplifiers used within the comparator each use a combination of NMOS and PMOS devices to sense the difference between feedback voltage and bandgap reference circuit output voltage. When comparing the feedback voltage signal from the design's desired 12.5V out with the bandgap voltage, the comparator will output a logic 0 if Vout > 1.25V and output a logic 1 if Vout < 1.25V. To be sure we have proper comparison our feedback voltage will be ran through a simple voltage divider to reduce the 12.5V output to match the bandgap's 1.25V. Below are calculations for the voltage divider portion feeding the comparator.

$$V_{ref} = V_{fb}\frac{R_1}{R_1 + R_2} \rightarrow 12.5V * \frac{1k\Omega}{1k\Omega + 9k\Omega} = 1.25V$$

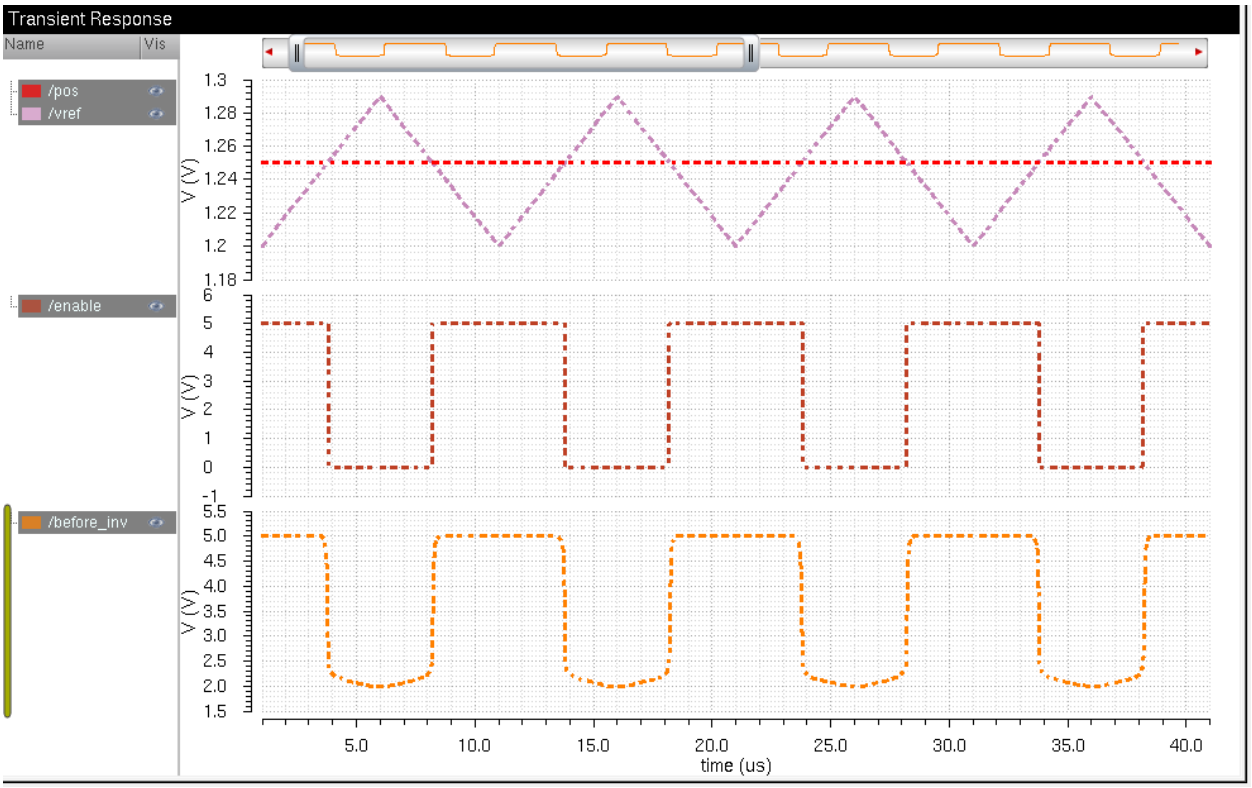
R_1 = 1k, R_2 = 9k

Each MOSFET size within the differential amplifier size was chosen out of simplicity for this design with a result of some noticeable disadvantages. Using a 10/1 (W/L) design within the differential amplifier devices causes a sacrifice in even switching points but in turn allows the design to using less overall power than larger sizes and reduces layout size. Following these three cascaded diff-amps will be a string of inverters used to clean up our logic signal. Simulations can

confirm that the added inverters, although taking up costly chip space, do in fact make a noticeable difference in comparator output signal which will be passed into the next component, the NAND gate. Below are layout views and simulation results showing the output signal improvement and overall operation of the comparator circuit.



Comparator Layout View



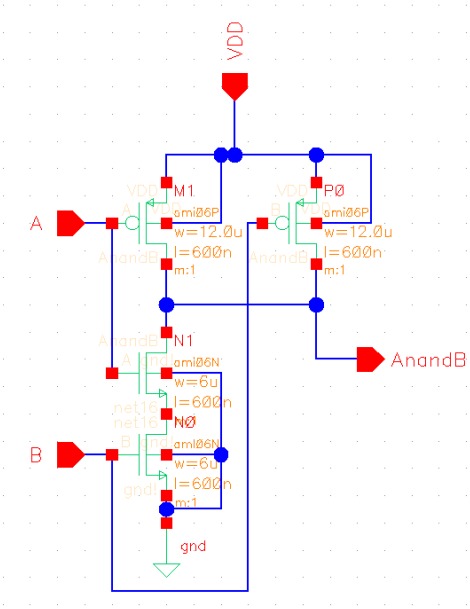
Comparator Simulation: Showing output before the inverters and after with a visibly cleaner logic signal. It should be noted that proper comparator operation can also be viewed here as the sensing voltage drops below bandgap voltage the device outputs a clean logic 1 enable signal and 0 when voltage is above the 1.25V bandgap voltage as expected.

The NAND Gate

Following the comparator is a single NAND gate responsible for controlling the oscillation frequency output and the comparator enable output signals. Among all the components within this design, this is by far the simplest. Building a simple NAND gate truth table, we get the following.

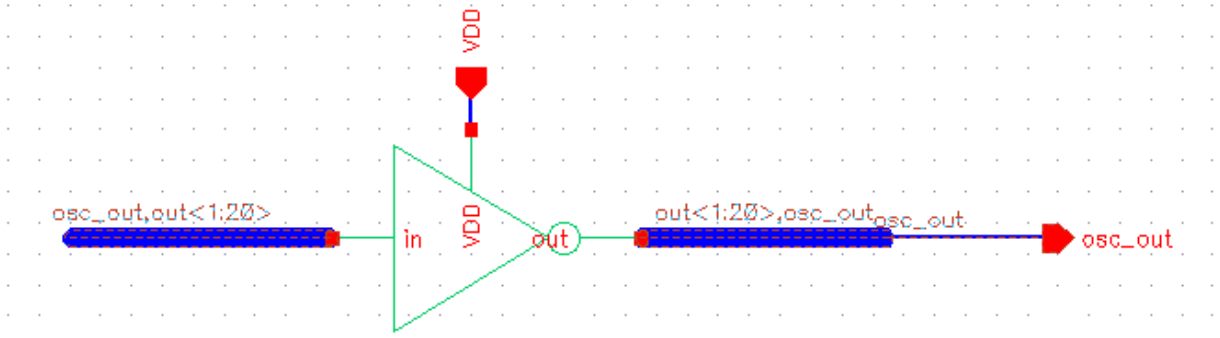
A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

Using this truth table you can see that it requires a high signal from the ring oscillator and high signal on the comparator enable to produce an output of zero. This would enable the off-stage or transformer charging stage in which magnetic energy is stored to be used once output voltage drops below 12.5V. When any other condition is met the NAND gate sends a logic high signal of varying frequency provided by the ring oscillator into the next device to prepare a final signal which will power the very large off-chip MOSFET mentioned just previously.



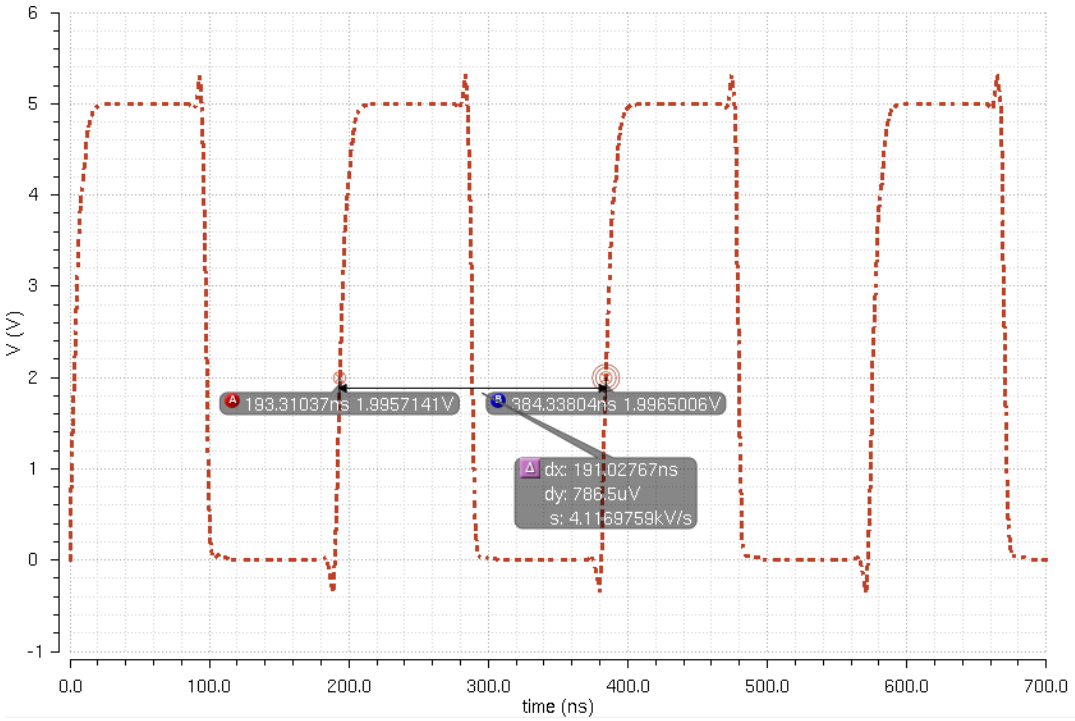
NAND Gate Circuit

The Ring Oscillator Circuit



Ring Oscillator Circuit Schematic using Cadence Symbol Notation

The ring oscillator circuit for my project was designed to operate near a 5MHz frequency and controls the duty cycle of the entire design. I chose to use 7.05/7.05 inverter sizes to keep my ring oscillator stages low and save in costly overall chip space, as well as to maintain design simplicity and unneeded additional added capacitances.



Ring Oscillator Simulation: plotting oscillation frequency

This goal in designing this device was an operation frequency of 5MHz. Using the above simulation results and following hand calculations, I determined my overall frequency to be 5.2Mhz. Calculations shown below.

$$f_{osc} = \frac{1}{T} = \frac{1}{191ns} = 5.2Mhz$$

Because the inverters are a 10/10 W/L ratio they are weak in design, but high in overall resistance leading to the requirement of less stages. It should be noted that these dimensions for an inverter are specific in my design to the oscillator only as they are only required to create and pass a clocked signal frequency. Resistance calculations are as shown below.

$$R_N = R'_N * \frac{L}{W} = R'_N = 20k\pi$$
$$R_P = R'_P * \frac{L}{W} = R'_P = 40k\pi$$

Hand calculations of device oscillation frequency were performed using C5 specific values as well as common MOSFET delay, frequency, and resistance formulas. With a stand C5 C'ox = 2.5fF/um^2, R'$_N$ = 20k, and R'$_P$ = 40k the following calculations were made.

$$C_{oxp} = C'_{ox} * W_P * L_P = 124fF$$
$$C_{oxn} = C'_{ox} * W_N * L_N = 124fF$$

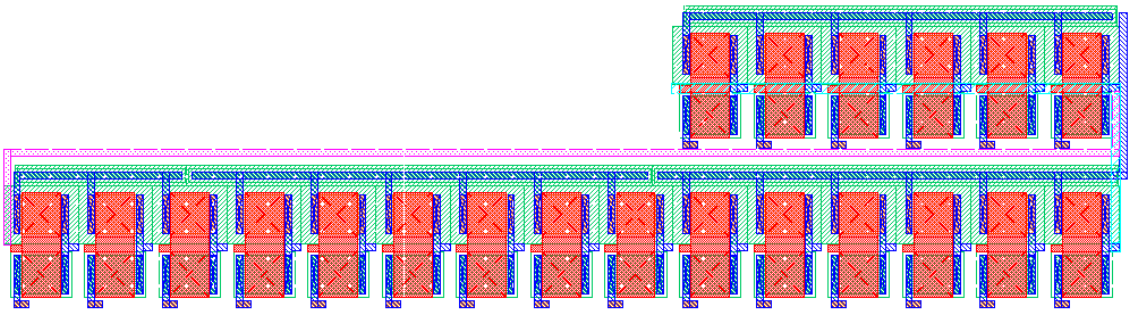
$$C_{tot} = \frac{5}{2}(C_{oxp} + C_{oxn}) = 621fF$$

$$\boldsymbol{t_{plh} = 0.7 * R_P * C_{tot}}$$
$$0.7 * 40k * 621fF = 17ns$$

$$\boldsymbol{t_{phl} = 0.7 * R_N * C_{tot}}$$
$$0.7 * 20k * 621fF = 8.6ns$$

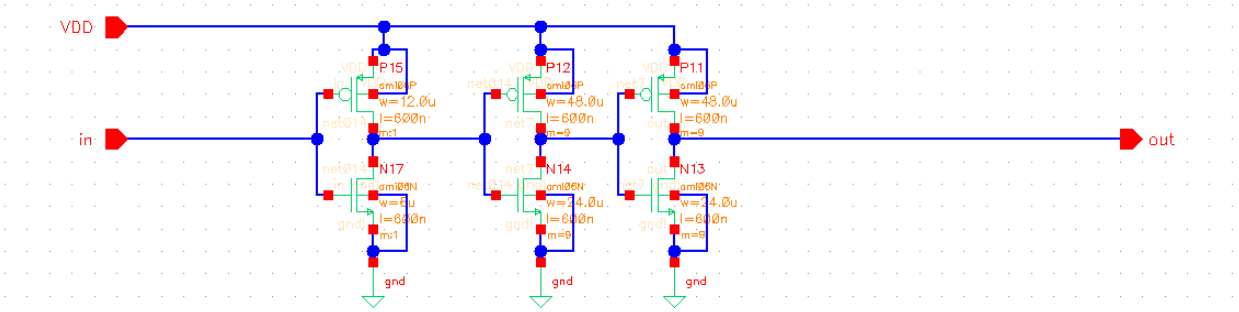
$$f_{osc} = \frac{1}{n(t_{plh}+t_{phl})}$$
$$f_{osc} = \frac{1}{21(25.6ns)} = 1.8\text{Mhz}$$

Upon review of the above hand calculations, I determined there to be a wide variance in how Candence simulations and the CMOS book calculate delay resistance and delay values, so I made a choice to carry on the remainder of the project with the simulation results and stay with the 7.05/7.05 sizes at 21 stages to remain consistent with the desired overall design outcome.



Ring Oscillator Layout: Displaying a folded design to save space

The Buffer



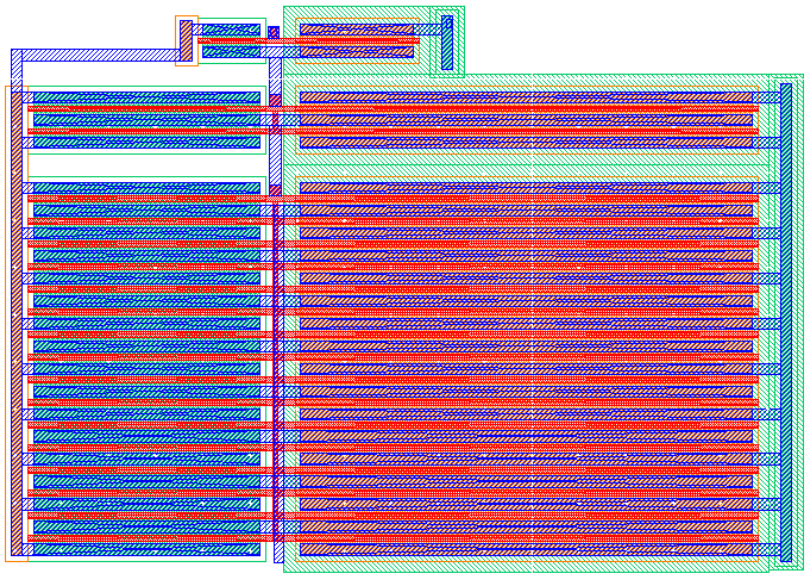
Buffer Schematic: showing three stages

The final device in my design is the buffer which drives a very large off-chip NMOS device responsible for grounding the transformer. Due to the extremely large size of this MOSFET it requires a very fast, strong signal to transition from cut-off to saturation mode. This transition must be as fast as possible to avoid any unnecessary power consumption and heat related effects which could lead to premature device failure.

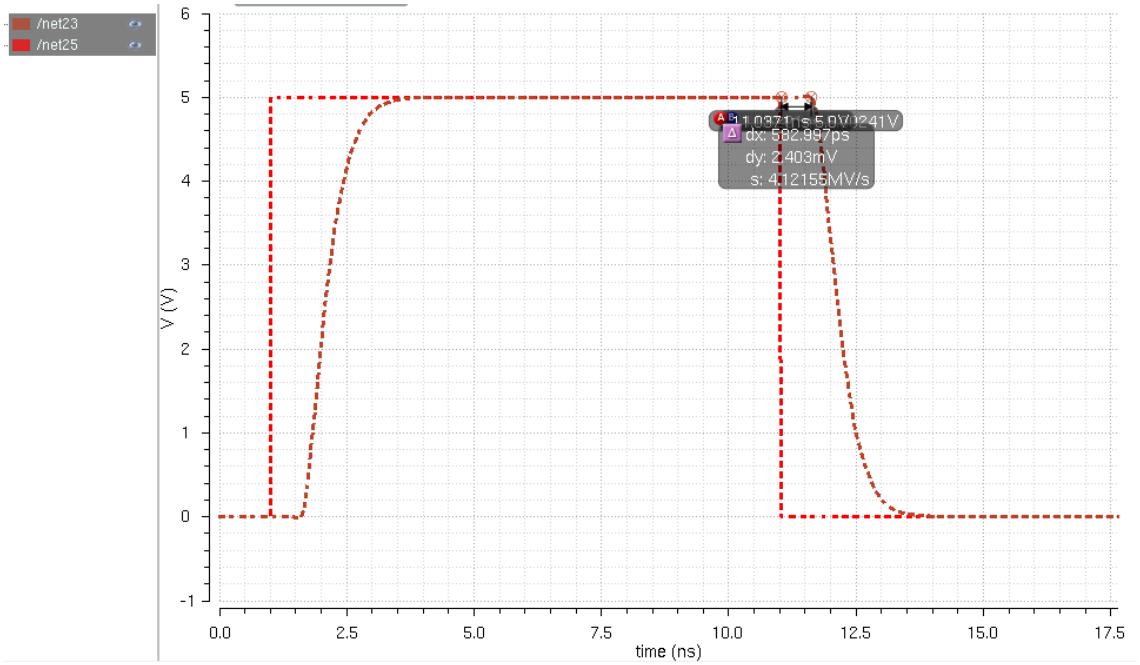
Careful decisions were made in choosing the MOSFET sizes for the buffer. The buffer needs to be strong and efficient in order to power the off-chip NMOS with minimum power loss. Load calculations for the NMOS were performed to determine the correct buffer sizing as follows below.

$$C_{load} = C'_{ox} * W_N * L_N$$
$$\frac{2.5fF}{um^2} * 10m * 1u = 25pF$$

My buffer design involved the use of three stages beginning at 12/6, followed by 48/24 with a multiplier of 2 and finally 48/24 with a multiplier of 16. Simulations were performed using a 37.5pF capacitor to simulate my chosen design's performance on driving the external NMOS load. Below are the simulation results showing the transition on time to be well within reason for a fast transition from cut-off to saturation.



Buffer Layout in C5 Cadence Process

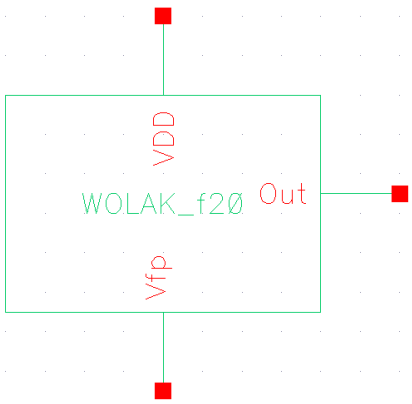


Buffer Simulation: Showing buffer transition time of approximately 1ns with 582ps delay

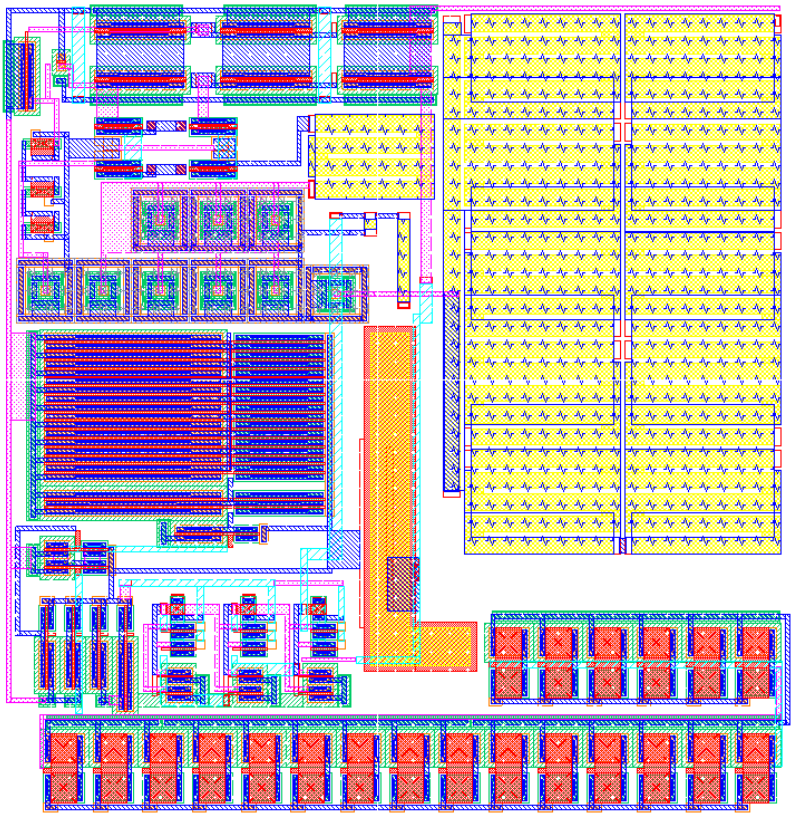
3. The Flyback SPS Assembled

Once all these components were individually designed laid out and tested for design rule compatibility using DRC and LVS checks, they were combined together to form the final product. Below are the final schematic, layout, symbol and extracted views.

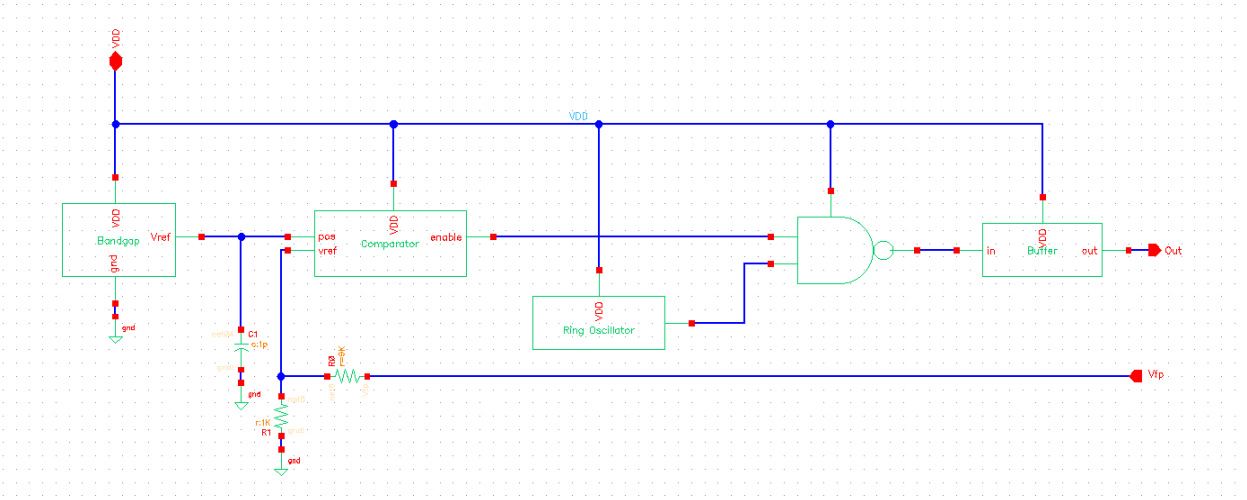
For my layout design I chose to maximize space and keep all components in a tight configuration. Extensive use of metal2 and metal3 layers allowed me to achieve a compact efficient footprint but does come with an associated cost of additional metal and via pricing. Had this been a production chip, the design may have been better suited with a lower cost model.



Final Symbol View

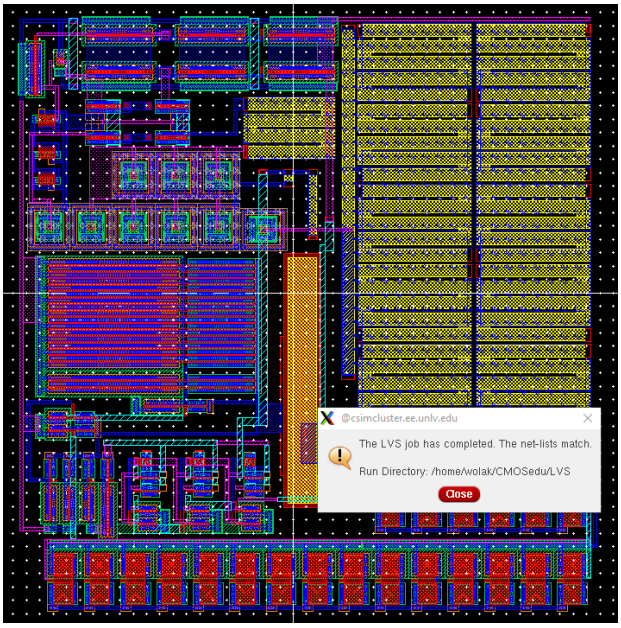


Final Master Layout

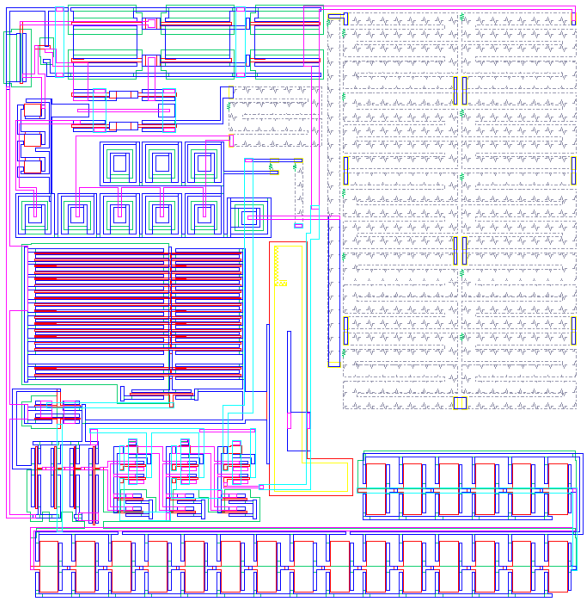


Final Master Layout using all Design Symbols

NOTE: The above schematic displays the importance of developing design symbols for each circuit in the overall layout for a cleaner and simplified schematic.



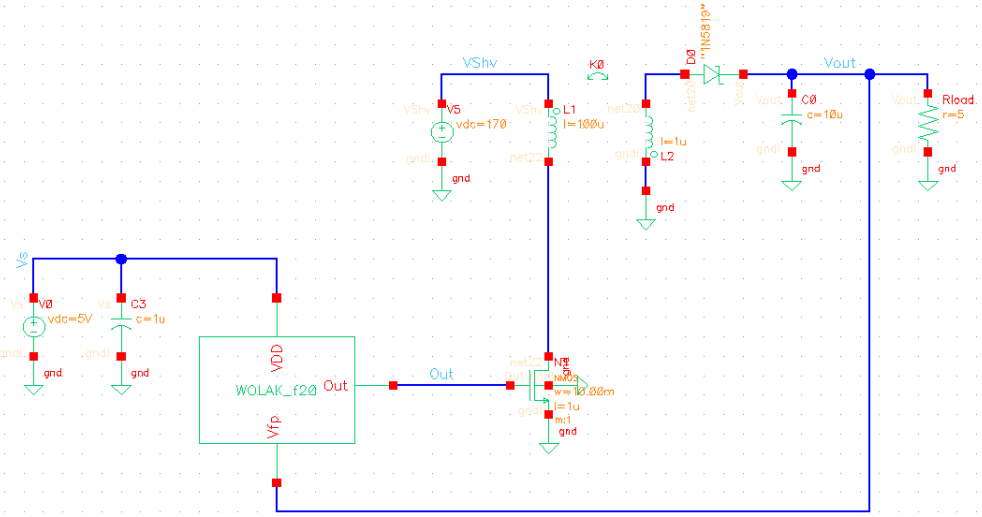
Master Layout Showing LVS Confirmation



Final Extracted View

4. Simulation and Testing

The final design was simulated under many conditions to provide a clear and concise conclusion on operation in variance of VDD, temperature, load resistance, power consumption and efficiency. Shown below is the test circuit created to model the power supply design and included after are results of each individual simulation with brief explanation.



Simulation Circuit Design using Project Symbol

My design was simulated to test the device's overall efficiency multiple times to achieve the most out of my buffer circuit as it struggled early on to power the massive off-chip NMOS device needed to ground the transformer. Below are formulas and results of these simulations.

Parametric Analysis of Varying Chip Temperature at 20Ω

Summary of Results at Temperature Variance					
Temp (^oC)	Avg(Vout)	Min(Vout)	Max(Vout)	V_{ripple}	Avg I(VDD)
27	12.5v	12.45v	12.56v	112mV	103.6mA
45.25	12.49	12.43	12.55	119mV	103.5mA
63.5	12.48	12.42	12.54	120mV	103.5mA
81.75	12.46	12.41	12.51	100mV	103.8mA
100	12.44	12.38	12.50	120mV	103.8mA

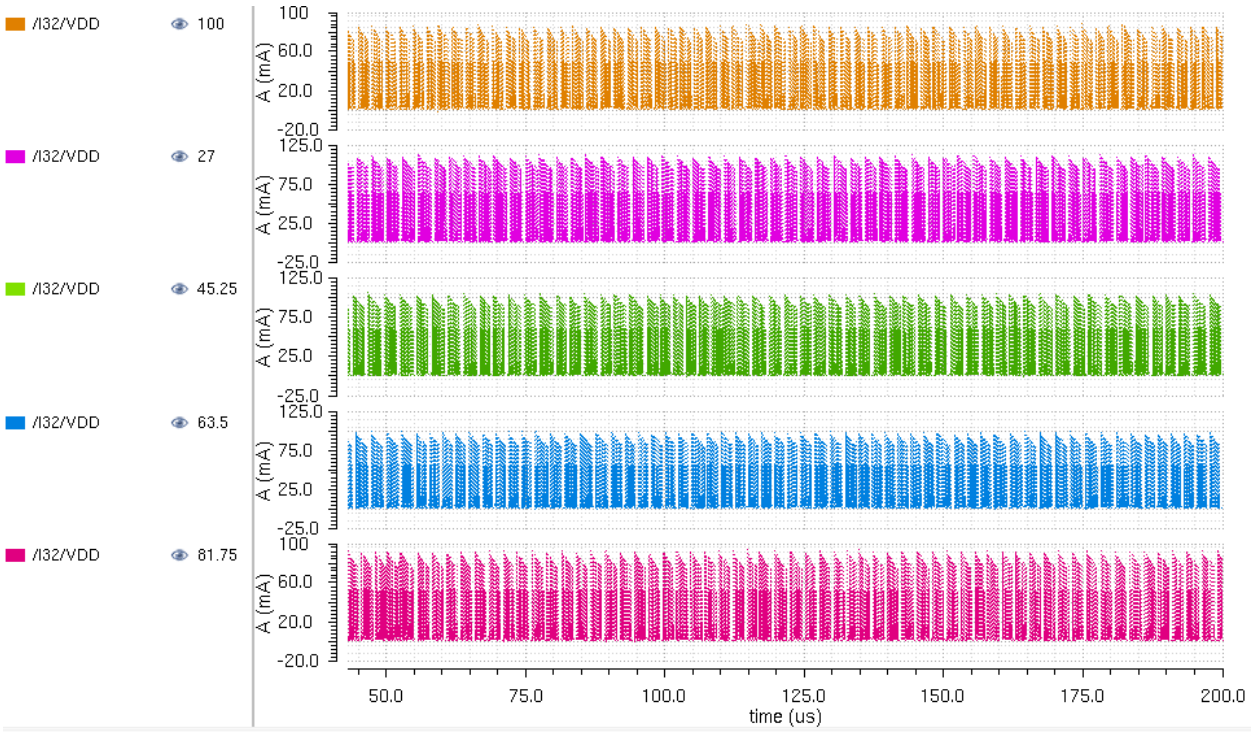
$$E = \frac{V_{out} * I_{load}}{V_{dd} * (avg(I(V_{dd}))}$$

Varying VDD Voltage at 10Ω

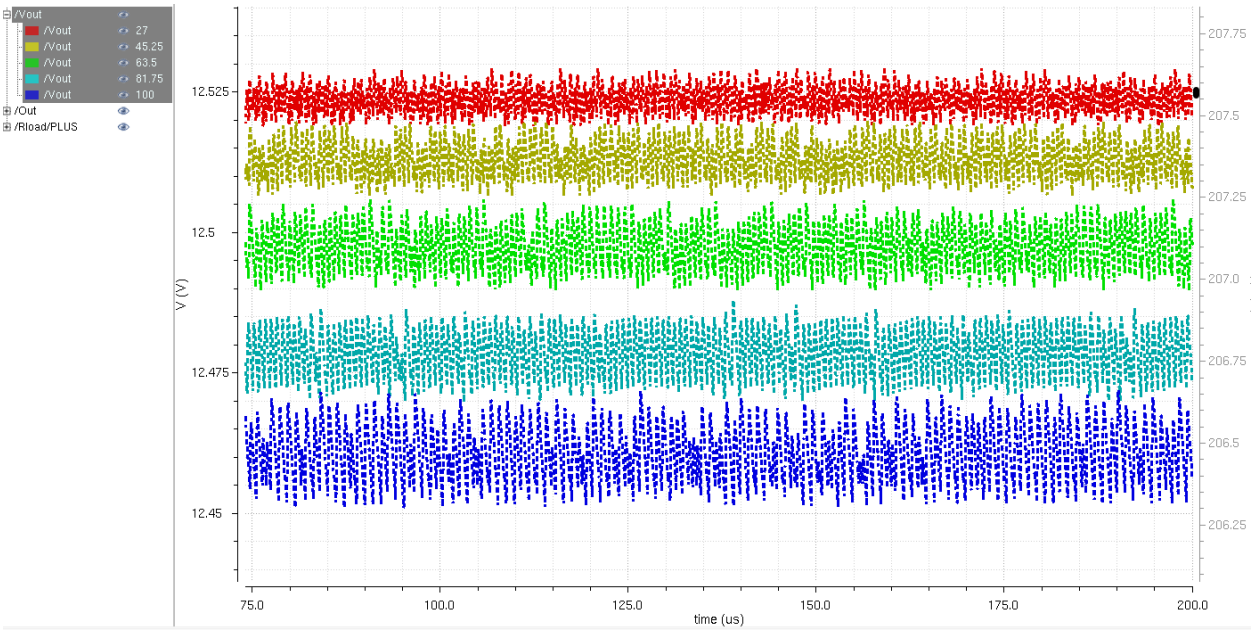
Summary of Results for Varying VDD				
VDD	Avg Vout	Min Vout (V)	Max Vout (V)	Vripple
4.0v	12.47	12.42	12.53	103mV
4.4v	12.48	12.43	12.54	109mV
4.8v	12.5	12.44	12.56	119mV
5.0v	12.5	12.44	12.56	119mV
5.2v	12.55	12.45	12.57	119mV
5.4v	12.52	12.46	12.57	116mV

Efficiency Determinations

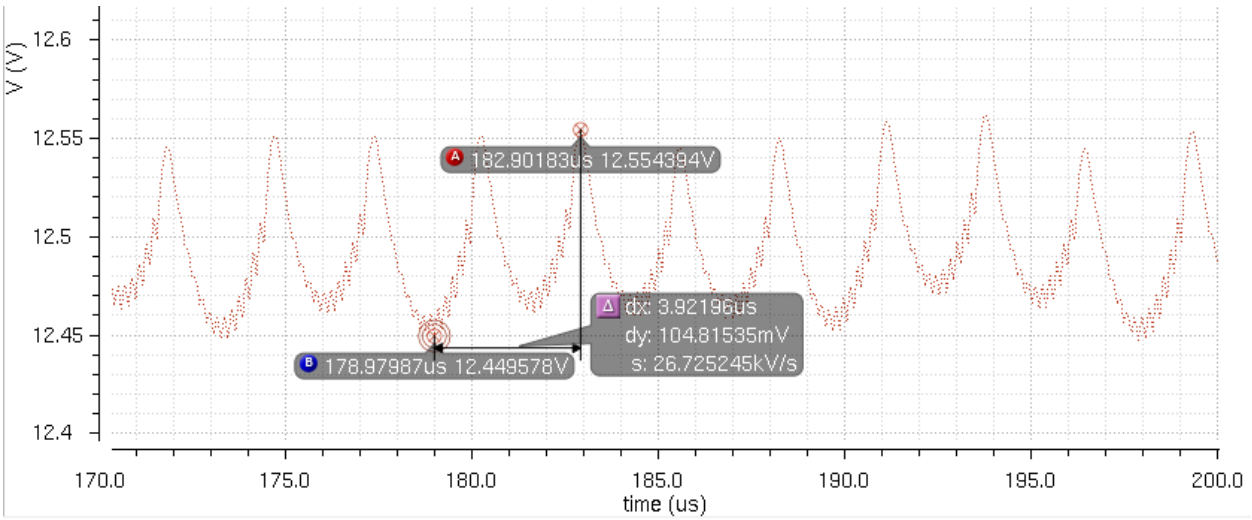
Summary of Results at Varying Load Resistance				
R_{load} (Ω)	**I(avg(170VDD))**	**I(avg(5VDD))**	**I_{load}**	**Efficiency**
2	538.8mA	1.65mA	6.25A	.83
5	243mA	1.60mA	2.5A	.75
10	150mA	1.7mA	1.25A	.61
15	119mA	1.76mA	830mA	.62
20	103mA	1.88mA	625mA	.45
25	94mA	2.1mA	500mA	.40



Temperature Variation Simulation: at VDD



Varying Temperature Simulation: Vout at 62.5ohms



Output Simulation at 10Ω Load

Overall, my device performed better at a slightly lower than usual 5V VDD voltage in the 5-20Ω load range. My output hysteresis lowered considerably to the 10-20mV range as the load resistance increased but output voltage began to creep past 12.5V. At a 100Ω load my output centered at 12.525V which means below 100mA the device displays a 2% variance in output voltage.

Temperature played a significant role in output voltage near 81.75^{o}C as seen above. The voltage dropped considerably below 12.5V and would fail to provide a consistent charge in this temperature range.

5. Conclusion

Although this design was my very first attempt at a switching power supply, it will certainly not be my last. Through the process I learned many lessons through research, trial and error. The most important of those are the trade-offs associated with designing a device. In devices like the comparator, I chose a smaller layout and design simplicity which led to reduced power consumption while understanding an associated sacrifice in delay and increasing resistance would follow. Again, in my oscillator I determined a sacrifice in greater power consumption due to the weak inverter design was well worth the reduced layout size and reduction in overall stages some of my classmates were struggling with. When it came to the buffer my design was atrocious in the beginning stages and received many remodels to achieve the high gain I was seeking through use of multipliers.

Due to the drop in efficiency as load resistance increases, more work could be done in making this device compatible at a wider range of amp ratings. This device could use further improvements with the use of a linear post regulator to filter the output ripple more effectively for an increase in output precision. Compared to linear voltage supplies, a mode switching supply produces more unwanted RF interference. With this in mind additional circuitry to filter RF and noise on the output would lead to a better design with yet again more precision.