The Boost Switching Power Supply

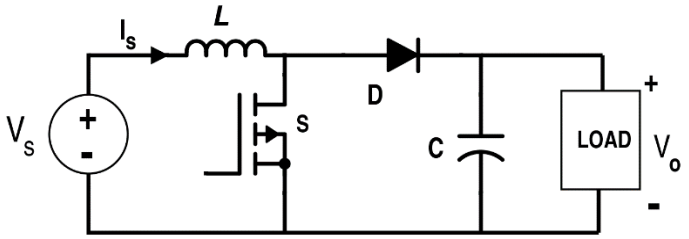
Design, Analysis and Implementation in the ONSEMI C5 Process

By Brian Wolak

1. Introduction / Theory of Operation

The boost switching power supply, or often times referred to as the boost switching converter, is one of three rather infamous electronic devices belonging to a family of devices known as switching mode power supplies (SMPS). These devices are far superior to linear voltage devices as they are smaller in size and weight, cut power consumption, and reduce heat dissipation. Nearly any electronic device currently in production uses some form of SMPS due to their high efficiency capabilities.

By definition mode switching power supplies are a type of power supply that use a semiconductor switching technique as opposed to previous linear technology. One of the biggest advantages yielded by the transition to SMPS over traditional linear models is the added step up or "boost" capability not previously available with linear methods. The two main components of a mode switching supply are a control circuit and power switching stage. The control circuit determines precise voltage control while the power switching stage performs the power conversion from a V_{IN} source to the V_{OUT} output.



Boost SMPS Circuit

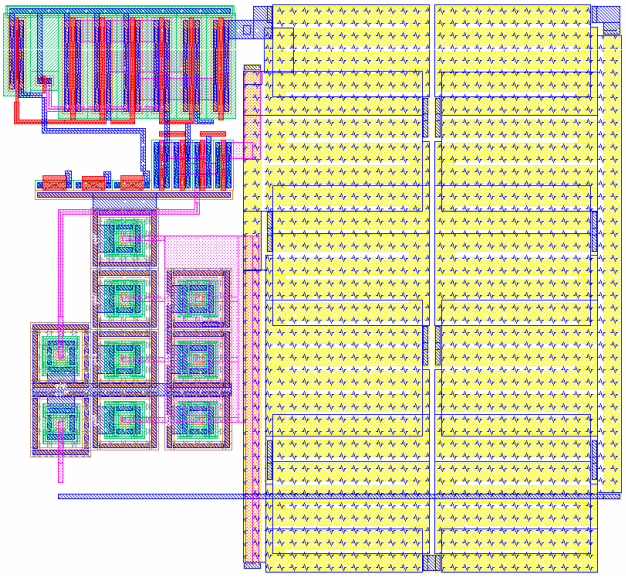
The boost converter steps up or "boosts" a DC voltage from a lower voltage source to supply a higher voltage output while maintaining polarity. The boost SMPS uses a parallel connected metal oxide semiconductor (MOS) device acting as a switching transistor to control output voltage. Operation is rather simple with two distinct modes. While the MOS device is fully 'on' current passes from the inductor directly to ground effectively reverse biasing the output diode to allow charge to be drawn from the output capacitor to supply the load. When in 'off' mode the diode becomes forward biased allowing current from the diode to pass through to the output increasing output voltage.

2. On-Chip Components

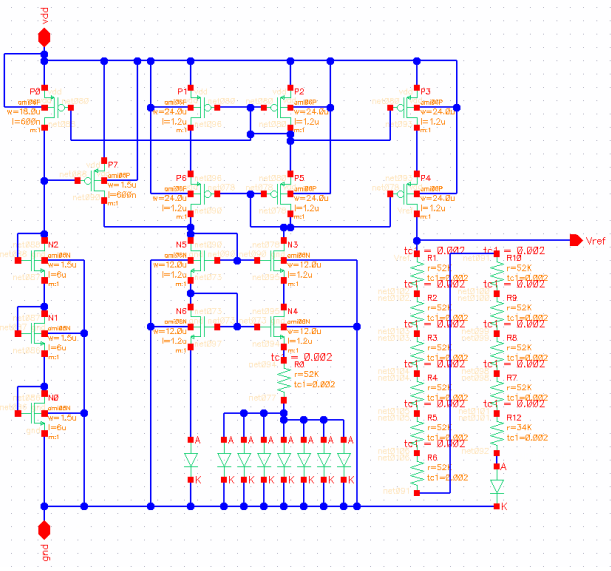
The boost switching power supply operates with a limited number of components, but each component plays an integral part in the device's overall operation. Each component for this project was designed independently using the ONSEMI C5 process ensuring design rule checks and LVS confirmations before being combined into the final circuit. This portion will cover the design of each component using the Cadence Virtuoso digital design environment and their respective role in the device's operation as well as some of the important design considerations that must be evaluated with each.

The Bandgap Reference Supply

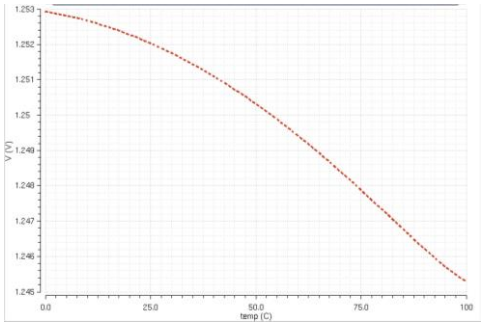
The heart of the boost switching converter begins with the bandgap reference circuit. This internal reference circuit serves as the 1.25V reference voltage that will be used in comparison to the output feedback voltage circuit. The bandgap circuit is designed to provide a constant 1.25V DC to the device's internal comparator circuit regardless of changes in temperature and VDD. We will see through analysis and simulations that the bandgap design used for this device does have some limitations. Included below is a circuit design schematic, layout, as well as descriptive simulations showing proper operation of the bandgap circuit.



Bandgap Circuit Layout



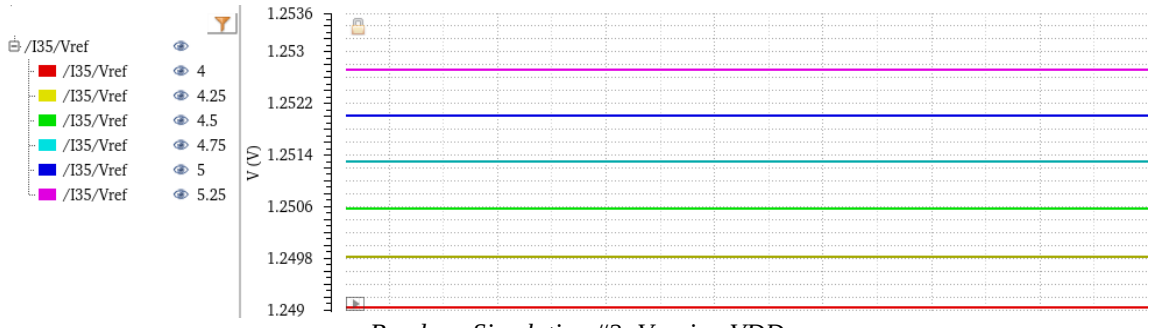
Bandgap Schematic



Bandgap Simulation #1

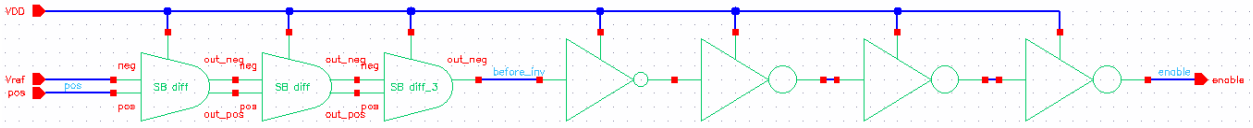
In simulation #1 shown to the left, we witness temperature increases from 0^0 C to 100^0 C on the bandgap circuit while verifying output only to vary by 8mV making this reference supply very suitable for a wide range of applications. Increases in temperature are important to consider in chip design as operating temperature of a semiconductor device can vary greatly from application to application.

One further simulation that will impact the results to follow, is witnessing the bandgap's change to VDD input voltage. In simulation #2 VDD is varied from 4v to 5.25V and the slight change in Vref output seems minimal but as explained further in this document does begin to effect output voltage as this will become our comparator's voltage reference. Both changes in temperature and VDD effect the bandgap reference voltage output slightly and when compounded together would have a considerable effect on output voltage variance. Analyzing simulation #2 we see that bandgap reference voltage centers closest to 1.25V with a 4.25-4.5V VDD. This will be noted again as final device simulations are performed.



Bandgap Simulation #2: Varying VDD

The Comparator



Comparator Schematic using Symbol Views

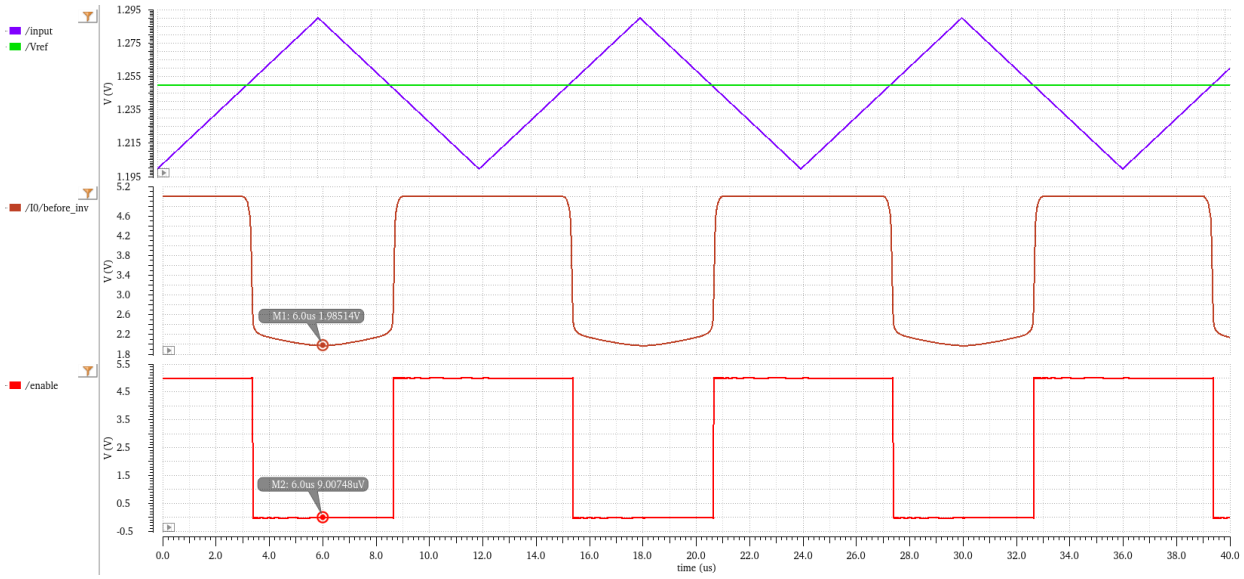
Moving on to the comparator circuit I will begin to set up the logic circuit which will control the device's sensing operation. The comparator is constructed by cascading three self-biasing differential amplifiers back-to-back in a series format. The differential amplifiers used within the comparator each use a combination of NMOS and PMOS devices to sense the difference between feedback voltage and bandgap reference circuit output voltage. When comparing the feedback voltage signal from the design's desired 12.5V output with the bandgap voltage, the comparator will output a logic 0 if Vout > 1.25V and output a logic 1 if Vout < 1.25V. To be sure we have proper comparison our feedback voltage will be ran through a simple voltage divider to reduce the 12.5V output to match the bandgap's 1.25V. Below are calculations for the voltage divider portion feeding the comparator.

$$V_{ref} = V_{fb}\frac{R_1}{R_1 + R_2} \rightarrow 12.5V * \frac{1k\Omega}{1k\Omega + 9k\Omega} = 1.25V$$

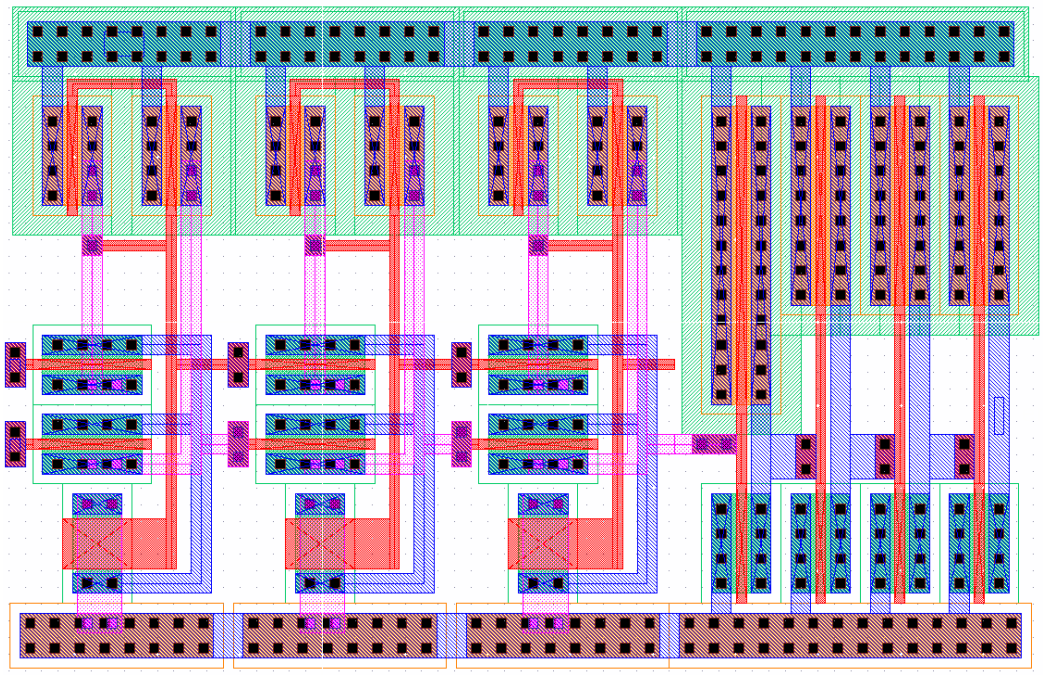
$R_1 = 1k, R_2 = 9k$

Each MOSFET size within the differential amplifier size was chosen out of simplicity for this design with a result of some noticeable disadvantages. Using a 10/1 (W/L) design within the differential amplifier devices causes a sacrifice in even switching points but in turn allows the design to using less overall power than larger sizes and reduces layout size. Following these three cascaded diff-amps will be a string of inverters used to clean up our logic signal. Simulations can

confirm that the added inverters, although taking up costly chip space, do in fact make a noticeable difference in comparator output signal which will serve as our enable signal entering the NAND gate to control the clock source. When comparing the simulation outputs below you see that before the inverters, we are unable to reach a true logic ‘0’ which would inhibit a full ‘off’ signal to be sent further into the sensing circuit.



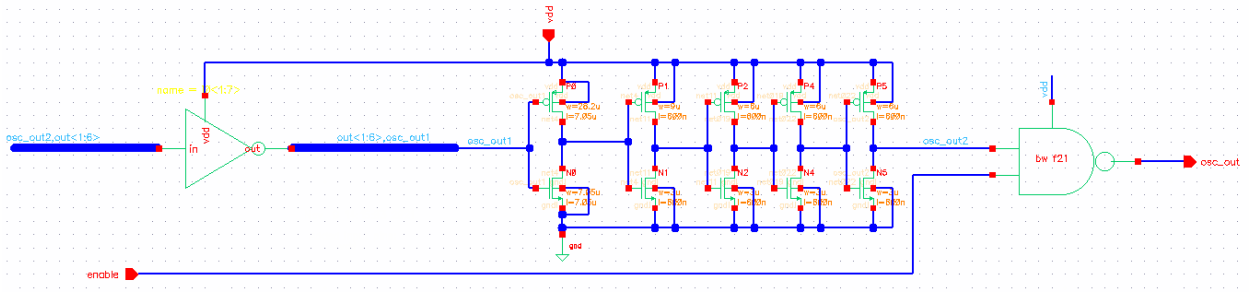
Comparator Simulation: Showing output before the inverters and after with a full logic swing from 0-5V. Note that proper comparator operation can also be viewed here as the sensing voltage drops below bandgap voltage the device outputs a clean logic 1 enable signal and 0 when voltage is above the 1.25V bandgap voltage as expected.



Comparator Layout View

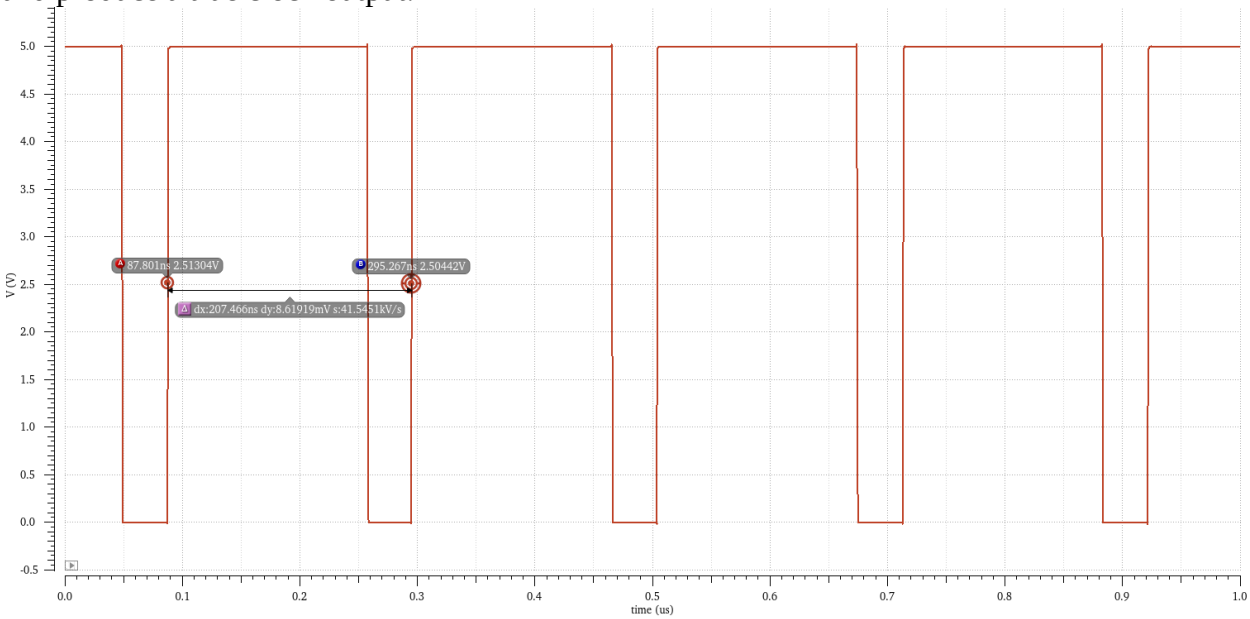
The Ring Oscillator Circuit

The ring oscillator circuit will be comprised of two components and provides a logic clock signal for the boost converter's large on chip NMOS switching device. I analyzed two unique oscillators created for my design before ending on a design with fewer stages containing alternating sizes of PMOS and NMOS devices to produce an approximate 80% duty cycle. The other consideration contained many more stages and operated at a lower frequency, but ultimately fell extremely short with triple the power consumption when simulated for efficiency.



Ring Oscillator Circuit Schematic using Symbol Notation

The ring oscillator circuit for this project was designed to operate near a 5MHz frequency with an 80% duty cycle. The reason for this decision was when researching the minimum necessary duty cycle to double input voltage on a boost converter I found 50% to be grossly incapable of performing such a feat. I chose to use 28.2/7.05 (PMOS/NMOS) inverter sizes on stage one and 7.05/28.2 on stage two, each with a length of 7.05, to keep my number of stages low and save in layout space. Following these alternating stages I used four short L inverters to square up the edges and produce a true clock output.



Ring Oscillator Simulation: plotting oscillation frequency

This goal in designing this device was an operation frequency of 5MHz. Using the above simulation results and following hand calculations, I determined my overall frequency to be 4.8Mhz when analyzed by simulation at the NAND gate output. Calculations shown below.

$$f_{osc} = \frac{1}{T} = \frac{1}{207ns} = 4.8Mhz$$

Because the inverter pairs are a 4/1 and 1/4 PMOS/NMOS size ratio they are strong in design, but high in overall resistance leading to the drastic reduction in stages when compared smaller ratio designs. It should be noted that these dimensions for inverter stages are specific to my design requirements as an 80% duty cycle was implemented. Hand calculations of device oscillation frequency were performed using the ONSEMI C5 specific values as well as common MOSFET delay, frequency, and resistance formulas. Using the ONSEMI C5 values of C'_{ox} = 2.5fF/um^2, R'_N = 20k, and R'_P = 40k hand calculations were performed. Resistance calculations are as shown below for each stage with overall delay calculations to follow.

Stage 1

$$R_N = R'_N * \frac{7.05}{28.2} = R_N = 5k\pi$$
$$R_P = R'_P * \frac{28.2}{7.05} = R_P = 160k\pi$$

Stage 2

$$R_N = R'_N * \frac{28.2}{7.05} = R'_N = 20k\pi$$
$$R_P = R'_P * \frac{7.05}{28.2} = R'_P = 10k\pi$$

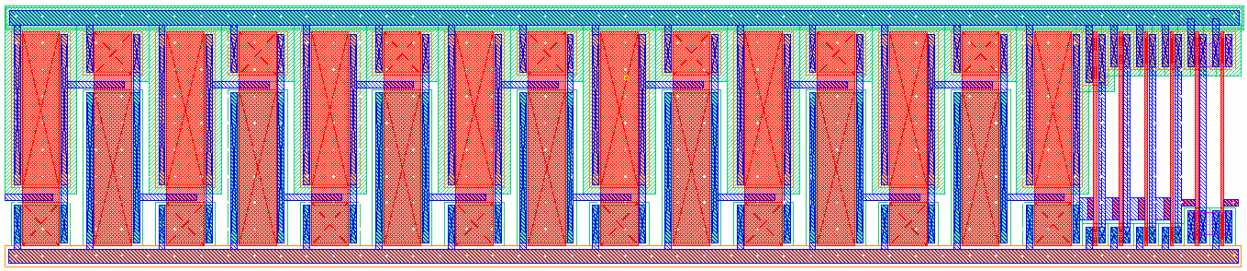
Stages 1 & 2

$$C_{oxp} = C'_{ox} * W_P * L_P = 497fF$$
$$C_{oxn} = C'_{ox} * W_N * L_N = 497fF$$

$$C_{tot} = \frac{5}{2}(C_{oxp} + C_{oxn}) = 2.49pF$$
$$\boldsymbol{t_{plh} = 0.7 * R_P * C_{tot}}$$
$$= 27ns \text{ \& } 17ns$$
$$\boldsymbol{t_{phl} = 0.7 * R_N * C_{tot}}$$
$$= 24ns \text{ \& } 47ns$$

$$f_{osc} = \frac{1}{stage\ 1\#(t_{plh}+t_{phl})} + \frac{1}{stage\ 2\#(t_{plh}+t_{phl})}$$
$$f_{osc} = \frac{1}{(192ns)} = 5.2\text{Mhz}$$

There was a slight variation in hand calculations and simulation output for the ring oscillator, but I determined this to be a results of the added inverters used to clean up the signal and NAND gate controlling the output.



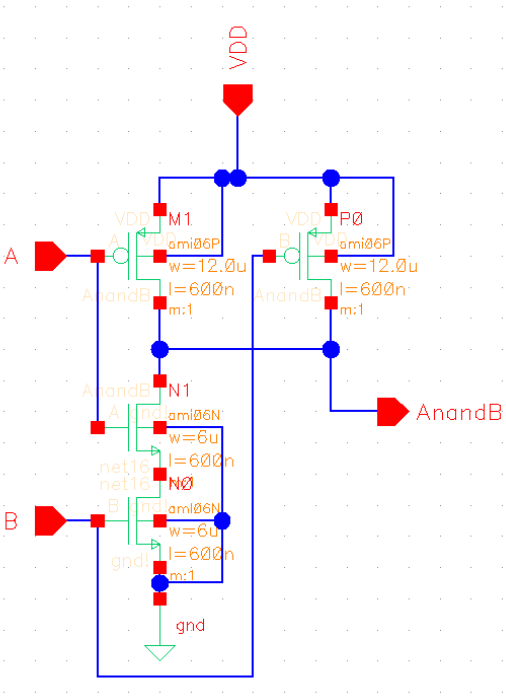
Ring Oscillator Layout with NAND Control Gate

The NAND Gate

Following the oscillator is a single NAND gate responsible for controlling the oscillation frequency output and the comparator enable output signals. Among all the components within this design, this is by far the simplest. Building a simple NAND gate truth table, we get the following.

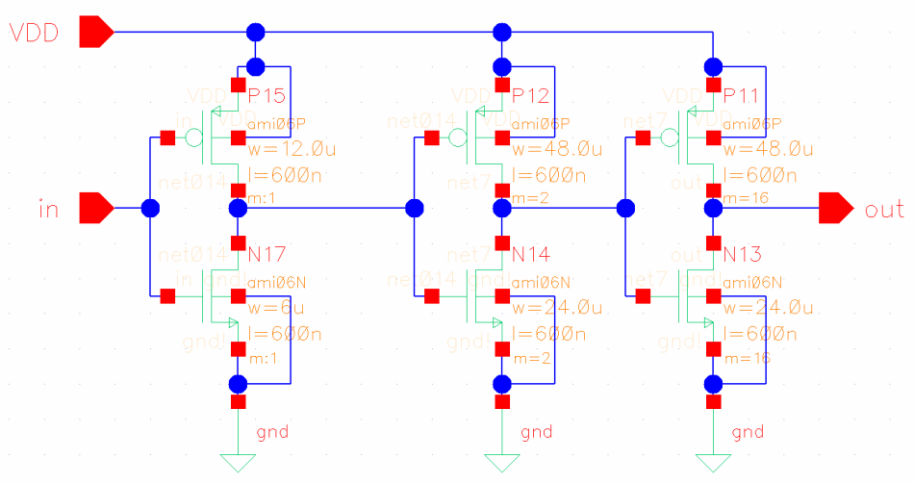
A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

Using this truth table you can see that it requires a high signal from the ring oscillator and high signal on the comparator enable to produce an output of zero. This would enable the off-stage or inductor charging stage in which inductor voltage is directed into the output of the circuit. When any other condition is met the NAND gate sends a logic high signal of varying frequency provided by the ring the buffer mentioned next.



NAND Gate Circuit

The Inverting Buffer



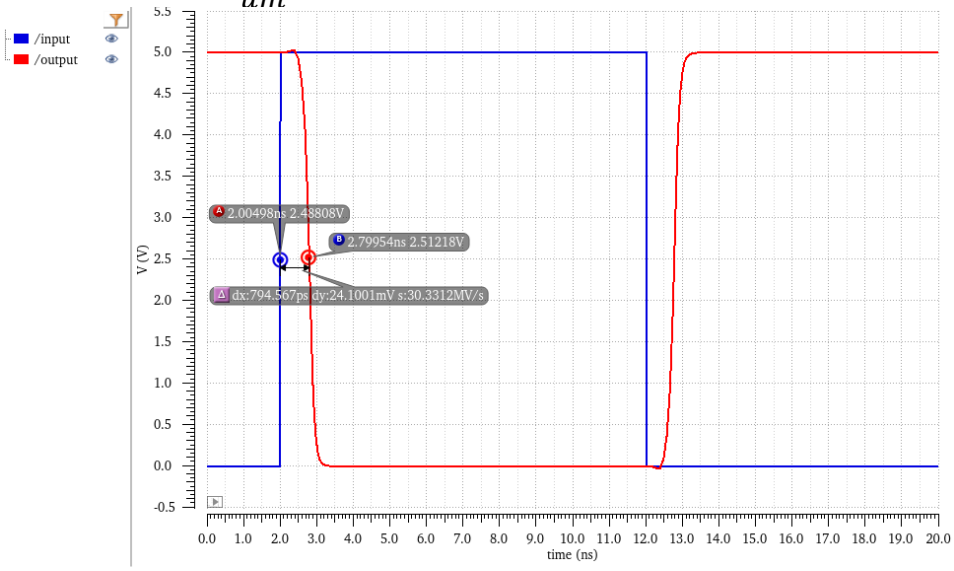
Inverting Buffer Schematic: showing three tiered stages

The inverting buffer which drives a large on-chip NMOS device for this design is responsible for grounding the off-chip inductor. Due to the large size of this MOSFET it requires a very fast, strong signal to transition from cut-off to saturation mode. This transition must be as fast as possible to avoid any unnecessary power consumption and heat related effects which could lead to premature device failure.

Careful decisions were made in choosing the MOSFET sizes for the buffer. The buffer needs to be strong and efficient in order to power the large 96u NMOS with a multiplier of 32 with minimum power loss. Load calculations for the NMOS were performed to determine the correct buffer sizing as follows below.

$$C_{load} = C'_{ox} * W_N * (multiplier) * L_N$$

$$\frac{2.5fF}{um^2} * 96u * (32) * 600n = 4.61pF$$



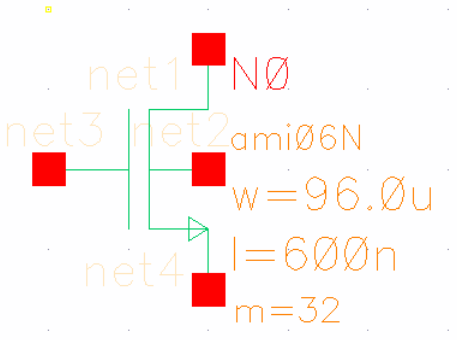
Buffer Simulation: Showing 794ps switching delay

The buffer in my design involved the use of three stages beginning at 12/6, followed by 48/24 with a multiplier of 2 and finally 48/24 with a multiplier of 16. Simulations were performed using a 5pF capacitor to simulate my chosen design's performance on driving the large NMOS switching load. Below are the simulation results showing the transition on time to be well within reason for a fast transition from cut-off to saturation.

Buffer Layout in ONSEMI C5 Process

On-Chip Driver NMOS

Grounding the off-chip inductor requires a fast and strong device to operate efficiently. For this device I chose a 96u/600n NMOS with a multiplier of 32. The device will operate fast with the minimum length creating low overall resistance, while also providing plenty of current due to the large length through use of the multiplier. It is important to note that device efficiency depends greatly on speed and internal component power consumption. Although the device will take up considerable layout space, it makes up for this in increasing efficiency values.



NMOS Driver Device

3. Off-Chip Components

The boost SPS has an even more limited number of off-chip components that were also fine-tuned during this design. Some items were restricted from change due to cost and production limitations, but the inductor specifically was open to modification. Two capacitors were used in the off-chip design, but restricted from variation. In the VDD supply circuit a 1uF capacitor acts as a decoupling capacitor to ensure the VDD remains at a nominal voltage. On the circuit's output an additional 10uF capacitor is used in a similar method to ensure output voltage remains constant relative to inductor activity.

82uH SMD Inductor

As explained previously described in this document, this design operates with use of one inductor and manipulation of inductor current by the use of a controlled grounding technique. Upon simulating the inductor from 40uH to 120uH at a 400Ω load, minimal change was noted, but when output resistance was varied under further analysis inductor sizing in the 80uH range produced more consistent output voltage and current values. Understanding that this device could be used under less than perfect conditions a value of 82uH was chosen due to low cost and high availability to produce a device with the best possible output in a range of load resistance.

82uH SMD Inductor

1N5819 SMD Diode

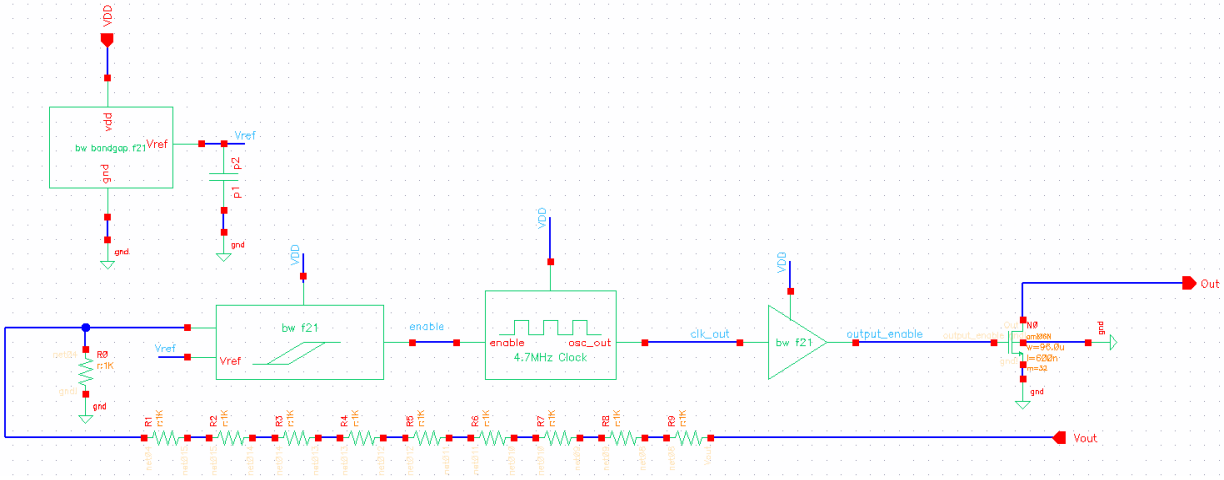
1N5819 SMD Diode

A 1N5819 diode is used in this boost SMPS design to effectively stop output voltage from bleeding back into the sensing circuit and draining the output capacitor while the inductor is grounded by the NMOS. When the inductor is grounded the reverse bias of this diode allows the 10uF capacitor to supply the output. Once the ground is removed from the diode, forward bias conditions resume.

4. The Boost SPS Assembled

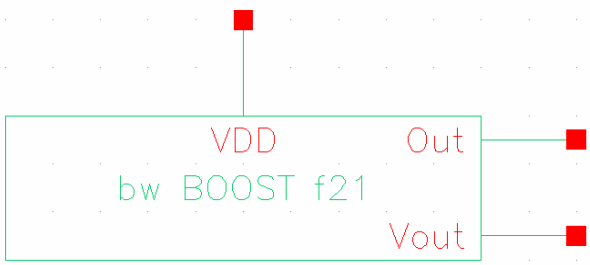
Once all these components were individually designed laid out and tested for design rule compatibility using DRC and LVS checks, they were combined together to form the final product. Below are final symbols, schematics, layouts, and extracted views.

For my layout design I chose to maximize space and keep all components in a tight configuration. Extensive use of metal2 and metal3 layers allowed me to achieve a compact efficient footprint but does come with an associated cost of additional metal and via pricing. Had this been a production chip, the design may have been better suited with a lower cost model.

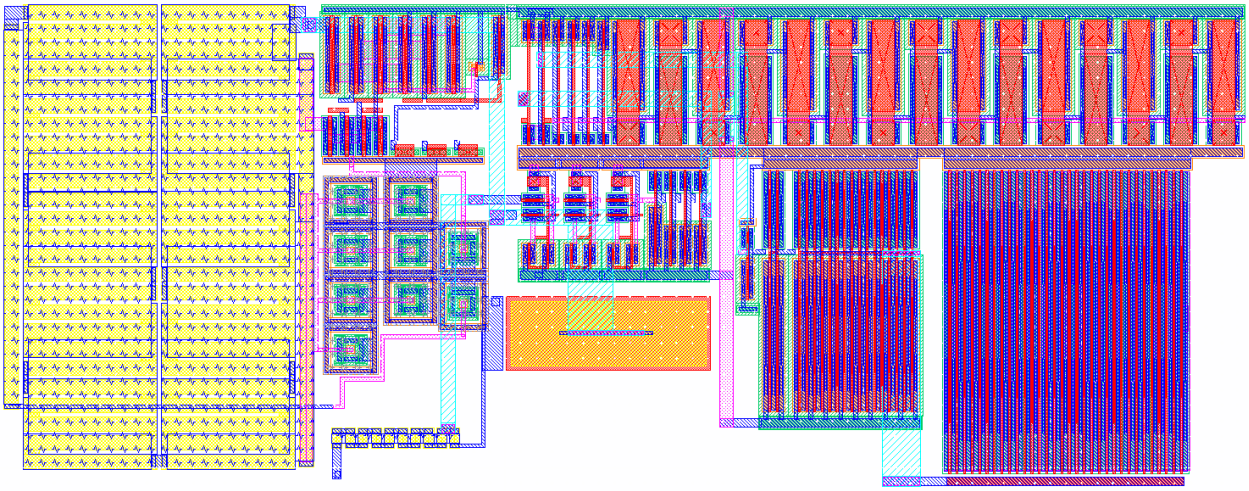


Final Master Schematic using all Design Symbols

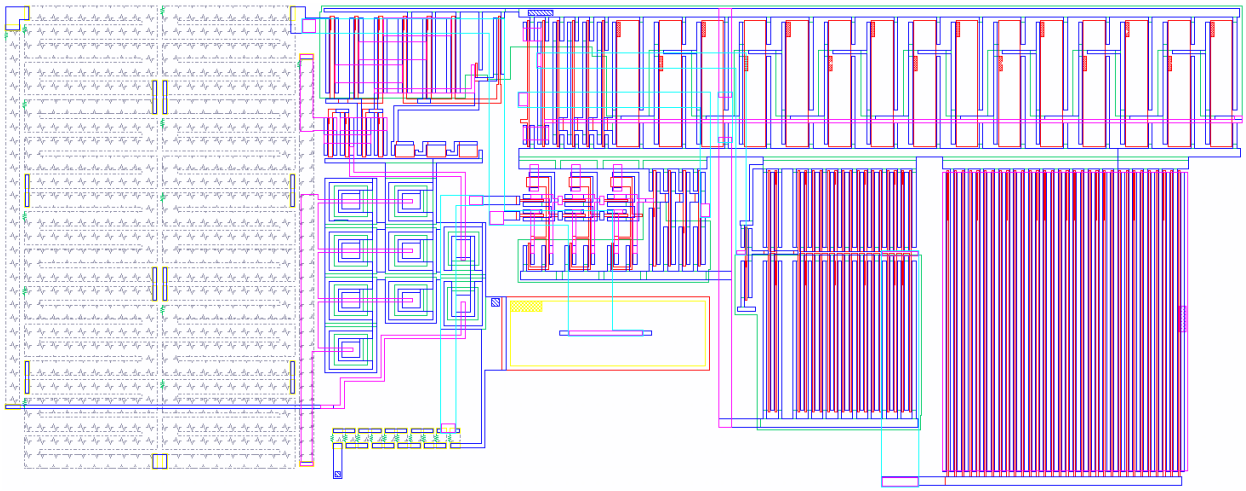
NOTE: The above schematic displays the importance of developing design symbols for each circuit in the overall layout for a cleaner and simplified schematic.



Final Schematic Symbol View



Master Layout View



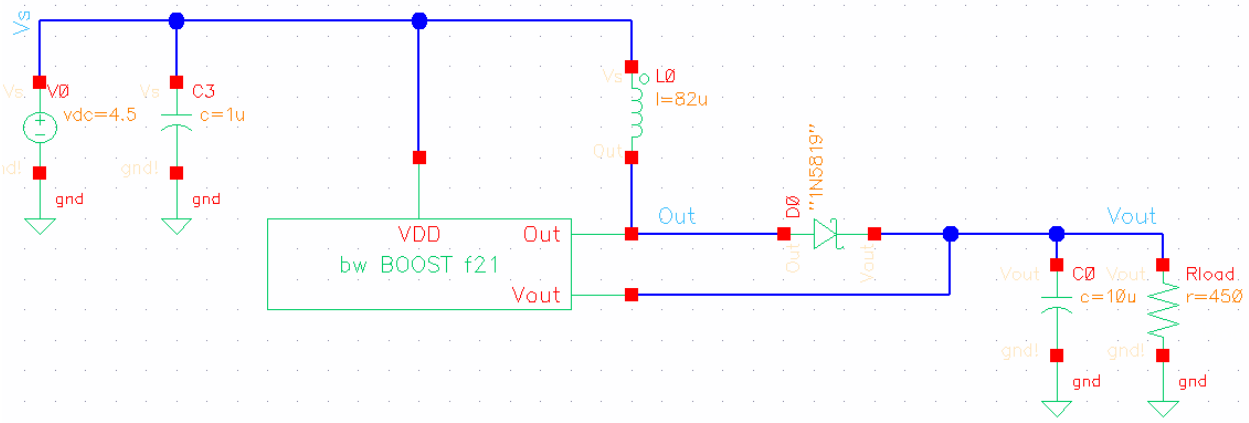
Master Extracted View

```
DRC started.......Tue Nov 30 13:06:43 2021
    completed ....Tue Nov 30 13:06:43 2021
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "MASTER_bw_f21 layout"   *********
   Total errors found: 0

Getting layout propert bagGetting layout propert bag
LVS job is now started...
The LVS job has completed. The net-lists match.

Run Directory: /home/wolak/CMOSedu/LVS
```

Master DRC / LVS Confirmation

5. Simulation and Testing

The final design was simulated under many conditions using the Cadence Virtuoso Spectre and UltraSim environments to provide a clear and concise conclusion on operation in variance of VDD, temperature, load resistance, power consumption and efficiency. Shown below is the test circuit created to model the power supply design and included after are results of each individual simulation with brief explanation.



Simulation Circuit Design using Project Symbol View

Parametric Analysis of Chip Temperature at 450Ω Load

Summary of Results at Temperature Variance					
Temp (^oC)	Avg(Vout)	Min(Vout)	Max(Vout)	V_{ripple}	Avg I(VDD)
27	12.520	12.49	12.55	60mV	27.83mA
45.25	12.505	12.48	12.53	50mV	27.80mA
63.5	**12.495**	**12.47**	**12.52**	**30mV**	**27.74mA**
81.75	12.475	12.45	12.50	50mV	27.72mA
100	12.445	12.42	12.47	50mV	27.67mA

Parametric Analysis of VDD Voltage at 600Ω Load

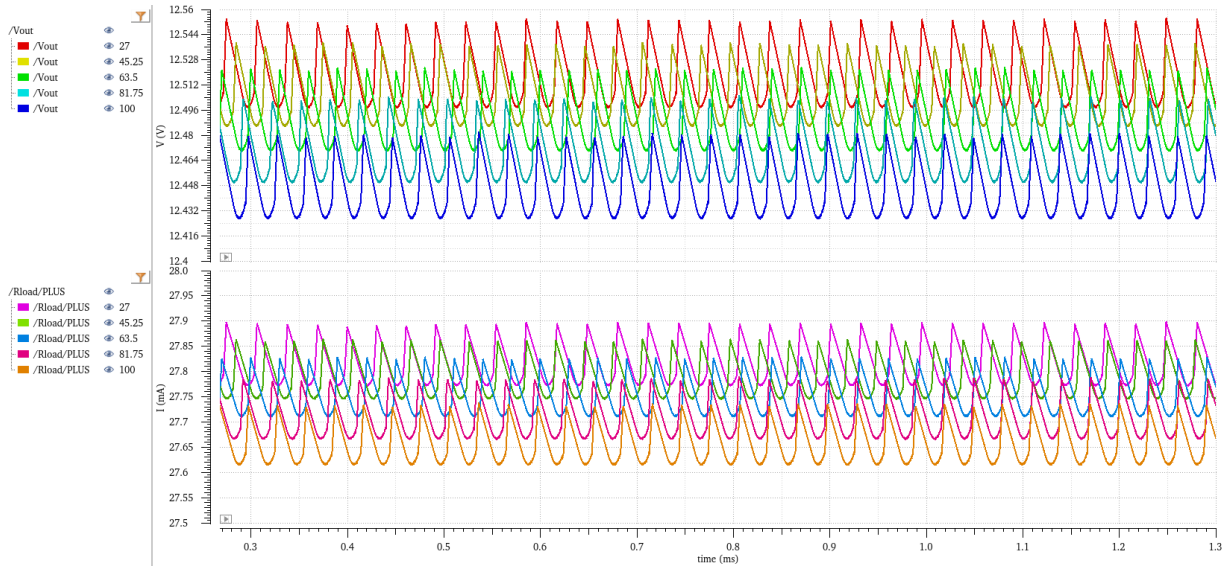
Summary of Results for Varying VDD				
VDD	Avg Vout	Min Vout (V)	Max Vout (V)	Vripple
4.0v	12.500	12.486	12.515	29mV
4.25v	**12.512**	**12.497**	**12.526**	**29mV**
4.5v	12.513	12.501	12.524	23mV
4.75v	12.528	12.512	12.544	32mV
5.0v	12.548	12.530	12.565	35mV
5.25v	12.544	12.520	12.567	47mV

Analyzing the values show above, both VDD and temperature play a significant role in the device's overall output with the ideal operating conditions produced near 63.5^0 C with a VDD voltage near 4.25V. We can see that as temperature climbs to 100^0 C the device cannot effectively provide the desired output voltage. This is largely due to our previous simulations regarding changes in Vref as a result of changes in temperature and VDD.

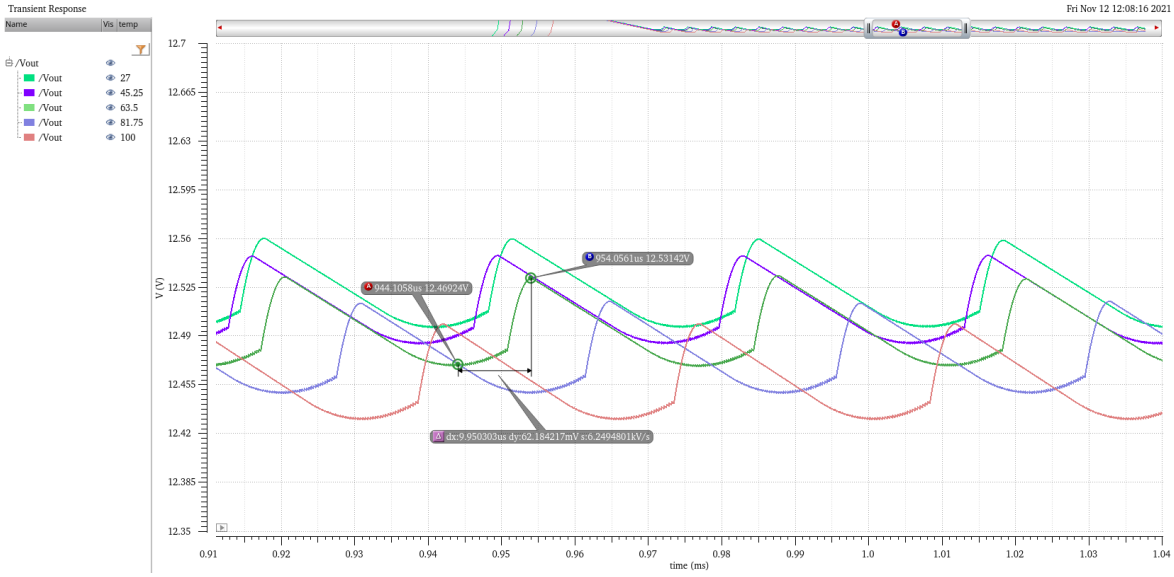
$$\eta = \frac{V_{out} * I_{load}}{V_{dd} * (avg(I(V_{dd}))} x100$$

Efficiency Determinations at 4.25V VDD

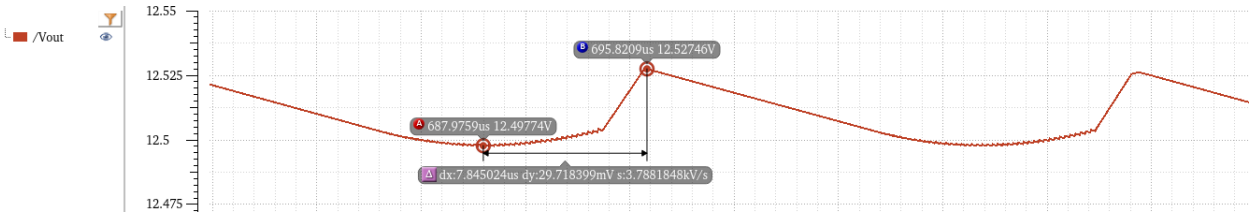
Summary of Results at Varying Load Resistance				
R_{load} (Ω)	**avg(I(VDD))**	**avg(I(out))**	**I_{load}**	**Efficiency**
300	140.1mA	41.83mA	41.6mA	87.3%
375	109.6mA	33.48mA	33.3mA	89.4%
450	89.6mA	27.91mA	27.8mA	91.2%
525	75.4mA	23.94mA	23.8mA	92.8%
600	66.0mA	20.96mA	20.8mA	92.7%



Temperature Variation Simulation: at 4.5V VDD



Varying Temperature Simulation: 4.5V VDD at 400Ω load



VDD = 4.25V Output Simulation at 600Ω showing 29mV hysteresis

Overall, my device performed better at a slightly lower than usual 5V VDD voltage in the 300-600Ω load range. My output hysteresis lowered considerably to around 29mV as the load resistance increased but output voltage began to creep past a nominal 12.5V. At a 600Ω load my output centered at 12.512V which means near 20mA output the device displays a 1% variance in output voltage.

Temperature played a significant role in output voltage above 81.75^0 C. The device began to fail to provide a consistent charge in this temperature range.

6. Conclusion

This project design vastly strengthened my chip design troubleshooting and power supply knowledge. Through the design creation I made several decisions in regard to trade-offs associated with the specifics of my device. In devices like the comparator, I chose a smaller layout and design simplicity which led to reduced power consumption while understanding an associated sacrifice in delay and increasing resistance would follow. Again, in my oscillator I determined power consumption trade-offs with wider widths and less overall inverter stages was well worth the reduced layout size and reduction in overall stage. Decisions like increased sizing of the output capacitor could fine tune the device's hysteresis even further with an increase in production cost.

Due to the raise in Vref voltage with increases in VDD above 4.5V, more work could be done in designing a better performing bandgap reference circuit. This device could use further improvements with the use of a linear post regulator to filter the output ripple more effectively for an increase in output precision. Compared to linear voltage supplies, a mode switching supply produces more unwanted RF interference. With this in mind additional circuitry to filter RF and noise on the output would lead to a better design with yet again more precision.