Project Introduction

We will be creating an SPS chip for a Flyback Converter Circuit. The switching power supply chip is made up of 4 parts which are the BandGap, Ring Oscillator, Buffer, and Comparator. Each component will need to be designed, simulated and laid out.

Project Goals:

- Your design symbol should have the same footprint as the one seen below so that it can be placed in the simulation to determine if it works correctly.
- Your design is a chip to be used on a printed circuit board with the rest of the components seen below.
- The output of your circuit should be nominally 12.5V and be able to supply well beyond 2A of current to a load. Your design should work with other load currents too including 0, 10mA, 200 mA, etc.
- You should submit a report characterizing your design, specifically the design considerations and associated schematics, and tables characterizing the behavior (especially power from the 5V supply), clear and concise (!) images of some simulations used to generate the data you entered in your tables.
    - For example, how does your design work at VDD = 4V and temperature of 100C? Characterize your design with changes in temperature and VDD.

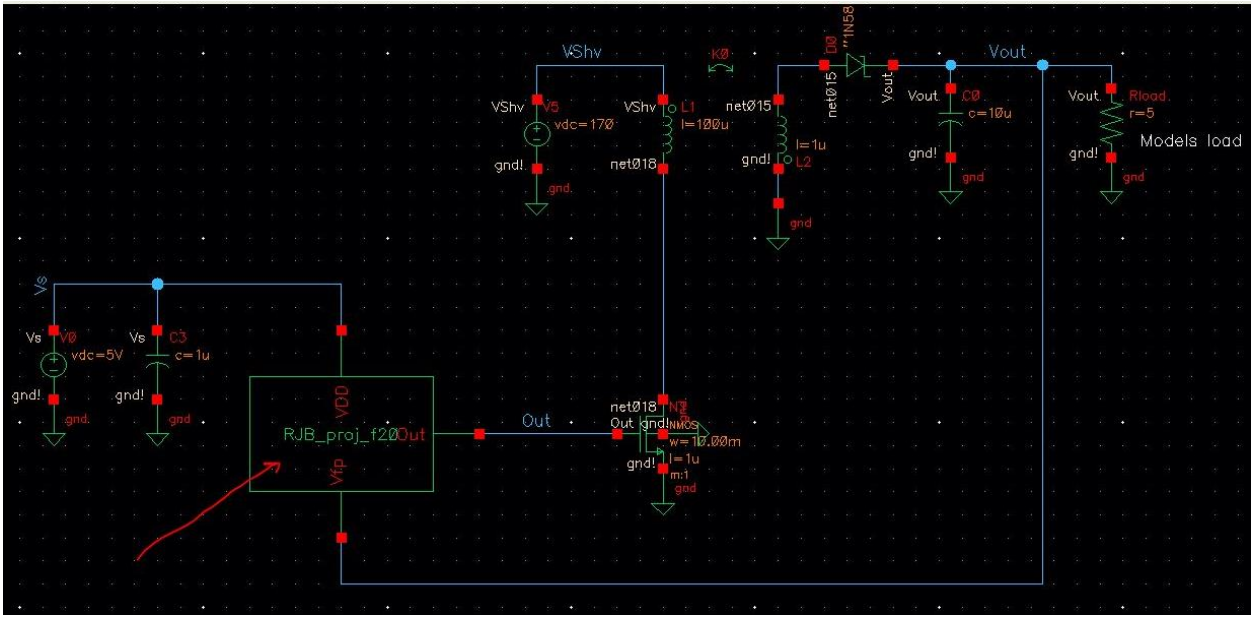

Figure 1 - Provided Flyback Converter Example

BandGap Design

The bandgap of the circuit is used to provide a constant Vref for the circuit that is resistant to the changes in both VDD and temperature. For this project we are going to be using the given design provided to us.

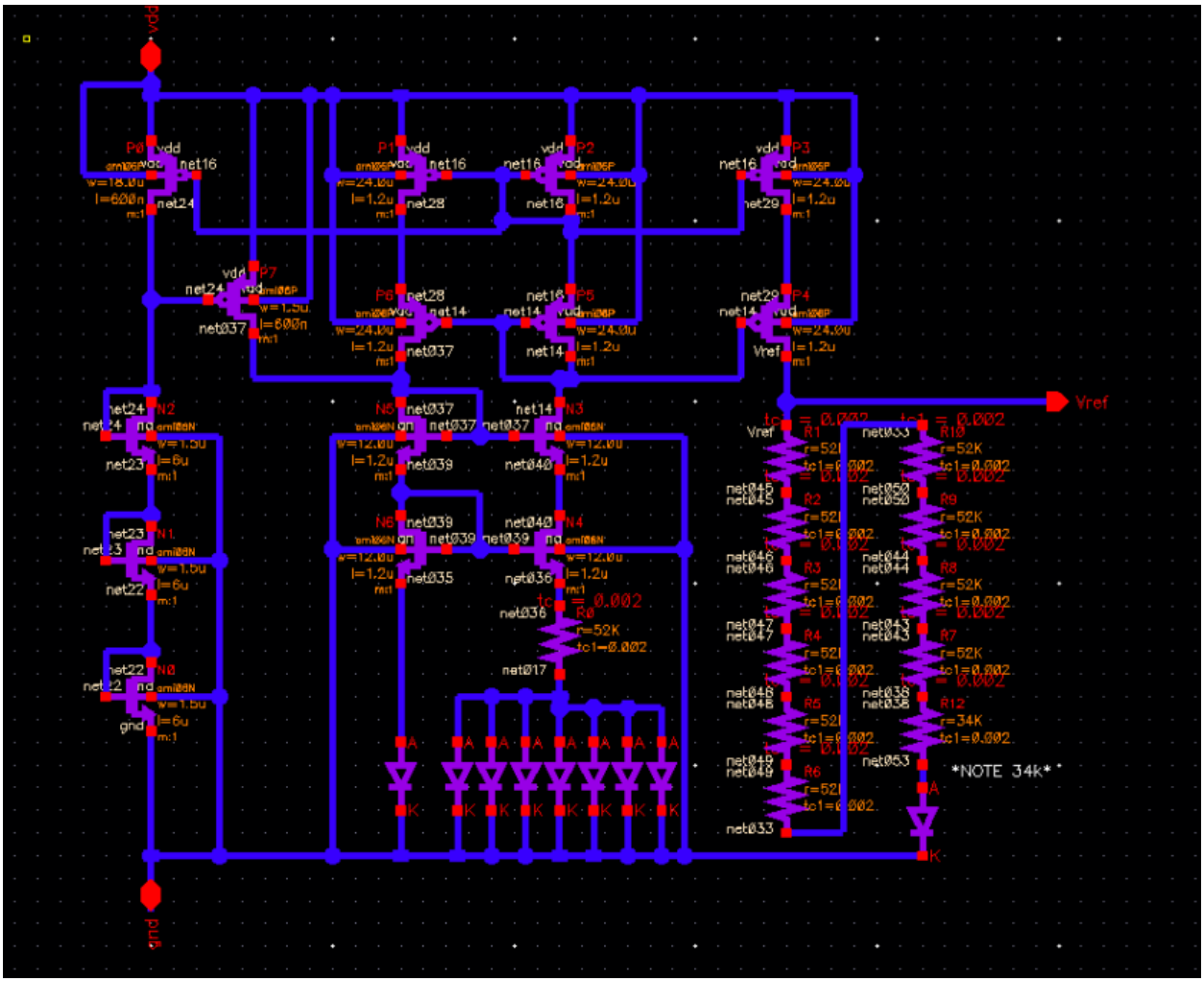

Figure 2 - BandGap Schematic

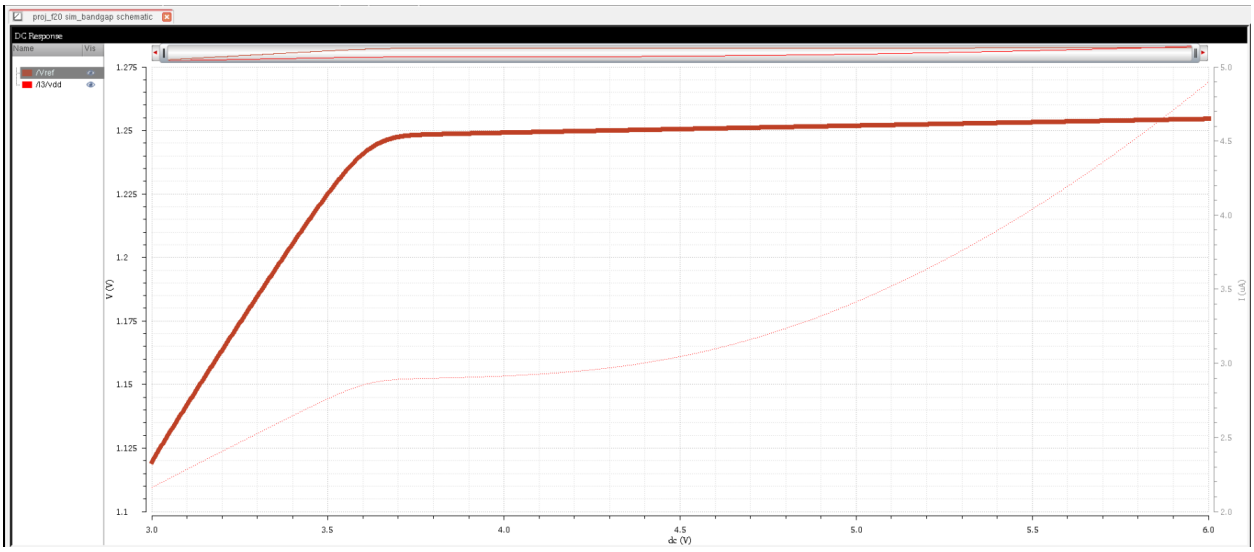

Figure 3 - BandGap Test

Based on the bandgap test graph, the bandgap works well at different VDDs all the way down to about 3.6V. Anything lower than that will cause the Vref to start decreasing.

BandGap Layout

To layout the bandgap, it was best to break down the schematic into 5 different pieces and then lay out each of the 5 pieces separately. Here is the final result.

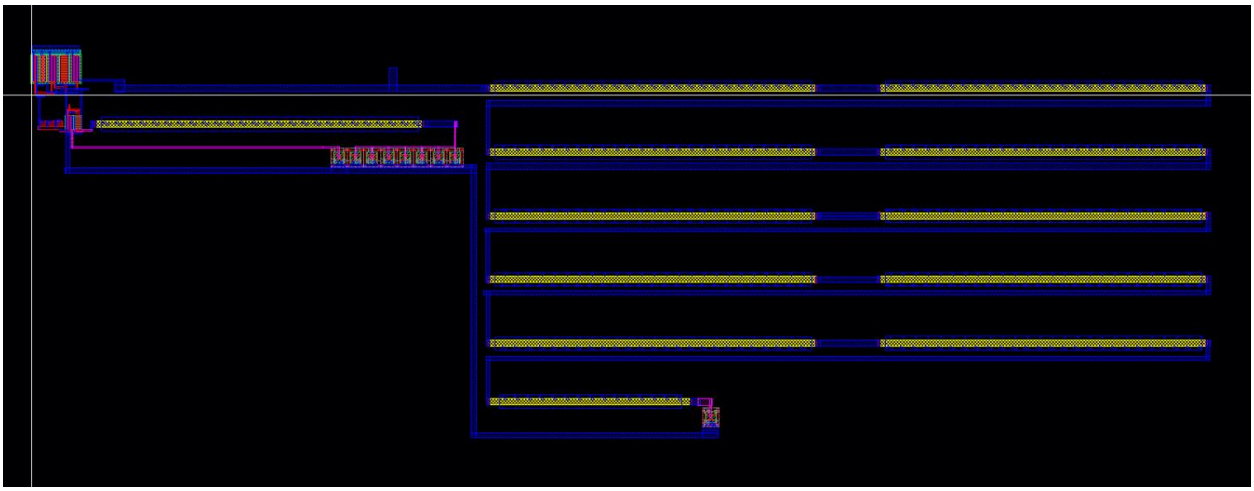

Figure 4 - Bandgap Layout

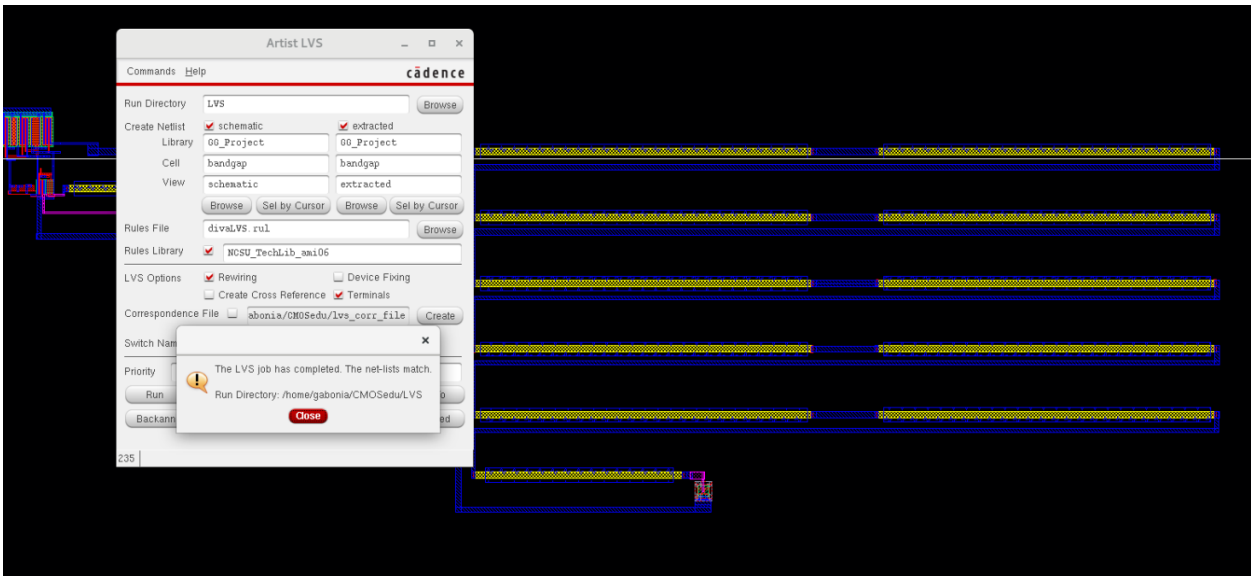

Figure 5 - Bandgap LVS

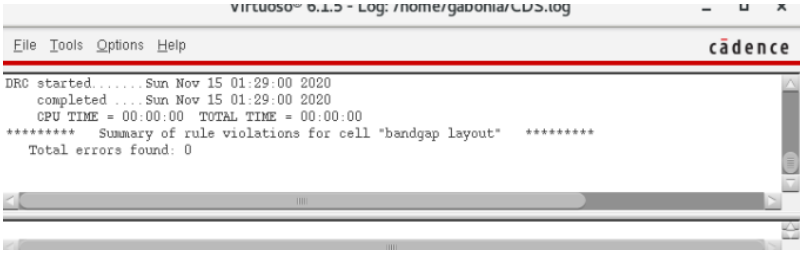

Figure 6 - Bandgap DRC

Ring Oscillator Design

For the Ring Oscillator the goal is to try to hit around 5MHz for the frequency oscillation. In order to reduce the amount of oscillators to be used to save space in the layout, I will create a slow oscillator. The slow oscillator will have a longer mosfet length which will translate into more delay, higher resistance, and higher capacitance. We'll need the longer delay in order to slow the oscillation down. We'll also need standard 12u/6u inverters along with the slow mosfet to square the input going in and out.

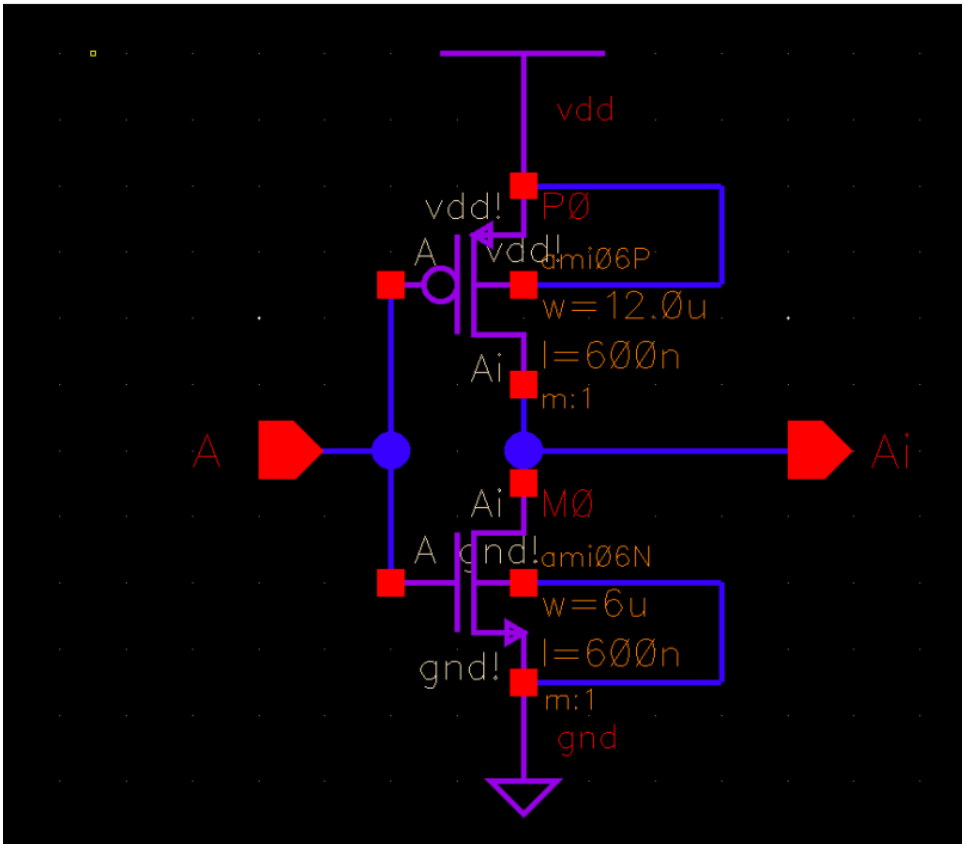

Figure 7 - 12u/6u Inverter Schematic

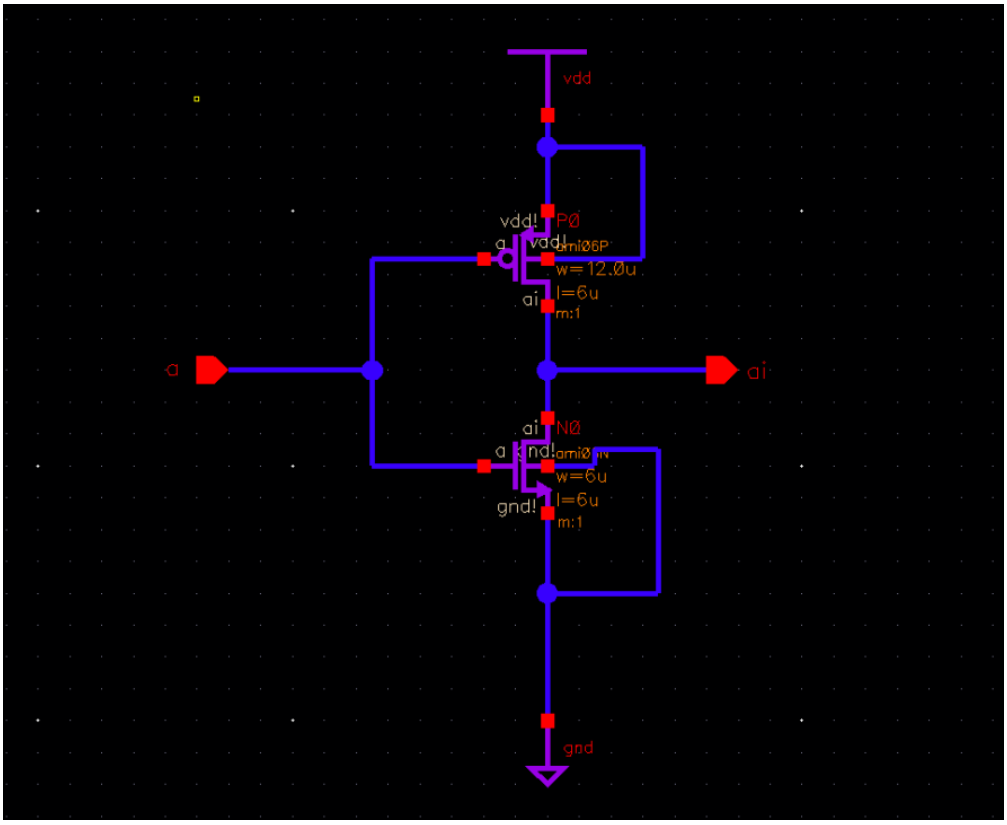

Figure 8 - Slow Inverter Schematic

Now that the inverters are done its time to create the NAND gate which will be used in the ring oscillator, the NAND gate will have the ring oscillators on one input and an enable on the other input which determines whether the ring oscillator is on or not.

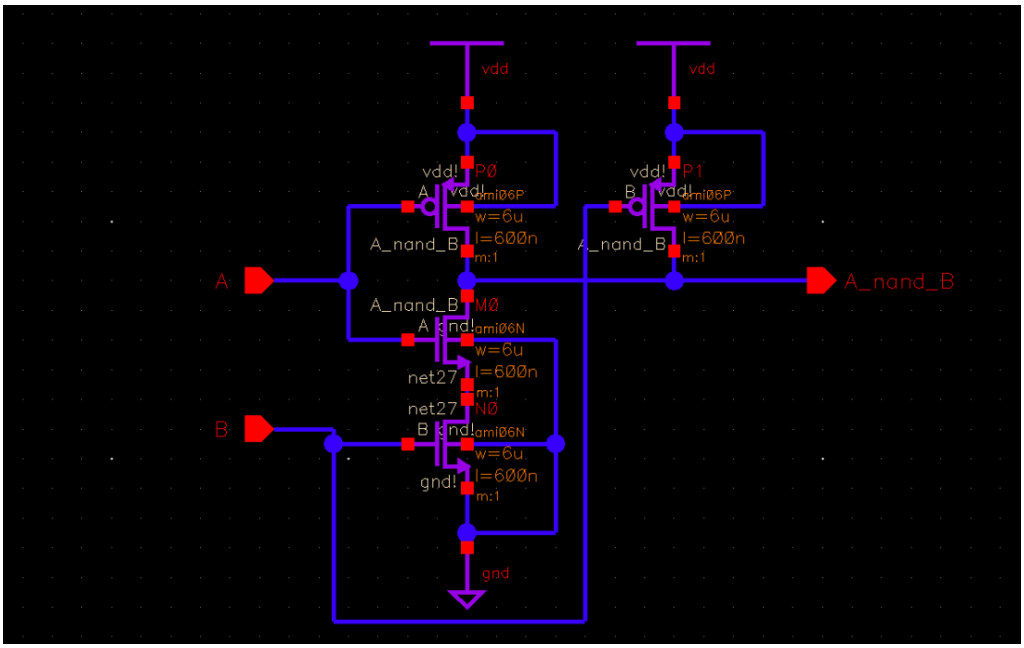

Figure 9 - NAND Gate Schematic

Now that the schematics are done for two inverters and the NAND gate, symbols will be created for each schematic. These symbols will be used to create the full ring oscillator for this part of the project. The first design we will start with will be a 4 stage osc, 8 stage slow osc, 8 stage osc finally going into the NAND gate which outputs into one inverter which will act as the buffer for this sim. Remember we must set an initial condition of 0 to get the oscillator to start.

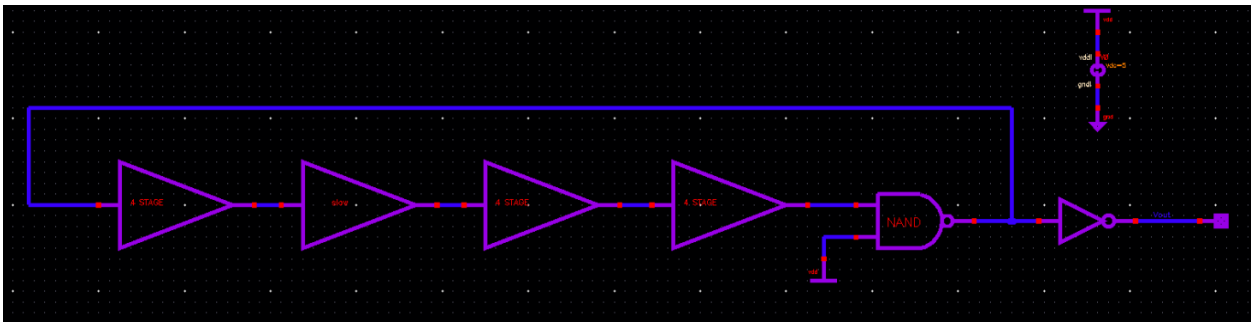

Figure 10 - Ring Oscillator Sim Test 1

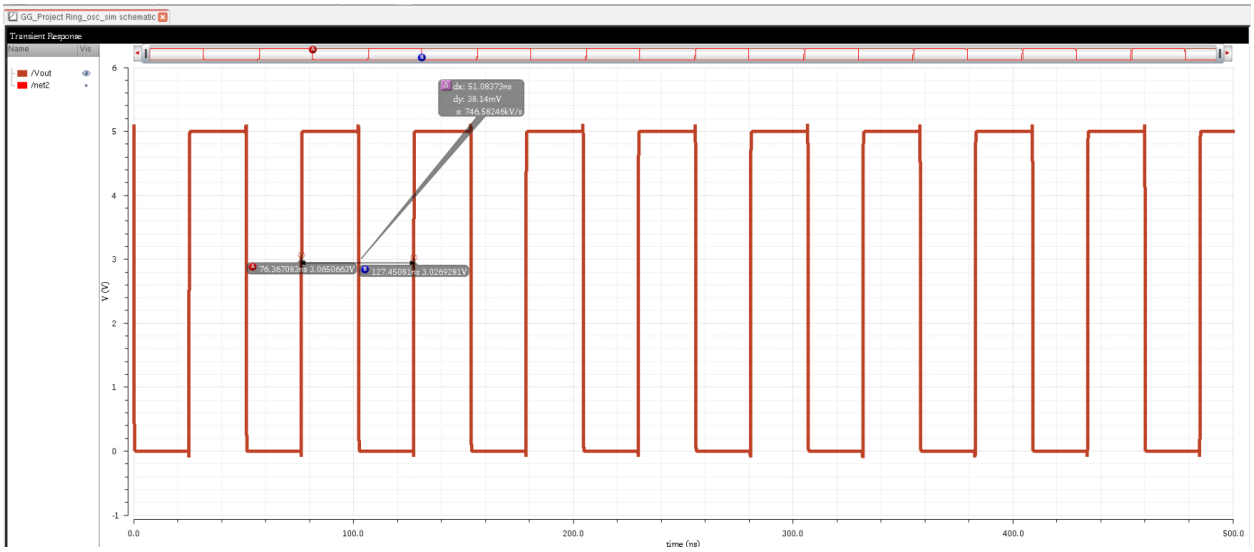

Figure 11 - Ring Oscillator Test 1 Graph

We can see that this design of the ring oscillator leads to a frequency of 20Mhz which is not our desired frequency. We need to do some math and find out roughly the amount of slow inverters we should use. Given that the frequency is still high we'll need to add more slow inverters.

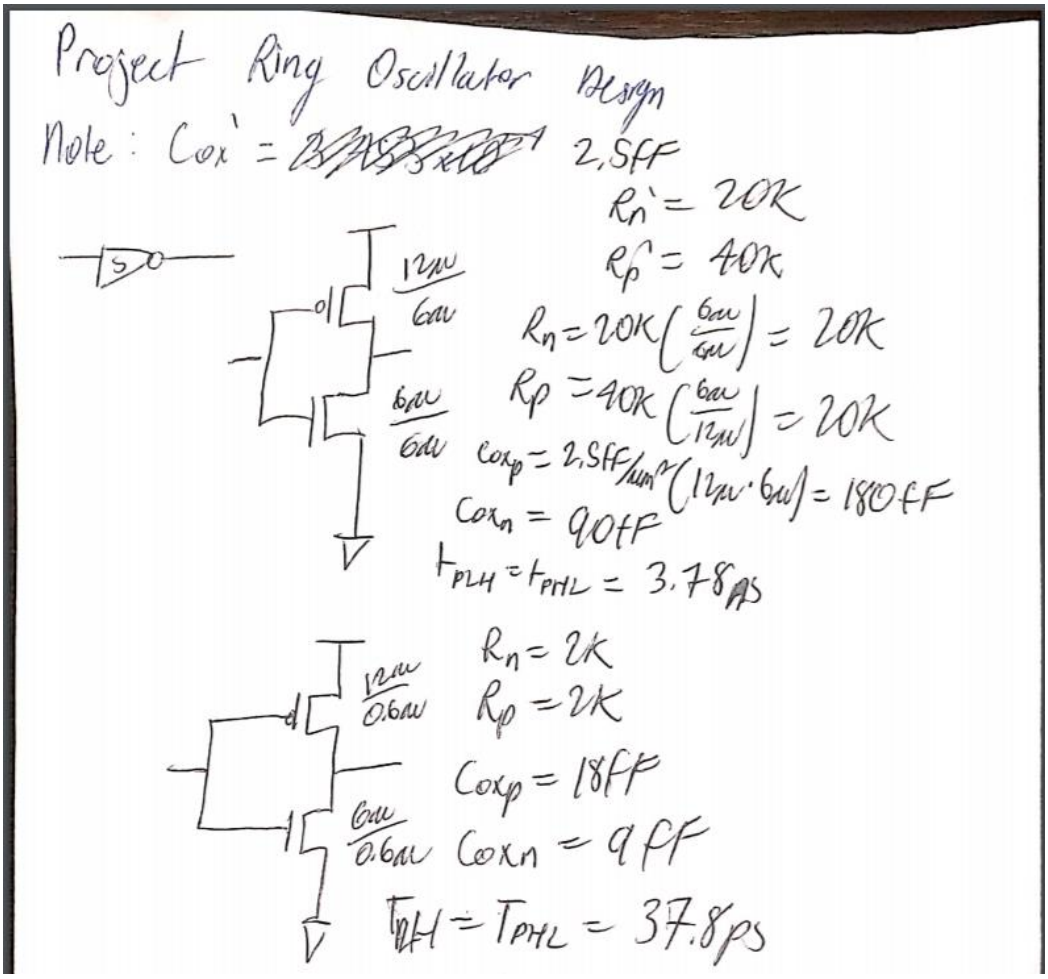

Figure 12 - Calculation of Inverter Delays

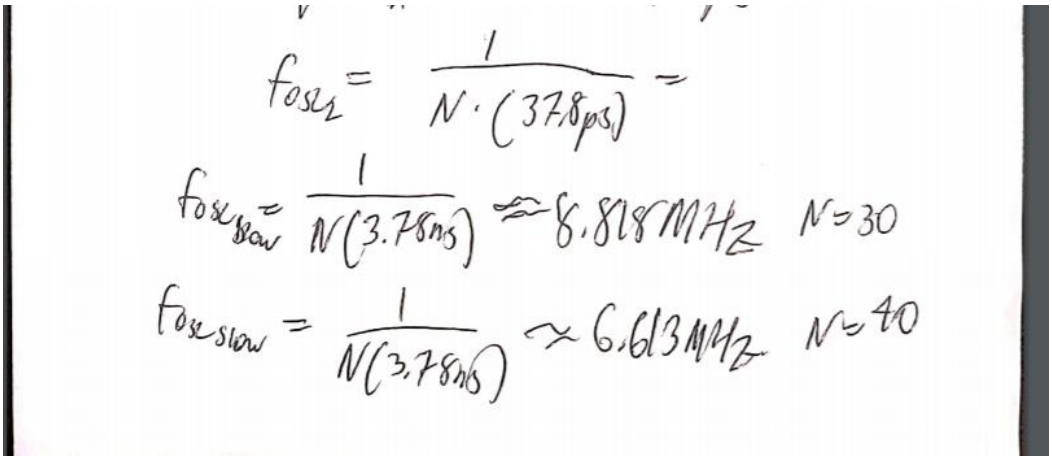

Figure 13 - Frequency Oscillation Hand Calculations

Given the hand calculations, we can see that the best range of inverter frequency oscillation would occur somewhere between 30 and 40 slow inverters. Going over 40 would result in using more than 50

inverters total which is undesirable. We will start at 30 slow inverters which were calculated at 8.18MHz, since there might be overshoot given that the output is much slower than hand calcs.

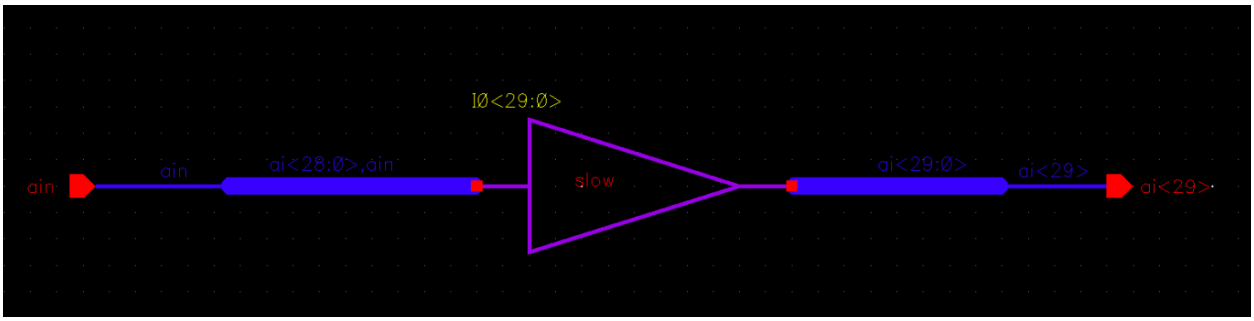

Figure 14 - 30 Stage Slow Inverter

We can implement this into our sim now. The sim will go as follows, 4 stage inverter, 30 stage slow inverter, 8 stage inverter and finally the nand gate. This should be a use of 42 inverters total.

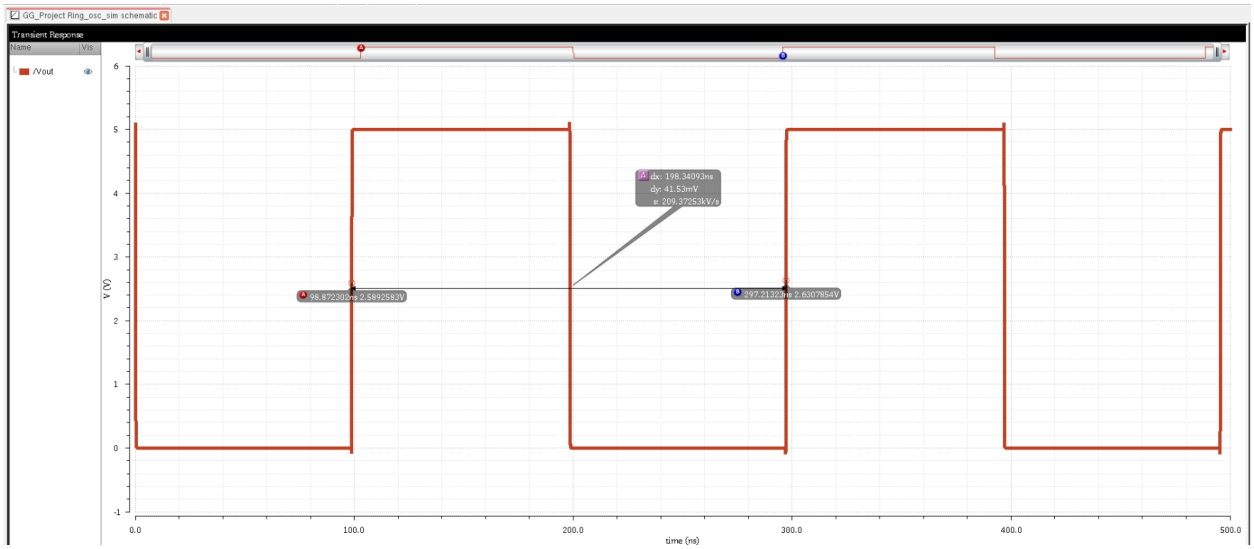

Figure 15 - Ring Oscillator Simulation Test 2

We can see that the 30 stage slow inverter works perfectly giving a ring oscillation frequency of 5Mhz. We can stop at 30 slow inverters and use this schematic for our project.

Ring Oscillator Layout

We will now begin the ring oscillator layout basing it on the following schematic.

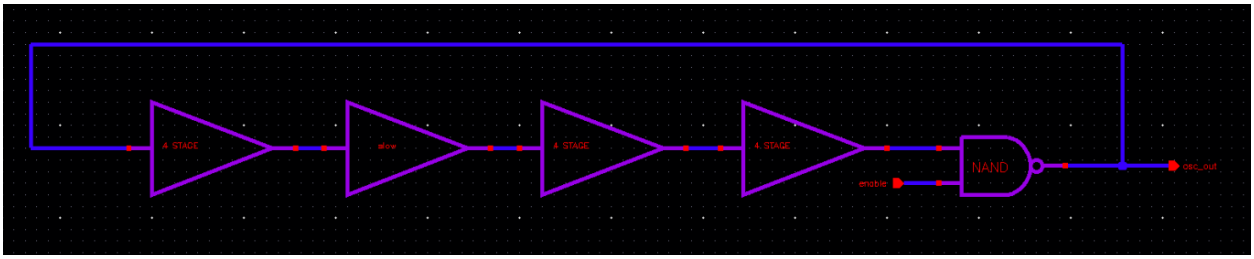

Figure 16 - Project Ring Oscillator Schematic

Figure 17 - Project Ring Oscillator Symbol

We can break the layout up by doing the layout of the 4 stage inverter, 30 stage slow inverter and nand gate separately and then putting them together.

Starting on the 4 Stage Regular Inverter we need to layout, DRC and LVS.

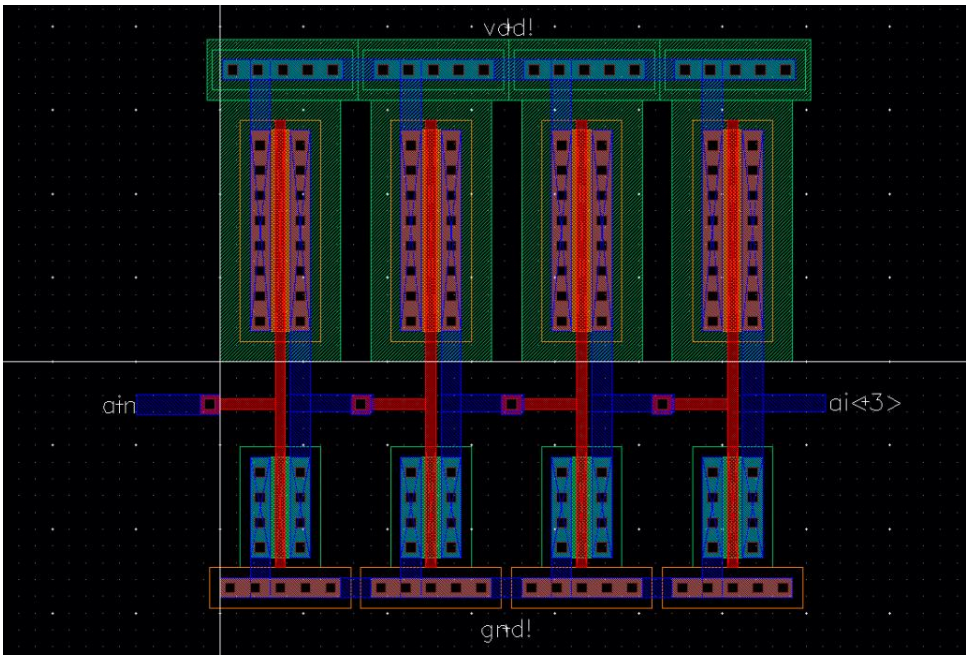

Figure 18 - 4 Stage Regular Inverter Layout

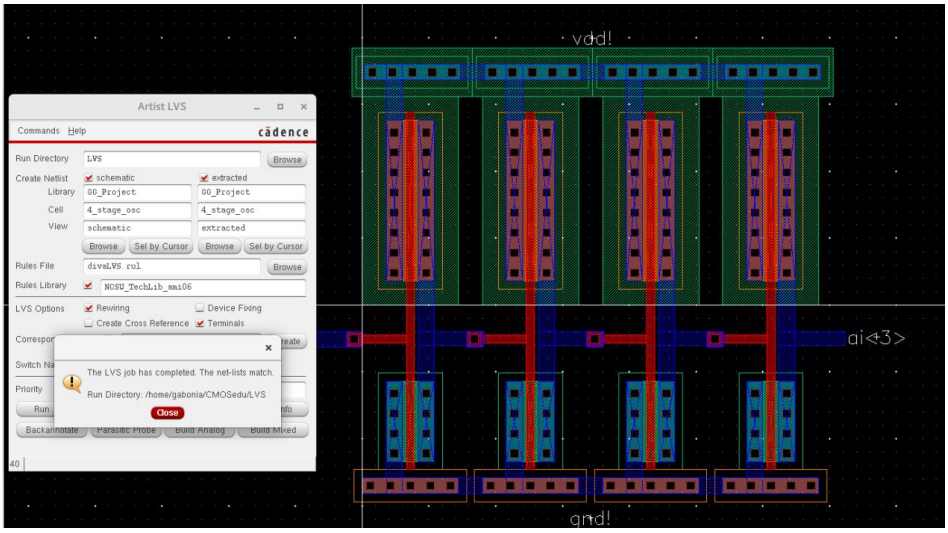

Figure 19 - 4 State Regular Inverter LVS

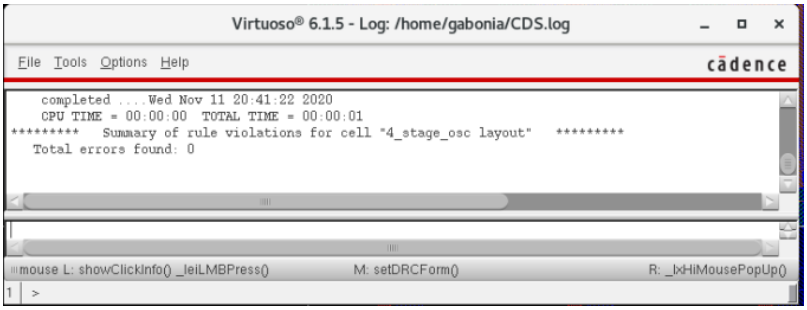

Figure 20 - 4 Stage Regular Inverter DRC

Next, we need to layout, DRC and LVS the 30 stage slow inverter.

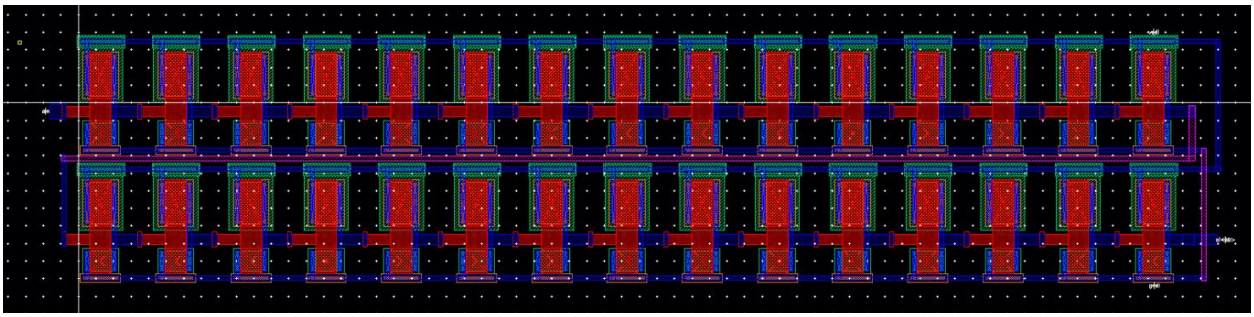

Figure 21 - 30 Stage Slow Inverter Layout

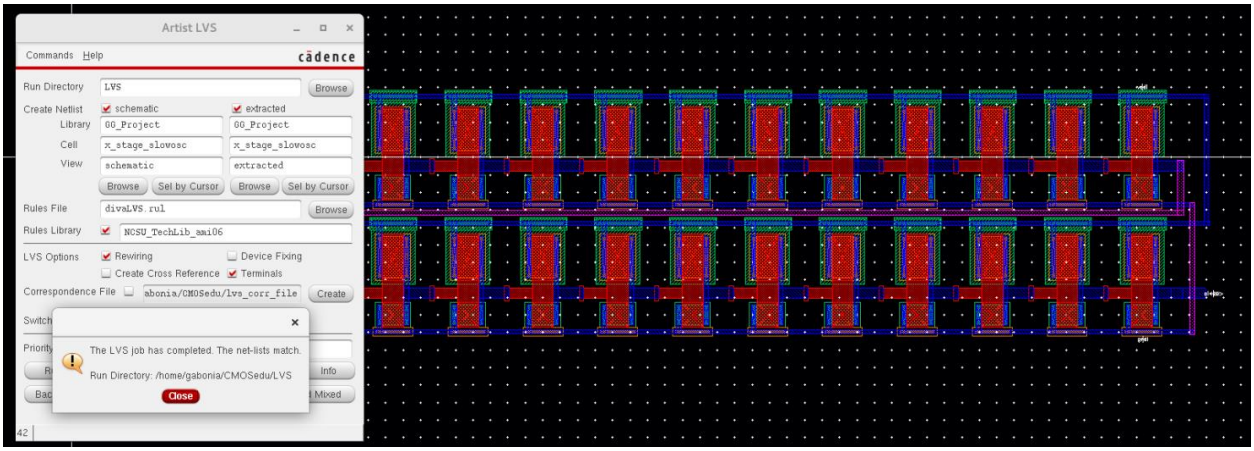

Figure 22 - 30 Stage Slow Inverter Layout LVS

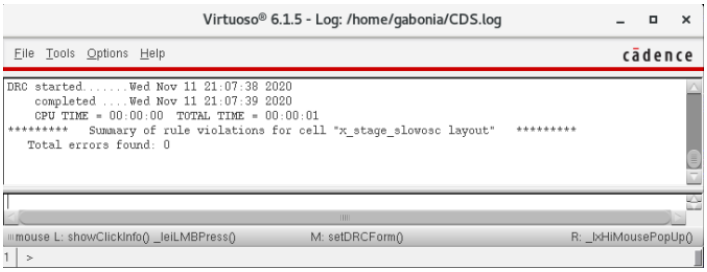

Figure 23 - 30 Stage Slow Inverter DRC

The last piece for this layout will be the nand gate. Note that this nand gate is made up of 6u/6u mosfets.

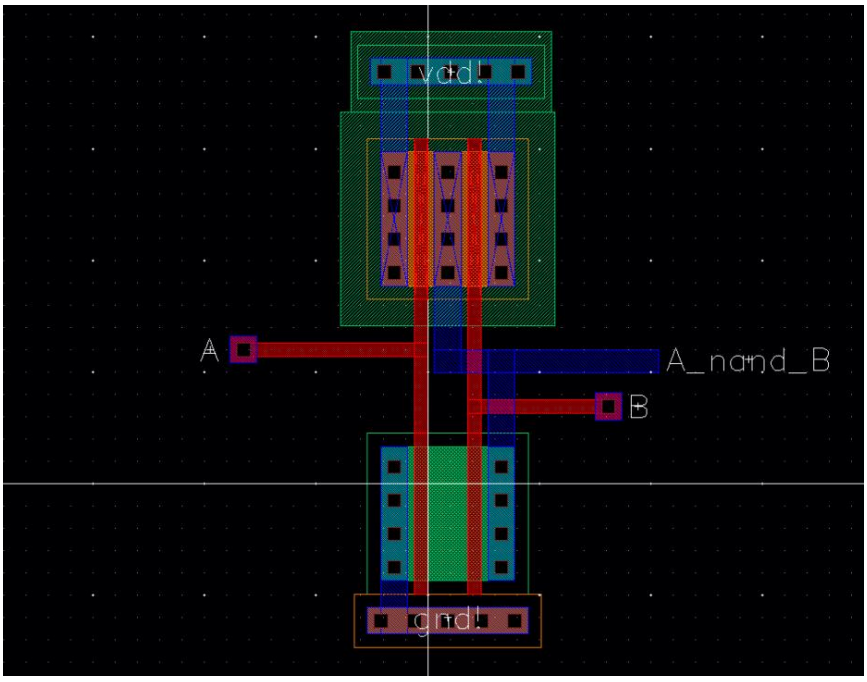

Figure 24 - NAND Gate Layout

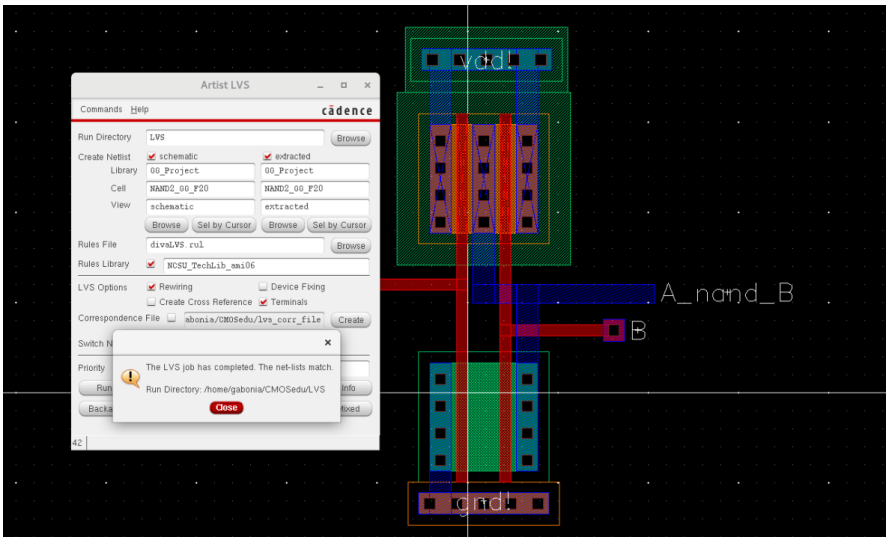

Figure 25 - NAND Gate Layout LVS

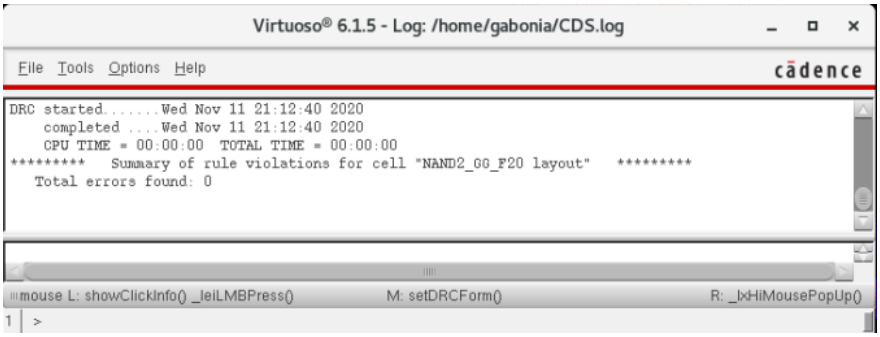

Figure 26 - NAND Gate Layout DRC

Now that all of the individual circuits are put together we can create the full layout of the Project Ring Oscillator.

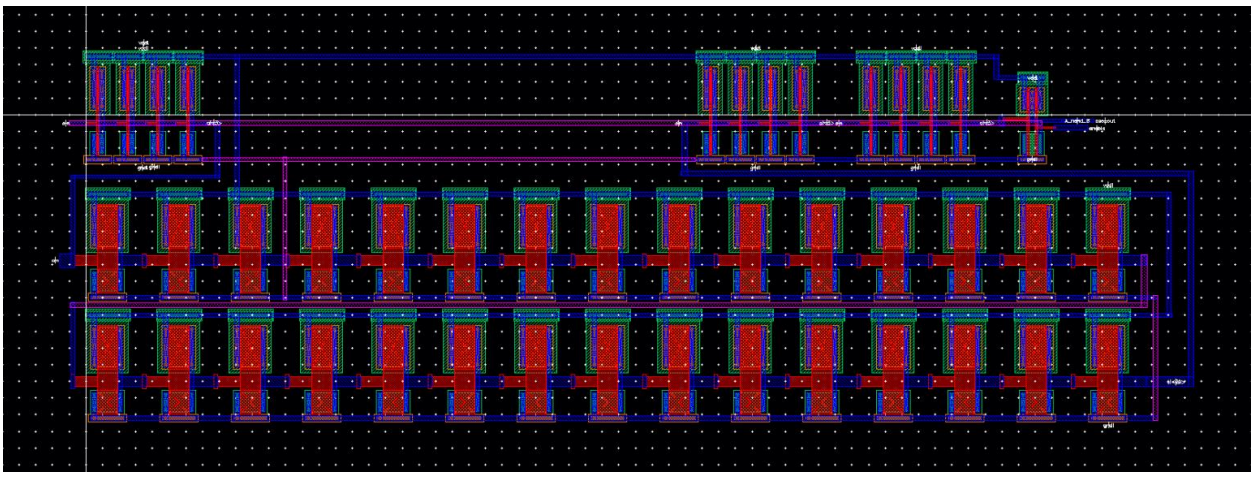

Figure 27 - Project Ring Oscillator Layout

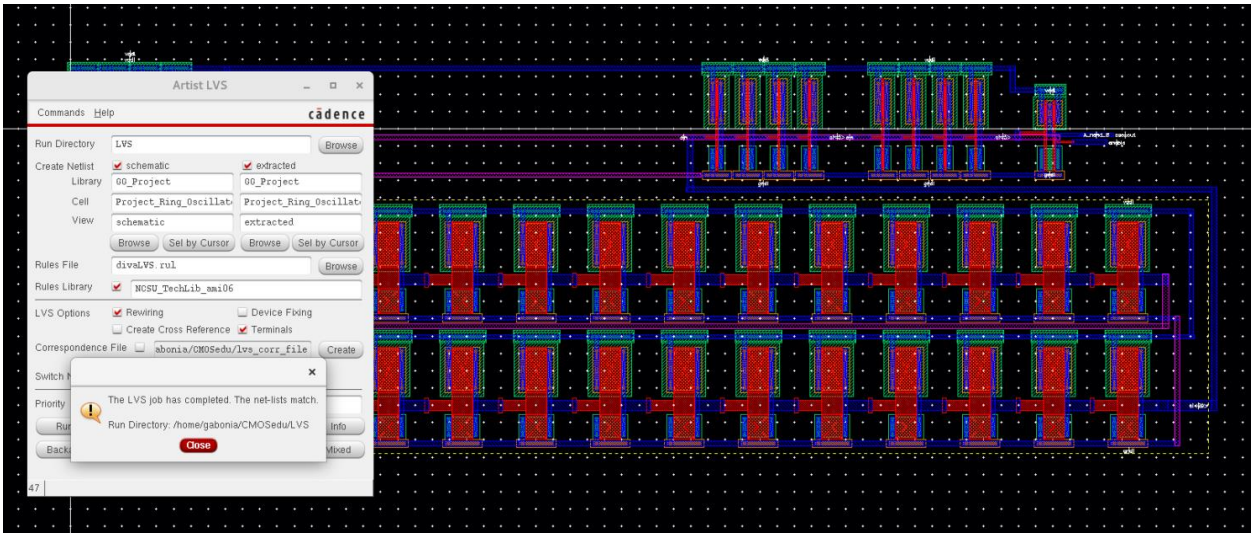

Figure 28 - Project Ring Oscillator Layout LVS

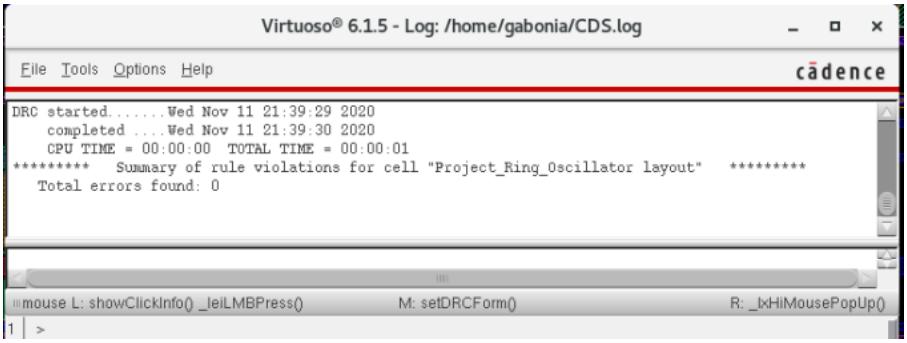

Figure 29 - Project Ring Oscillator DRC

Buffer Design

Our buffer design needs to be able to drive a 5pF load. This load is the estimated input capacitance of the power mosfet that is separate from the chip. First, calculations should be made to ensure that the buffer can effectively drive a capacitive load of 5pF.

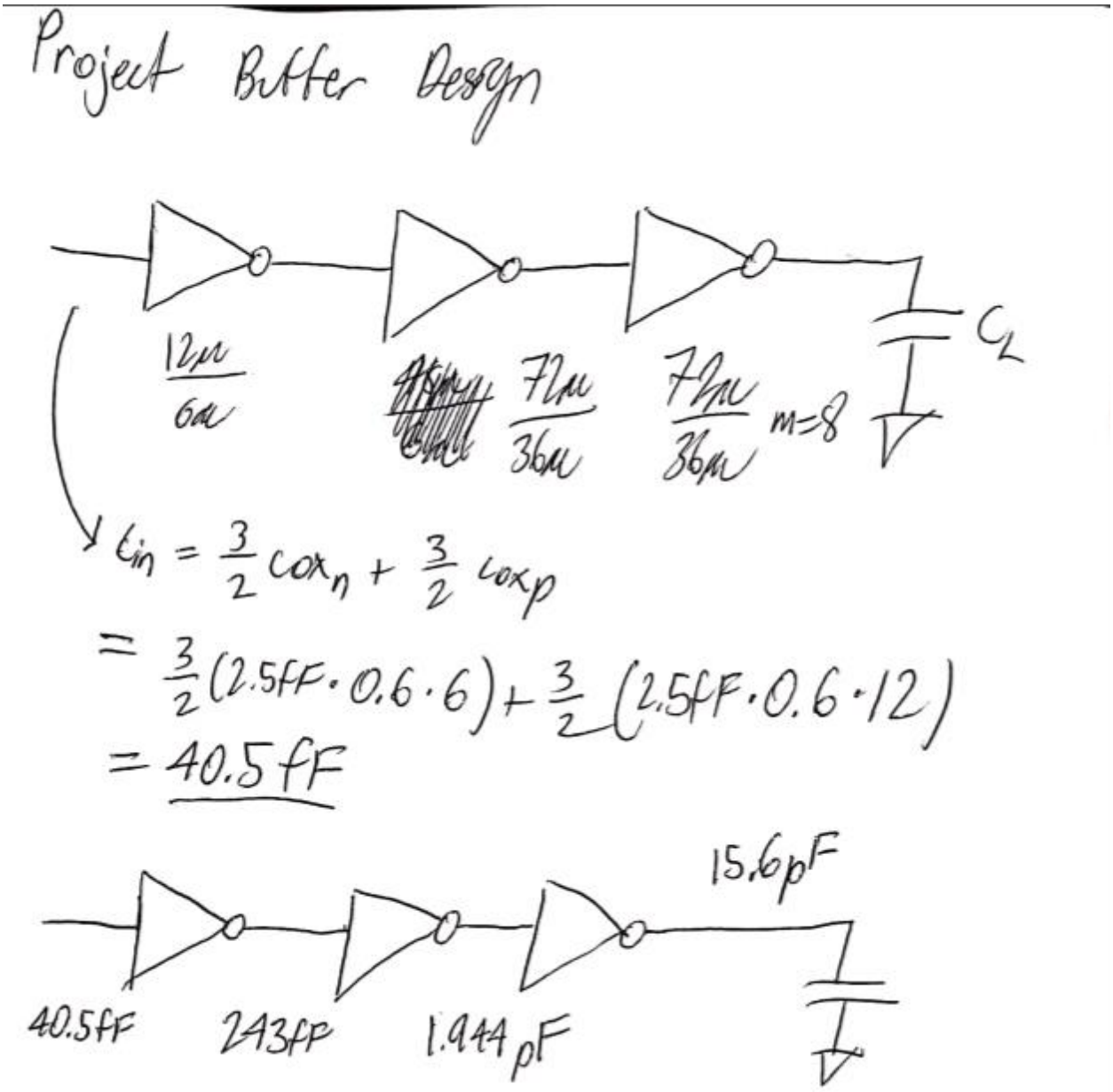

Figure 30 - Buffer Design 1 Calculations

In this first buffer design, a factor of 6 for the inverters were used. This factor of 6 using 72u/36u inverters leads to a calculation that overshoots the capacitive load goal. We can see that it hits 15.6pF. We can use a smaller factor and see if we can lower that final input capacitance.

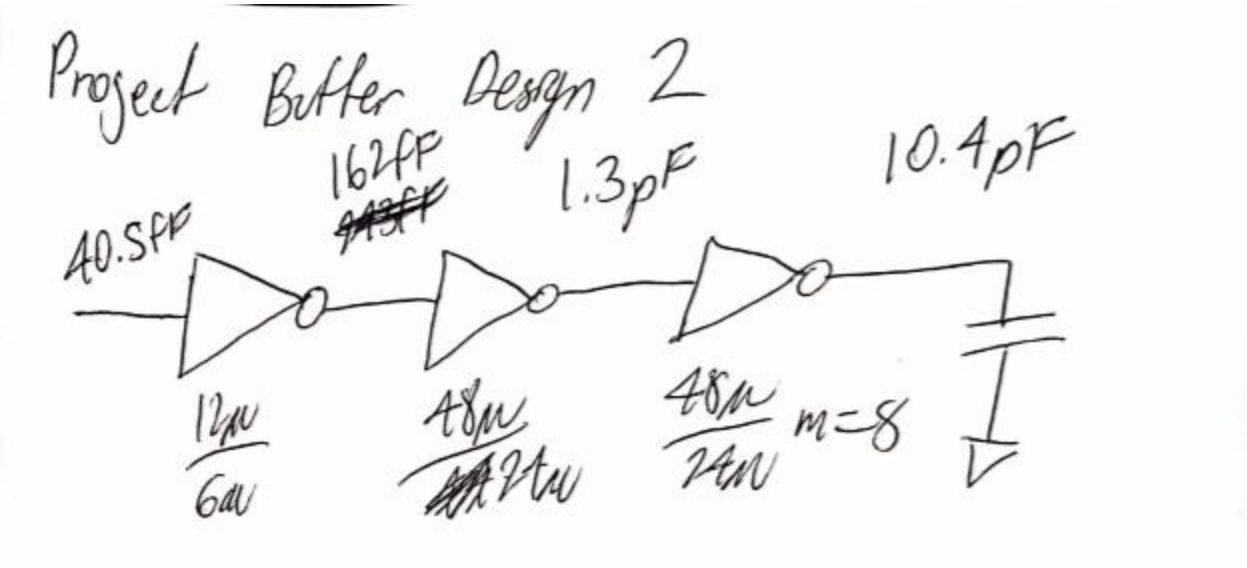

Figure 31 - Buffer Design 2

In this second buffer design, a factor of 4 was used. We can see that a factor of 4 yields a smaller final input cap of around 10pF which should be a decent starting design for driving our power mosfet load. We can easily test if this buffer design is effective with a simulation. The simulation will have an input with a frequency of 5Mhz (note that this is the output frequency for the oscillator) going into a 48u/24u m=8 inverter.

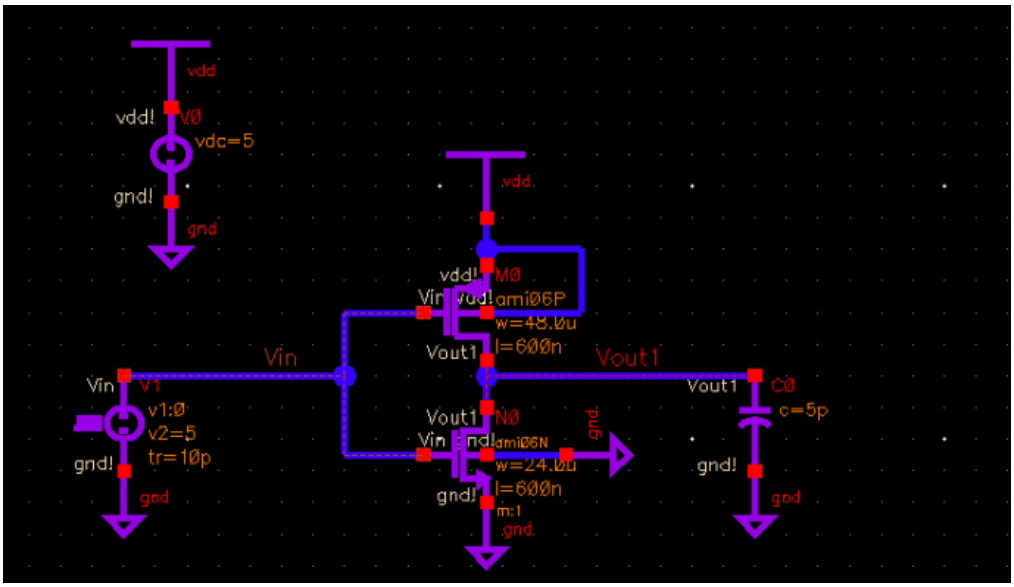

Figure 32 - Buffer Design Test

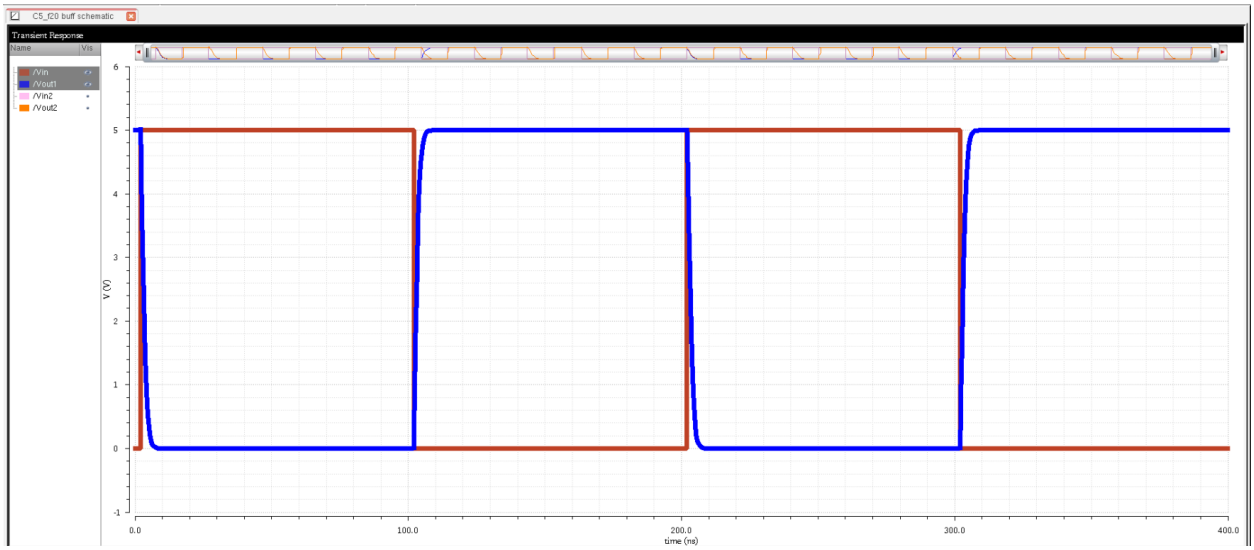

Figure 33 - Buffer Design Test Graph

Testing this buffer size shows that the inverter works, the inverter is not slow to switch at our desired frequency. Knowing this, we can now begin to create the buffer design used for the project.

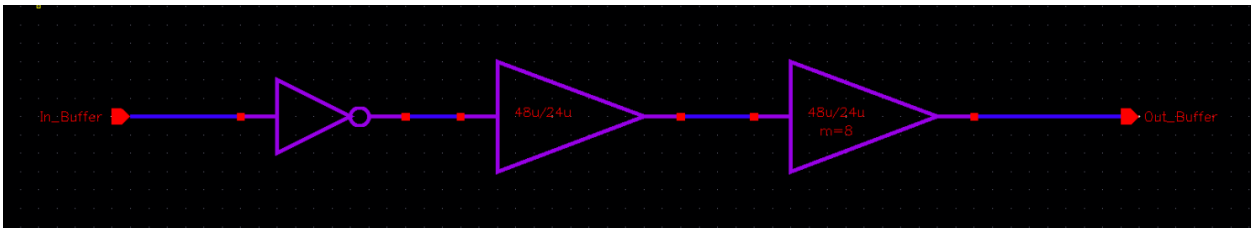

Figure 34 - Project Buffer Schematic

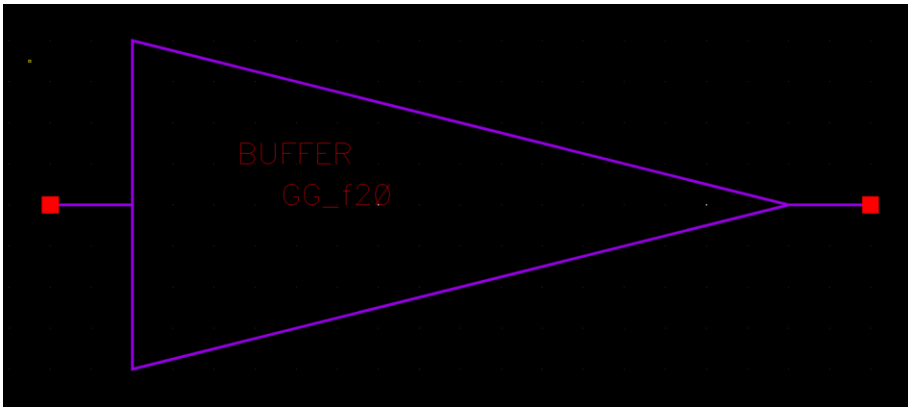

Figure 35 - Project Buffer Symbol

Now that the schematic and symbol are created for the buffer, the buffer should be tested with the 5Mhz input and with a capacitive load of 5pF.

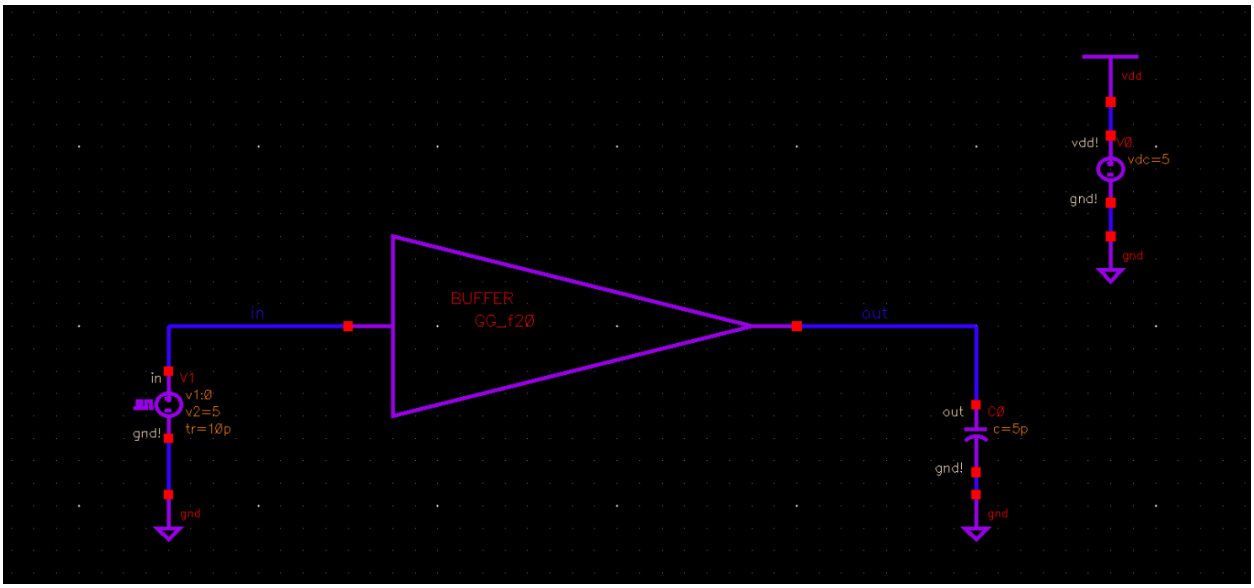

Figure 36 - Project Buffer Sim

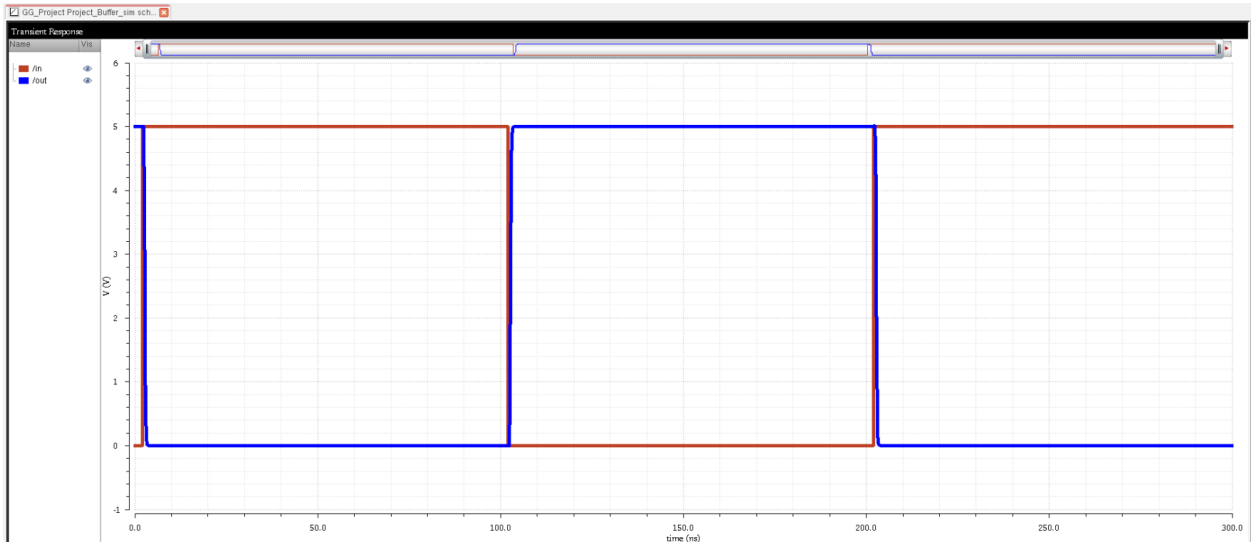

Figure 37 - Project Buffer Sim Graph

As we can see in the simulation, the project buffer works perfectly with a 5pF load at 5Mhz.

Buffer Layout

Now that the schematic of the Project Buffer is complete we can begin the layout, DRC and LVS of the circuit.

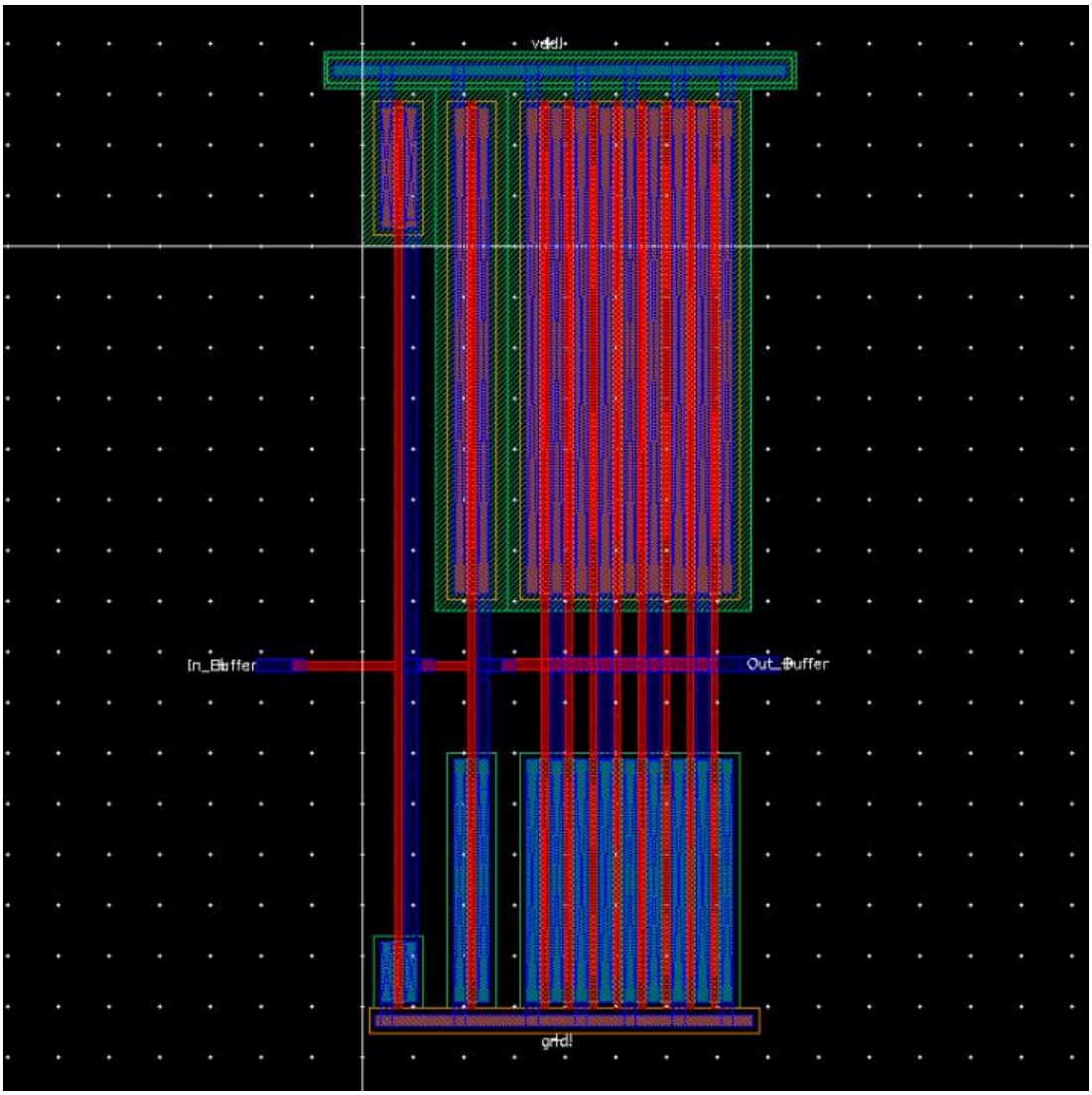

Figure 38 - Project Buffer Layout

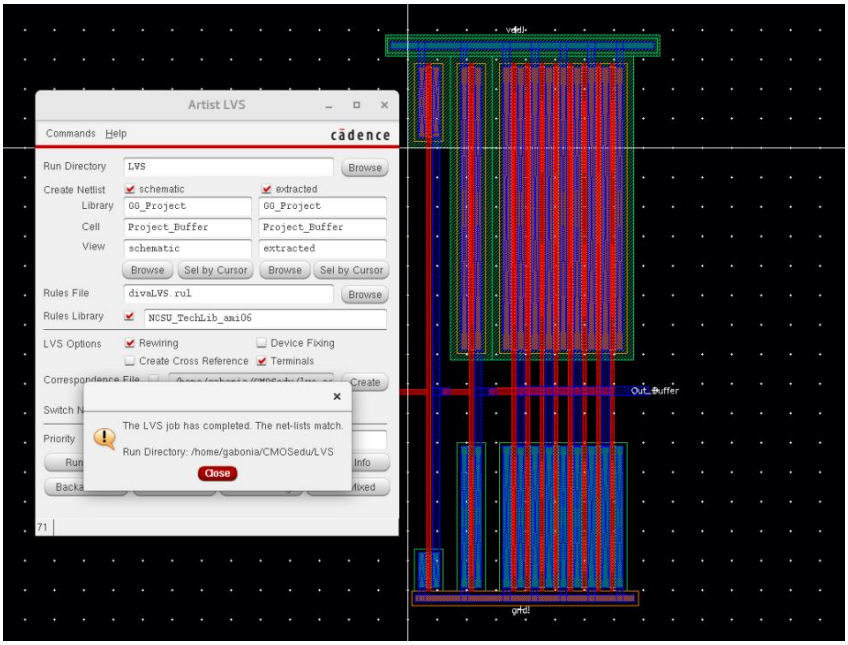

Figure 39 - Project Buffer LVS

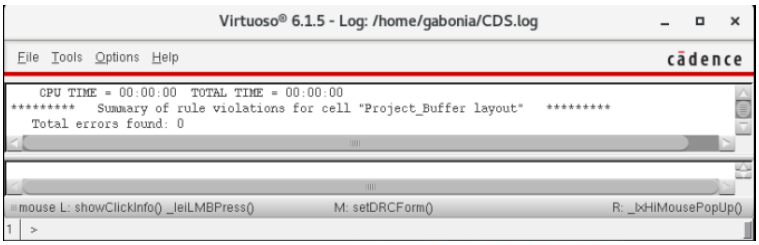

Figure 40 - Project Buffer DRC

Comparator Design

For our comparator design we will first create an nmos diff amp.

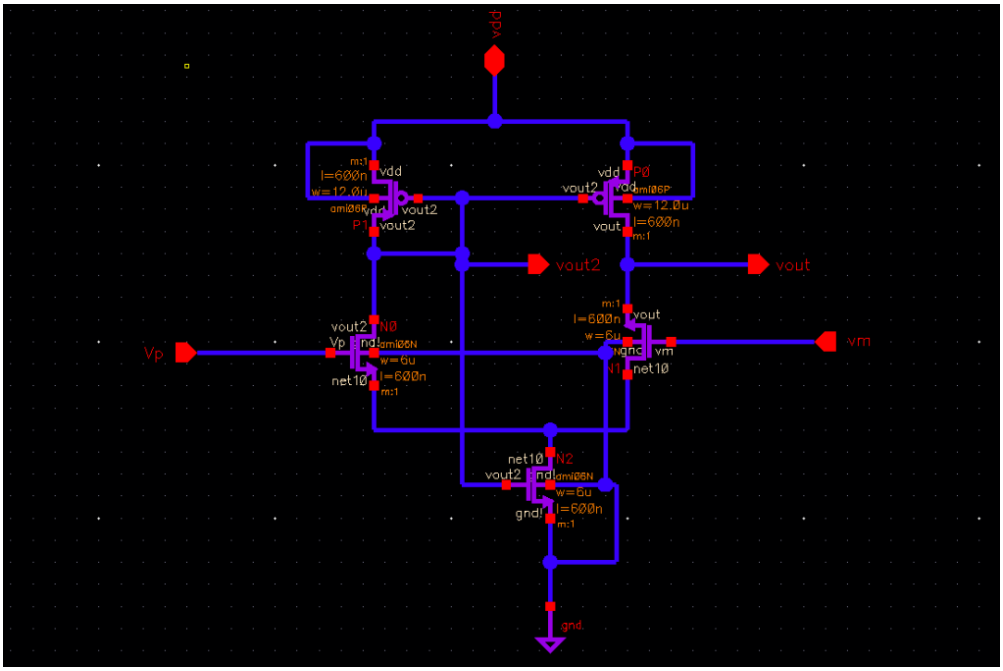

Figure 41 - NMOS Diff Amp Schematic

Note that in this circuit we have the vdd as an input output pin, we will have to switch out the other schematics to have this as well in order to begin testing all of our components together.

For this comparator we will need to have enough gain so we can start by cascading this circuit 3 times. The comparator will also need a string of inverters at the output. These inverters at the output will again help square the signal and act as a buffer to the NAND. For one of the inverters it needs to have a higher switching point which involves using a stronger PMOS. This makes sure that the signal will swing close to VDD and ground.

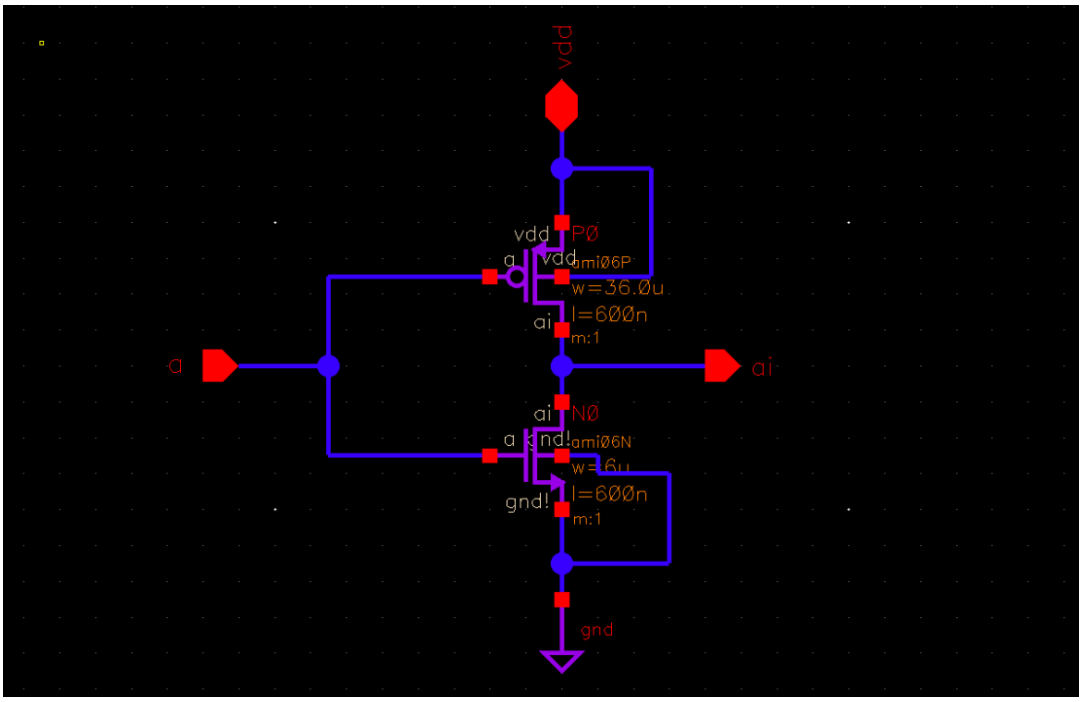

Figure 42 - Inverter High Switching Point

This inverter is a high switching point inverter with a stronger PMOS. The pmos in this inverter has a 36u width which is 3x wider than the standard inverters we use.

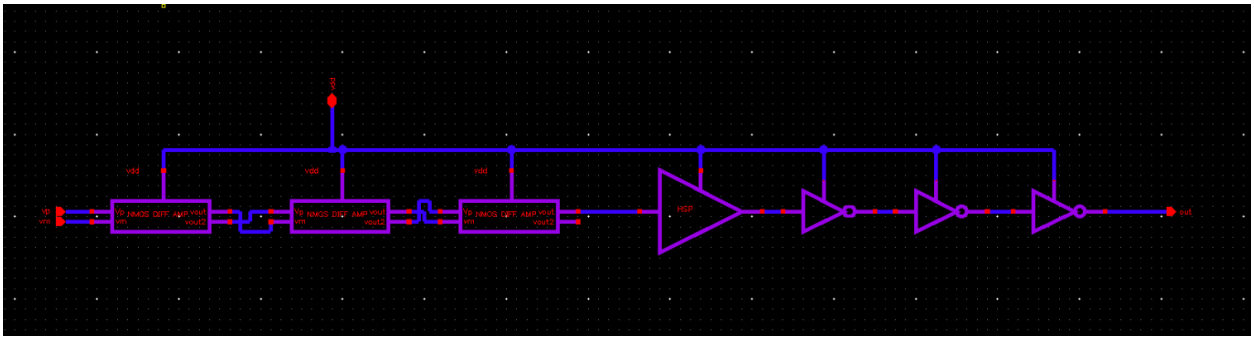

Figure 43 - Comparator Schematic

We have a total of 4 inverters in order to keep the vp and vm in the same spots.

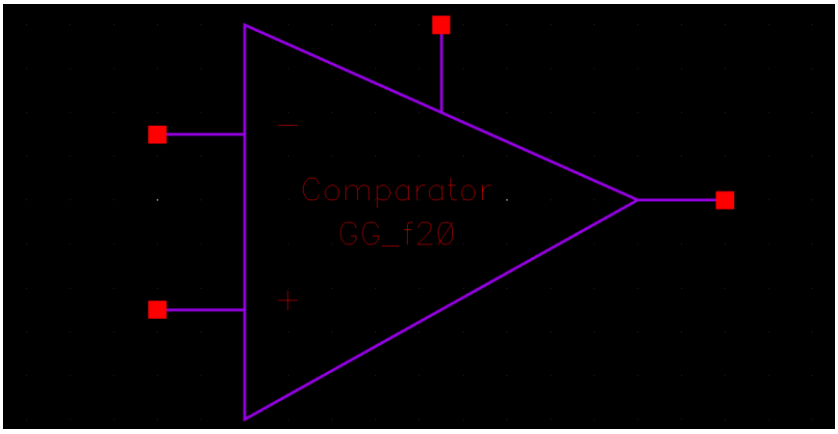

Figure 44 - Comparator Symbol

Comparator Layout

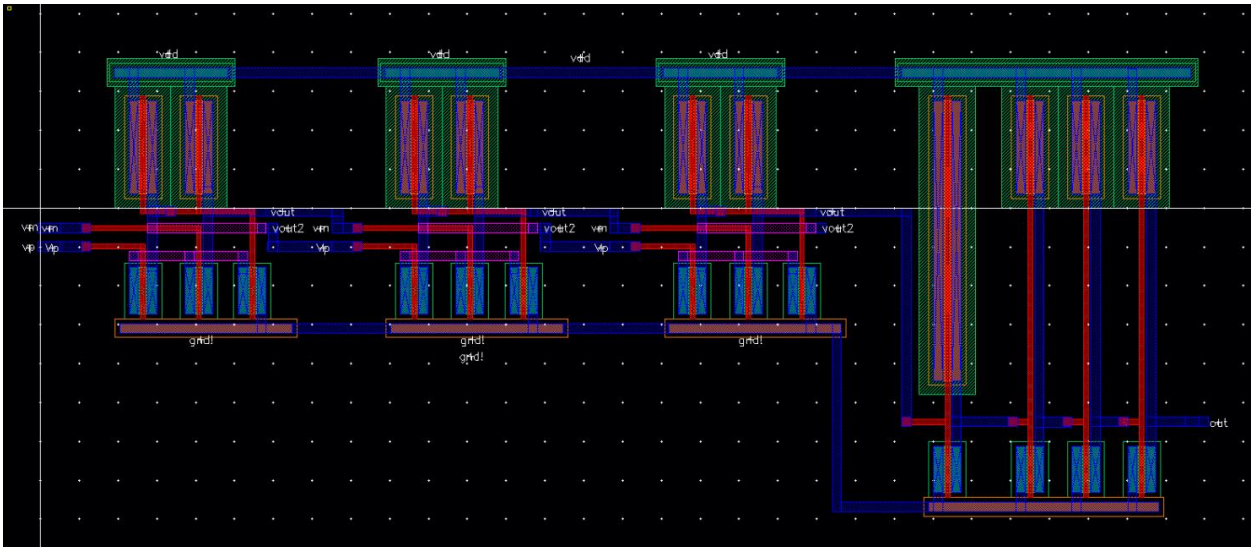

Figure 45 - Comparator Layout

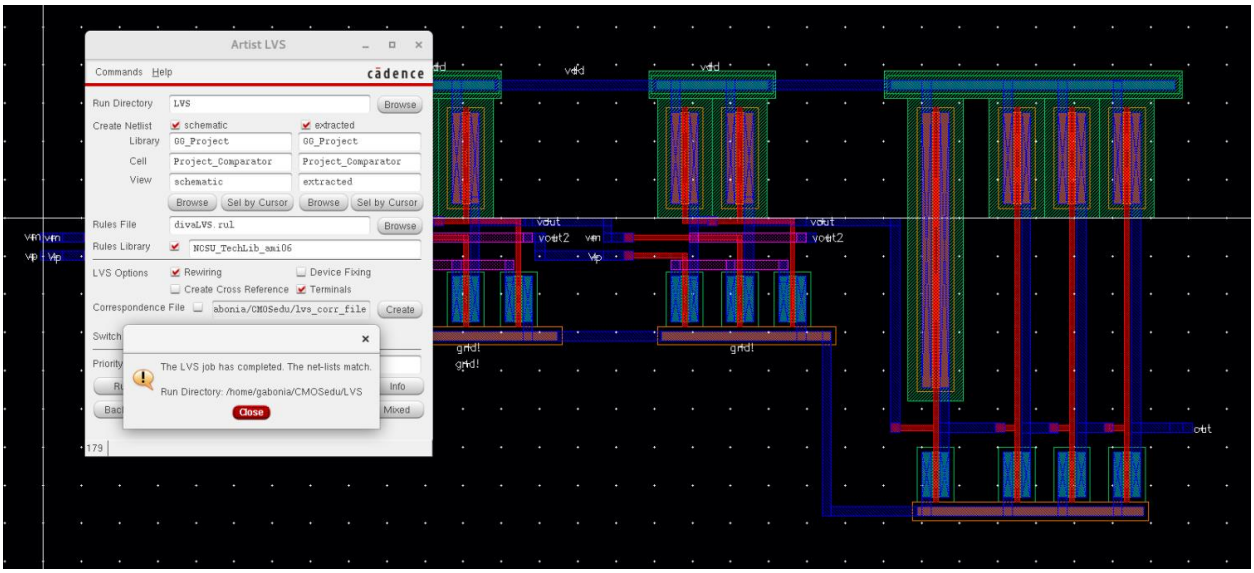

Figure 46 - Comparator Layout LVS

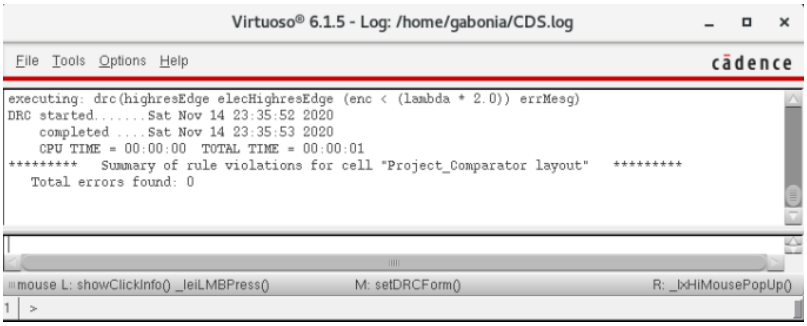

Figure 47 – Comparator Layout DRC

Flyback Converter Design and Test

We will now test all of the components put together and see if we get our desired output. The first thing that needs to be done before we put it all together is that the components need to be changed and have a vdd pin for every schematic. Once all of the desired components have a vdd pin connection added we can put it all together.

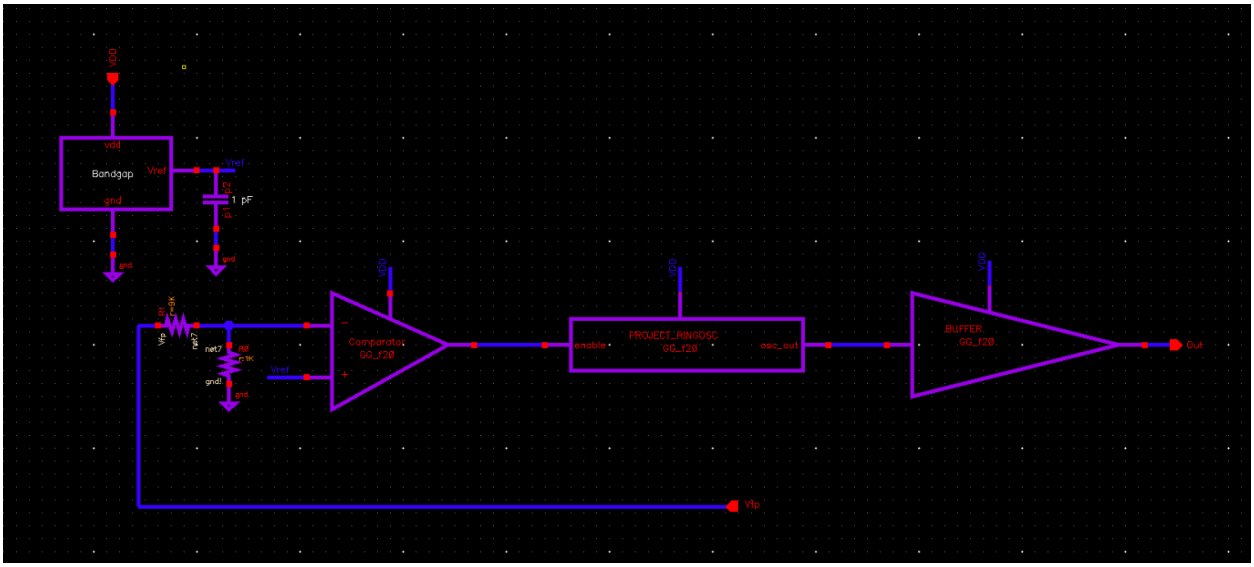

Figure 48 - Gabonia SPS Chip Project Schematic

After all of the components are put together, a symbol for the project can be created and then implemented.

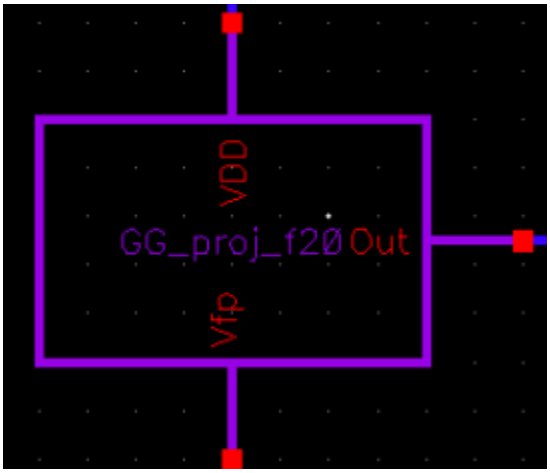

Figure 49 - Gabonia Project Symbol

Now we can test the flyback converter and simulate its function. We can plug in this project onto the sim and test it. It is important to remember to set the oscillator at an initial condition of 0 before graphing the sim. It is also important to note that the project block was copied onto the sim in the provided proj_f20 file, the library where all of these components are made are separate and doesn't have the provided sim.

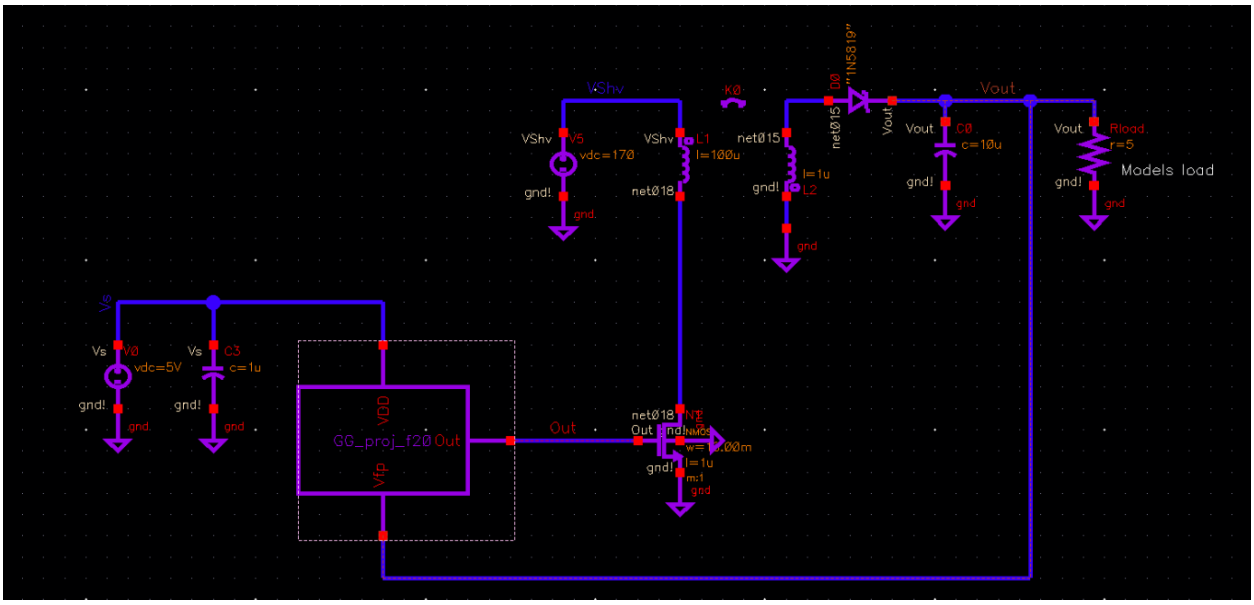

Figure 50 - Flyback Converter Sim Circuit

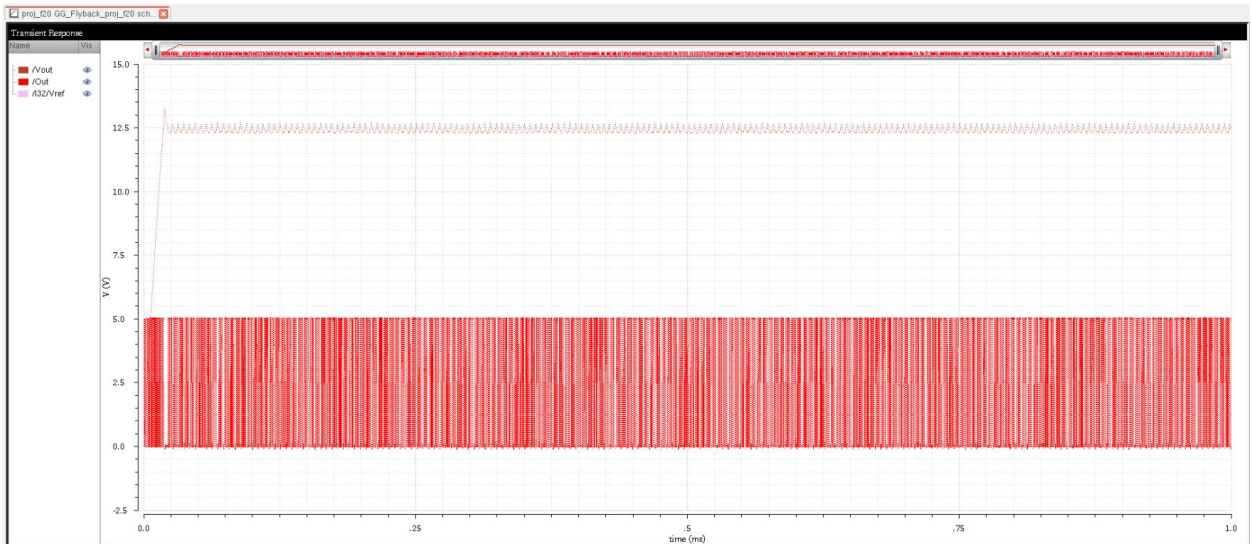

Figure 51 - Flyback Converter Simulation Graph

We can see in this graph that the flyback converter created from my design works. We can view a closeup of the graph to see clearly how it works.

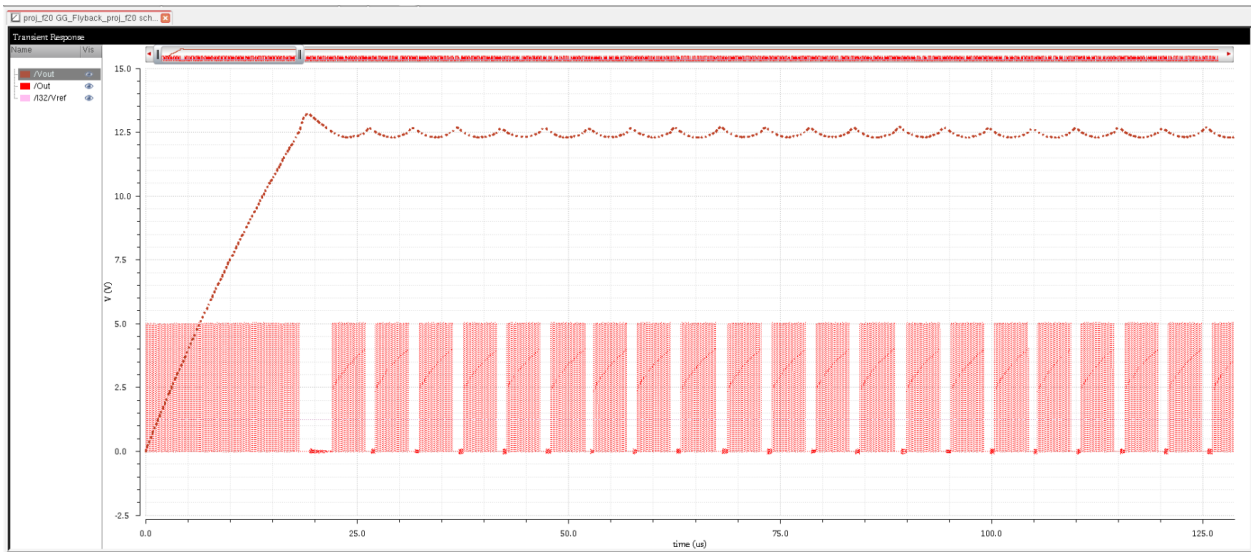

Figure 52 - Flyback Converter Simulation Graph Closeup

We can see that at a certain point when vout drops below 12.5V, the circuit begins pedaling and increases the vout to a point a little bit above 12.5V. This cycle then repeats over and over again. What is happening is that the circuit activates the power mosfet, which increases the current linearly on the 1st inductor. When the power mosfet shuts off, that current gets transferred to the next inductor through magnetic flux. This current increases the Vout.

Testing with Different Loads

Now that we know that circuit works we can test the circuit with different loads. We first tested the circuit with 5 ohms but we can start at 10 and sweep until 50 and see the difference in the simulation.

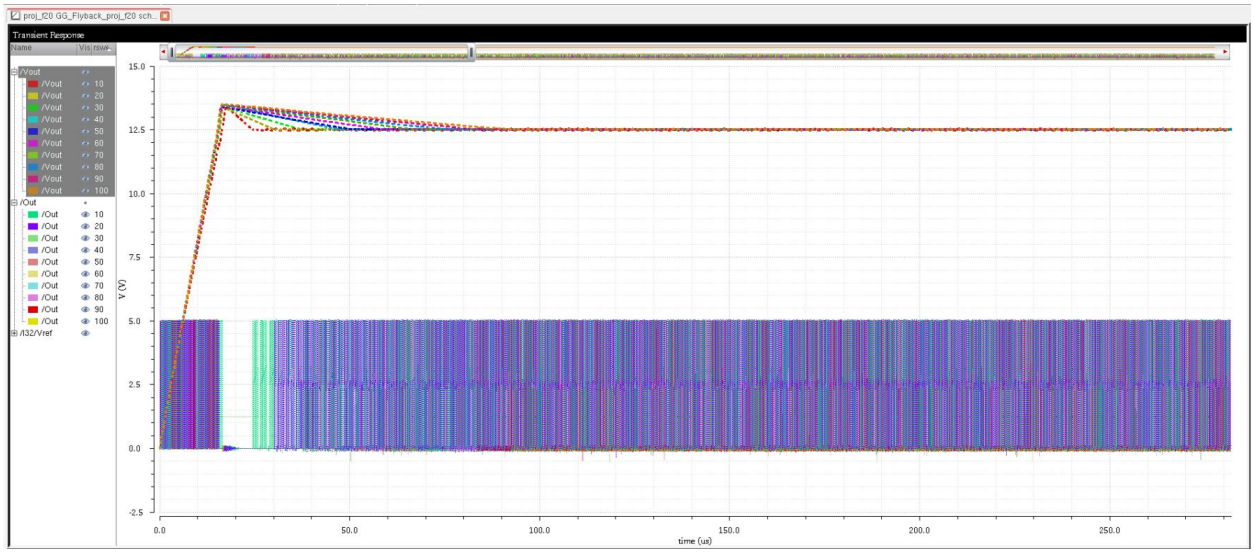

Figure 53 - Load Sweep Graph

Here the Load was swept from 10 ohms to 50ohms. As the load increased the circuit has to pedal more and more up until we get to the highest load where the circuit begins to pedal continuously as it has to work harder.

Testing at Different Temperatures

We will now bring the load back to 5 ohms and sweep the temperature from 0 to 100 in 25 step increments to see how the circuit will react.

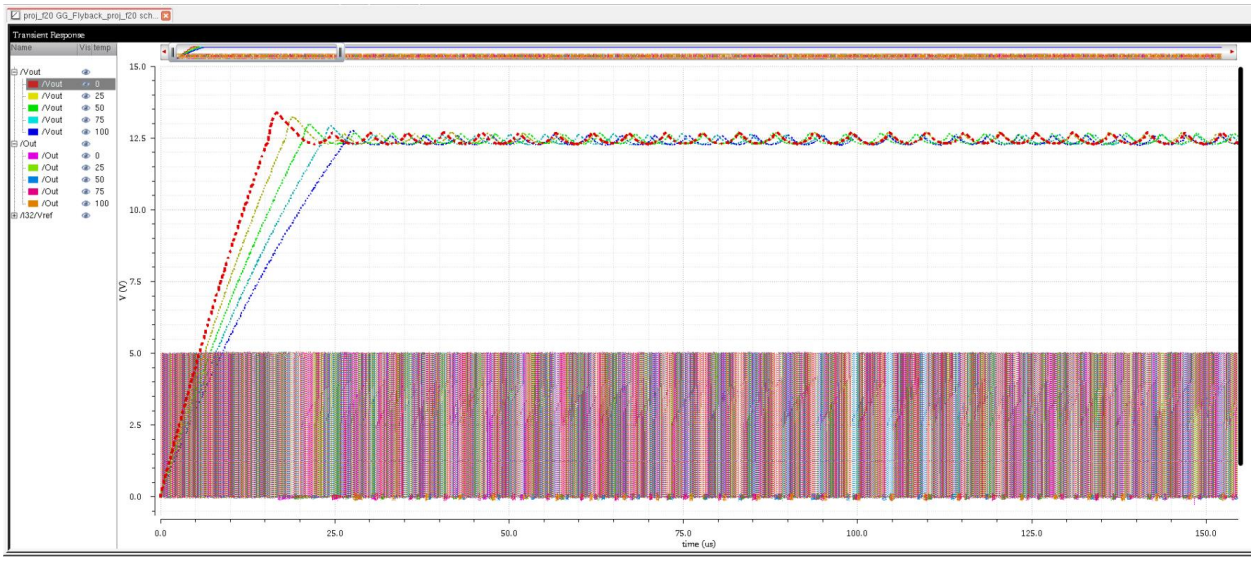

Figure 54 - Flyback Converter Temperature Sweep 1

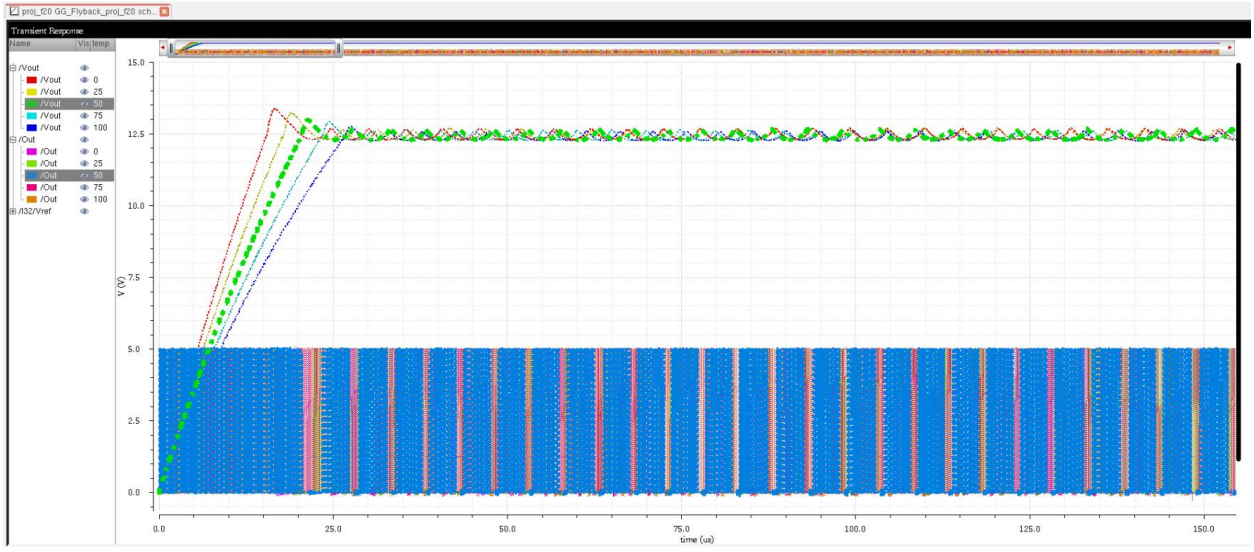

Figure 55 - Flyback Converter Temperature Sweep 2

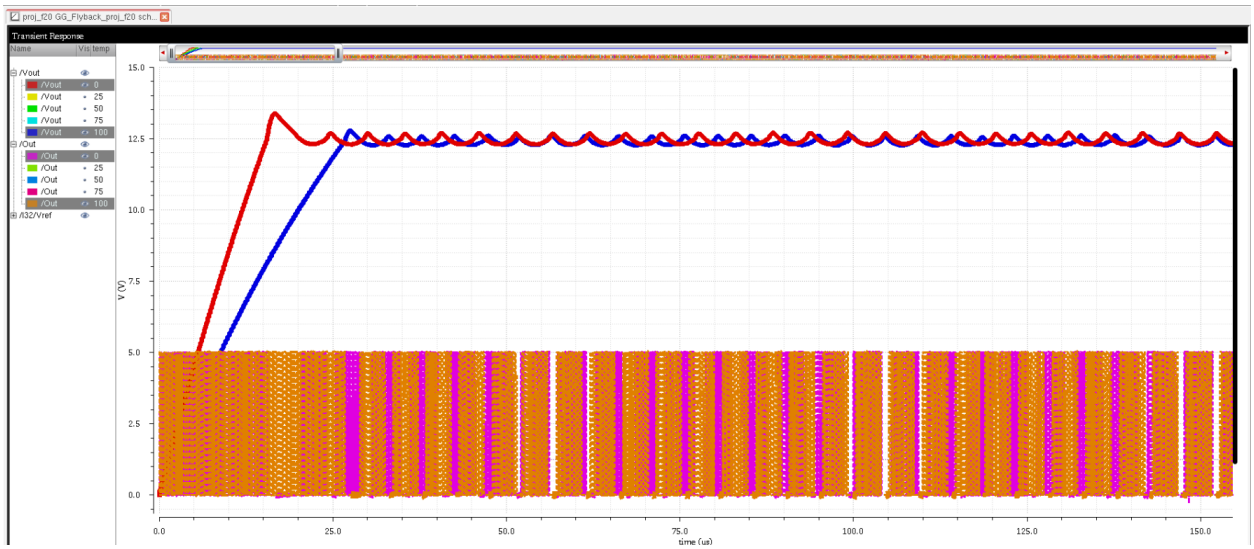

Figure 56 - Flyback Converter Temperature Sweep 3

The graph shows that the vout curves and out curves start shifting more and more to the right as the temperature increases. Initially, we can see that the vout takes longer to charge up to 12.5V. Although the curve is changing slightly, temperature has a relatively low effect on the circuit. This is likely due to the bandgap part of the schematic as the bandgap feeds a constant vref even with changes in temperature and vdd.

Testing at Different VDDs

We will now sweep the VDD from 0 to 5 and see how the circuit is affected at different VDDs.

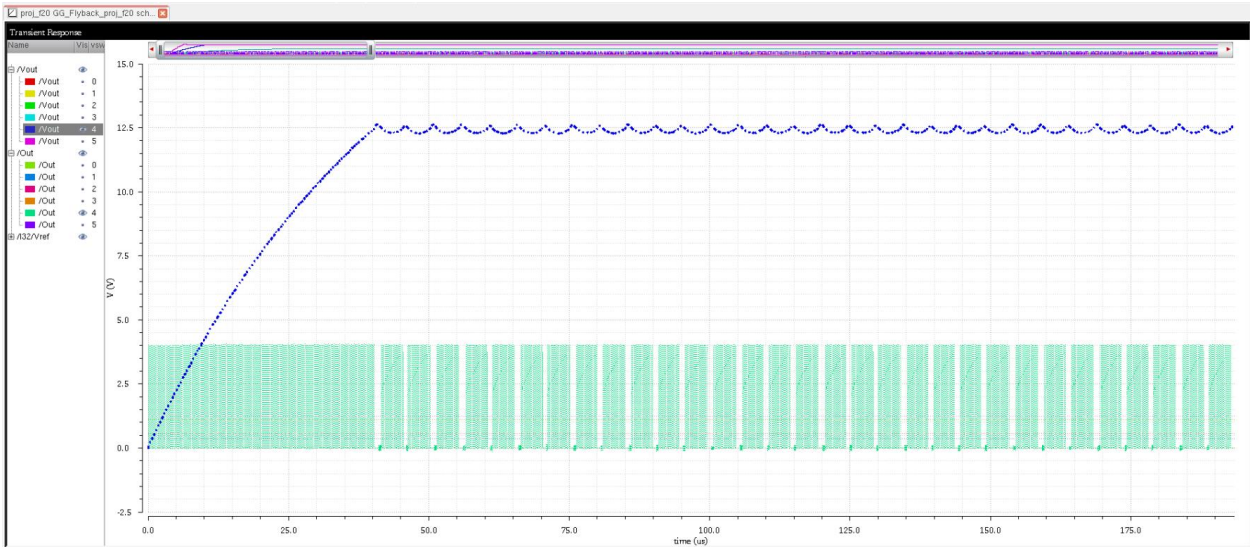

Figure 57 - Flyback Converter VDD at 4

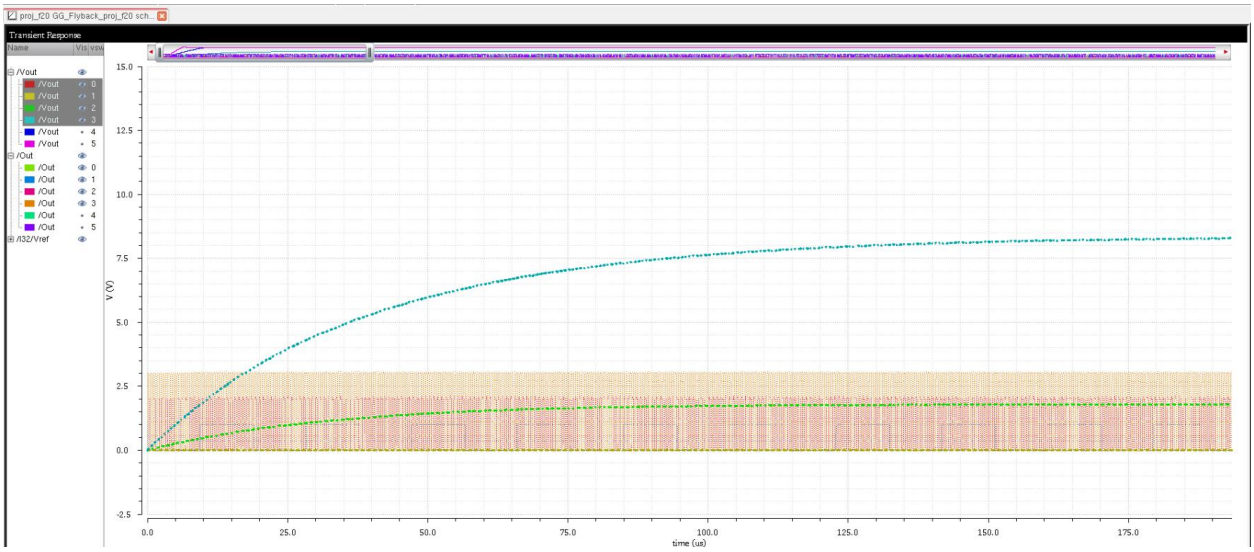

Figure 58 - Flyback Converter VDD Below 4

Based on the graphs, the circuit performs well at VDD 4 but below 4V, the circuit stops working correctly. We know from the bandgap test that Vref would start decreasing below 3.6V thus 3.6V or higher would be a better operating range.

Testing Power Throughout the Circuit

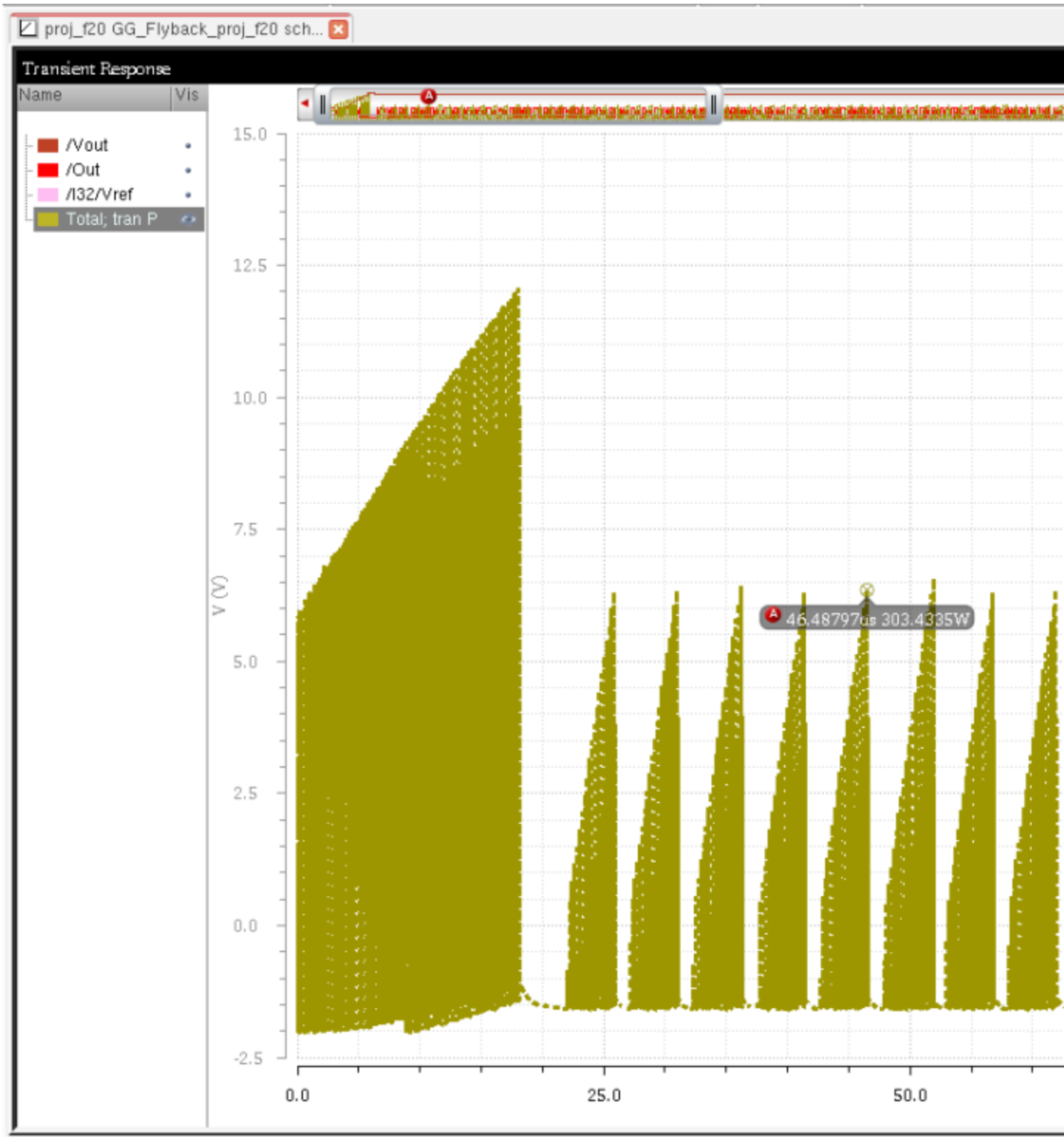

Figure 59 - Flyback Converter Power Graph

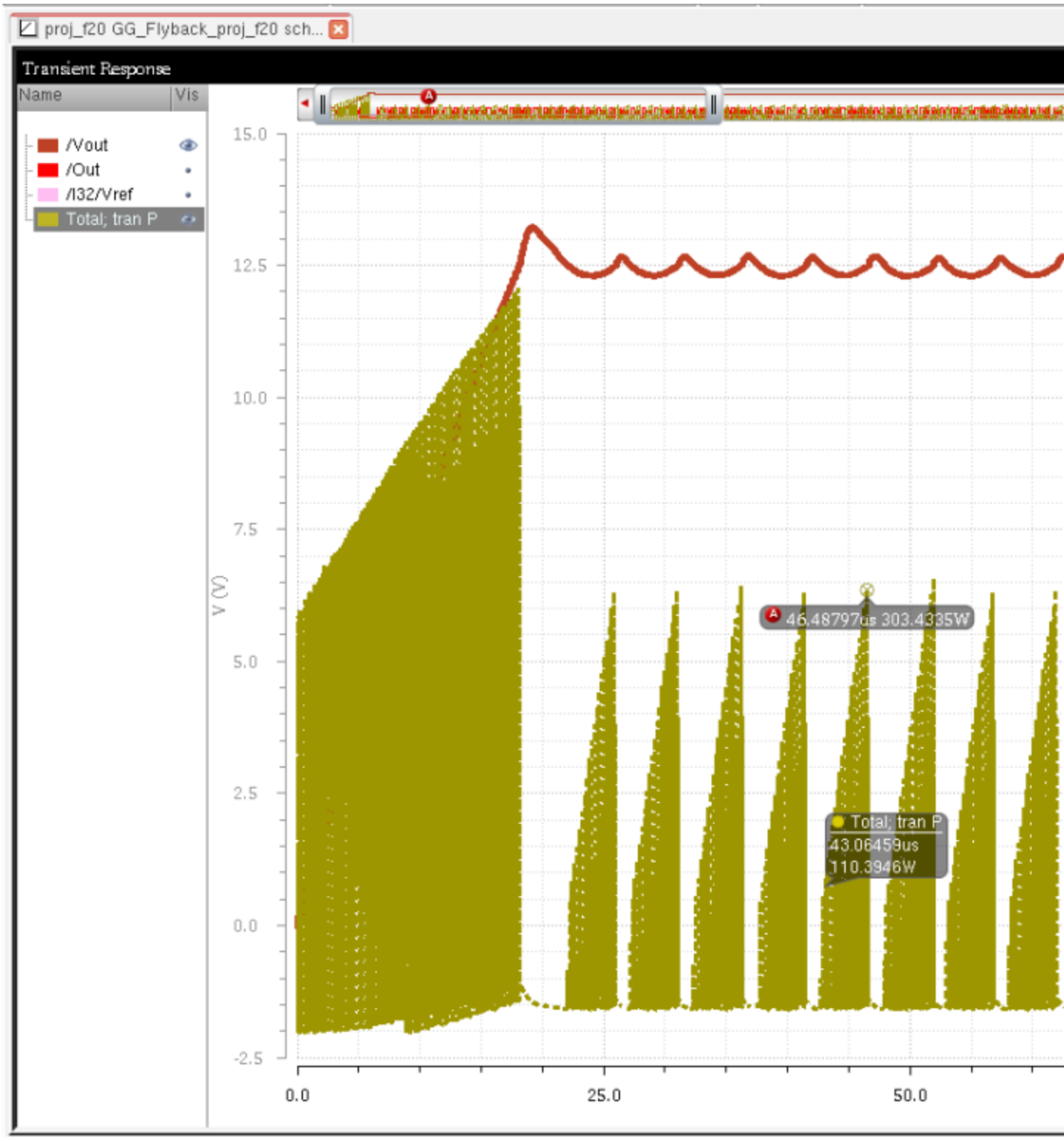

Figure 60 - Flyback Converter Power with Vout

In these graphs we can see that the power peaks at around 300 Watts after the circuit has started. Power usage starts around 100 Watts when the circuit begins pedaling from below 12.5V. When the

circuit reaches the end of pedaling the vout back up to 12.5V the power waveform is at it's peak where it then drops and the cycle restarts as the circuit drops down to below 12.5V again.

SPS Chip Layout

Laying out the full project involves putting all of the separate component layouts together into one big layout. We first need to create some missing pieces, the 1K and 9K resistor. Afterwards, we can instantiate all of our components onto the layout and make the appropriate connections.

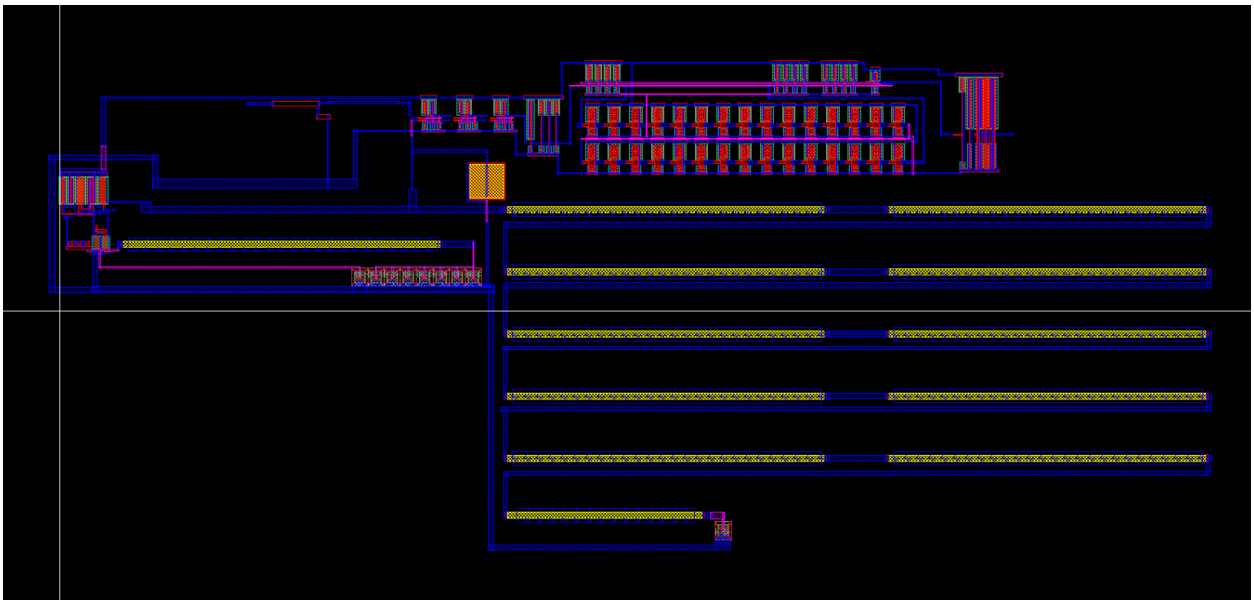

Figure 61 - Full Project Layout

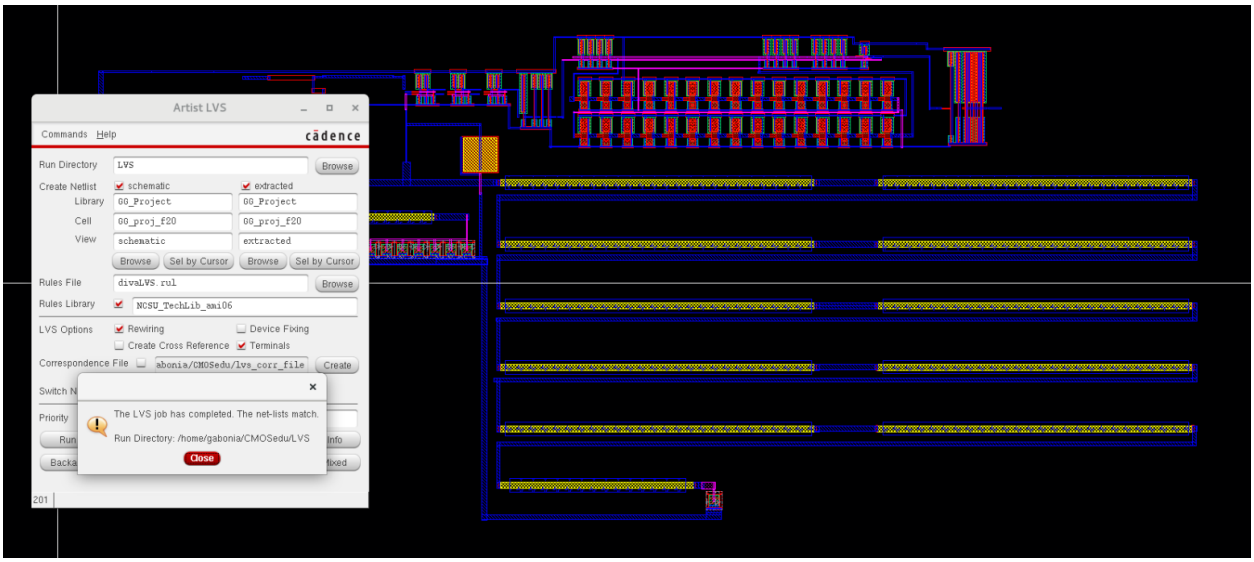

Figure 62 - Project Layout LVS

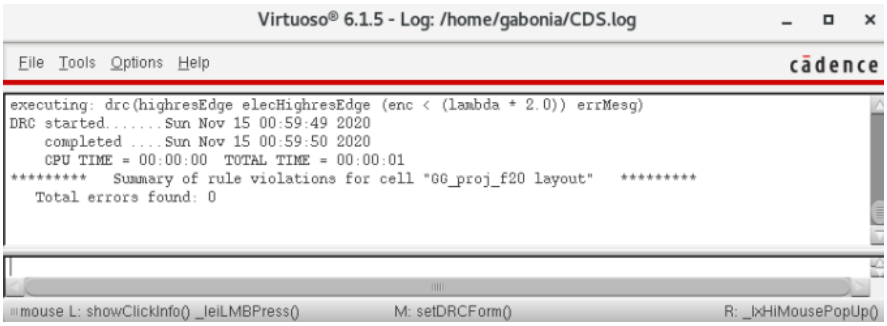

Figure 63 - Project Layout DRC

Project Summary

If someone were to look at my design, they should focus on the design of the comparator. Improving the comparator design would improve the function of the flyback converter simulation. In my comparator design I used standard mosfet sizes of 12u/6u for PMOS and NMOS and did a 3 times cascade on the NMOS diff amp with 4 connecting inverters on the output. I believe there would be a way to reduce the amount of power that would be consumed by using all of those components. One way might be reducing the amount of inverters being used on the output. Another way would be to reduce the gain on the cascaded nmos diff amps by either adjusting the current going through each or reducing the amount of cascades. Introducing hysteresis into the design might have also made the output of the flyback converter better.