Bryan Callaway

Dr. Baker

EE421

29th November 2020

Switching Power Supply (SPS) Controller Chip for a Flyback SPS Design

Task:

EE 421/ECG 621 project is to design a switching power supply (SPS) controller chip for a flyback SPS.

Flyback SPSs are found in virtually all off-line (from 120V AC) power supplies such as those in USB, phone chargers, laptop supplies, etc. that plug into the wall.

- Your design symbol should have the same footprint as the one seen below so that it can be placed in the simulation to determine if it works correctly.
- Your design is a chip to be used on a printed circuit board with the rest of the components seen below.
- The two DC supplies seen below (170V and 5V) are generated with half-wave rectifiers from the AC line and an additional low voltage tap on the transformer (neither shown below).
- The output of your circuit should be nominally 12.5V and be able to supply well beyond 2A of current to a load. Your design should work with other load currents too including 0, 10mA, 200 mA, etc.
- The controller chip (seen below) in the simulations found in proj_f20.zip use nearly ideal components. You need to design a replacement using real CMOS in C5.

- Your design should use the bandgap voltage reference you laid out in HW#13. This bandgap is used in the design seen below
- You should submit a report characterizing your design, specifically the design considerations and associated schematics, and tables characterizing the behavior (especially power from the 5V supply), clear and concise (!) images of some simulations used to generate the data you entered in your tables.
    - For example, how does your design work at VDD = 4V and temperature of 100C? Characterize your design with changes in temperature and VDD.

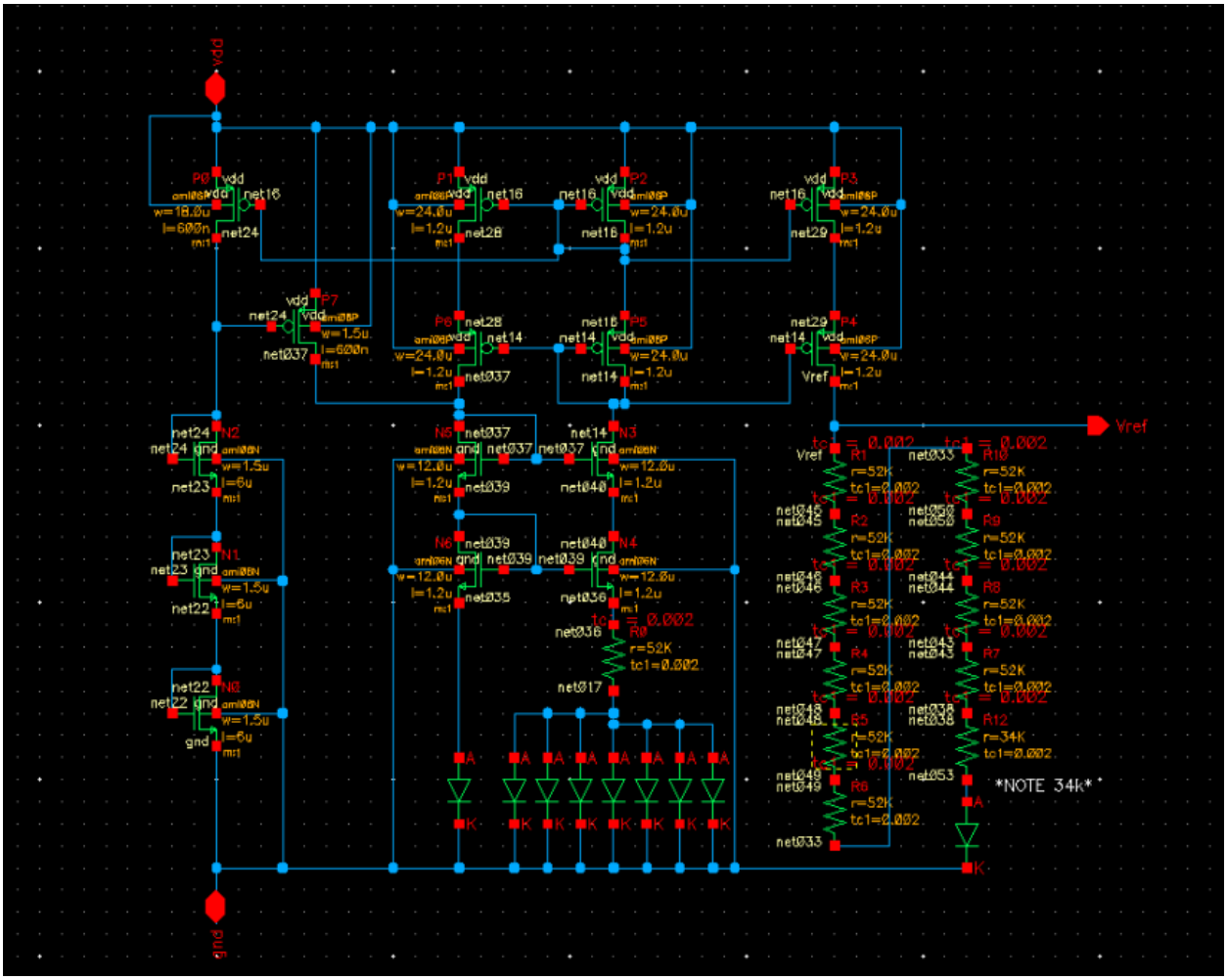
- Your report should also detail where you think someone trying to improve your design (future work) should focus their time and efforts.
    - Turning in a bunch of images with no coherent associated narrative or just turning in a report with no coherent organization or flow will receive a very low grade (the point is that the design needs to work well, as indicated by simulations, AND your report has to detail the performance of your design and why you did what you did.)
- **I should receive the PDF of the electronic report and a zipped–up directory of your design via email (r.jacob.baker@unlv.edu) before 5 pm on Friday, December 4, 2020. Receiving the project via email at 5:01 pm, as indicated in my email mailbox, or later will result in a significant penalty.**

Design:

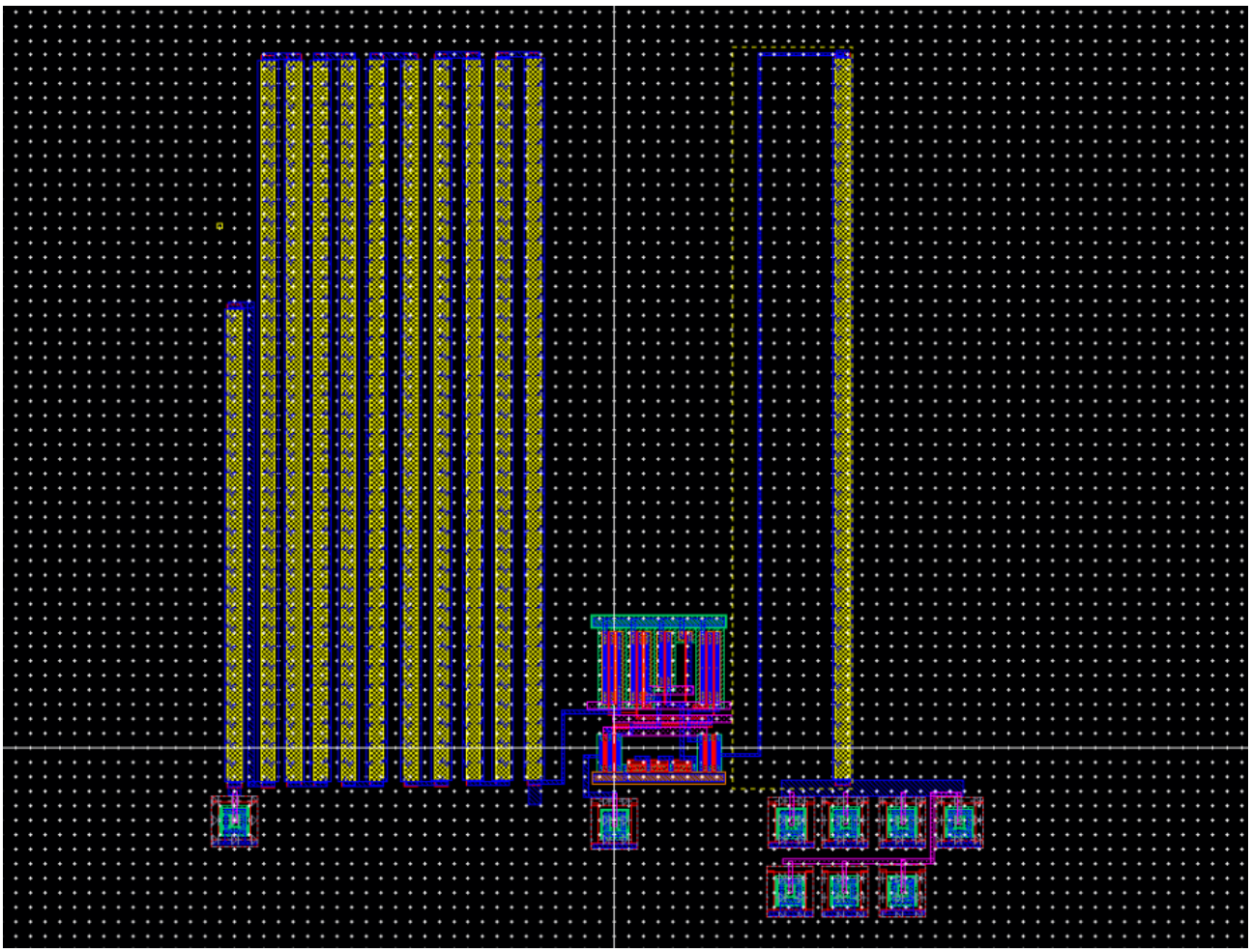
Bandgap:

The bandgap of this controller chip is utilized in order to generate a constant reference voltage that is independent to changes in temperature, power supply variations, and circuit loading from a device. This reference voltage is used for our comparator.

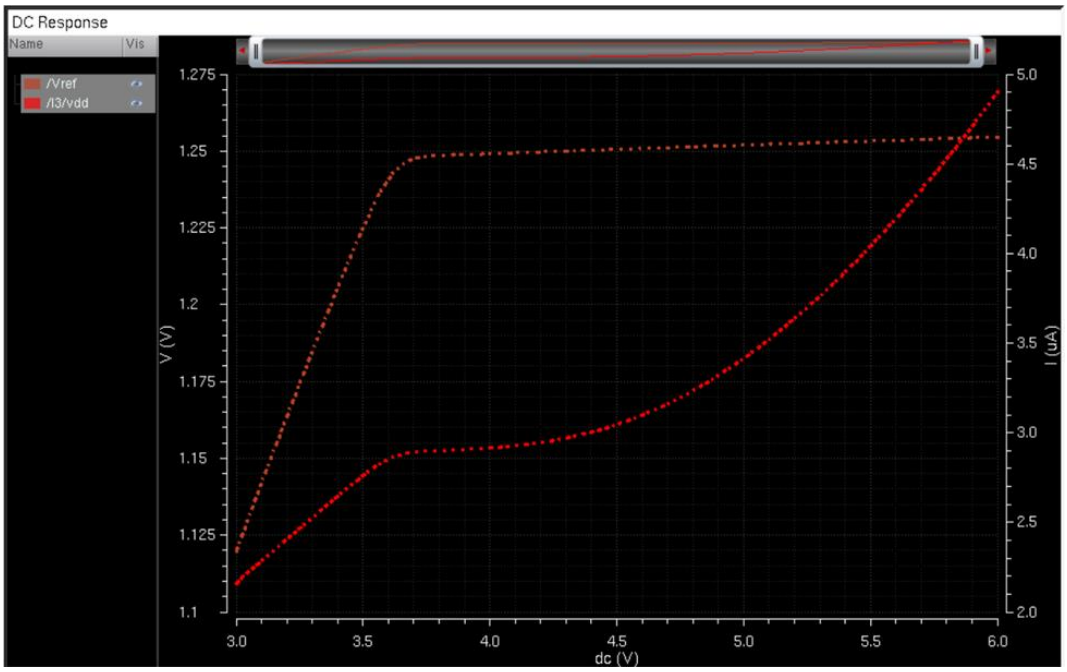
Schematic:



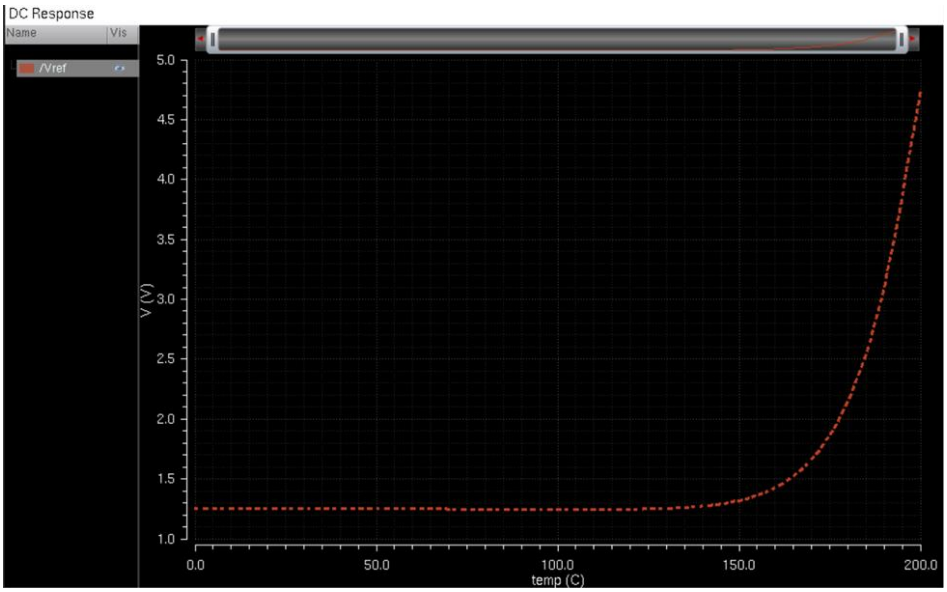
Layout:



Simulation results:



We can see that the output voltage does not vary much with changes to the input voltage. A voltage below 3.6V will cause Vref to start decreasing.

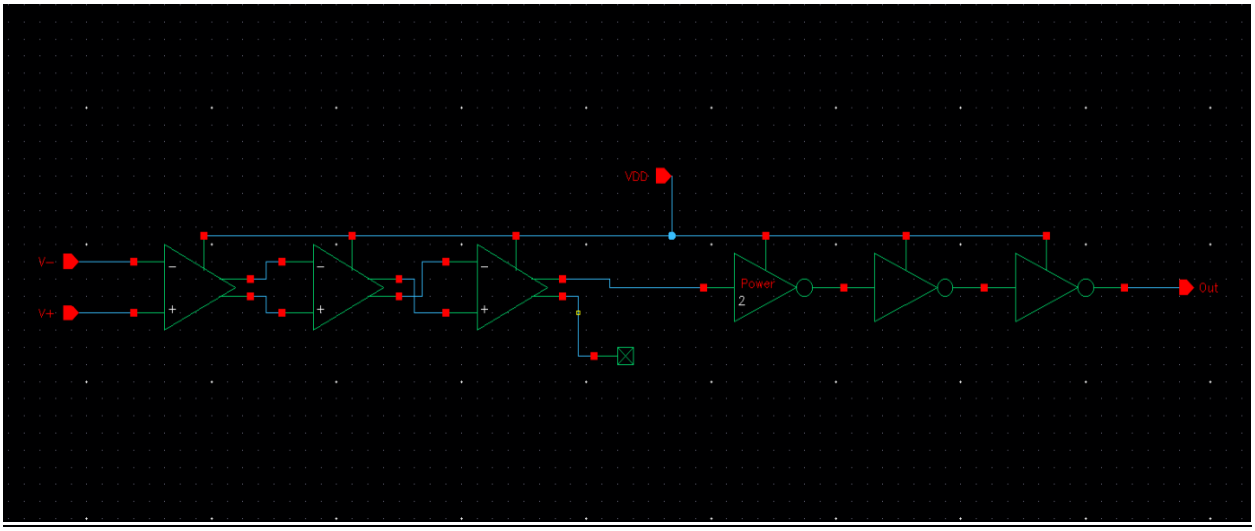


The bandgap circuit works for a wide range of temperatures. It seems to work well up to 150°C.

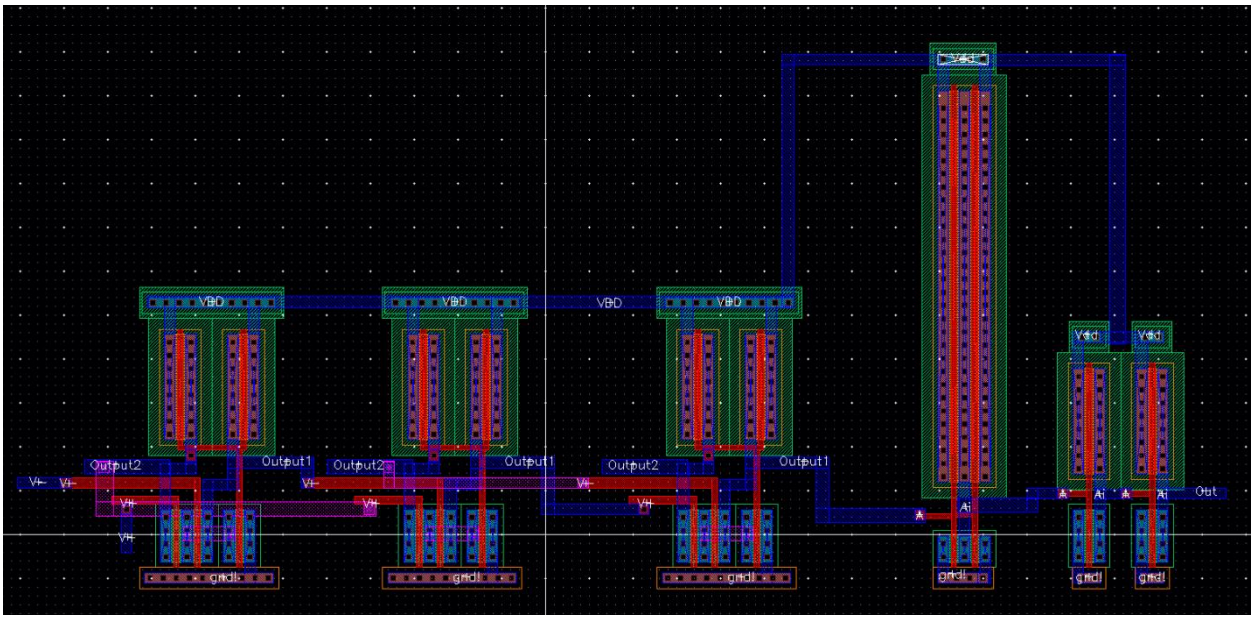
Comparator:

The bandgap voltage is applied to the V_+ input of the comparator and the V_- input of the comparator is connected to the output of the flyback SPS (V_{fp}). If $V_+ > V_-$ then V_{out} (the output of the comparator) is 1, if $V_+ < V_-$ then V_{out} is 0.

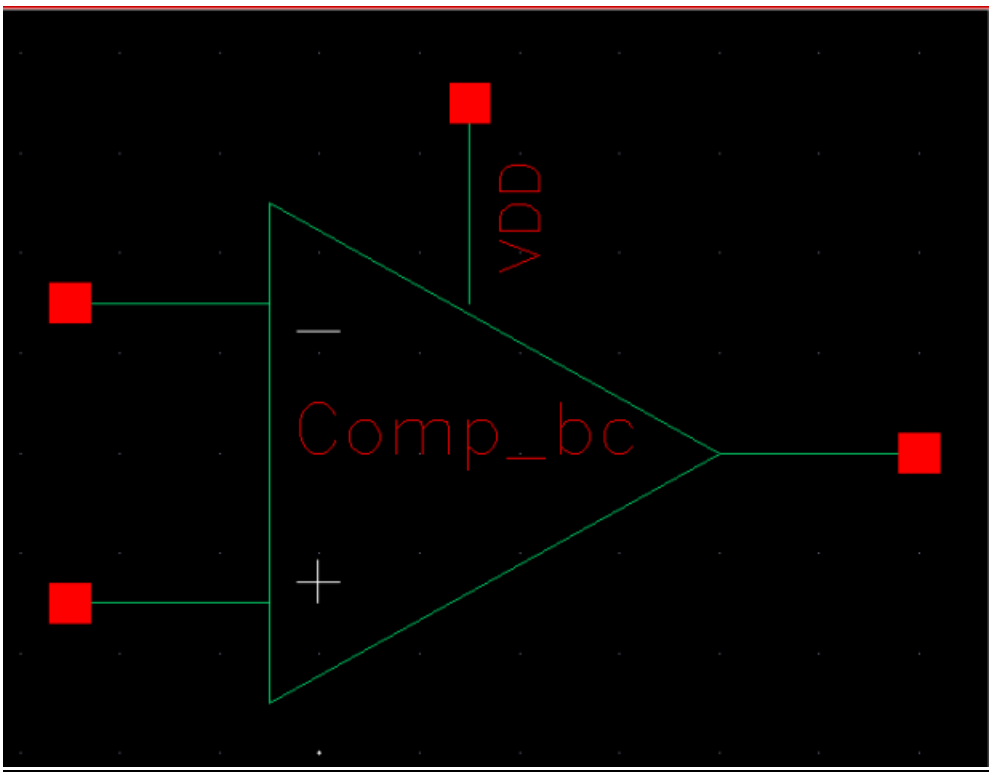
Schematic:



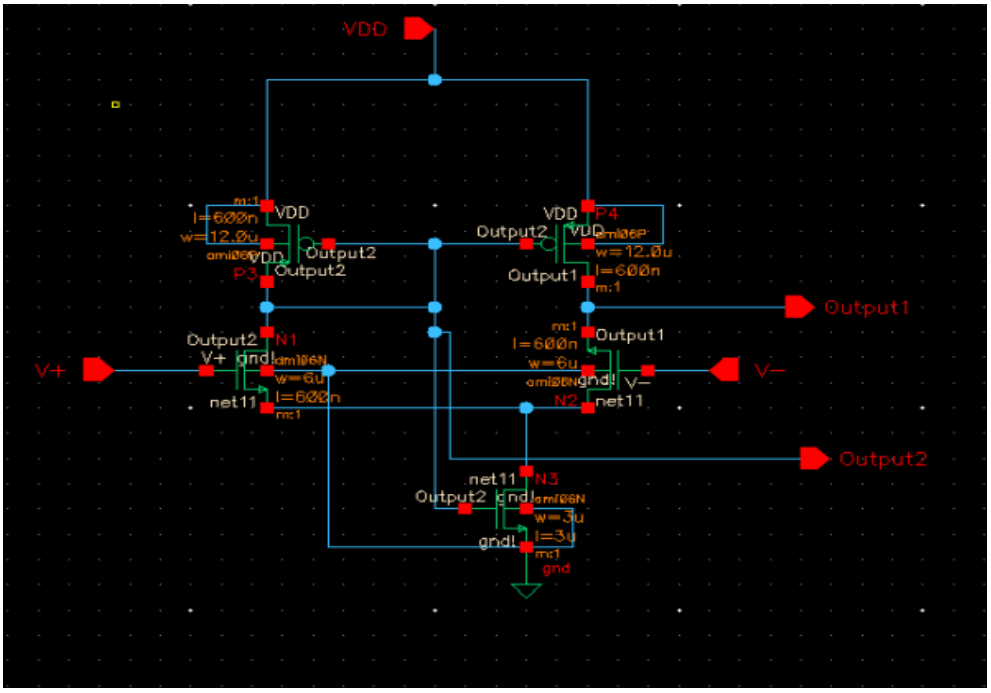
Layout:



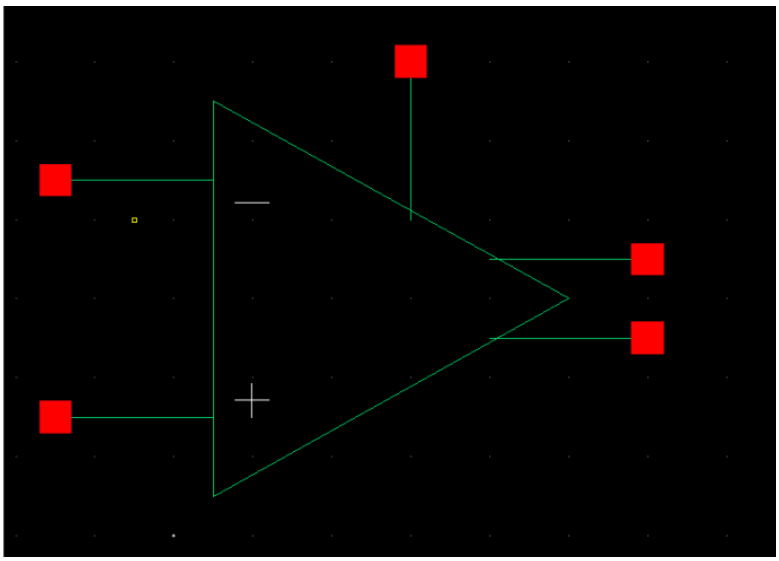
Symbol:



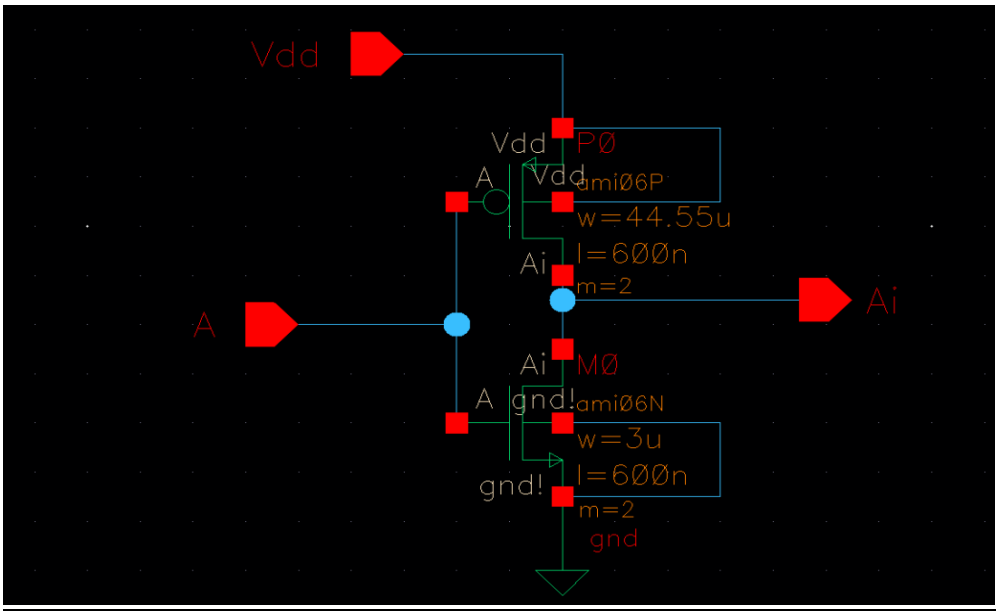
Differential Amplifier schematic:



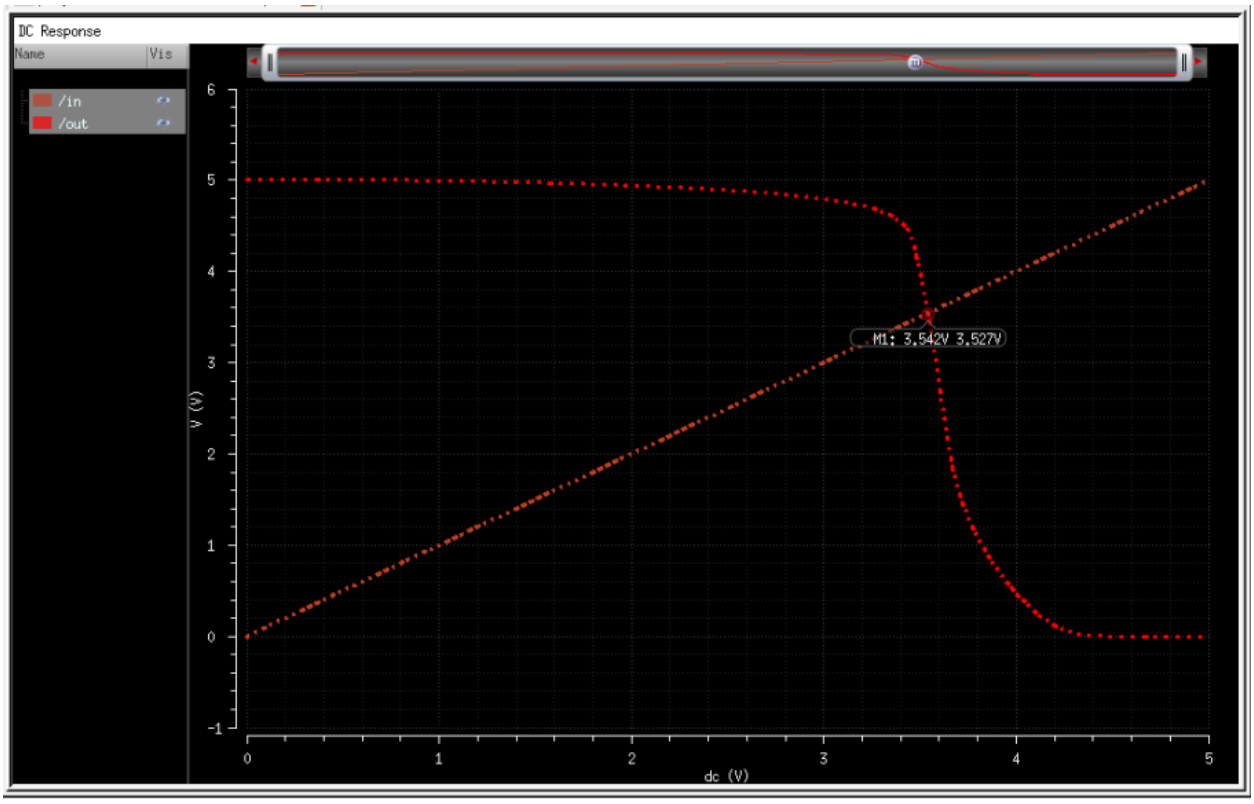
Differential Amplifier symbol:

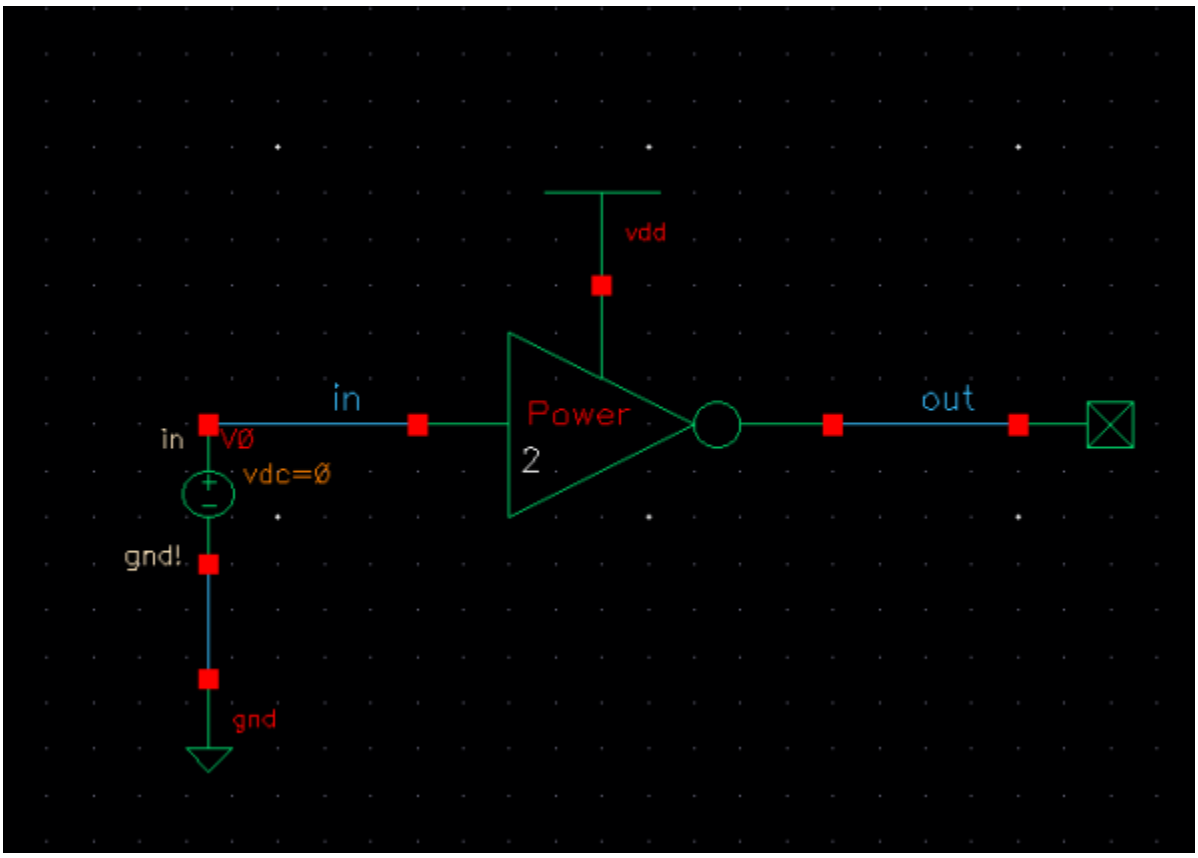


"Power 2" inverter:



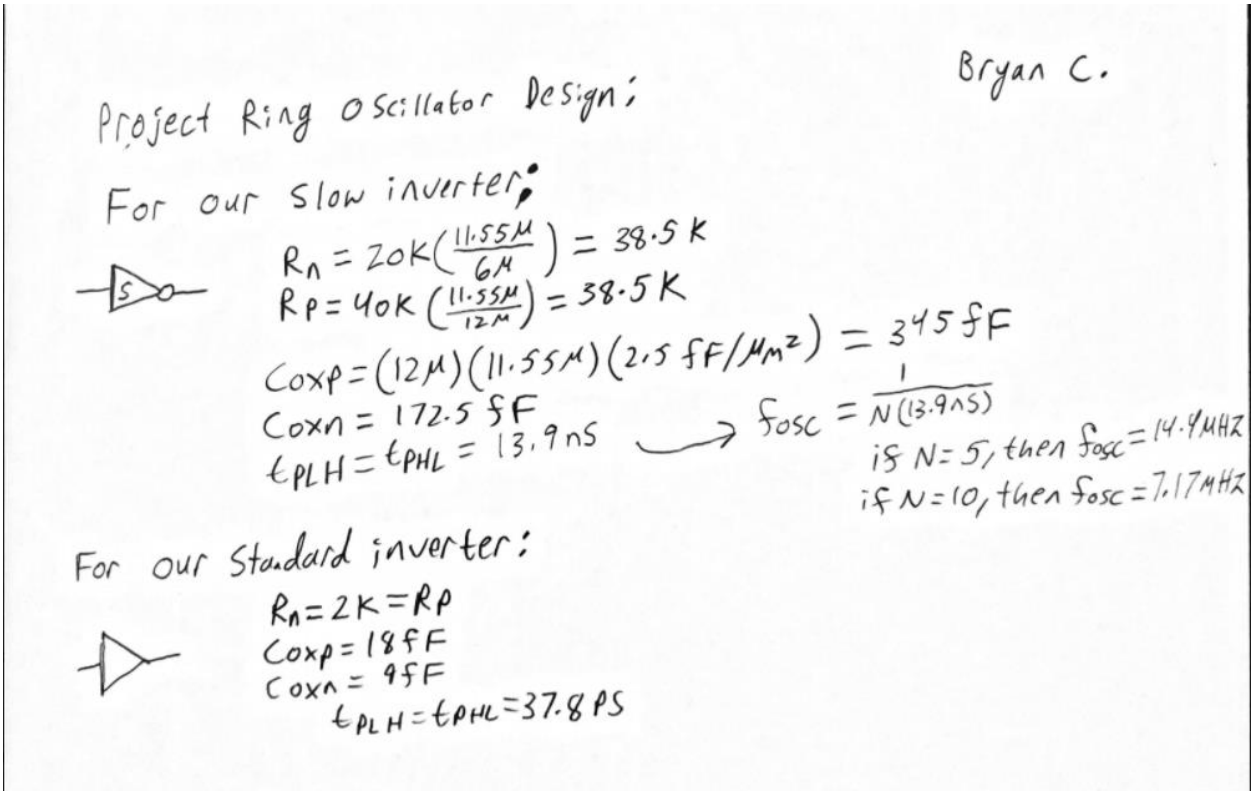
The power inverter was sized this way in order to pull Vsp up to 3.5V. This is because our output node swings closer to VDD than to ground. We want to slice the data in the middle more easily. The switching point of the inverter can be seen below:


DC Response
Name
Vis
/in
/out
M1: 3.542V 3.527V
V (V)
dc (V)
6
5
4
3
2
1
0
-1
0
1
2
3
4
5

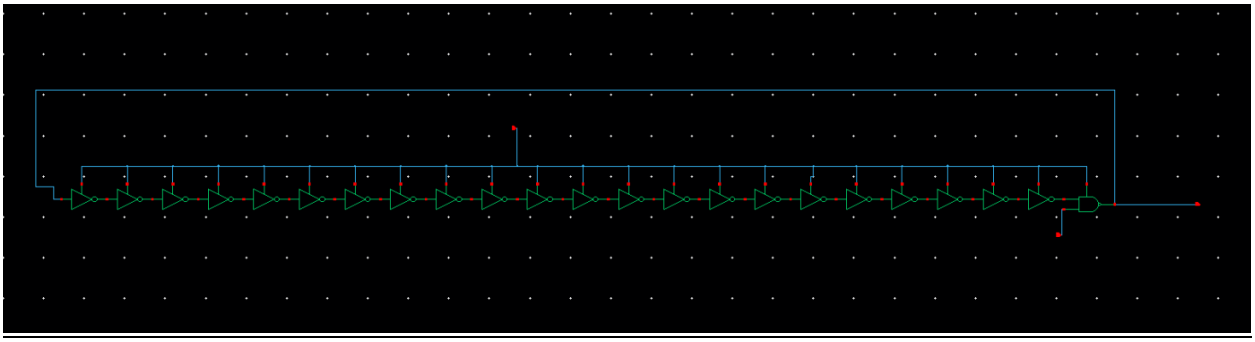

vdd
in
Power
2
out
in
VØ
vdc=Ø
gnd!
gnd

Ring Oscillator:

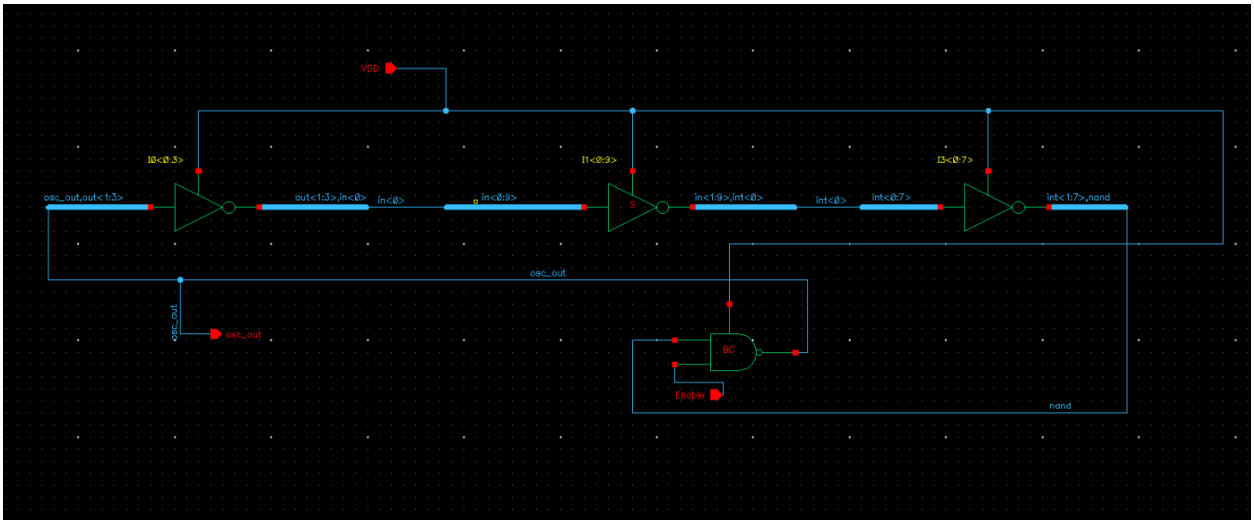
The ring oscillator is turned on by the comparator. The output of the comparator enables the NAND gate contained within the oscillator so it will turn on and drive the buffer. The buffer is connected to the gate of the NMOS transistor contained within the flyback SPS and utilized so we can drive a capacitive load (the transistor has internal capacitance). The oscillator and buffer together cause the transistor to switch on and off. When the transistor is turned off, the energy is transferred from the first inductor (primary) to the second inductor (secondary) in the flyback SPS, this causes Vout to increase. This process is continued until the required voltage is reached (12.5V). We want our ring oscillator to oscillate at a frequency of 5MHz.



Schematic:

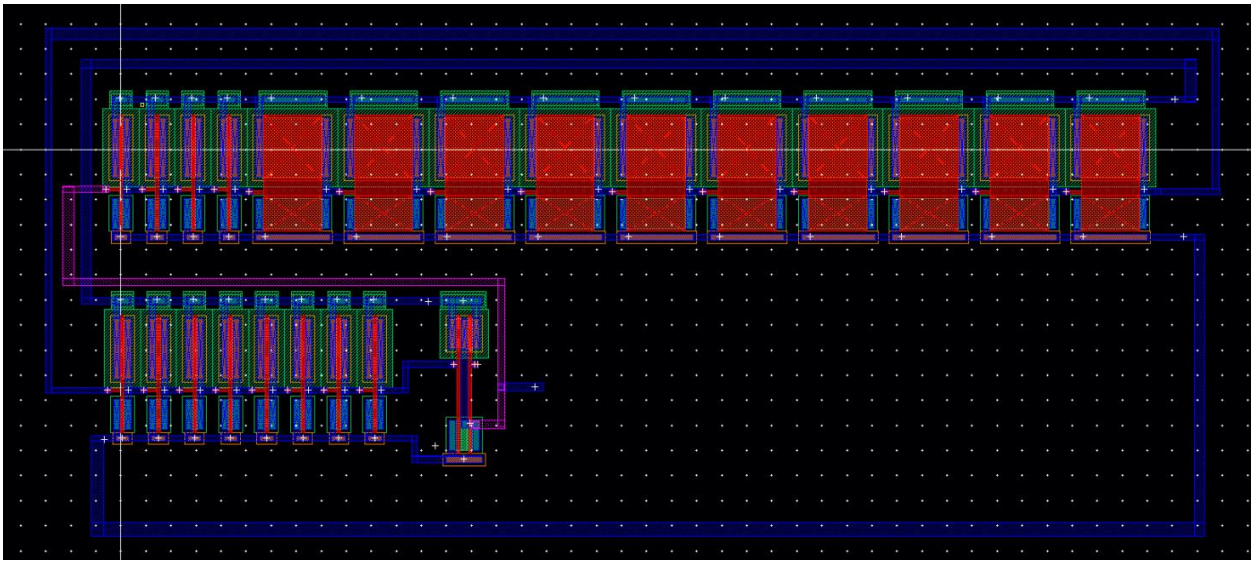


We can make this design compact!

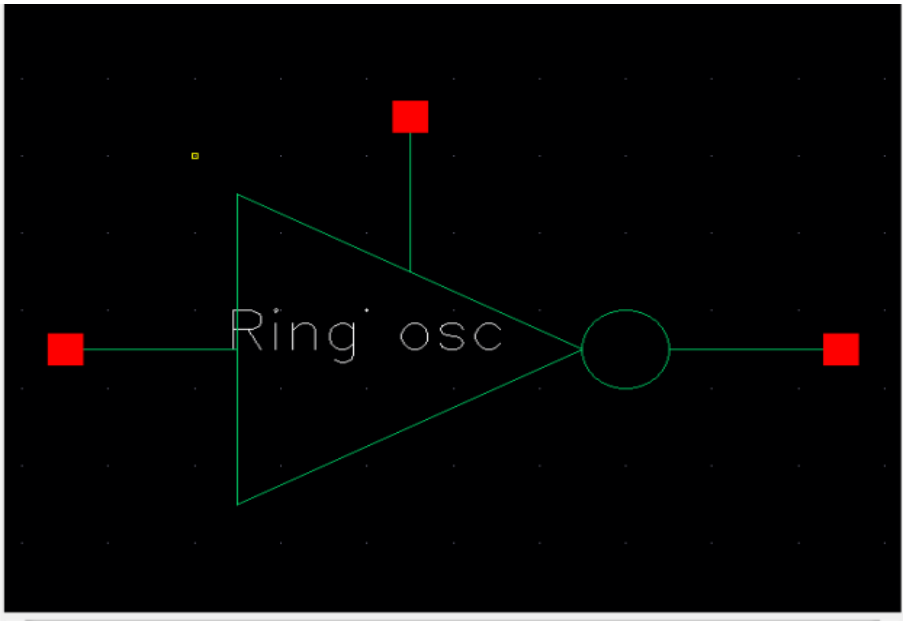


My design utilizes 4 stages of standard 12/6 inverters, 10 stages of slow inverters (discussed below), and finally another 8 stages of standard 12/6 inverters. The input to the NAND gate (Enable) comes from the comparator and the output of the oscillator (osc_out) goes to the input of the buffer.

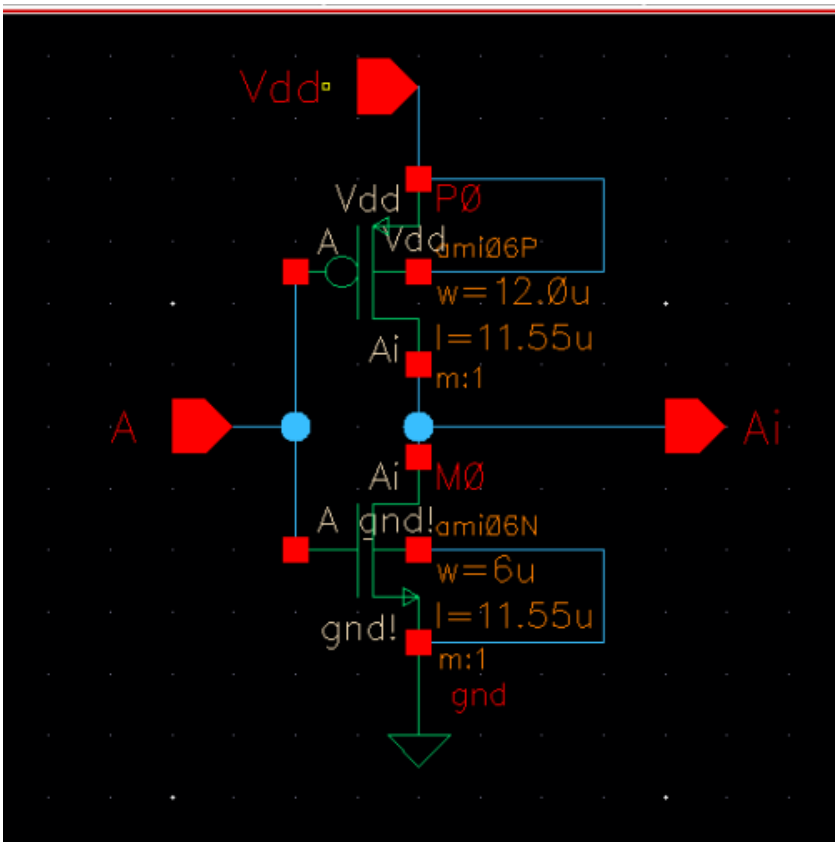
Layout:



Symbol:

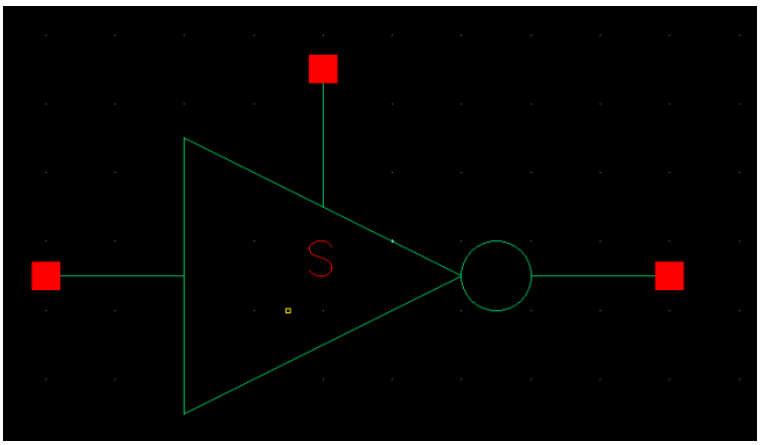


"Slow" Inverter:

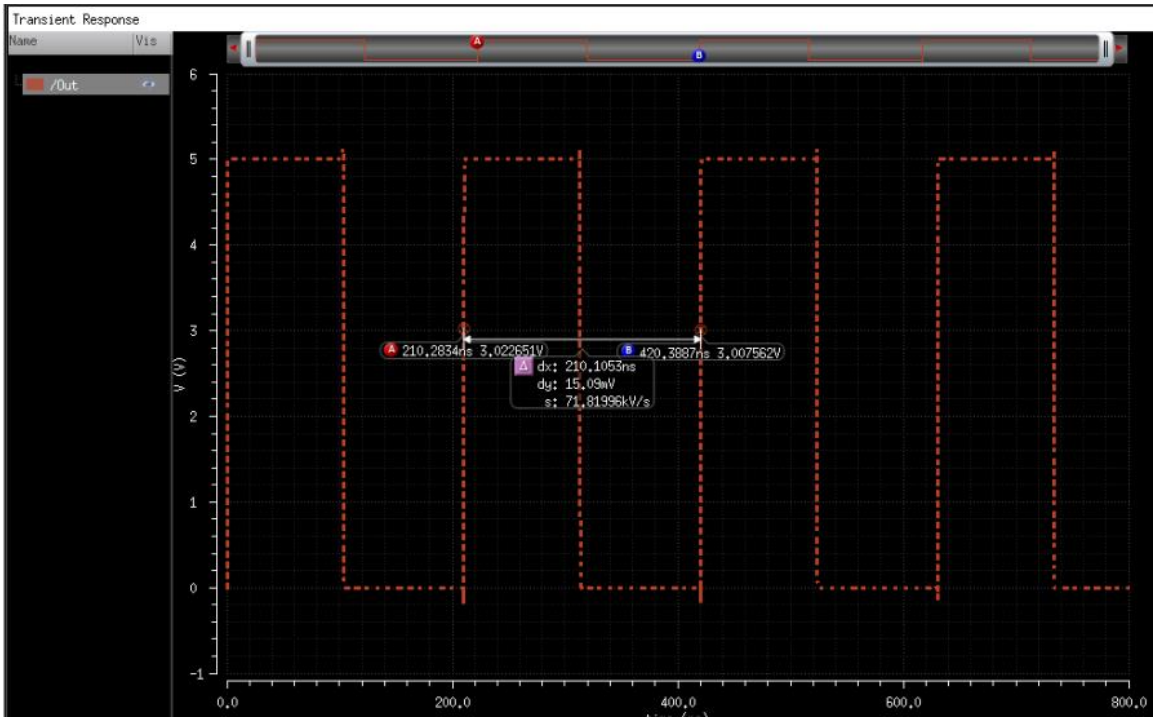


I chose this inverter based on hand calculations and some trial/error.

Symbol:



Simulation of Ring Oscillator:

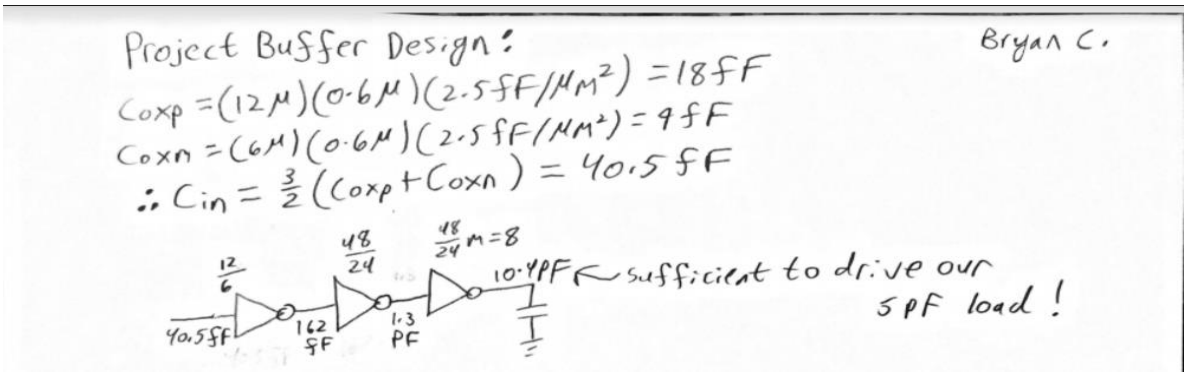


The period is roughly 210 ns. This means that the frequency of the oscillator is roughly 4.8 MHz.

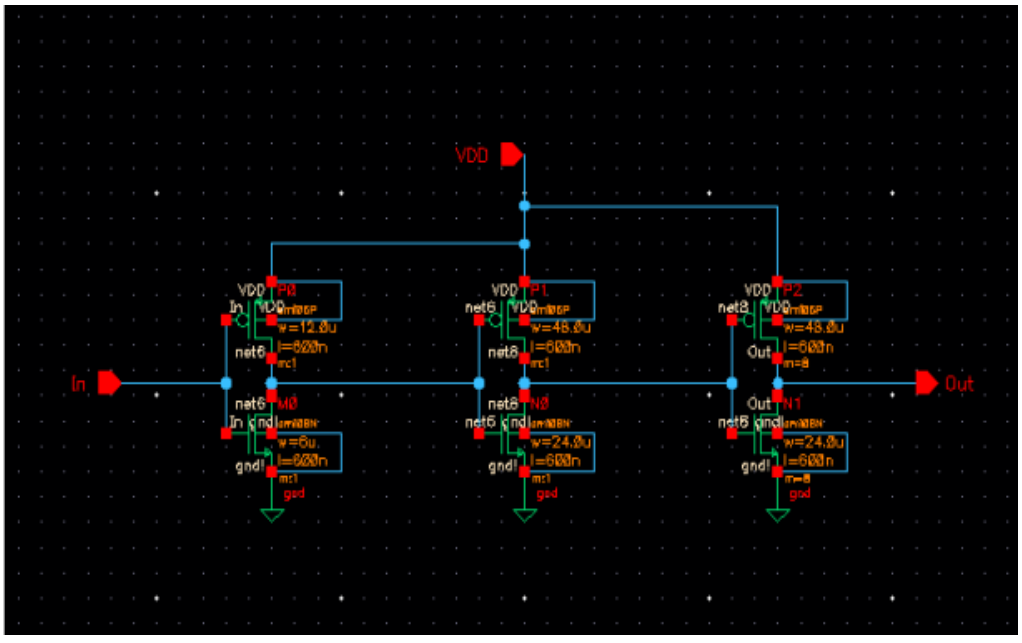
It’s not exactly 5 MHz, but after examining the final design I found it to be sufficient.

Buffer:

The buffer is utilized so we can drive the NMOS transistor contained within the flyback SPS. It consists of cascaded inverters which differ in width by a multiplied value. We want our buffer to be able to drive a capacitive load of 5pF (the internal capacitance of the NMOS). *The buffer is the component which consumes the most power in the control chip.*

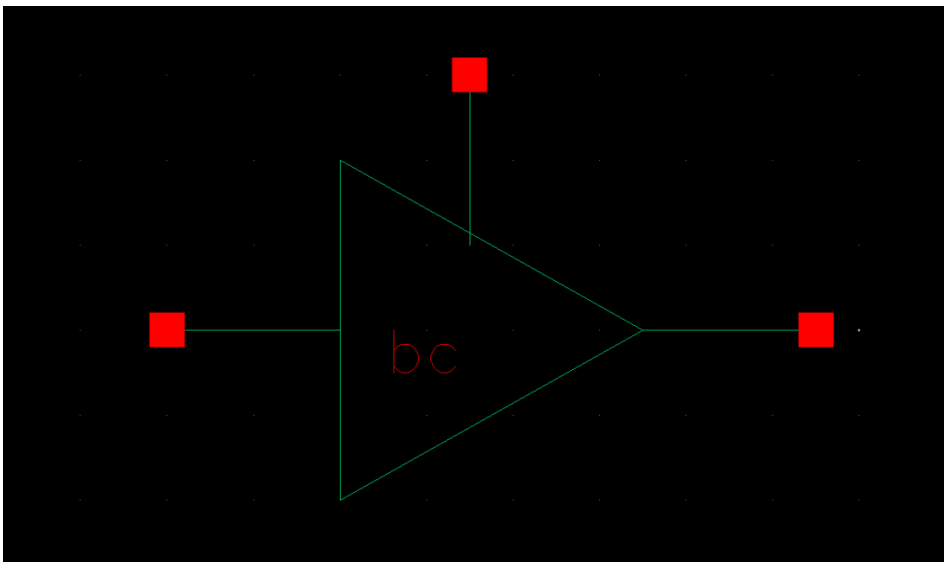


Schematic:

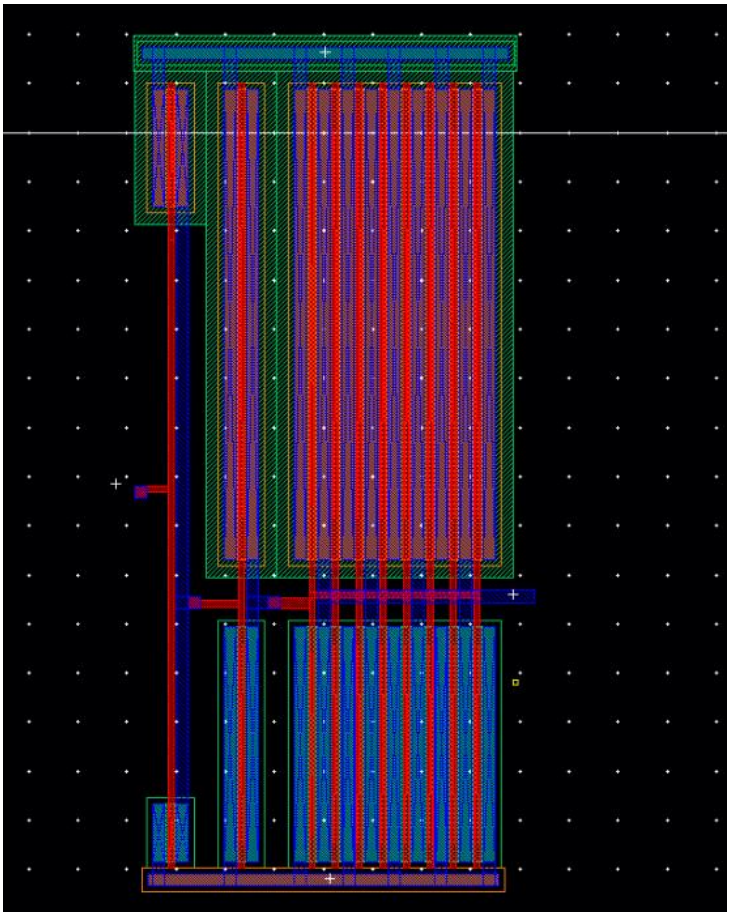


Our first stage consists of a 12/6 inverter, the next stage is a 48/24 inverter (4 times the widths of the PMOS and NMOS in the first inverter), the final stage is a 48/24 inverter with a multiplication factor of 8.

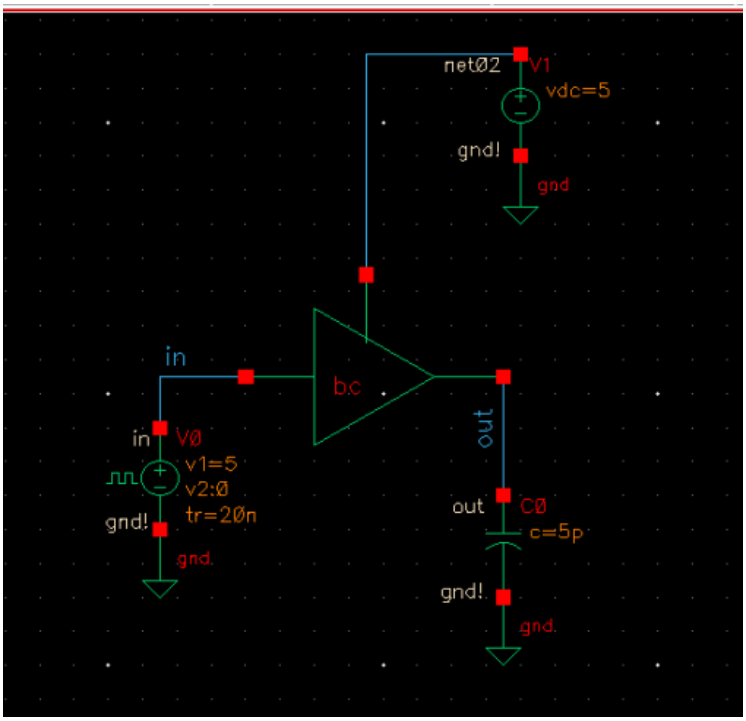
Symbol:

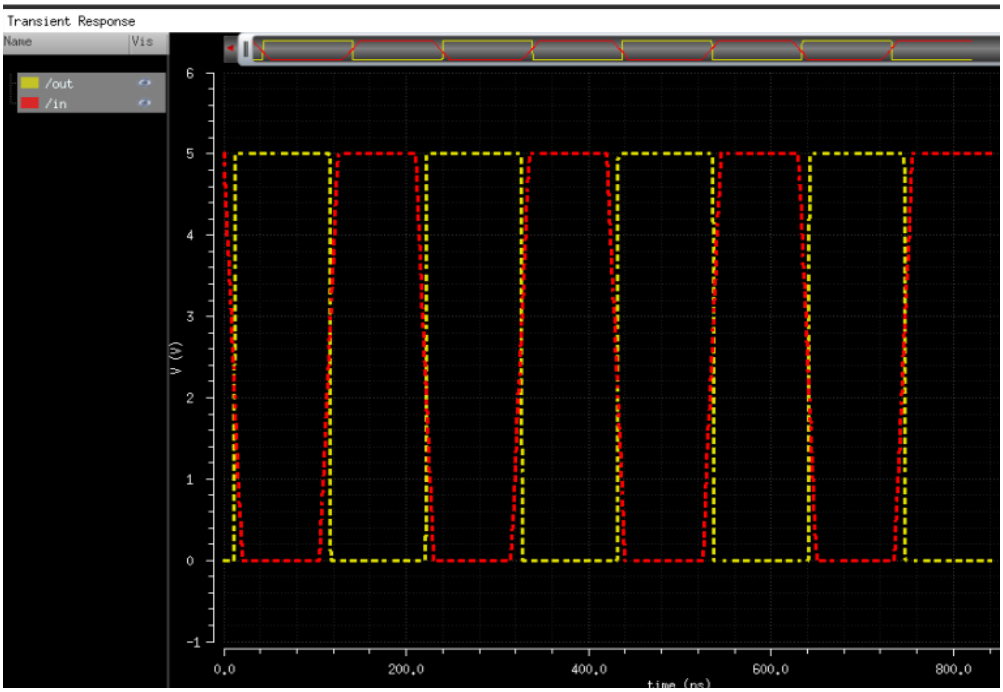


Layout:



Simulation:



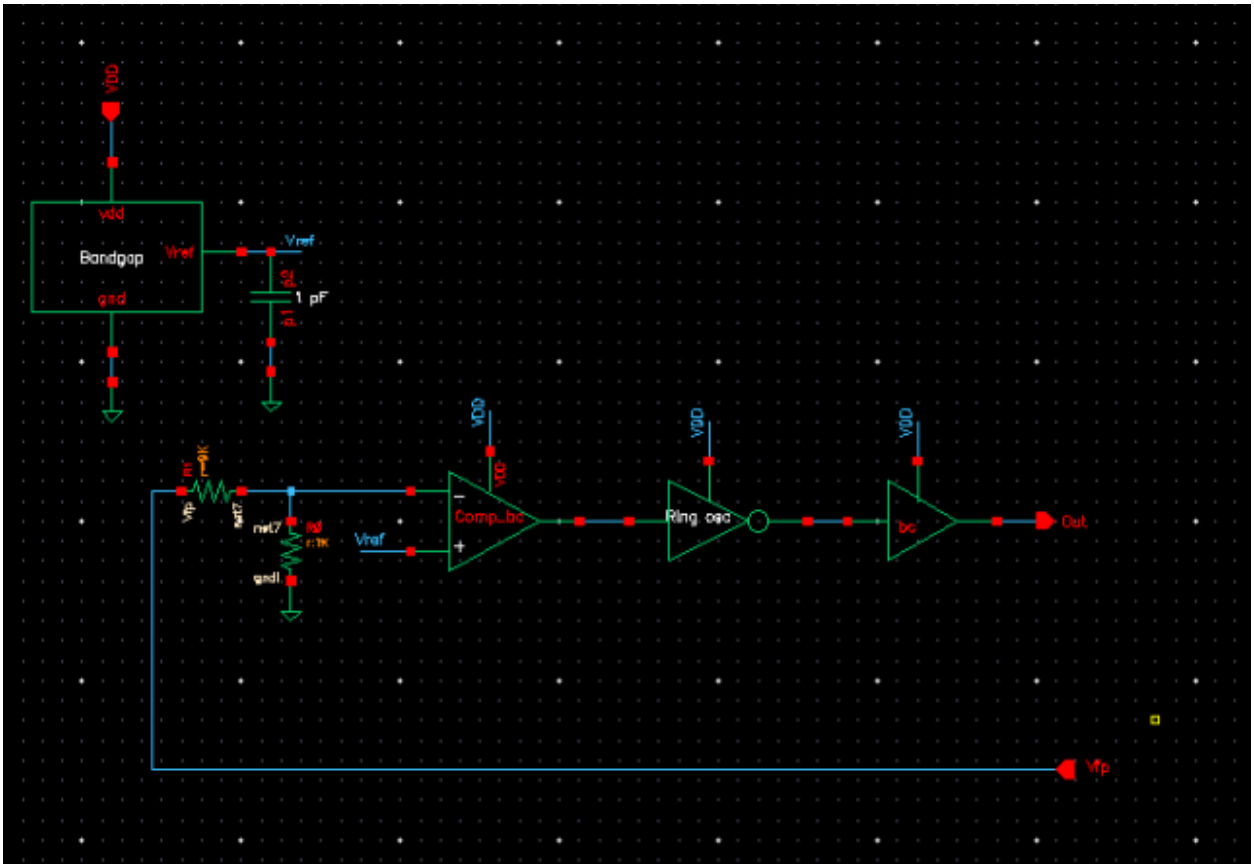


For the pulse source I utilized, I chose a frequency which corresponded to the frequency of my oscillator design (a period of 210 ns).

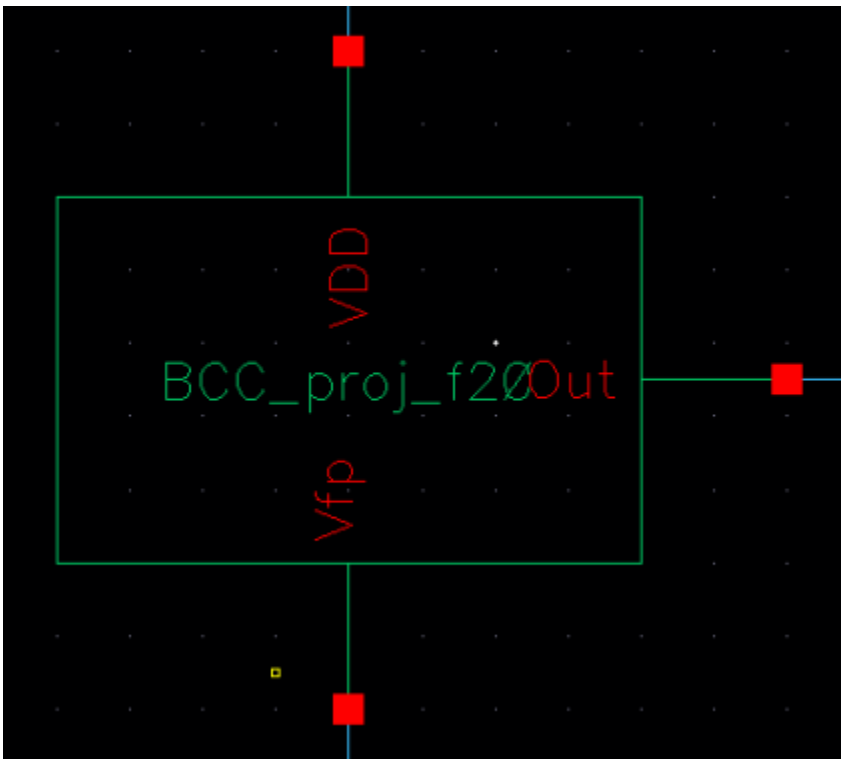
SPS Controller Chip:

The switching power supply controller chip combines the bandgap, comparator, buffer, and ring oscillator together into a circuit that can be utilized with a flyback SPS. When Vfp gets too low, the controller chip turns on the NMOS transistor in the SPS, which in turn causes a current to be pulled through the inductor which has a constant 170V across it (the primary of the transformer). This causes the current to linearly increase. When the transistor is turned off, the energy in the primary is transferred to the secondary which causes Vout to increase. The process is repeated until our desired output voltage is reached. The primary and secondary side of our circuit are isolated.

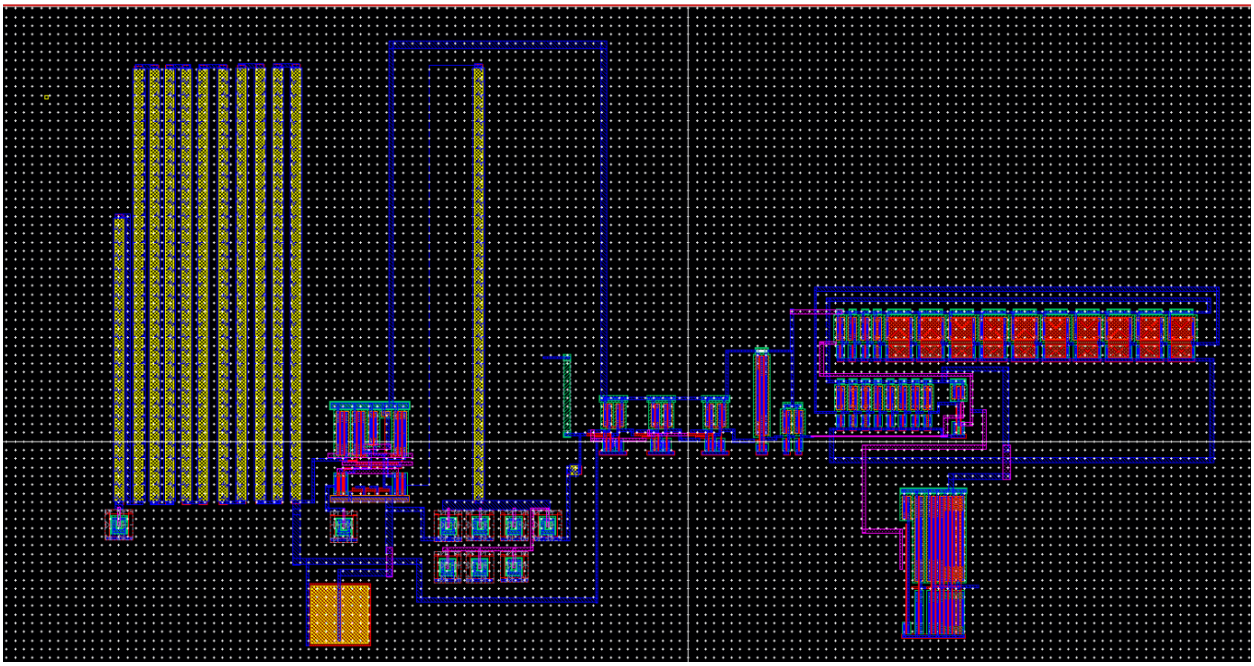
Schematic:



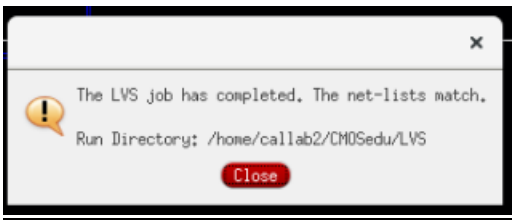
Symbol:



Layout:



LVS/DRC:

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    CPU time = 00:00:00  Total time = 00:00:01
*********   Summary of rule violations for cell "BCC_proj_f20 layout"   *********
   Total errors found: 0
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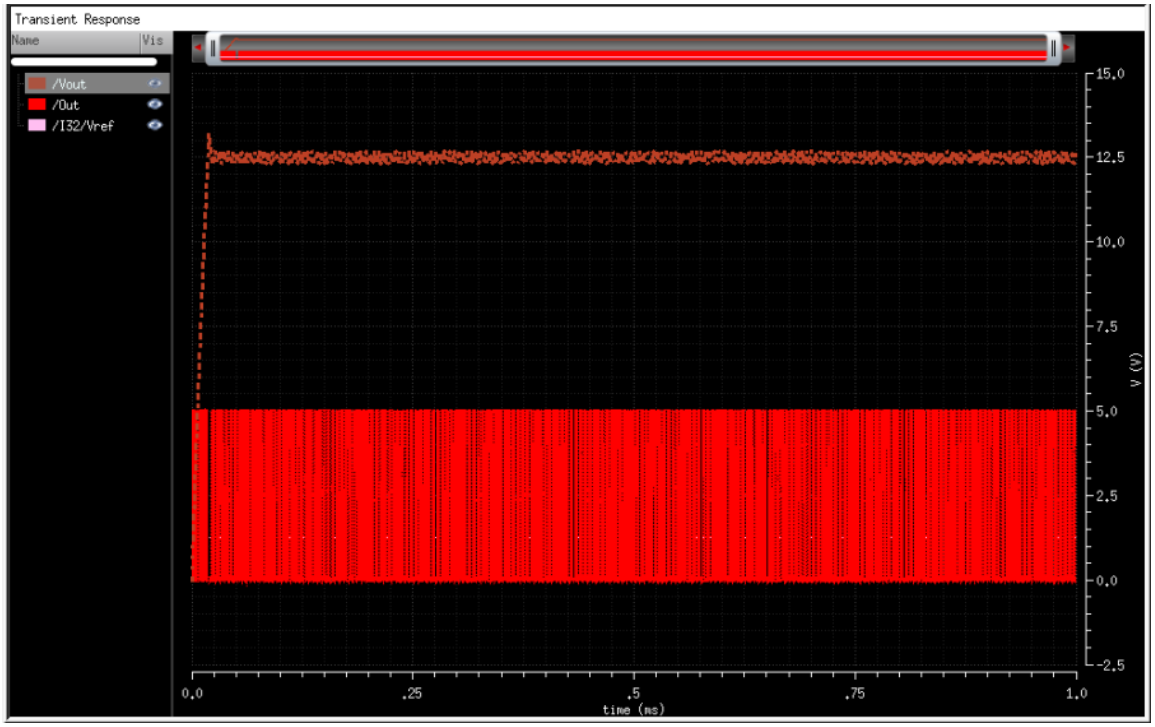
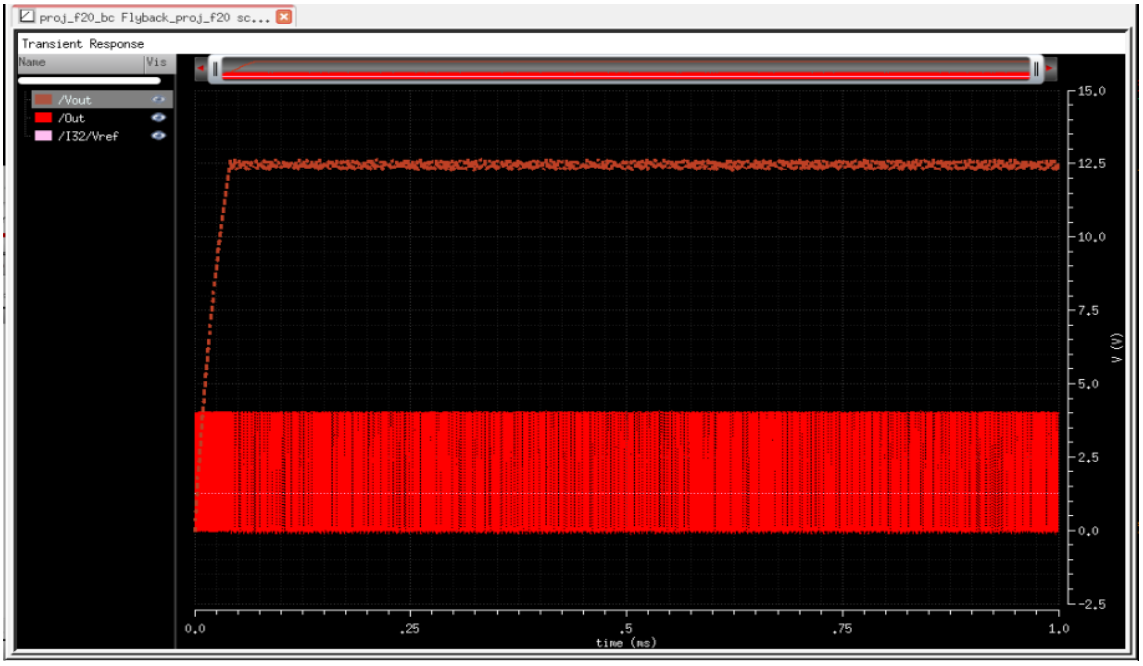
Simulation results:

VDD= 5V:

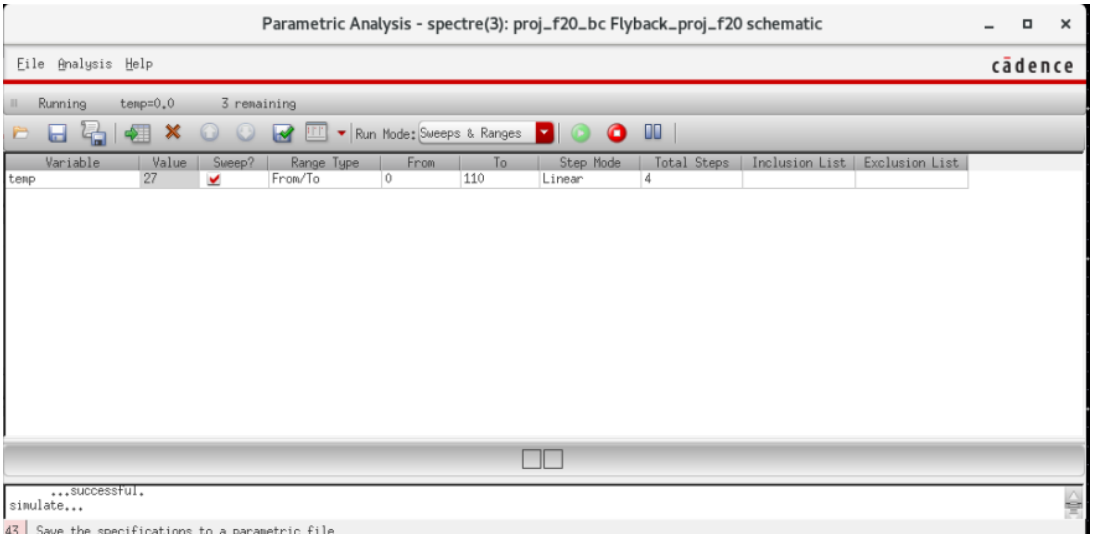


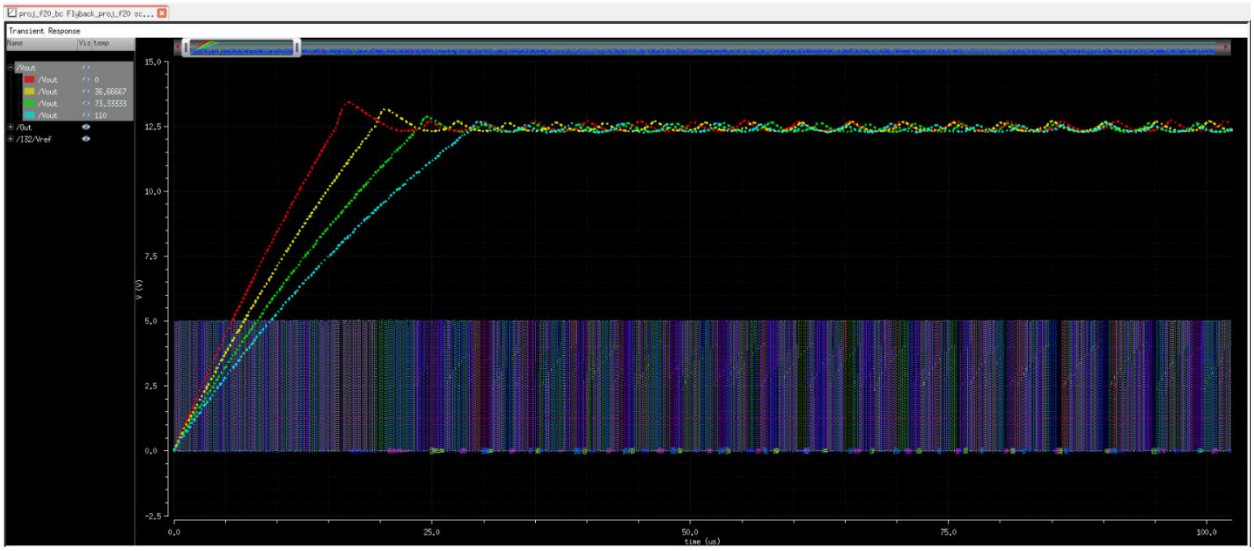
VDD = 4V:



(If VDD goes below 3.7V, the bandgap will not function properly. As stated above.)

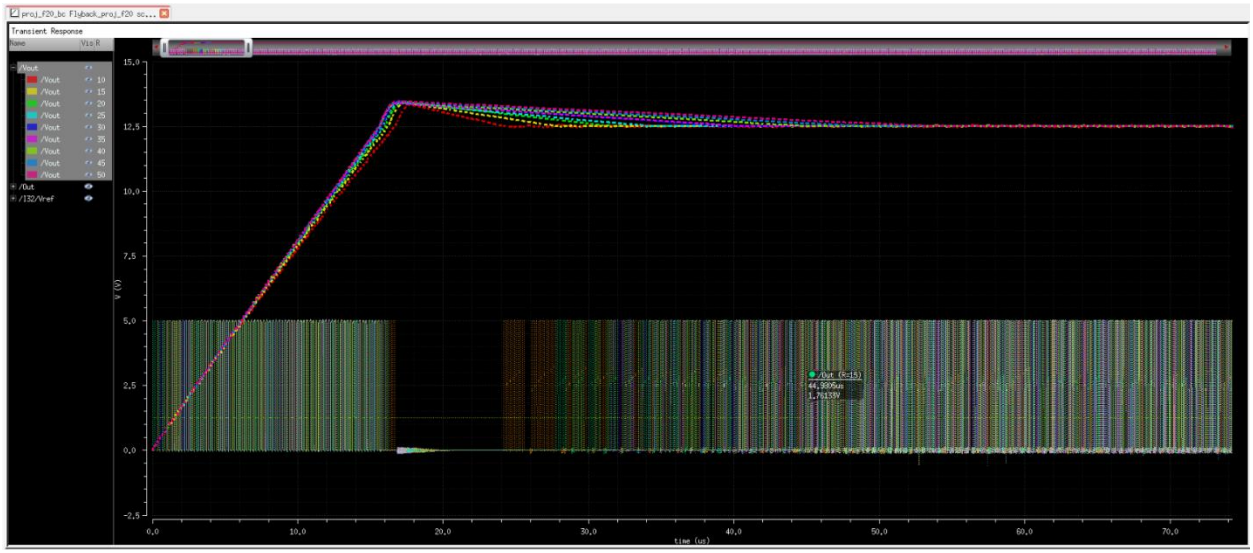
<u>Temperature simulation:</u>

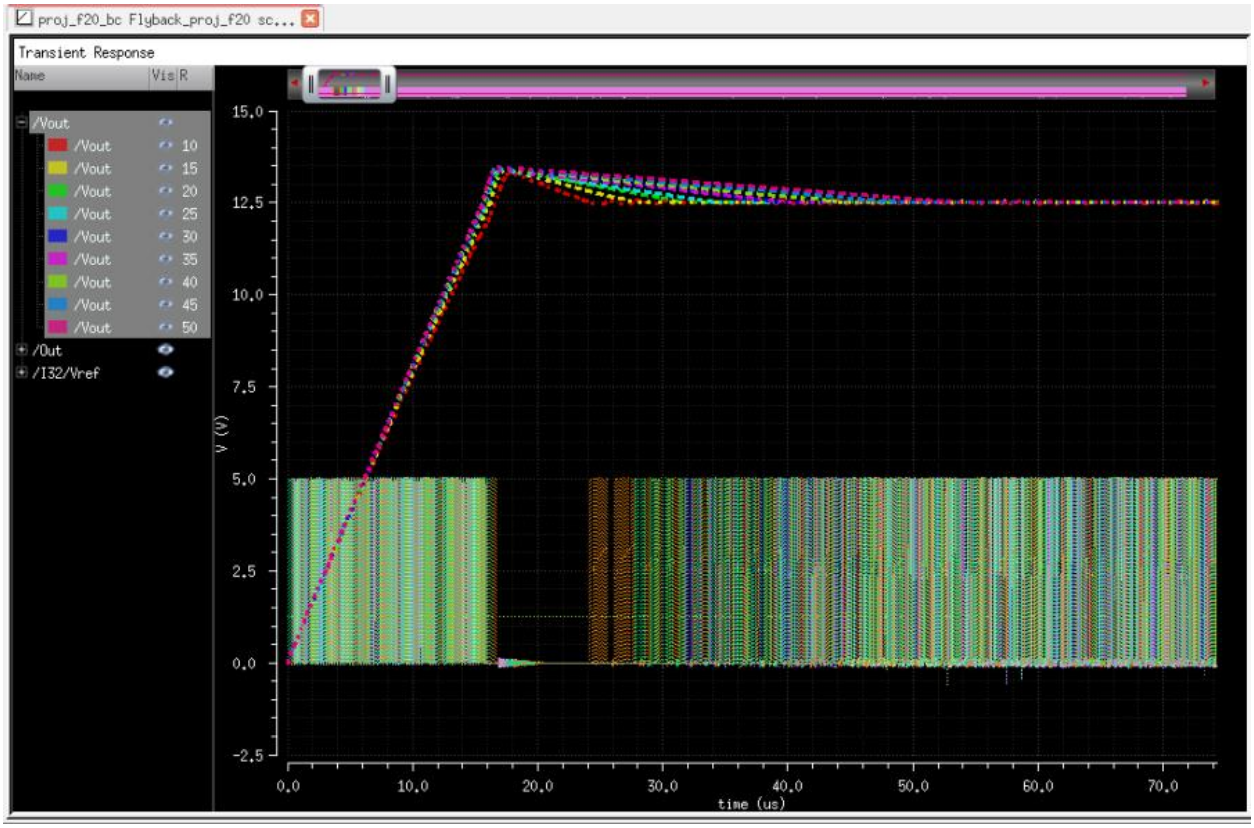




We can see that as temperature increases, the curve seems to shift towards the right. This change appears to be slight, implying that changing temperature does not have a major impact on this circuit.

Various loads:

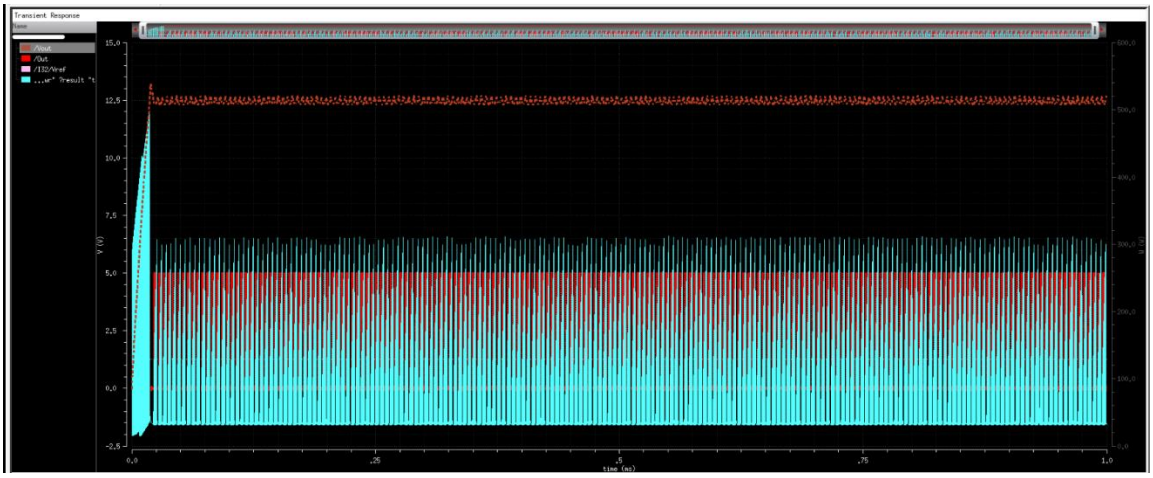


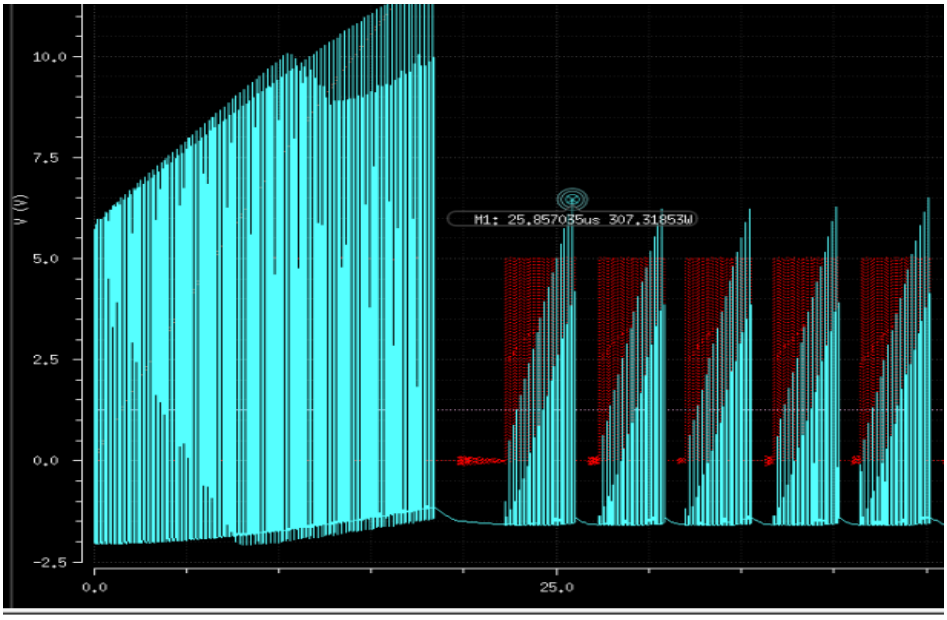


We can see that the circuit works for various loads. As the load size increases, the circuit must "pedal harder" in order to reach the desired 12.5V.

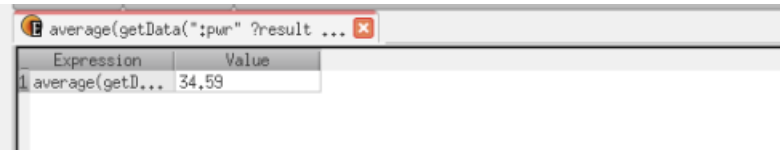
Average Power:

Below we can see a plot of the power consumed by the circuit.



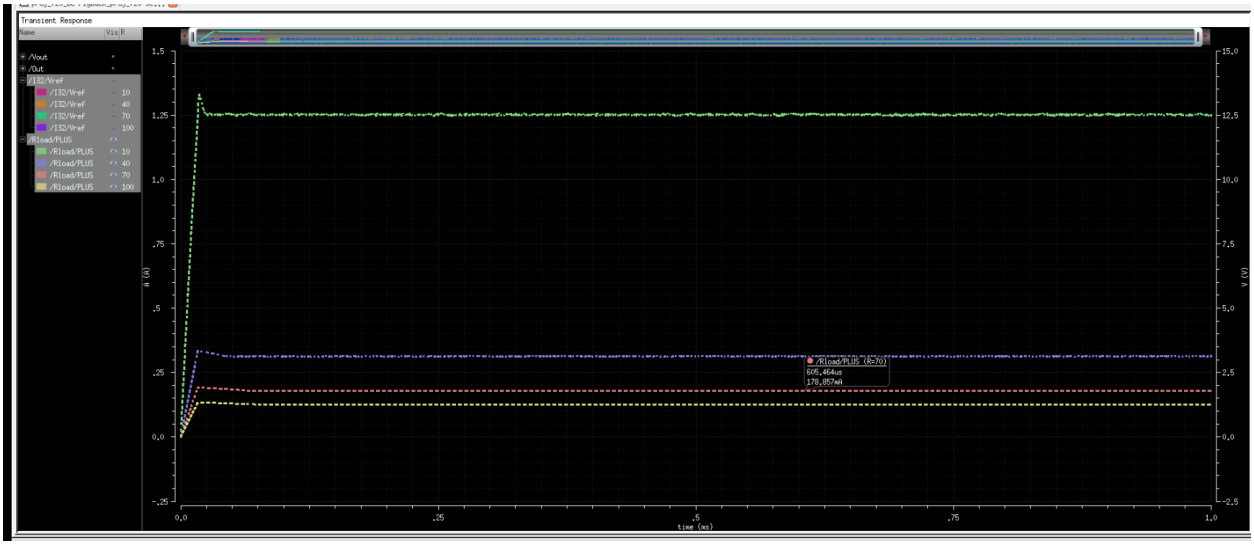


Once the circuit starts working, the peak power is around 307W.



The average power consumed by the circuit is around 35W (for a load of 10 ohms and a VDD of 5V).

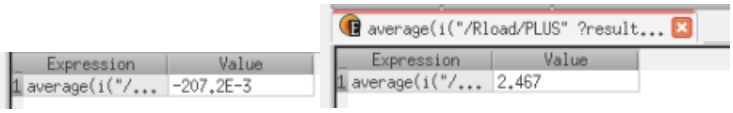
<u>Operation for various load currents:</u>



We can see that the circuit operates properly for the specified range of currents.

Efficiency:

Eff = P_o/P_i

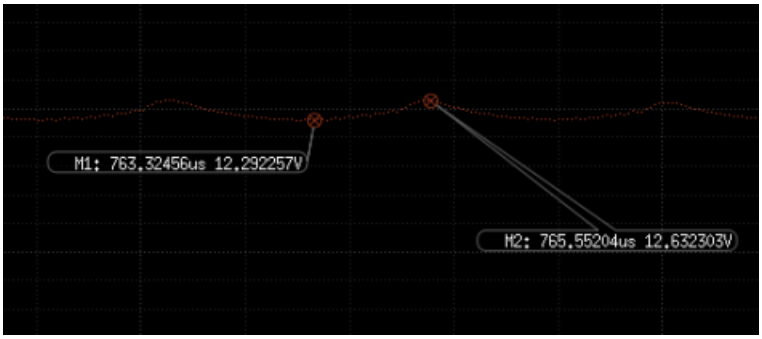


(Input current on the left and output current on the right)

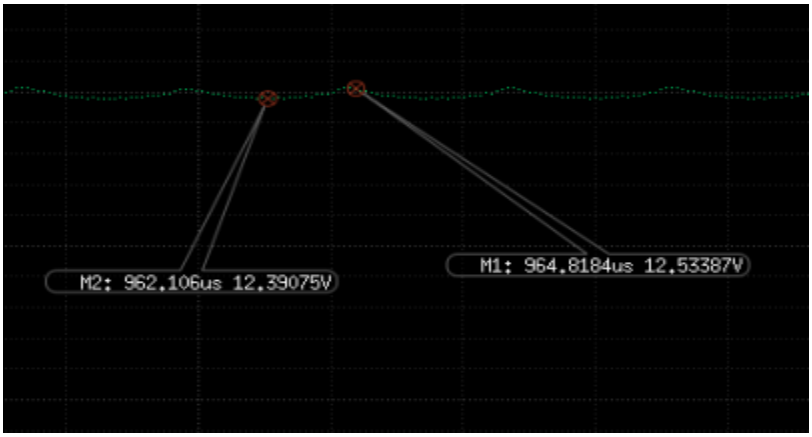
Eff= (12.5*2.467)/(170*207.2*10^-3) = 87.5%, or roughly 88%.

Conclusions/Other Considerations:

With regards to the design of this control chip, the buffer is the component which draws the most power. This is because it relies on large MOSFETs in order to properly drive a capacitive load (the internal capacitance of the NMOS in the flyback SPS). If someone were to attempt to expand on my design and improve it, a few things could be done. First, if possible, the buffer should be optimized such that it can properly drive the NMOS in the flyback SPS while consuming minimal power. Second, the oscillator design should be improved to obtain a generated frequency that is closer to 5MHz. My design functions properly for the intents and purposes of this project, but it is reasonable to consider making minor adjustments to the oscillator in order to increase its frequency. Third, the filtering of the flyback SPS could be increased to eliminate AC ripple and obtain a smooth 12.5V on output. Perhaps this could be done in the control circuit somehow, but it could also be done in the actual power supply (at the expense of using a larger capacitor). In the image below, we can see that our output contains close to 300mV of AC ripple:

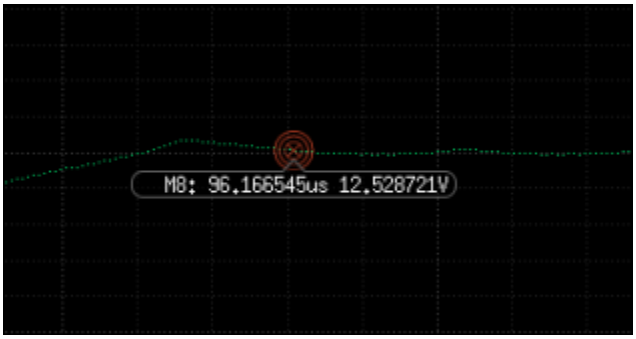


If we change the filter capacitor to a size of 20uF, our ripple improves to roughly 140mV:

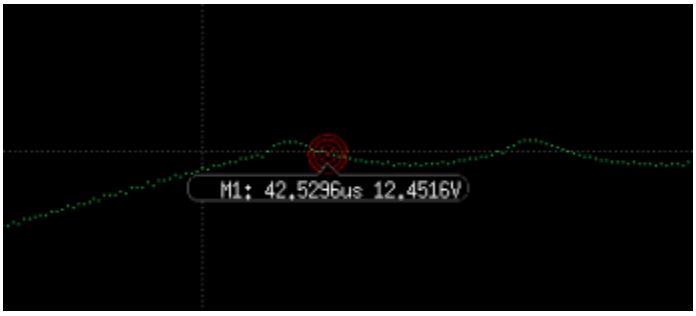


This comes at the cost of paying for a larger capacitor and making the circuit slower. If we change the filter capacitor to a size of 50uF, our ripple improves to roughly 85mV:

But it takes roughly 96us for us to “pedal up” to the desired 12.5V:



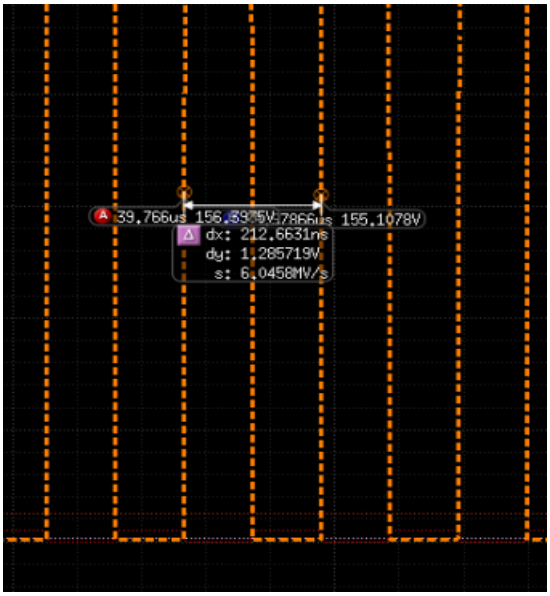
Compared to a circuit with a 10uF filter capacitor:

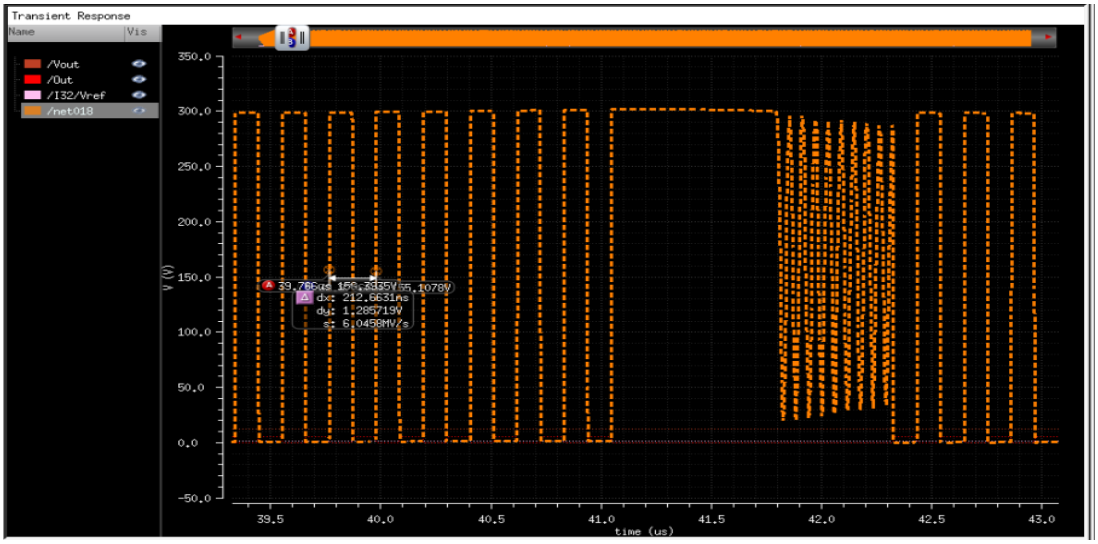


We can see that there is a difference. It takes around an additional 53.6us in order to “pedal up” to our 12.5V.

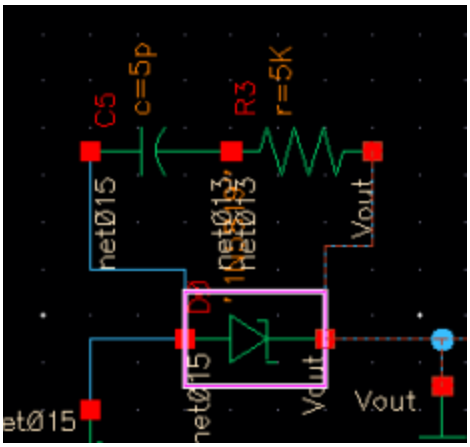
If this circuit were to really be implemented (if we were to build the full flyback SPS), it is likely that we would want to use a laminate core transformer in order to prevent eddy currents and hysteresis losses. Our oscillator operates at a frequency of 5MHz and (as we can see below) the primary of the transformer generally has a frequency which is much greater than 15kHz (the maximum suggested frequency for usage of an iron core transformer as detailed in the Radio Amateurs Handbook published by The American Radio Relay League (ARRL)) applied to it. Eddy current losses occur because the induced e.m.f. in the primary will cause a current to flow in the core of the transformer. Hysteresis losses occur because iron tends to resist any change in

its magnetic state, and thus, a rapidly changing current is forced continually to supply energy to the iron to overcome the “inertia.”

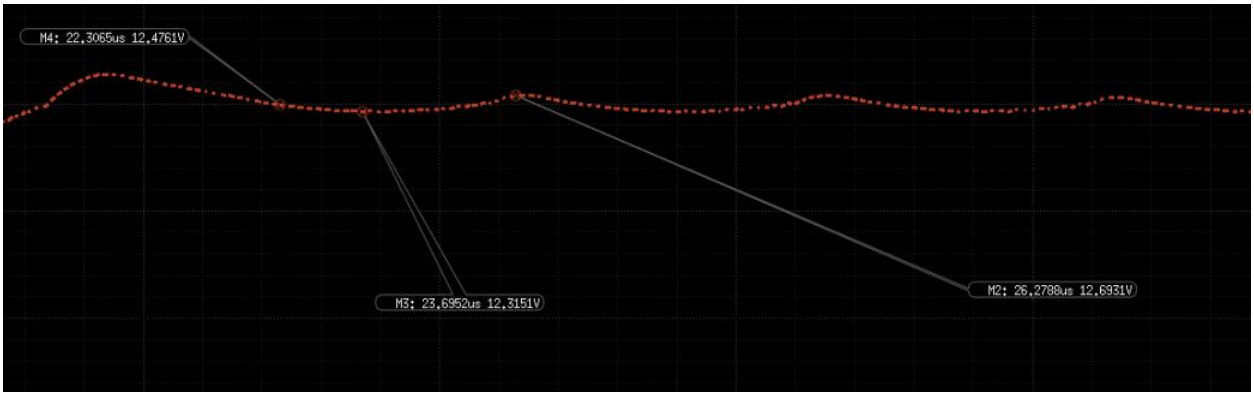




We could also utilize a resistor and capacitor in parallel with our 1N5819 Schottky diode. This is useful for pulse suppression and allows the circuit to work faster (This, of course, comes at the cost of the circuit being more expensive to manufacture):



(Example with a 5pF capacitor and 5kΩ resistor)



The circuit starts working at around 22.3us. For a 10pF load the ripple is around 250mV.

All in all, the circuit works well, and I feel as if this project was a valuable learning experience with regards to understanding how a flyback SPS works. There is always room for improvement in anything, and with enough time (and willpower), this flyback SPS could be improved, manufactured, and implemented. There are many tradeoffs in this circuit, and it is important to optimize the design for maximum functionality and minimal cost.

Project Design Files