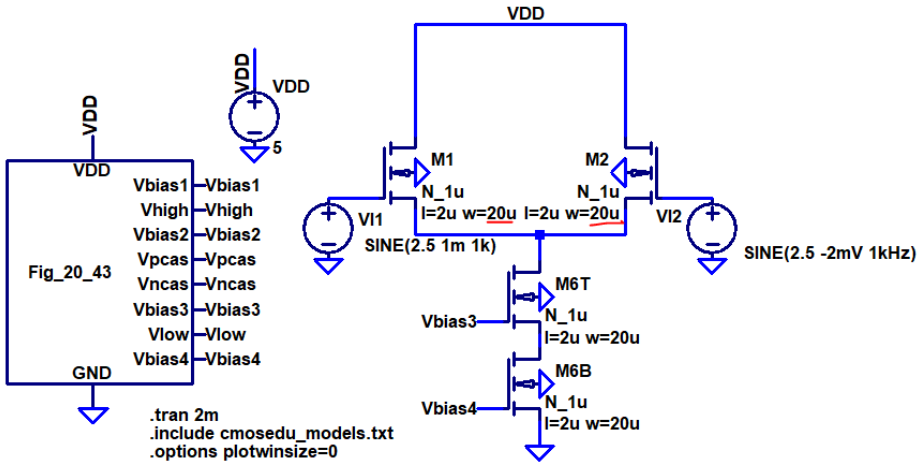
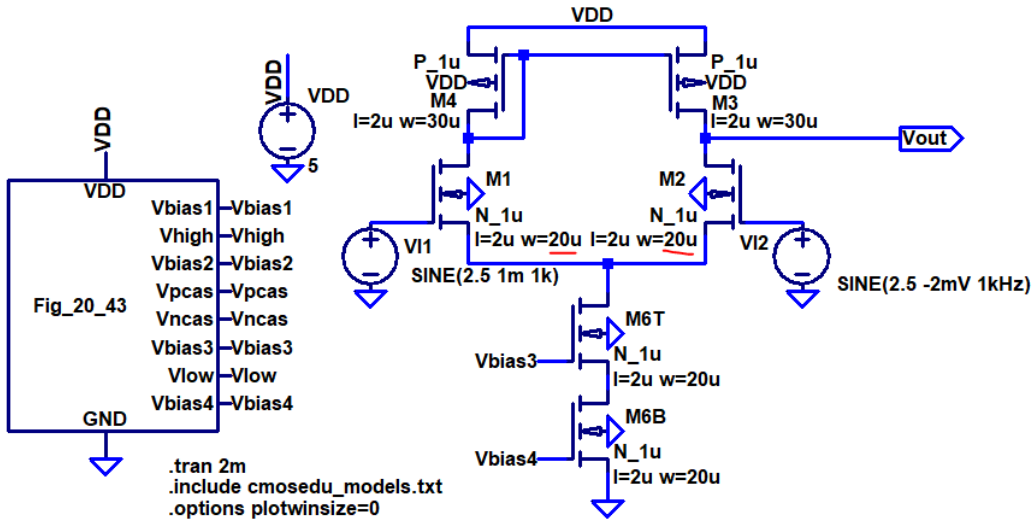
H.W. #17 EE 420/ECG 620 Spring 2020

Show your work for credit and put a box around each of your answers (follow the hw guidelines!) Unless otherwise indicated use the book's long-channel (1 um) process.

1. For the following diff-amp what is the input CMR? What are the AC gate-source voltages of M1 and M2? What are the AC drain currents of M1 and M2? Verify your hand calculated answers using LTspice. (4 points)



2. What is the input CMR for the following diff-amp? What is the allowable (so that all transistors stay in the saturation region) range of the output voltage? Finally, what is the output voltage (DC + AC). Verify your hand calculations using LTspice. (4 points)



3. Repeat problem 2 for the PMOS diff-amp using the same size devices. Of course the tail current is biased with Vbias1/2 and the devices are 60/2.