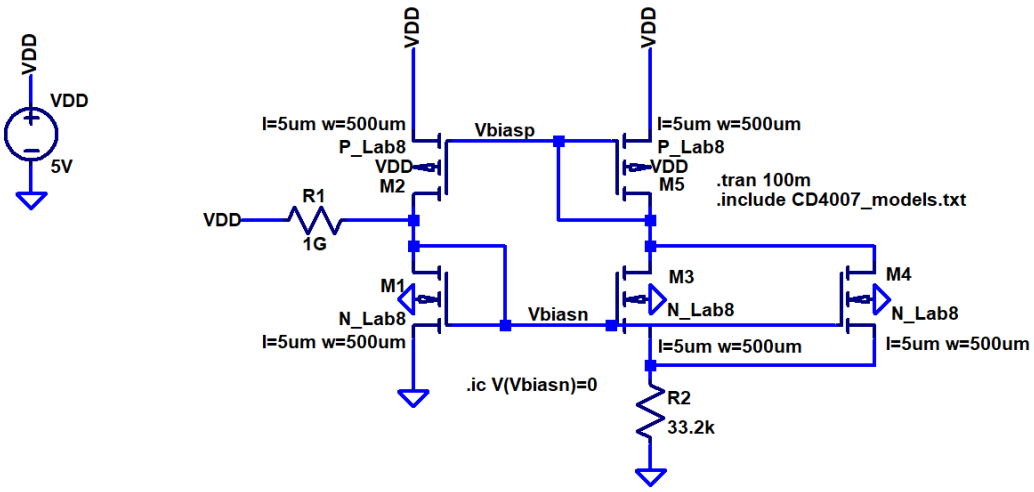
Lab 9 Pre-lab Assignment (Beta Multiplier Reference Design)



Gm = 20.4 uA/V (start-up circuit included)

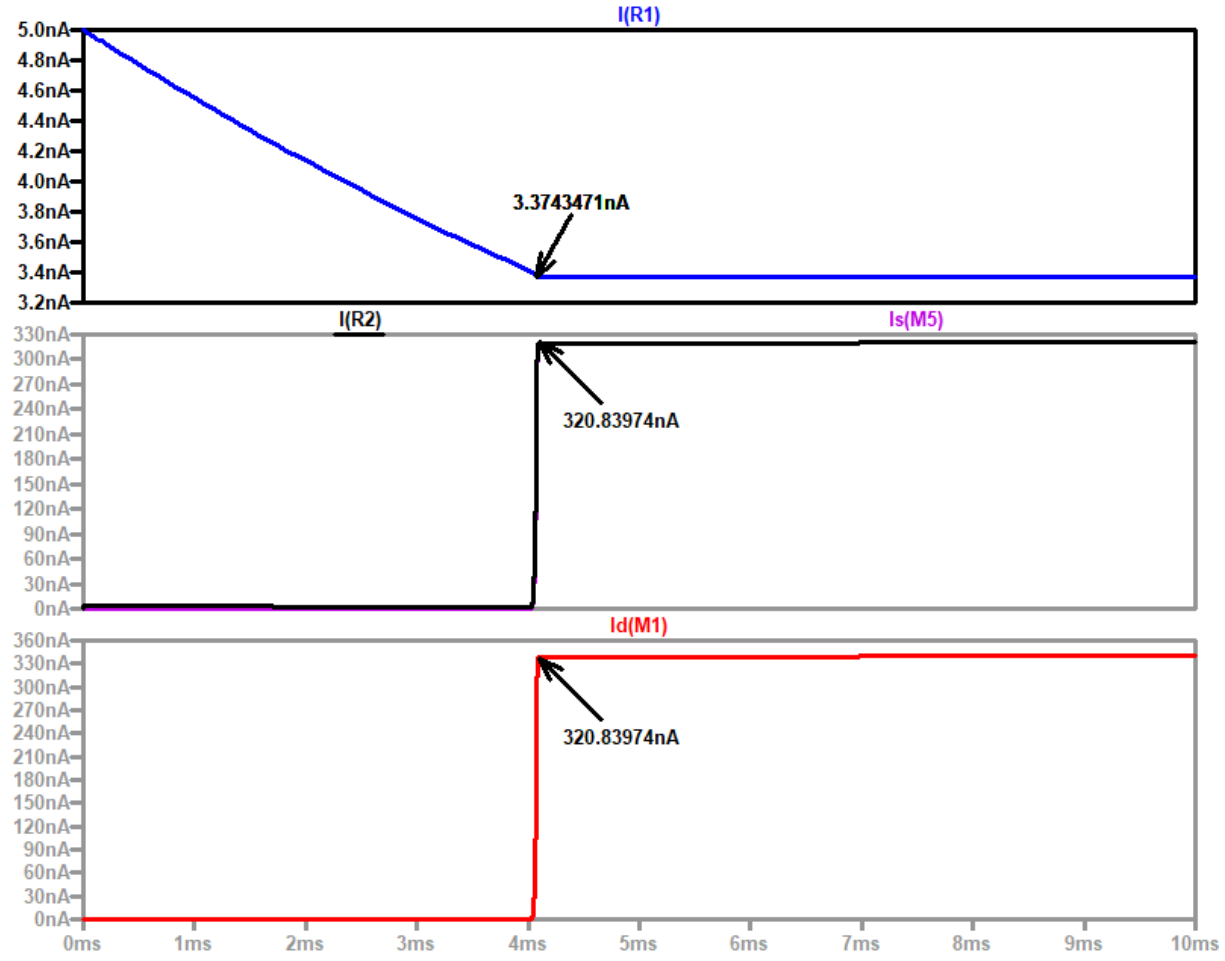
Name:	m5	m2	m4	m3	m1
Model:	p_lab8	p_lab8	n_lab8	n_lab8	n_lab8
Id:	-3.20e-07	-3.37e-07	1.60e-07	1.60e-07	3.41e-07
Vgs:	-1.53e+00	-1.53e+00	1.62e+00	1.62e+00	1.63e+00
Vds:	-1.53e+00	-3.37e+00	3.45e+00	3.45e+00	1.63e+00
Vbs:	0.00e+00	0.00e+00	-1.06e-02	-1.06e-02	0.00e+00
Vth:	-1.50e+00	-1.50e+00	1.60e+00	1.60e+00	1.60e+00
Vdsat:	-3.50e-02	-3.50e-02	2.27e-02	2.27e-02	3.34e-02
Gm:	1.83e-05	1.93e-05	1.41e-05	1.41e-05	2.04e-05
Gds:	9.19e-09	9.19e-09	1.55e-09	1.55e-09	3.35e-09
Gmb:	5.91e-06	6.22e-06	9.02e-08	9.02e-08	1.32e-07
Cbd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgsov:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgdov:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgbov:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgs:	3.34e-12	3.34e-12	3.34e-12	3.34e-12	3.34e-12
Cgd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgb:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00

Gm = 20.0 uA/V (start-up circuit excluded)

Name:	m5	m2	m4	m3	m1
Model:	p_lab8	p_lab8	n_lab8	n_lab8	n_lab8
Id:	-3.11e-07	-3.27e-07	1.55e-07	1.55e-07	3.27e-07
Vgs:	-1.53e+00	-1.53e+00	1.62e+00	1.62e+00	1.63e+00
Vds:	-1.53e+00	-3.37e+00	3.46e+00	3.46e+00	1.63e+00
Vbs:	0.00e+00	0.00e+00	-1.03e-02	-1.03e-02	0.00e+00
Vth:	-1.50e+00	-1.50e+00	1.60e+00	1.60e+00	1.60e+00
Vdsat:	-3.45e-02	-3.45e-02	2.24e-02	2.24e-02	3.27e-02
Gm:	1.80e-05	1.90e-05	1.39e-05	1.39e-05	2.00e-05
Gds:	8.91e-09	8.91e-09	1.50e-09	1.50e-09	3.22e-09
Gmb:	5.82e-06	6.12e-06	8.89e-08	8.89e-08	1.29e-07
Cbd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgsov:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgdov:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgbov:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgs:	3.34e-12	3.34e-12	3.34e-12	3.34e-12	3.34e-12
Cgd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgb:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00

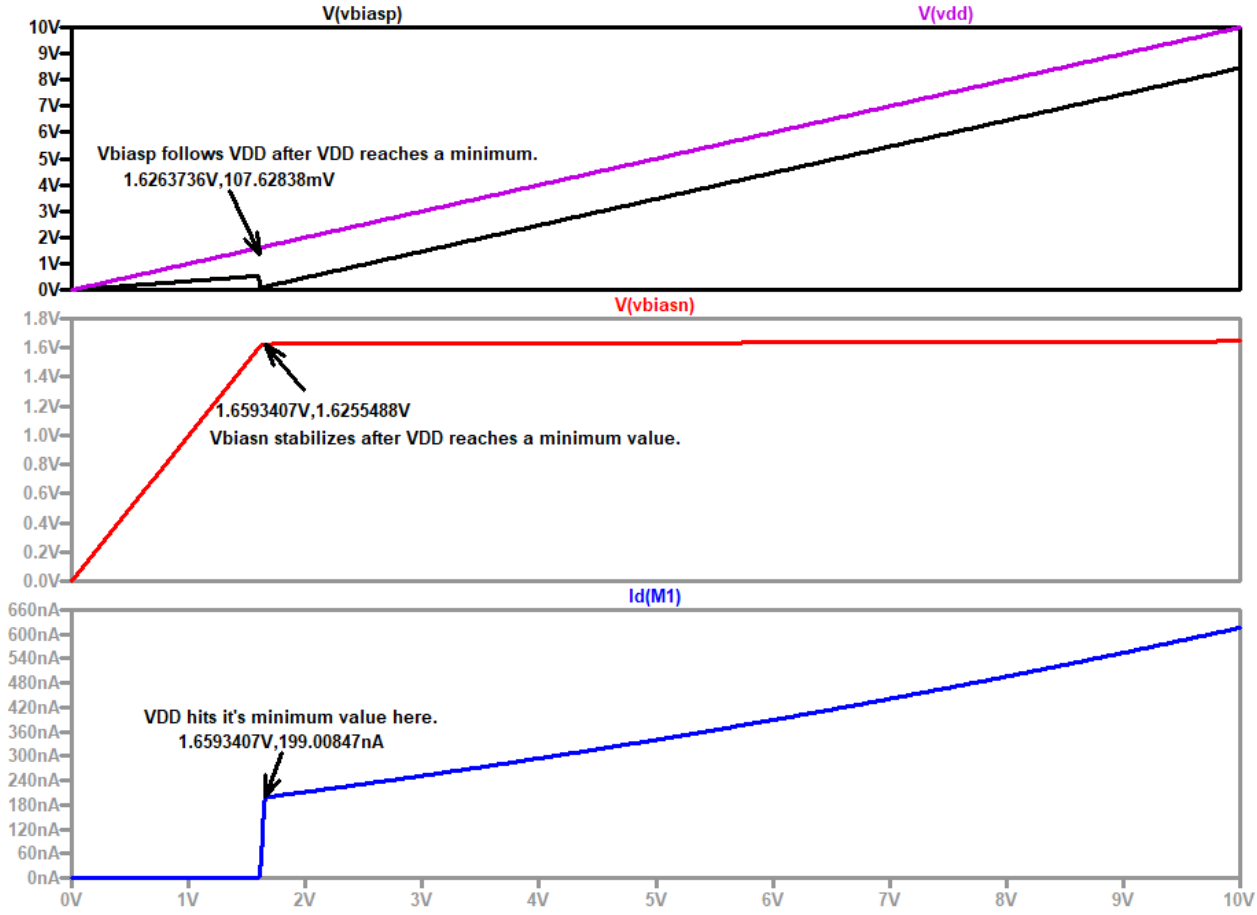
Start-up Circuit Operation

The resistor connected from Vbiasn to VDD ensures that the circuit will start up correctly by forcing a current through this big resistor into the drain of device M1 (or drain of device M2), pouring charge into the BMR. By injecting current to Vbiasn, which is the gate-drain connected note of the NMOS device M1, we drive the voltage on this node up, forcing device M1 into the saturation region, in which it immediately begins sinking current, and the circuit starts up from there.



The initial voltage across R1 (the start-up resistor) is 5V. 5V divided by a gigaohm gives 5nA of current, by Ohm's law. This current is injected into the drain of device M1, driving the voltage on the drain of the device up. We know that diode connected devices with nonzero drain voltages are always operating in the saturation region. Therefore, as soon as spice recognizes the voltage on the node as a nonzero voltage, the circuit snaps into operation and the devices begin sinking the expected current (0.333 uA). As we can see from the simulations, the current through the start-up resistor during operation is 100 times smaller than the current in each of the branches.

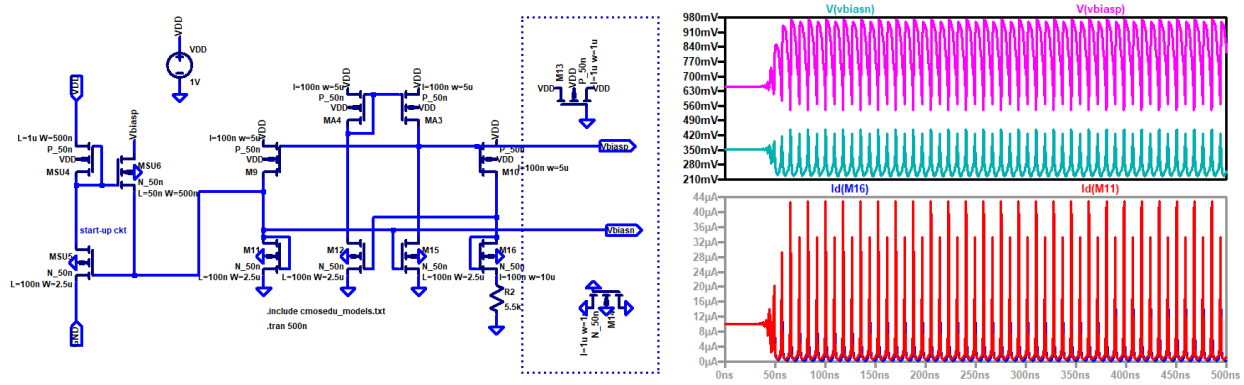
Operation as VDD Sweeps from 0V to 10V



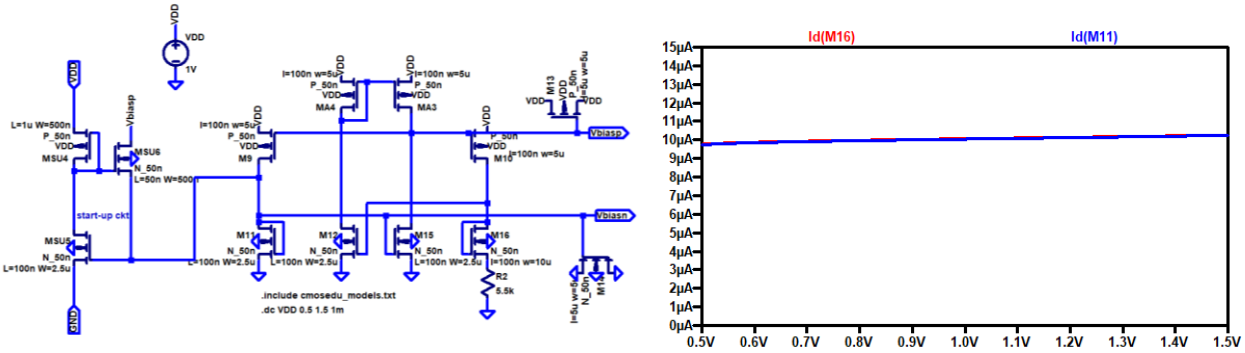
We see here that the minimum VDD from simulations is right around 1.65V. We expect a value of roughly 1.6V or VTHn because device M1 is diode connected, meaning it always operates in the saturation region. Once the gate-to-source voltage of this NMOS is equal to a threshold voltage through the startup circuit, the device begins sinking substantial amounts of current.

From the simulations above, the desired results were obtained, as Vbiasn stabilizes at VDD,min and Vbiasp vollows VDD at VDD,min.

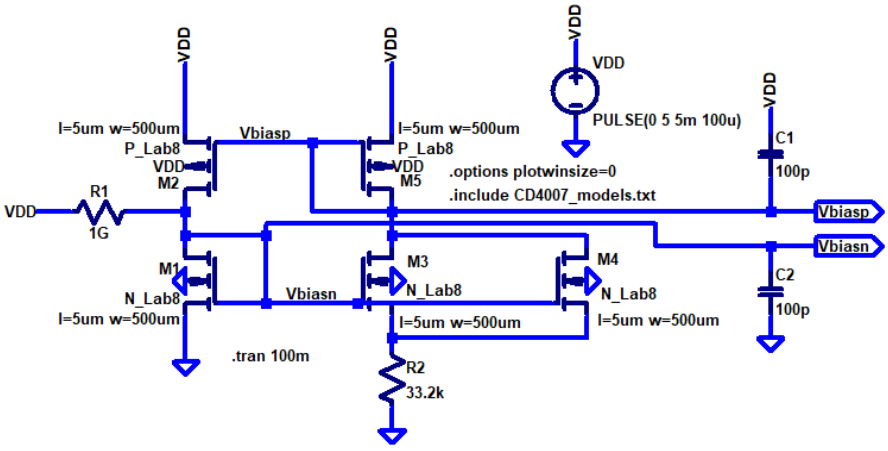
Instability Due to Capacitance



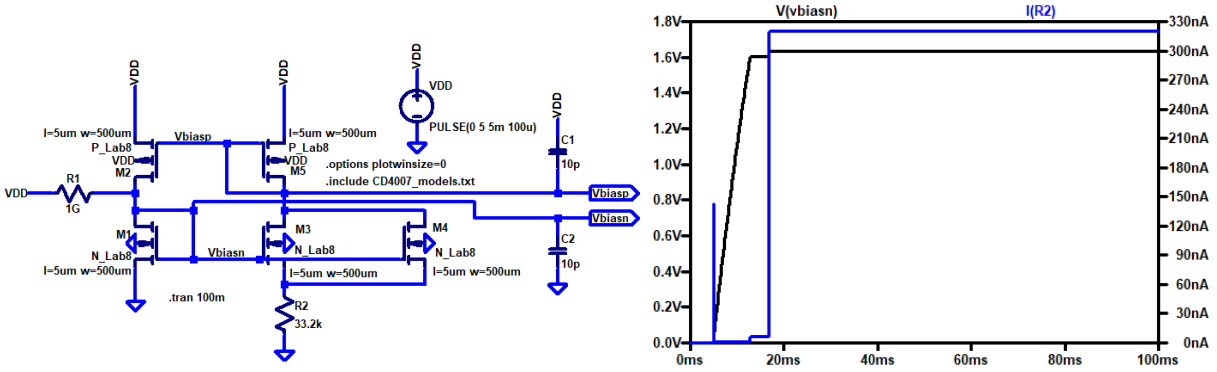
The snips found here are from HW 11 from EE 420 lecture. In the HW assignment, we were asked to show that adding the capacitors would ensure stable operation (below).



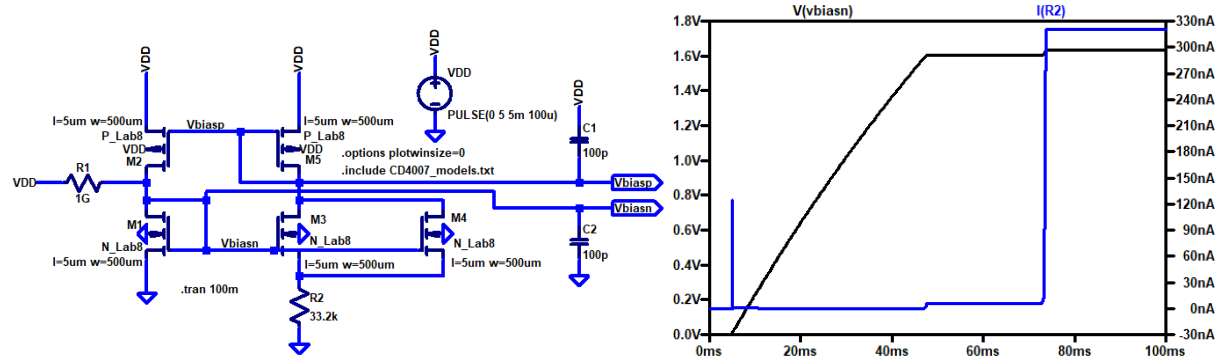
However, our assignment asks us to show unstable operation as a result of too much capacitance shunting the resistor. No matter how much capacitance was added, the circuit's startup time increased, but the operation still stabilized and did not oscillate. The conclusion is that level 1 models are too ideal and will not be unstable, even with large capacitors shunting the resistor.



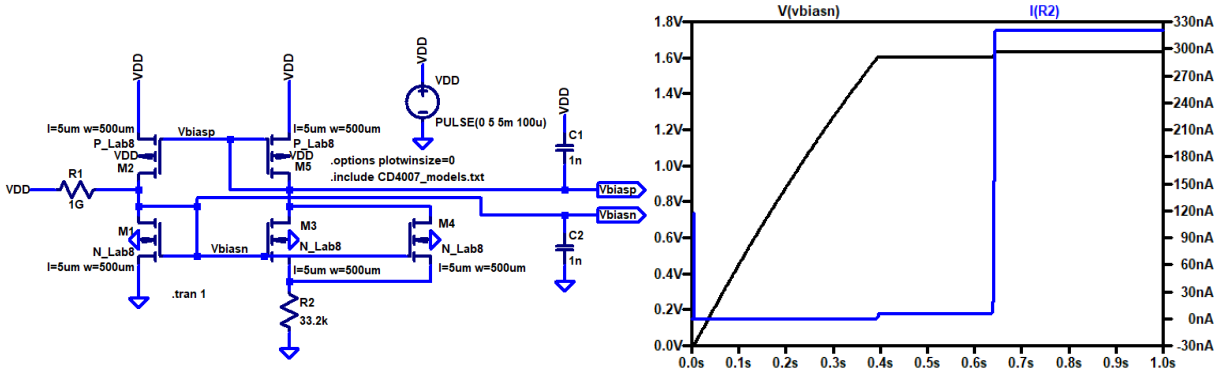
Adding 10pF capacitors



Adding 100pF capacitors



Adding 1nF capacitors



Comments:

The hand calculated resistor value was 29k. When a 29k resistor was used in spice, the transconductance gm was not precisely equal to the desired gm. Adjusting the resistance would change the current, by the equation

$$I_{REF} = \frac{2}{R^2 * KP_N * \frac{W}{L}} * (1 - \frac{1}{\sqrt{K}})^2$$

We see that the current is inversely proportional to the square of the resistance. We also know from the equation

$$g_m = \sqrt{2 * I_{REF} * KP_N * \frac{W}{L}}$$

that gm is directly proportional to the square root of the current. This means that in order to decrease gm, we need to increase resistance. Increasing the resistor from 29k to 33.2k makes the gm precisely 20uA/V.

The hand calculated current at the desired gm is 333 nA. The current in simulation when the BMR is operating is 320 nA, reasonably agreeable with the hand calculated value.

Finally, the minimum value of VDD was hand-calculated/estimated to be roughly Vthn or 1.6V, where simulation gave 1.65V, which are also agreeable values.