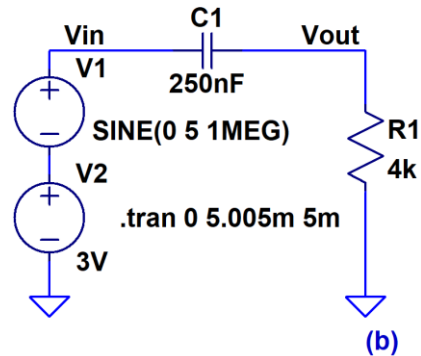
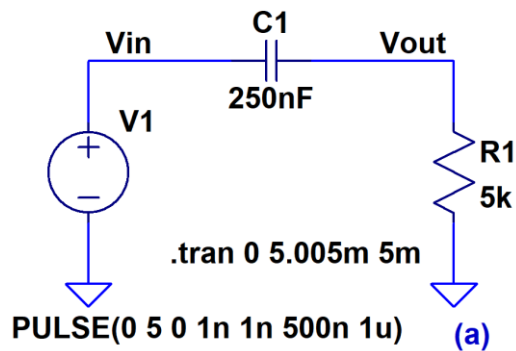


Show your work for credit!

- In steady-state conditions what is V_{out} ? When the input signal first starts, what is V_{out} ? Why? Verify your answers with four LTSpice simulations (one for each case, that is, when the simulation starts saving data at 0 and at 5 ms [around 5 time constants] and after the circuit reaches steady-state). Note, that no calculations are needed except for calculating the time constant and comparing it to the input period. These circuits **are practically important** and demonstrate AC coupling (as in an oscilloscope) an input signal. (4 points)



- Determine V_{out} for each of the following circuits. Sketch V_{out} and V_{in} on the same plot. Show your hand calculations for credit. Verify your answers using LTSpice. (8 points)

