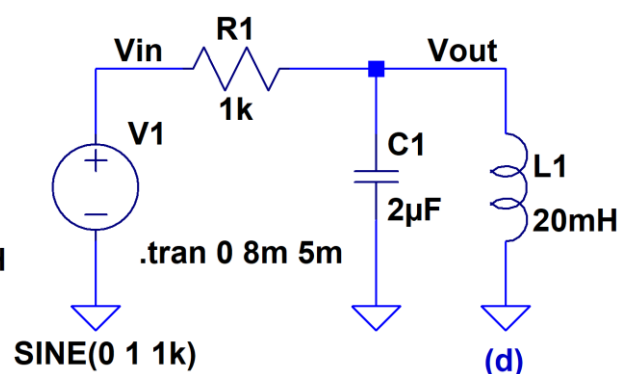
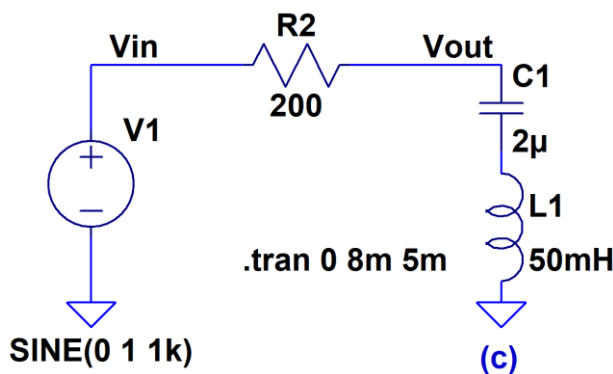
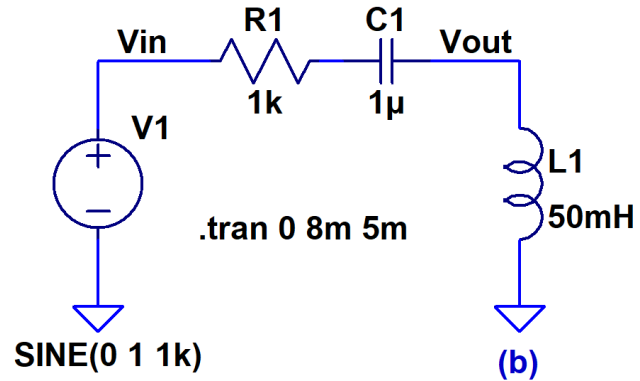
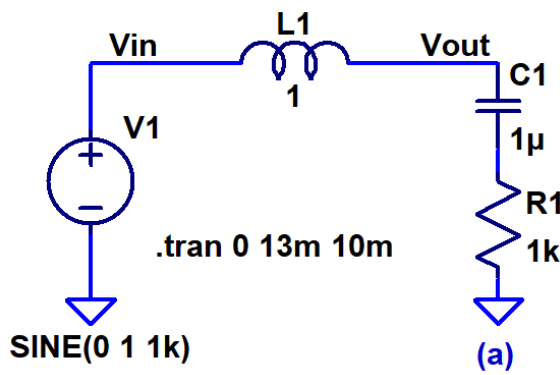


Show your work for credit!

- Determine V_{out} in each of the following circuits using phasor analysis in steady-state (not the start-up transient). Sketch V_{out} and V_{in} in the time domain on the same plot showing the phase shift. Verify your hand calculations and sketches using LTspice. (8 points)



- For the circuit in 1(c) determine the input frequency when V_{out} goes to 0. This is called series resonance. The energy stored in the capacitor is equal to the energy stored in the inductor. The energy is transferred back and forth between the two components during each oscillation cycle. A series resonant LC circuit behaves like a short so V_{out} is shorted to ground through LC and this is why V_{out} is zero. Also show that the current flowing in the circuit is $2V(\text{peak})/200\Omega$ or 10 mA peak when the input is at the resonant frequency and V_{out} is 0. Verify your hand calculations using LTspice. (2 points)
- For the circuit in 1(d) determine the input frequency when V_{out} is equal to V_{in} (parallel resonance, the LC behaves like an open). Show that no current flows in input source and $R1$ at this resonant frequency. Verify your hand calculations using LTspice. (2 points)