Self-Biased PLL/DLL

ECG721
60-minute Final Project Presentation

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Outline

• Motivation
• Self-Biasing Technique
• Differential Buffer Delay
  – Symmetric Load
• Bias Generator
• Self-Biased DLL
  – Zero-offset charge pump
• Self-Biased PLL
  – Feed-forward Zero
Motivation

• High-speed I/O ↔ High-freq. clock signal
• Jitter:
  supply and substrate noise
  process variation

Target: design a low jitter PLL/DLL
Jitter

• Definition: jitter is the deviation from, or displacement of true periodicity of a presumed signal in electronics and telecommunications, often is relation to a reference clock source.

• Jitter can be observed in frequency of successive pulses, the signal amplitude, or phase of periodic signals.
Jitter - Time Domain

- Observed Voltage
- Phase
- Frequency

Graphs showing voltage, phase, and frequency over time.
Jitter-Freq. Domain

IDEAL SINE WAVE  AMPLITUDE NOISE  PHASE NOISE

TIME DOMAIN

FREQUENCY DOMAIN

Model
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Self-Biasing

• Avoid the need for external biasing circuit
• Allow circuits to choose the operating bias levels in which they function best
• Operating bias levels are essentially established by the operating frequency
Self-Biasing Merits

- Provide a bandwidth tracking the operating frequency
- Broad frequency range minimized supply and substrate noise
- Fixed damping factor
- Bandwidth to operating frequency ratio is determined by a ratio of capacitances giving effective process technology independence
- No need of external bias circuit
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Differential Buffer Delay

- PLL/DLL needs buffer stage with low noise
- Symmetric load and replica-feedback biasing (half-replica bias circuit)
Symmetric Load

- Diode-connected PMOS in shunt with an equally sized biased PMOS
- Voltage-controlled resistor (Fig.19.57)

Output Swing

Vref to ground

Figure 19.57 A differential delay element based on a voltage-controlled resistor. The bias circuit adjusts the value of the resistors used in the delay elements to sink the current sourced by the p-channel MOSFETs.
Symmetric Load

- $V_{BN}$ dynamically changing the bias current which is two times of diode-connected PMOS with $V_{ctrl}$ as gate voltage
- Different $V_{ctrl}$ has different bias current
- Output swing is VDD to $V_{ctrl}$
Symmetric Load

- Load I-V curve is symmetric about the output center voltage
- Effective resistance changes with $V_{\text{ctrl}}$ → buffer delay changes with the control voltage
- $V_{\text{BN}}$ is changed by $V_{\text{ctrl}}$ to maintain the symmetric IV characteristics
Differential Buffer Delay

- Good control delay
- High dynamic supply noise rejection
- $V_{BN}$ can compensate drain and substrate voltage variations by dynamically biasing the NMOS current source
- The layout is very compact
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Prevent the $V_{CS}/V_{BN}$ from completely turning off the bias current sources
Bias Generator

- $V_{BN}$ and $V_{BP}$ produced by $V_{ctrl}$
- $V_{BN}$ keeps Bias current for buffer delay (constant and independent of supply voltage) by using a differential amplifier and a half-buffer replica
- $V_{BP}$: Additional half-buffer replica to provide a buffer of $V_{ctrl}$
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Self-Biased DLL

- Phase detector/Phase comparator
- Charge pump
- Loop filter
- Bias generator
- VCDL
Self-Biased DLL

- DLL is designed to re-buffer the input clock without adding any effective delay.
- PFD detects the phase error between the input and feedback output.
- Forward path integrates the phase error and adjust the delay through VCDL.
- Once in lock, the VCDL delay is the integer multiple of the input period.
Zero-offset Charge Pump

- In-phase inputs requires the UP and DN with an equal and short period of time.
- If the inputs of PFD produce no UP or DN pulses, it will take some finite phase difference before a large enough pulse is produced to turn on the charge pump, which leads to a dead-band region.
Zero-offset Charge Pump

• Produce equal duration of UP and DN outputs when DLL is in lock
• Composed of Two NMOS source coupled pairs with separate same buffer bias current and connected by a current mirror made from symmetric loads
Zero-offset Charge Pump

- The left source-couple pair behaves like half-buffer replica and produce Vctrl at the current mirror node
- The right PMOS has Vctrl in its gate and drain
Zero static phase offset when both the UP and DN outputs of the phase comparator with equal duration on every cycle of in-phase inputs
Zero-offset Charge Pump

- $\Delta \omega = \omega_o - \omega_{ref} > 0$, UP pulse is longer than DN pulse. $I_{d1}=I_{d2}, I_{up}>I_{d2}$, so $I_{cap}$ will discharge the cap of loop filter, reducing $V_{ctrl}$.
- $\Delta \omega = \omega_o - \omega_{ref} = 0$, UP and DN outputs for equal durations on every cycle. $I_{d1}=I_{d2}=I_{up}$
Zero-offset Charge Pump

\[ \Delta \omega = \omega_o - \omega_{\text{ref}} > 0, \] smaller \( V_{\text{ctrl}} \) makes the \( V_{SG} = V_{DD} - V_{\text{ctrl}} \) larger, which means larger current and smaller effective resistance. Hence, large charge offset leads to reduce the delay or small phase offset \( \rightarrow \text{Unlocked} \)
• $\Delta \omega = \omega_o - \omega_{ref} = 0$, UP and DN outputs for equal durations on every cycle. Vctrl is fixed. The delay is integer multiple of input reference period. $\rightarrow$ Locked
Self-Biased DLL

\[ \omega_o > \omega_{\text{ref}}: \text{UP longer pulse, discharging C1, reducing Vctrl, larger current, smaller effective resistance, smaller delay} \]

\[ \omega_o < \omega_{\text{ref}}: \text{DN longer pulse, charging C1, increasing Vctrl, smaller current, larger effective resistance, larger delay} \]
Self-Biased DLL

• Input tracking jitter will be further reduced by setting the loop bandwidth as close as possible to the operating frequency

• The loop bandwidth $\omega_N$ is given by

$$\omega_N = I_{CH} \times K_{DL} \times F_{REF} \times \frac{1}{C1}$$

• If charge pump current $I_{CH}$ and VCDL gain $K_{DL}$ are constant, the loop bandwidth will track the operating frequency
Self-Biased DLL

• The VCDL gain for a n-stage is given by

\[ K_{DL} = \left| \frac{dD}{dV_{ctrl}} \right| = \frac{C_B}{4* I_D} \]

\( C_B \) is the total buffer output capacitance for all stages, \( D \) is the delay for an n-stage VCDL

• \( I_{CH} \) is set equal to the buffer bias current \( 2*I_D \) cancelling the \( K_{DL} \) depending on \( 1/I_D \) and leading to loop bandwidth that track the operating frequency without constraining the operating frequency range
Self-Biased DLL

- $I_{CH}$ can be set to some multiple $x$ of the buffer bias current such that

$$I_{CH} = x \cdot 2I_D$$

- The loop bandwidth to operating freq. ratio is given by

$$\frac{\omega_N}{\omega_{ref}} = I_{CH} \cdot K_{DL} \cdot \frac{1}{C1} \cdot \frac{F_{REF}}{\omega_{ref}}$$

$$= x \cdot 2I_D \cdot \frac{C_B}{4 \cdot I_D} \cdot \frac{1}{C1} \cdot \frac{1}{2\pi} = \frac{x \cdot C_B}{4\pi \cdot C1}$$
The loop bandwidth to operating frequency ratio is given by
\[
\frac{\omega_N}{\omega_{ref}} = \frac{x}{4\pi} \frac{C_B}{C_1}
\]

The capacitance ratio determined the loop bandwidth to operating frequency ratio and reduced the process technology sensitivity.
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Self-Biased PLL

- Phase detector, charge pump, loop filter, bias generator, and VCO, feedback divider
- Loop filter needs one resistor for stability
- Once in lock, the VCO generates output frequency \( N \) times larger than input reference
- The PLL can be used to multiply and rebuffer an input clock without adding delay
Self-Biased PLL

- Use the second-order system knowledge to analyze the closed loop response to get the damping factor and natural frequency.

\[
\xi = \frac{1}{2} \sqrt{\frac{1}{N} I_{CH} K_{VCO} R^2 C_1} \quad \xi = \frac{\omega_n}{2} RC_1
\]

\[
\omega_n = \frac{2\xi}{RC_1} \quad \omega_n = \sqrt{\frac{K_D K_{VCO}}{NC_1}}
\]
Self-Biased PLL

• Make both damping factor and $\omega_n / \omega_{ref}$ are constant to get no limit on the operating frequency range and so that the jitter performance can be improved

$$\xi = \frac{1}{2} \sqrt{\frac{1}{N} I_{CH} K_{VCO} R^2 C_1}$$

• Constant damping factor = $I_{CH}$ equal to the buffer bias current + $R$ vary inversely proportionally to $\sqrt{\text{buffer bias current}}$
Self-Biased PLL

\[ \xi = \frac{\omega_n}{2} RC_1 \]

- Constant \( \xi \) makes \( \omega_n \) is proportional to the \( \sqrt{\text{buffer bias current}} \)
- In order to keep \( \omega_n/\omega_{\text{ref}} \) constant, the VCO operating frequency should also be proportional to the \( \sqrt{\text{buffer bias current}} \)
VCO frequency is proportional to $V_{\text{ctrl}} - V_{\text{th}}$ which is the square root of $I_D$, the slope is constant means $K_{\text{VCO}}$ is constant. So the reference frequency is proportional to the square root of the buffer bias current.
Feed-Forward Zero

- Transformation of the loop filter for the integration of the loop filter resistance
- Make the resistor is proportional to \(1/\sqrt{I_{buffer}}\)
- diode-connected PMOS with resistance 1/gm, which is inversely proportionally to the \(\sqrt{buffer\ bias\ current}\)
Self-Biased PLL

- Voltage drop across capacitor and resistor are generated separately and summed to form the control voltage $V_{CTRL}$, as long as the same charge pump current applied to each of them.
- Bias generator can conveniently implement this voltage source and resistor since it buffers $V_{CTRL}$ to form $V_{BP}$ with finite output resistance.
- The self-biased PLL can be completed by adding an additional charge pump current to generate $V_{BP}$. 
The operating frequency for an n-stage VCO is

\[ F = \frac{\sqrt{2 \cdot k \cdot I_D}}{C_B} \]

VCO gain \( K_{VCO} \) is given by

\[ K_{VCO} = \frac{k}{C_B} \]

The charge pump current and loop filter resistor are

\[ I_{CH} = x \cdot (2 \cdot I_D) \quad R = \frac{y}{\sqrt{8 \cdot k \cdot I_D}} \]
Self-Biased PLL

• The damping factor is then given by

\[
\xi = \frac{1}{2} \sqrt{\frac{1}{N} I_{CH} K_{VCO} R^2 C_1} = \frac{y}{4} \sqrt{\frac{x}{N} \frac{C_1}{C_B}}
\]

• The loop bandwidth to operating frequency ratio is given by

\[
\frac{\omega_n}{\omega_{ref}} = \frac{2\xi}{R C_1} \frac{1}{2\pi F_{ref}} = \frac{\sqrt{xN}}{2\pi} \sqrt{\frac{C_B}{C_1}}
\]
Self-Biased PLL

- The damping factor is a constant times the square root of the ratio of two capacitances.
- The loop bandwidth to operating frequency ratio is also a constant times the square root of the ratio of the same two capacitances.
- The loop bandwidth will track operating frequency and sets no constraint on the operating frequency range.
- Constant $\omega_n / \omega_{ref}$, $\xi$ can be set to minimize jitter accumulation over all operating frequencies.
References


3. ece.wpi.edu/analog/resources/plljitter.pdf