

K-Delta-1-Sigma Analog-to-Digital Converters

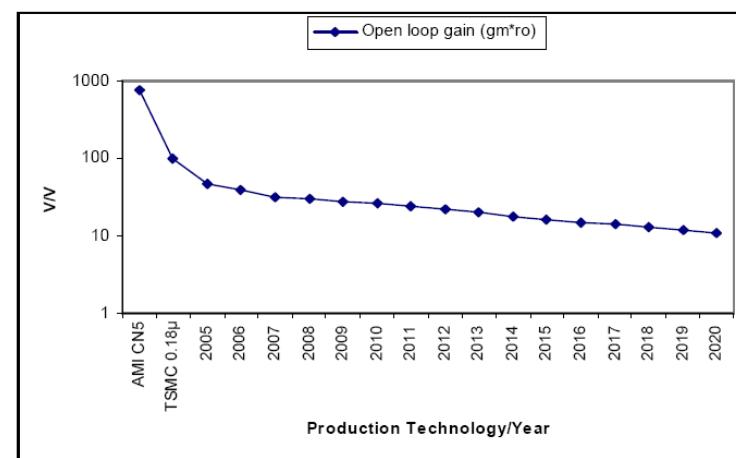
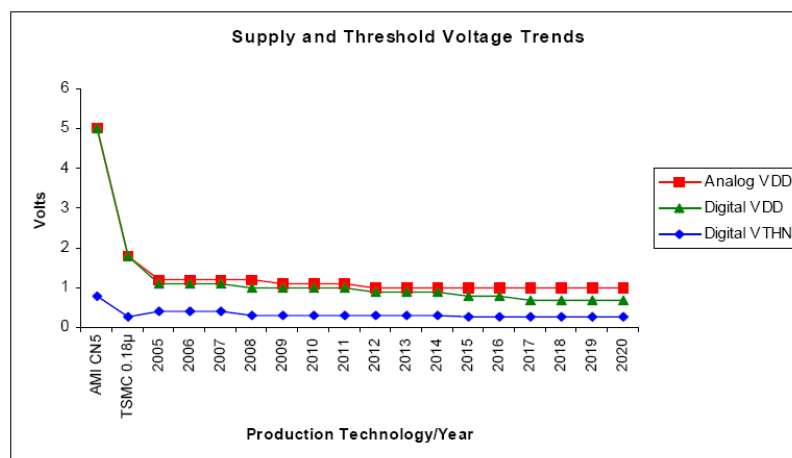
Vishal Saxena, Kaijun Li, Geng Zheng, and Jake Baker
Department of Electrical and Computer Engineering
Boise State University
jbaker@boisestate.edu

Abstract - As CMOS technology shrinks the transistor speed increases enabling higher speed communications and more complex systems. These benefits come at the cost of decreasing inherent device gain, increased transistor leakage currents, and additional mismatches due to process variations. All of these drawbacks influence the design of quality analog-to-digital converters (ADCs) in nanometer scale CMOS processes. To move towards a manufacturable ADC topology in nanometer CMOS our group at Boise State has developed the K-Delta-1-Sigma (KD1S) modulator-based ADC. The architecture has the potential to provide a solution to high-speed data conversion in nano-CMOS to replace the pipeline and flash architectures. This talk provides an overview of the KD1S ADC and provides experimental results verifying the data converter's operation.

Outline

- ❑ CMOS Scaling Trends
- ❑ ADC Design in nano-CMOS
- ❑ Delta-Sigma Modulation
- ❑ KD1S Modulator Topology
- ❑ Second-order KD1S Topology
- ❑ Conclusions and On-going Research

CMOS Scaling Trends



❑ V_{DD} is scaling down but V_{THN} is almost constant.

✓ Design headroom is shrinking faster.

❑ Transistor open-loop gain is dropping (~10's in nano-CMOS)

❑ Random offsets due to device mismatches.

$$\sigma_{\Delta V_{TH}} \propto \frac{1}{L \cdot W}$$

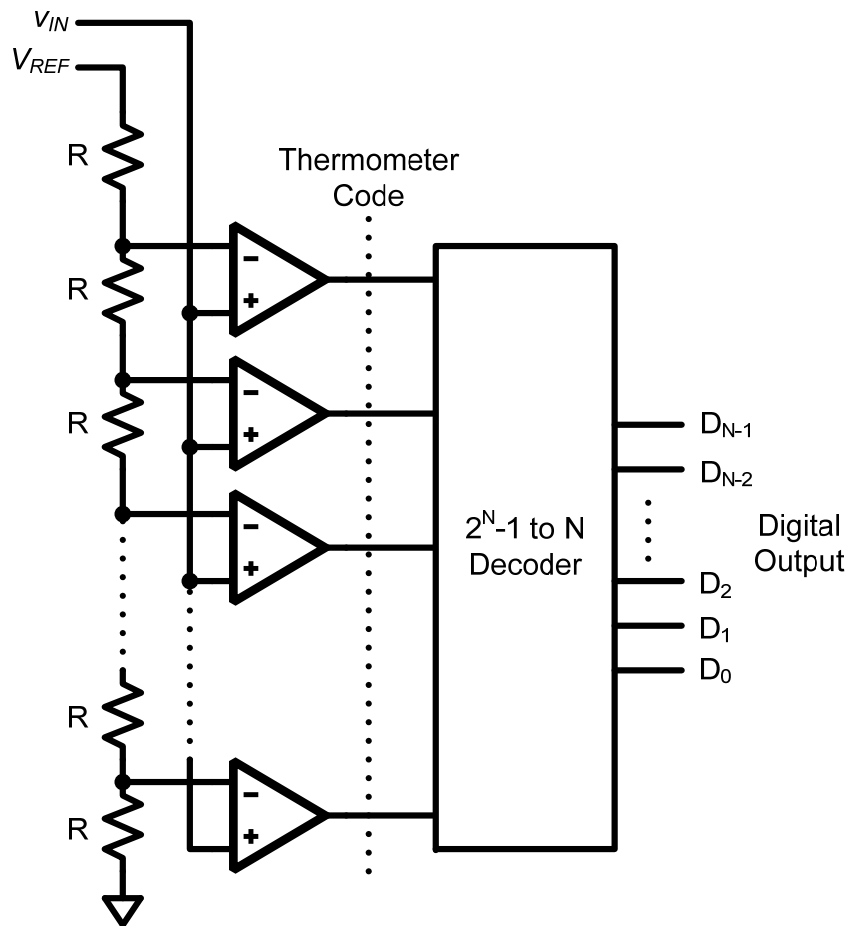
Ref: The International Technology Roadmap for Semiconductors (ITRS), 2006 [Online].

Available: <http://www.itrs.net/Links/2006Update/2006UpdateFinal.htm>

Analog to Digital Converters (ADC)

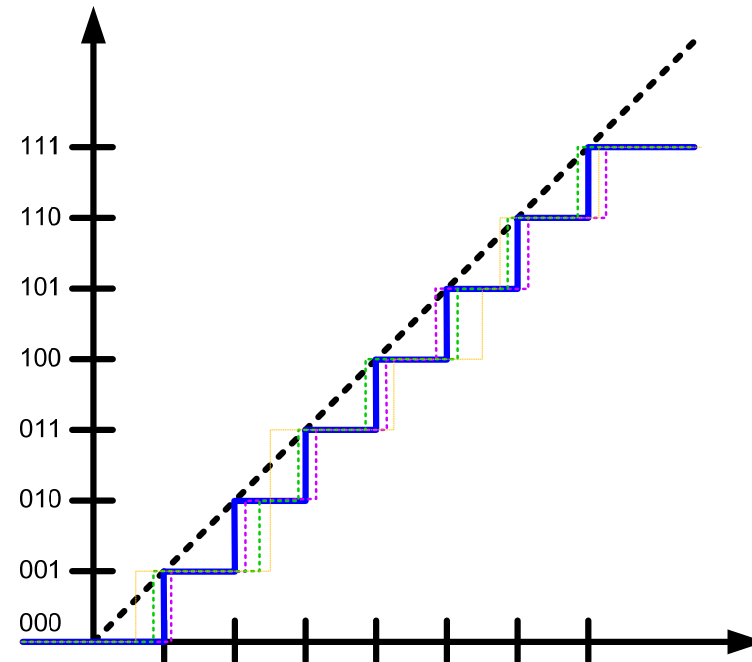
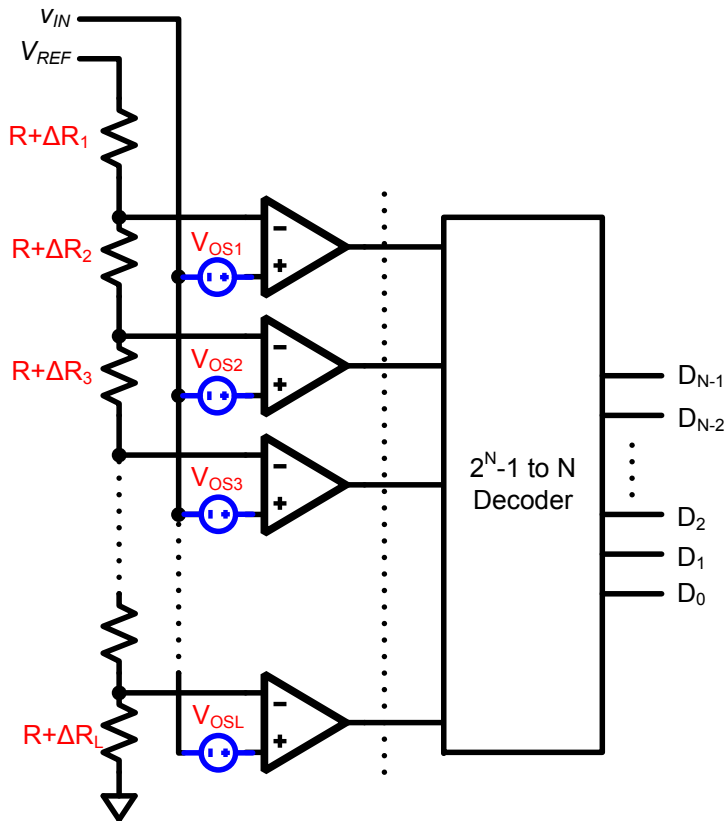
- ❑ ADCs form the interface between the analog and digital domains in a communication system
 - ✓ Rx and Tx path of an RF chain (1 MHz - 25 MHz)
 - ✓ Front-end for 10 Gb/s serial/optical links
 - ✓ Audio (44.1 kHz, 24 bits)
- ❑ Upcoming standards and application
 - ✓ UWB, Multiband WLAN, Software/Cognitive Radio (~1-10 GHz)
 - ✓ PAM signaling and equalization on serial/optical links (to 120 Gb/s)
- ❑ CMOS scaling enables higher sampling speed but at the cost of component mismatches and reduced gain (non-linearity).

Flash ADC Architecture



- ❑ 2^N-1 comparators in parallel for N -bit resolution.
- ❑ Equally spaced voltage references generated by a string of resistors.
- ❑ The resulting thermometer code is then converted to its digital equivalent output.
- ❑ Highest sampling speed at low bit resolution
 - ✓ 4-to-8 bit resolution and operate at speeds up to 1-4 GHz in CMOS.

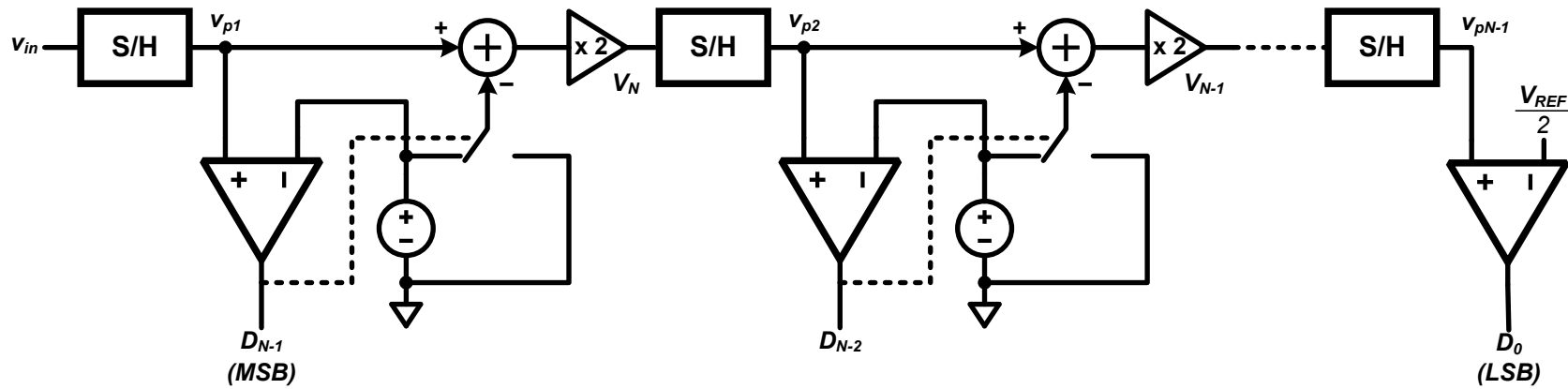
Flash ADC: Effect of Component Mismatches



$$|INL|_{\max} = \frac{V_{REF}}{2} \left| \frac{\Delta R_k}{R} \right|_{\max} + |V_{os,i}|_{\max}$$

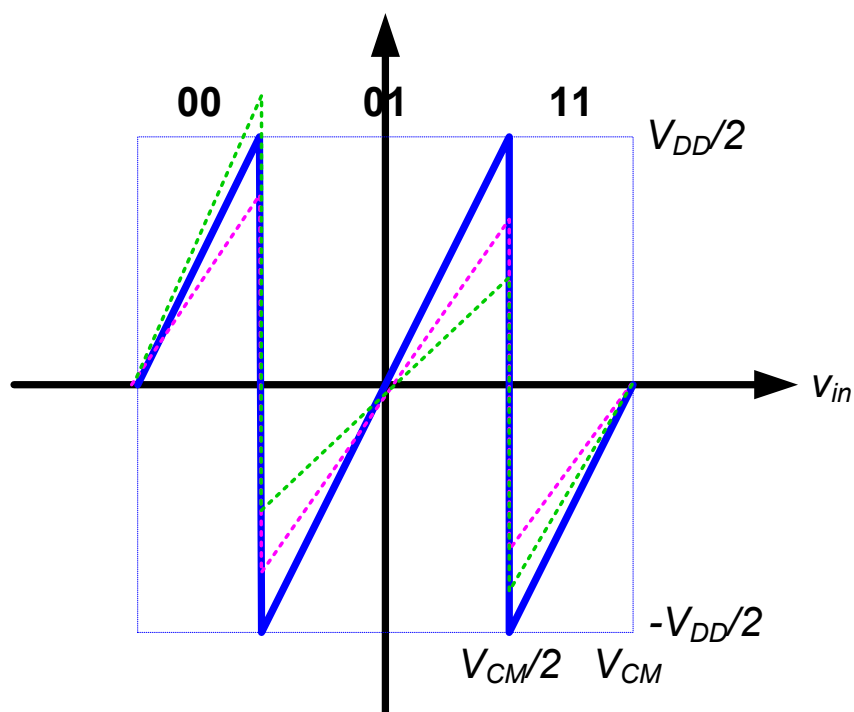
$$|DNL|_{\max} = \frac{V_{REF}}{2^N} \left| \frac{\Delta R_i}{R} \right|_{\max} + 2|V_{os}|_{\max}$$

Pipelined ADC Architecture



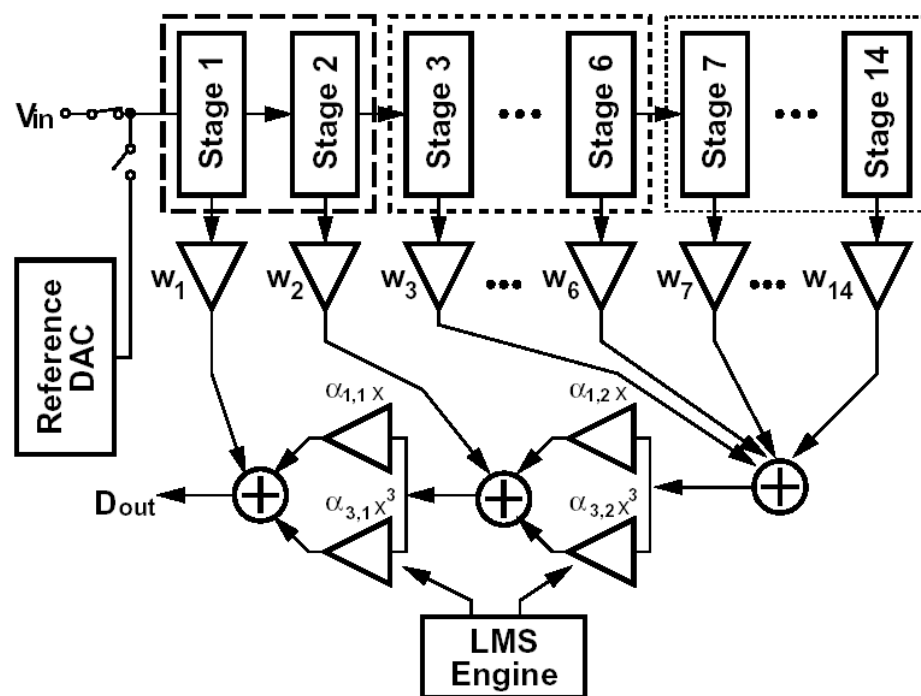
- ❑ N pipelined digitizing stages (MDACs)
- ❑ Algorithm: $(D_{k-2} = v_k > V_{ref}/2) \quad v_{k-1} = 2 * (v_k - V_{ref}/2) : 2 * v_k$
- ❑ Uses opamps for S/H in each MDAC.
- ❑ 1.5 bits/stage for robustness against comparator error.
- ❑ Moderate sampling speed at medium resolution
 - ✓ 100-500 MHz, 9-12 bits

Pipelined ADC: Effect of Component Mismatches



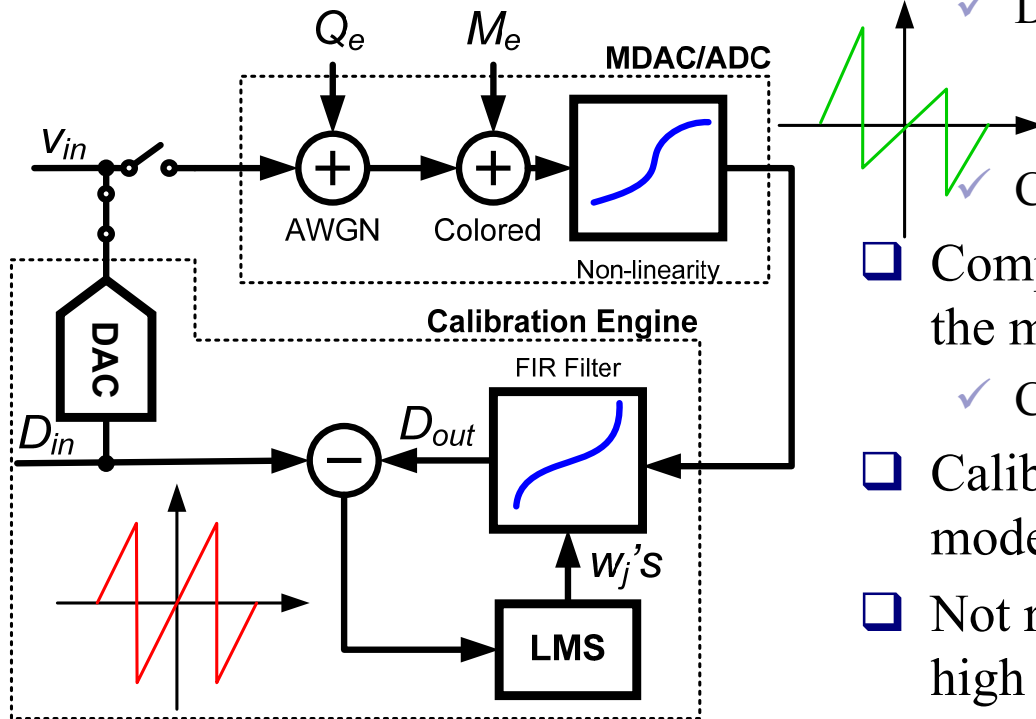
- ❑ For each MDAC in the pipe
 - ✓ Capacitance mismatch in S/H.
 - ✓ Opamp gain error.
 - ✓ Opamp non-linearity.
- ❑ Cascading MDAC non-linearity leads to
 - ✓ Reduction in resolution
 - ✓ Increase in INL and DNL.
 - ✓ Increase in harmonic distortion.
- ❑ Very hard to manufacture for high resolution in nano-CMOS.

Digital Calibration of ADCs



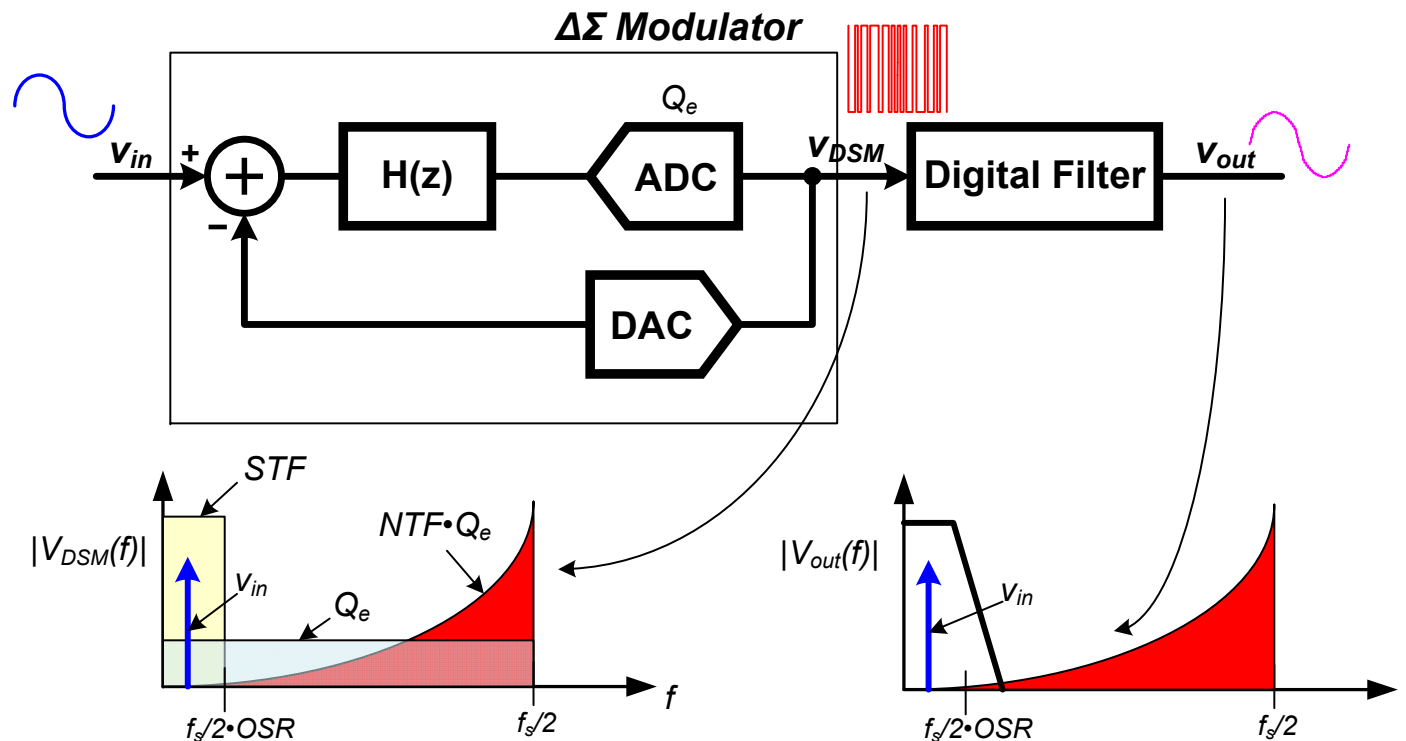
- ❑ Need digital calibration for rectifying the errors and non-linearity.
 - ✓ Model the analog block non-idealities and use adaptive filter to digitally compensate them (LMS fit).
- ❑ A high precision reference DAC needed for error estimation
 - ✓ DAC is slower (100 MHz).

Digital Calibration of ADCs



- ❑ Needs a higher precision DAC to adaptively equalize ADC response
 - ✓ DAC runs at slower frequency
 - ❑ Calibration may break down at high frequencies.
 - ✓ Circular clause and consequence problem!
- ❑ Compensates for the non-linearity but not the mismatch noise
 - ✓ Channel with colored noise.
- ❑ Calibration is as good as the error modeling!
- ❑ Not robust with further CMOS scaling and high speed operation.
 - ✓ Need topologies which are inherently robust to mismatches.

Delta-Sigma ($\Delta\Sigma$ or DS) Modulation

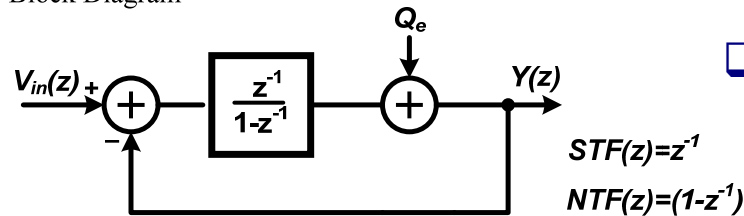


- Use oversampling ($f_s = 2 \cdot OSR \cdot BW$) to shape the quantization noise out of the signal band.
- Digitally filter away the out-of-band shaped (modulated) noise.
- Trades-off SNR with oversampling ratio.

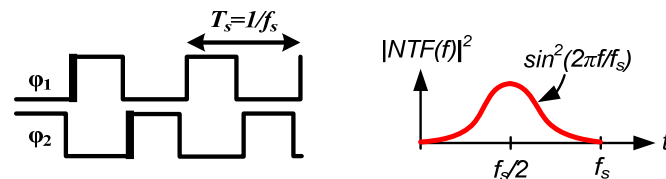
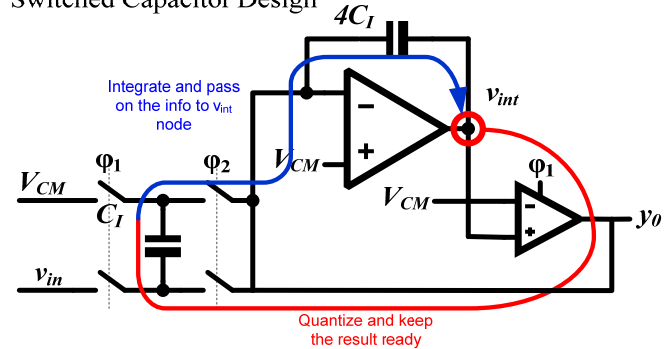
Ref: Baker, R. J., "CMOS Mixed-Signal Circuit Design, 2nd edition," Wiley-IEEE, 2009.

First Order DSM

Block Diagram



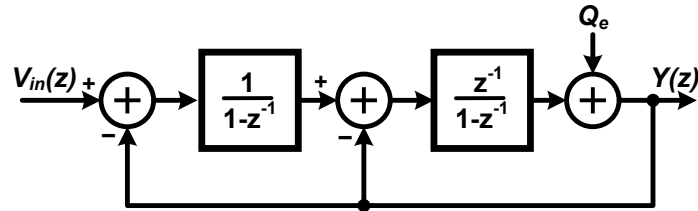
Switched Capacitor Design



- $Y(z) = z^{-1}V_{in}(z) + (1 - z^{-1})Q_e(z)$
 - ✓ Quantization noise is differentiated and pushed out of baseband.
- $N_{eff} = N - 0.566 + 1.5 \cdot \log_2(OSR)$
 - ✓ N is the resolution of the quantizer
 - ✓ $SNR = 6.02N + 1.76 - 5.17 + 30 \cdot \log_{10}(OSR)$
 - ✓ 9.43 bits for $OSR = 64$ and $N = 1$.
- Feedback structure desensitizes the component mismatches and nonlinearity in the forward path.
- Can use simple comparators with low gain, and larger offsets, noise etc.
- Op-amp can be lower gain ($A_{OL} > OSR$) and lower f_{un} .

Second-Order DSM

Block Diagram



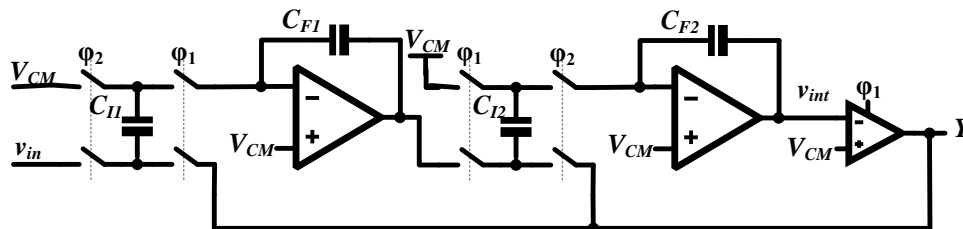
$$Y(z) = z^{-2}V_{in}(z) + (1 - z^{-1})^2Q_e(z)$$

- ✓ Quantization noise is double-differentiated.
- ✓ $N_{eff} = N - 1.85 + 2.5 \cdot \log_2(OSR)$
- ✓ $SNR = 6.02N + 1.76 - 12.9 + 50 \cdot \log_{10}(OSR)$
- ✓ 13.8 bits for $OSR = 64$ and $N = 1$.

$$STF(z) = z^{-2}$$

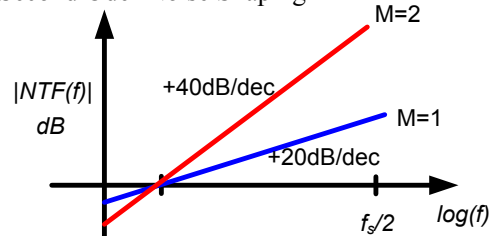
$$NTF(z) = (1 - z^{-1})^2$$

Switched Capacitor Design



- Reduced spurs due to randomization of noise.

Second Order Noise Shaping



- Can be generalized for any higher order modulator (M^{th} order)

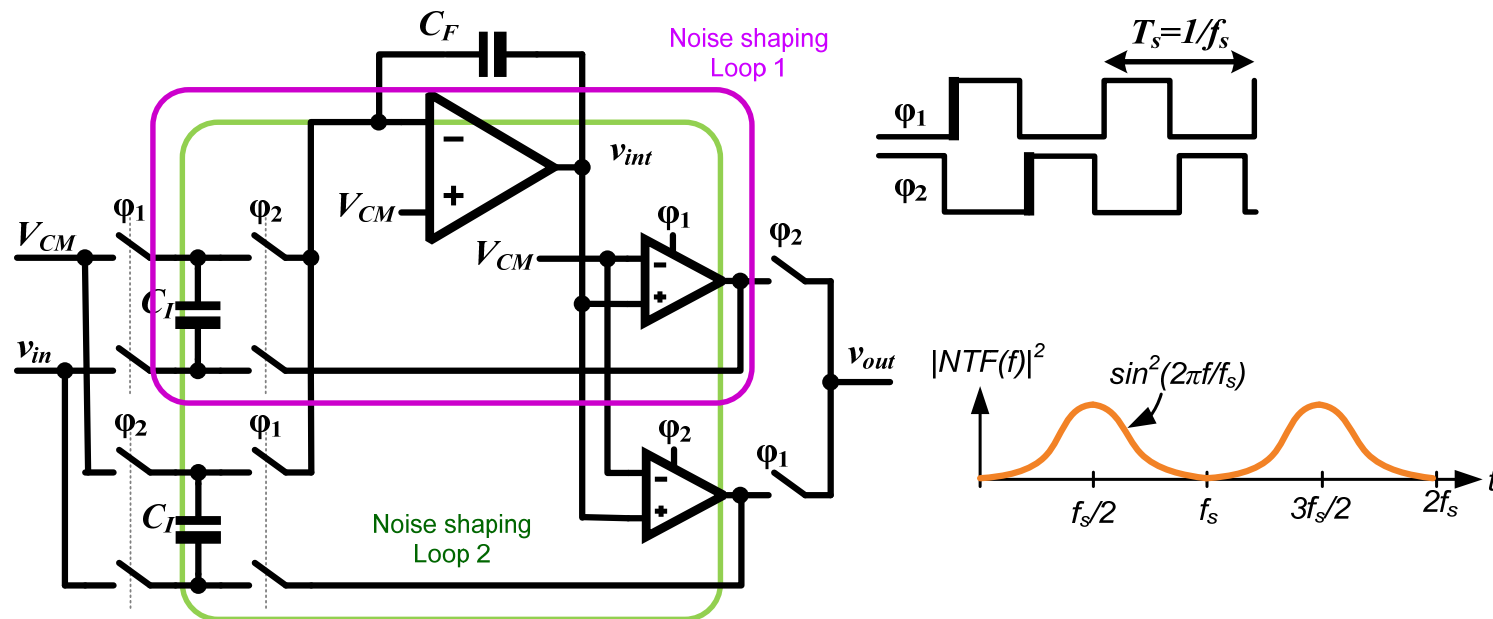
- ✓ $N_{eff} = N + (M + 0.5) \cdot \log_2(OSR)$
- ✓ Stability concerns for high-orders.

DSM for Wideband Data Conversion?

- ❑ Delta-Sigma ADC is suitable for nano-CMOS, but it requires oversampling.
 - ✓ Signal bandwidth is a fraction of the sampling rate ($< f_s/2 \cdot OSR$).
 - ✗ Not Nyquist-rate sampling as desired.
- ❑ Use many DSM's in parallel
 - ✓ Double Sampling
 - ✓ Time-Interleaved/Parallel DSMs.
- ❑ Cascade of low-*OSR* DSMs.

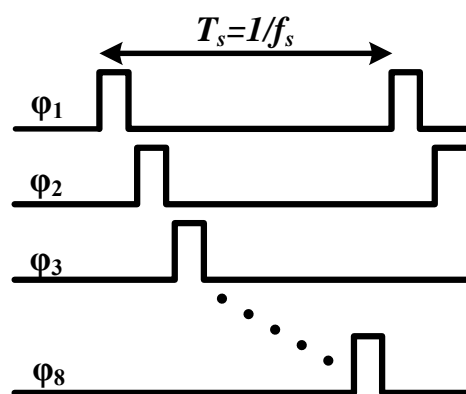
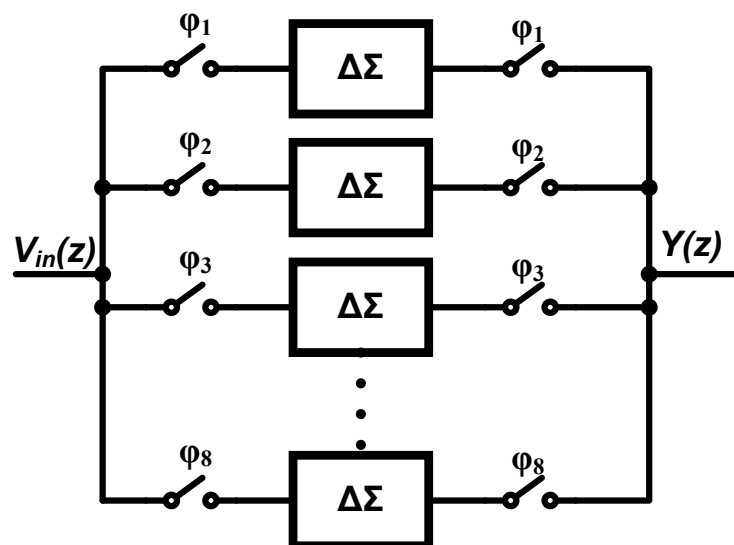
Double Sampling DSM

- Sample input at both the clock phases
 - ✓ Integrator is utilized for both the clock phases.
 - ✓ Can also use a single comparator clocked on both the phases.
- Two noise shaping loops exist, leading to two lobes in *NTF*.
- ✗ Path mismatches lead to folding of noise into baseband.



Ref: Yang, H.-K., El-Masry, E. I., "Double-Sampling Delta-Sigma Modulators," *IEEE TCAS-II*, vol. 43, no. 7, pp. 524-529, July 1996.

Time-Interleaved DSM

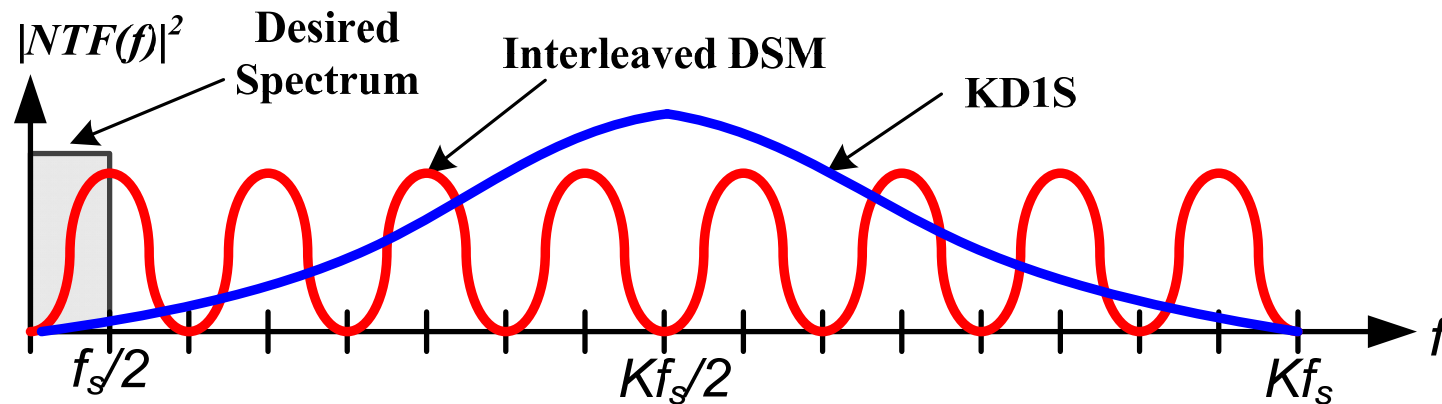


Non-overlapping Clocks

- Use K parallel time-interleaved DS Modulators.
 - ✓ Standard technique for Nyquist-rate ADCs.
- K -sets of opamps and comparators
 - ✗ K -times power consumption
 - ✗ Large area
 - ✗ Path mismatches will lower SNR and cause spurious tones.
- Does it really behave like a DSM with $K \cdot OSR$ oversampling?
 - ✗ No!

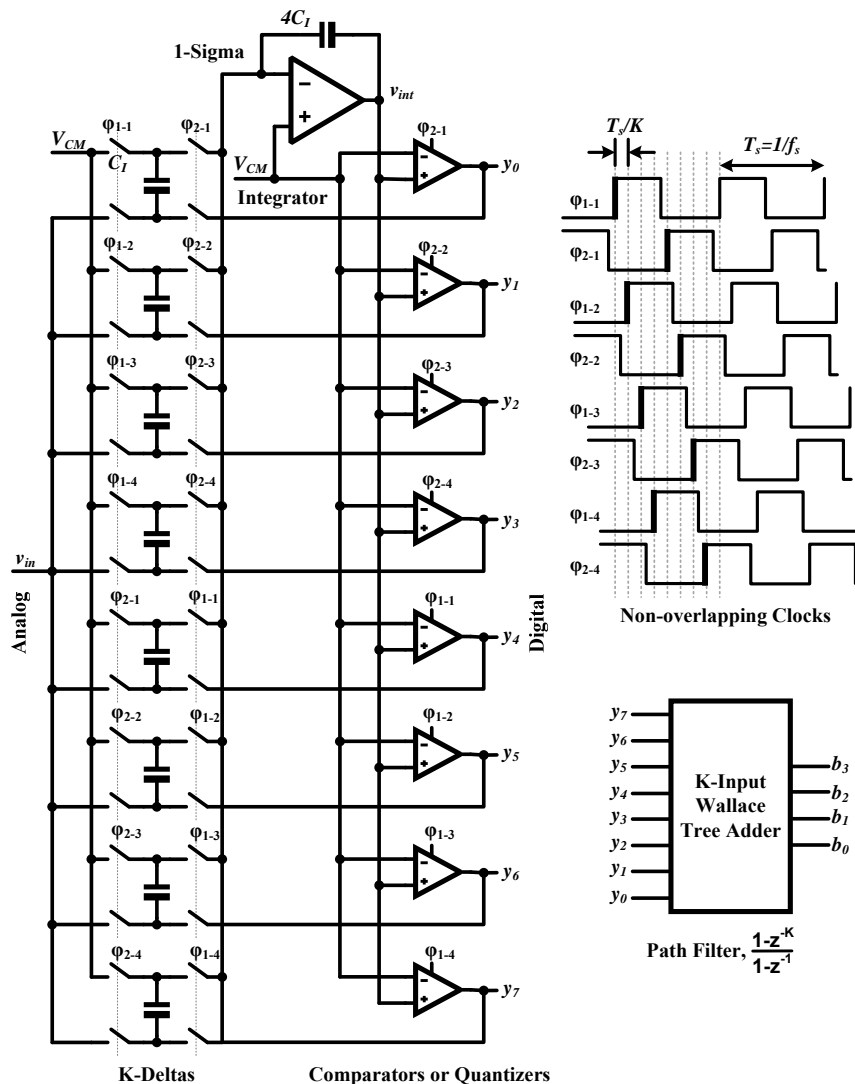
Ref: Eshraghi, A., and Fiez, T. S., "A Comparative Analysis of Parallel Delta-Sigma ADC Architectures," *IEEE TCAS-I: Regular Papers*, vol. 51, no. 3, Mar 2004.

Time-Interleaved DSM: Noise Shaping

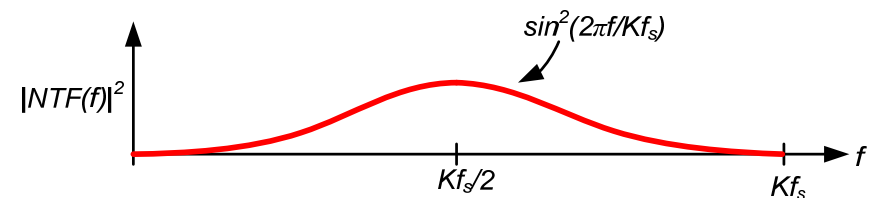


- ❑ Ripples in NTF with peaks at odd multiples of $f_s/2$.
 - ✗ Not true noise-shaping.
 - ✗ Only 0.5-bit increase in resolution with doubling in number of paths.
 - ❑ $N_{eff} = N + (M + 0.5) \cdot \log_2(OSR) + 0.5 \cdot \log_2(K)$
- ❑ The feedback signal in the delta-sigma loop arrives back to the input only after a delay of $T_s (= 1/f_s)$.
 - ✓ Noise shaping looks like a single DSM path.
- ❑ True noise shaping only possible when the feedback delay is less than T_s/K .
 - ✓ DSMs don't quite stack up like Flash or pipelined ADCs due to the feedback structure.

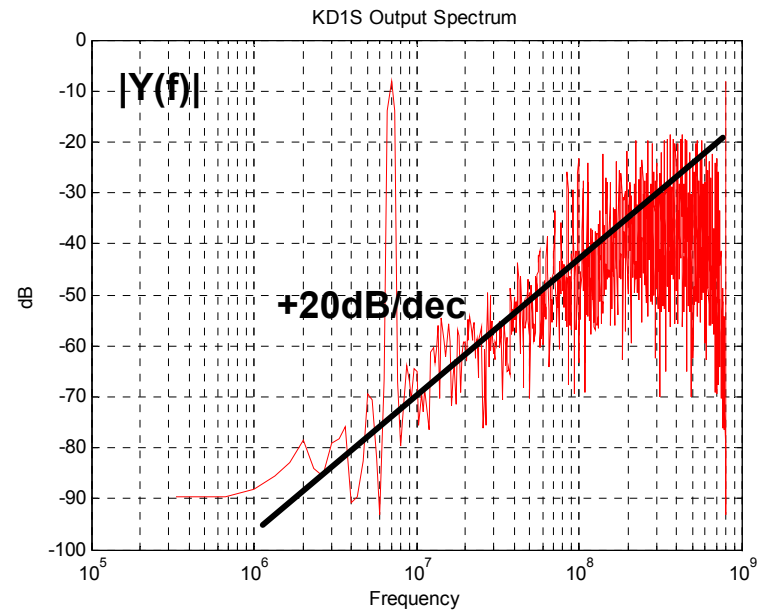
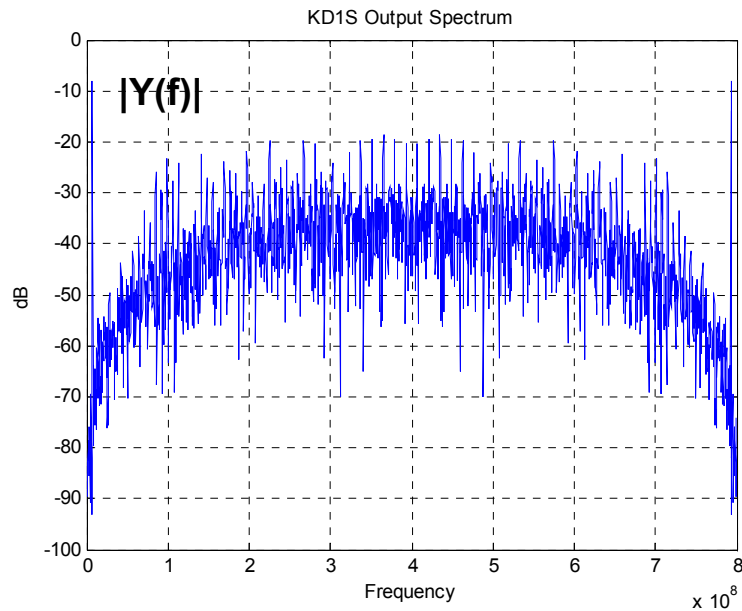
K-Delta-1-Sigma Modulator (KD1S)



- ❑ Share the op-amp across K -paths to realize a K -Delta-1-Sigma (KD1S) topology.
- ❑ Initially assume ideal components:
 - ✓ Comparators settle in $T_s/2K$ time.
 - ✓ Integrator $f_{un} \gg K \cdot f_s$
- ❑ Thus the error signal ($v_{in}[n] - Y[n]$) is cycled through the integrator within T_s/K duration.
 - ✓ True first-order noise shaping.
 - ✓ $N_{eff} = N + (M + 0.5) \cdot \log_2(OSR \cdot K)$

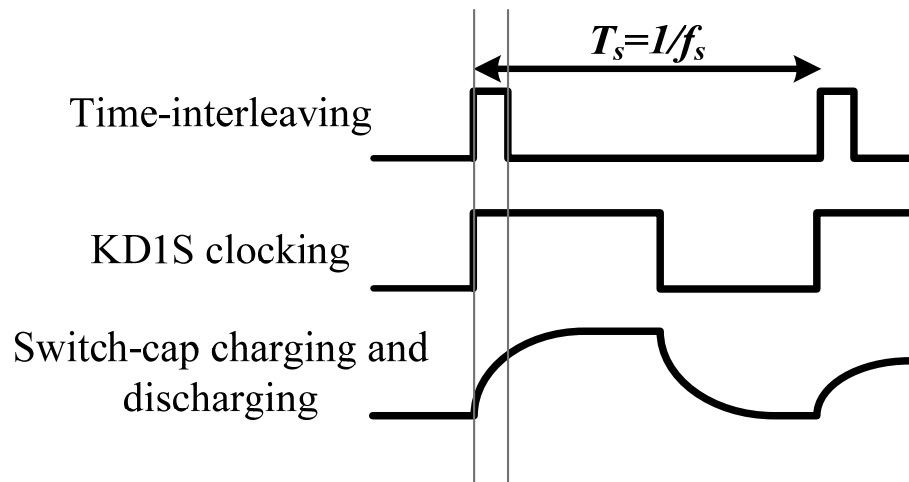


KD1S Simulation



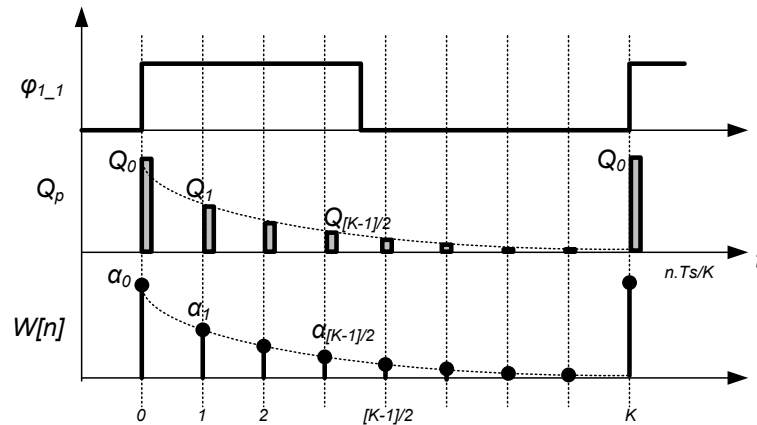
- $N = 1\text{-bit}$, $K = 8$, $OSR = 8$, $f_s = 100\text{ MHz}$, $f_{s,new} = K \cdot f_s = 800\text{ MHz}$.
- $BW = f_{s,new} / (K \cdot OSR) = 800\text{ MHz} / (2 \cdot 8 \cdot 8) = 6.25\text{ MHz}$.
- SNR = **58dB**, 9.34 bits.
 - ✓ Ideal first-order noise shaping.

KD1S with Non-ideal Components

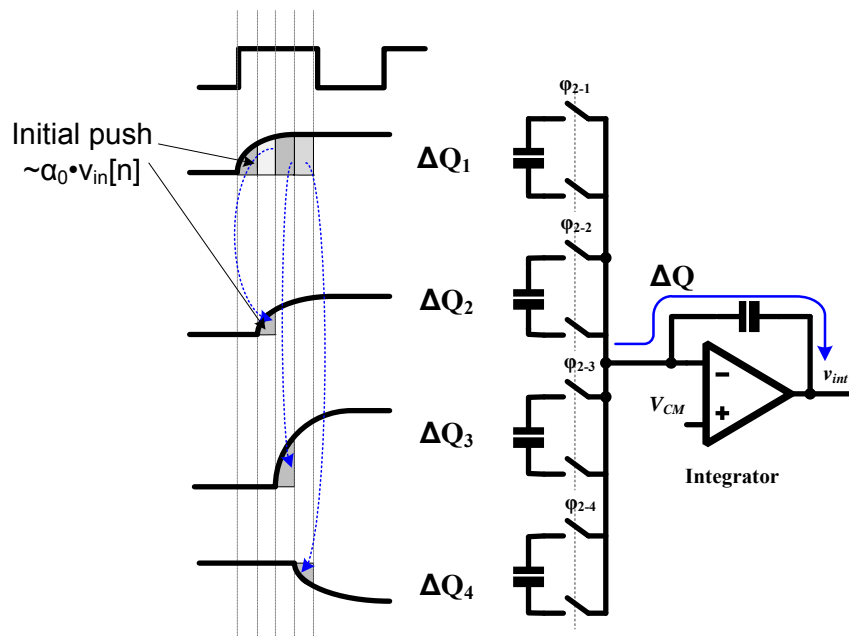


- ❑ Use a slow op-amp ($f_{un} \approx f_s$)
 - ✓ Each integrating path takes $T_s/2$ time to fully settle.
- ❑ Finite comparator speed.
- ❑ Effective sampling frequency ($f_{s,new}$) is only limited by the comparator speed and not the op-amp f_{un}
 - ✓ Significant speed and power benefits!
- ❑ Signal spreads into other paths due to the clocking scheme
 - ✓ Need to study the effects.

Charge Spreading



- ❑ Each path settles over $T_s/2$ duration.
- ❑ At any instance $K/2$ switch capacitors are connected to the integrator.
 - ✓ Charge from path- i leaks into path- j .
- ❑ The impulse response of the block is convolved with the charge spreading filter



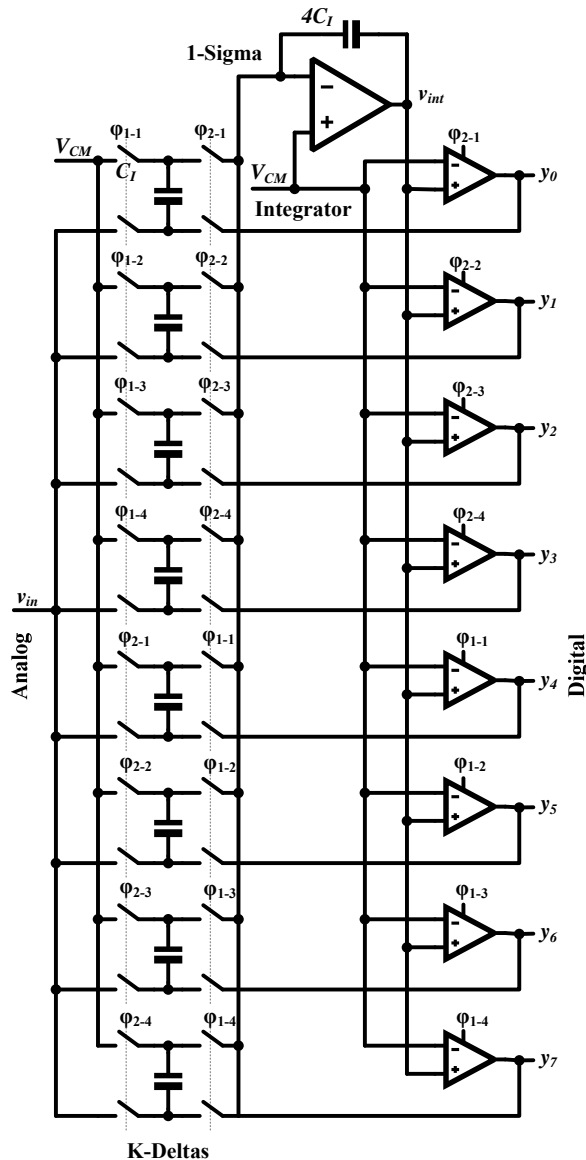
$$W(z) = \sum_{n=0}^{\infty} \left(\frac{3}{4} \alpha_0\right)^n z^{-n} = \frac{1}{1 - \left(\frac{3}{4} \alpha_0\right) z^{-1}} = \frac{1}{1 - \left(\frac{(K/2)-1}{(K/2)} \alpha_0\right) z^{-1}}$$

where

$$\alpha_0 = \left(1 - e^{-\beta f_{in}/Kf_s}\right)$$

is the partial settling factor (initial push) of the integrator.

KD1S with Non-Ideal Op-amp

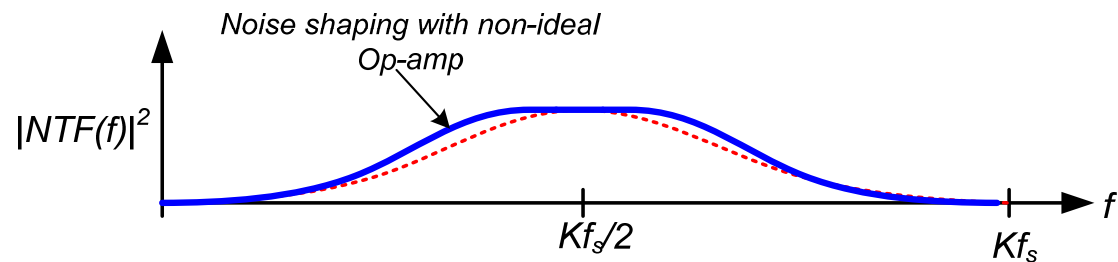


□ The theoretical result for the K-path Integrator are plugged into the KD1S Modulator:

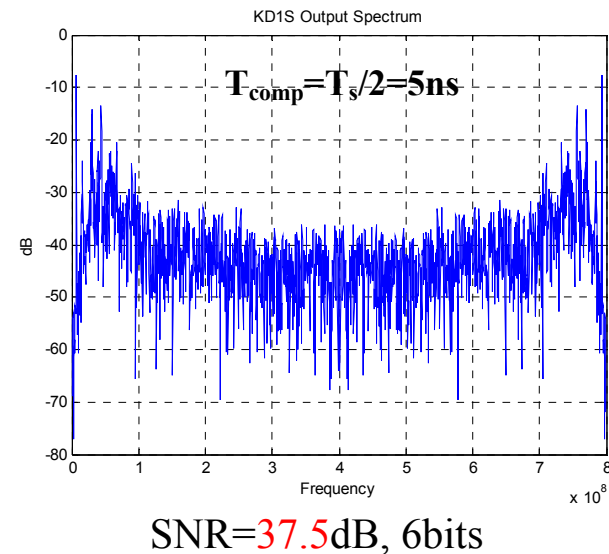
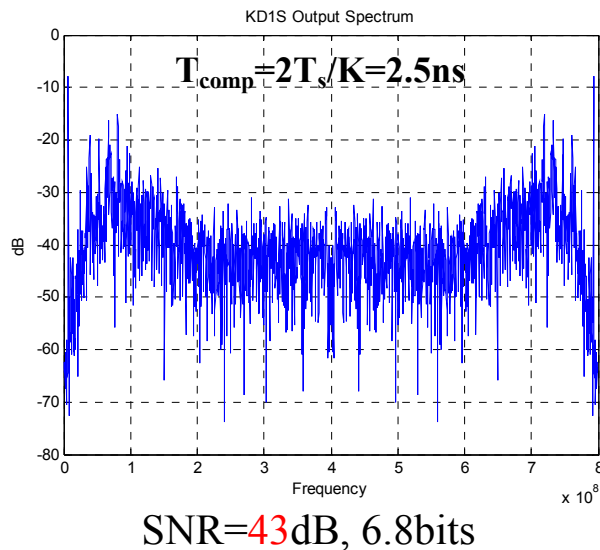
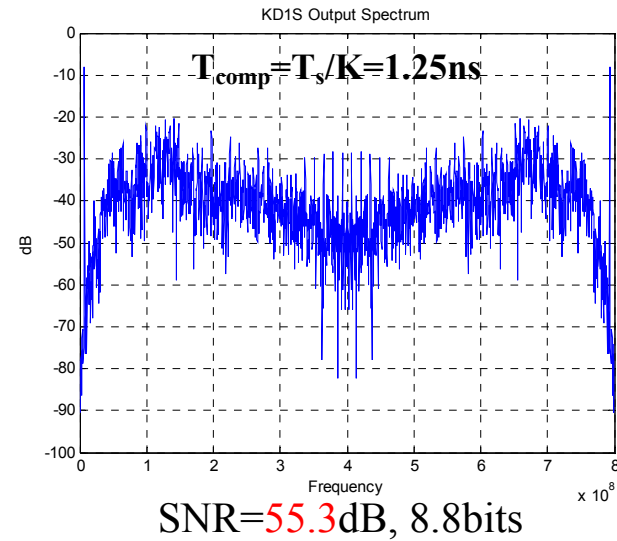
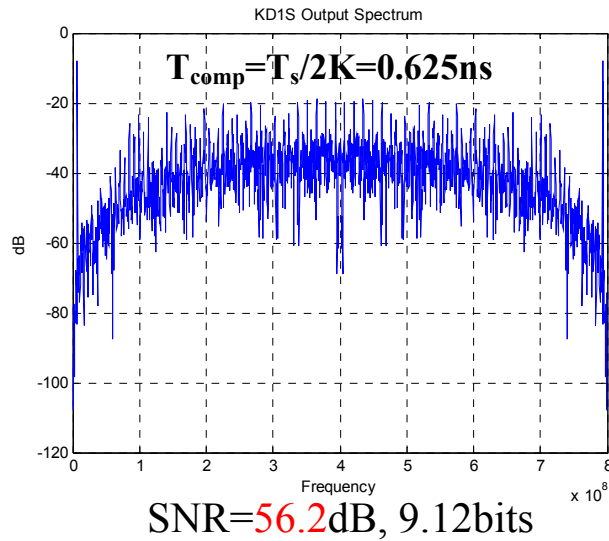
$$NTF(z) = \frac{1}{(1 + H(z) \cdot W(z))}$$

$$STF(z) = \frac{H(z) \cdot W(z)}{(1 + H(z) \cdot W(z))}$$

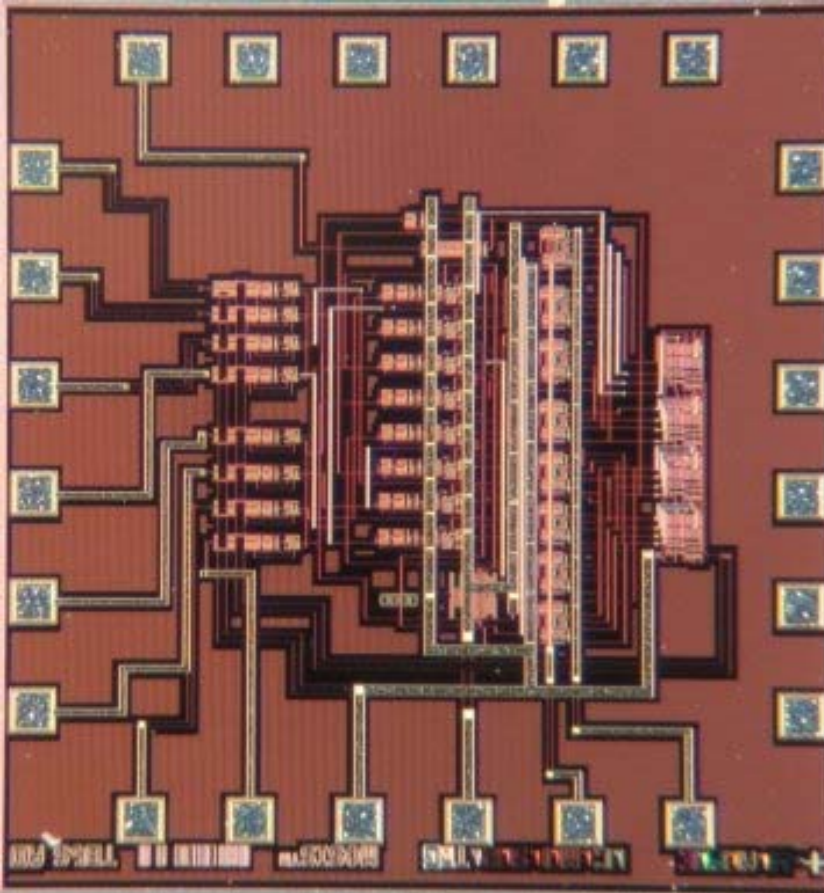
□ Worst case loss of ~1-bit resolution over ideal KD1S



KD1S: Effect of Comparator Delay



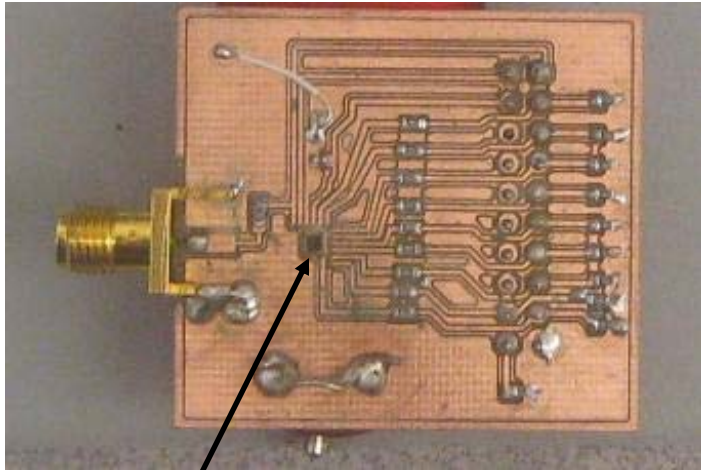
KD1S Test Chip Design from Mixed-Signal Book



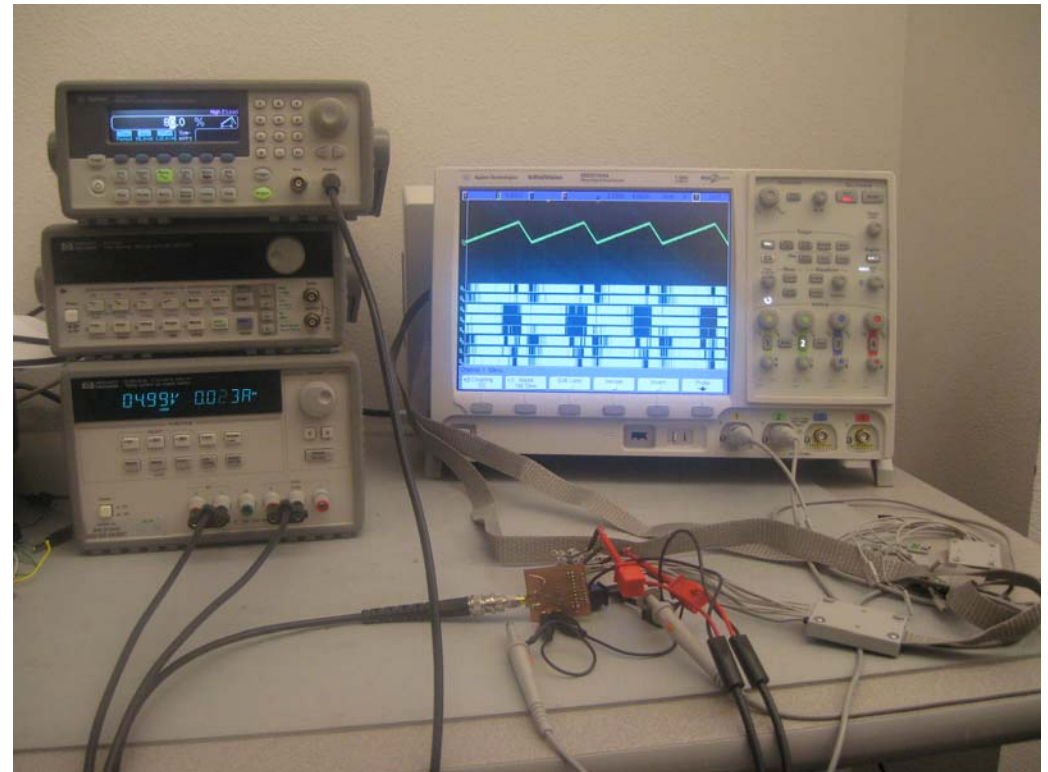
- ❑ KD1S Modulator design in 500 nm CMOS process.
 - ✓ Designed using comparator delay of $T_s/2$ (worst case performance)
 - ✓ Currently designs in the queue for higher performance
- ❑ DSP using Matlab and Agilent MSO7104.
- ❑ 8-path outputs registered on a 100 MHz clock.
- ❑ Measured SNR for 6.25 MHz BW = 36 dB
 - ✓ 6-bit resolution.
 - ✓ Proof of Concept
 - ✓ Follows the theory!

Harvesting Data

- ❑ The bare die was bonded to PC board to minimize the parasitics
- ❑ Agilent MSO7104A used to capture analog input and digital outputs



Chip bonded to PC board



Design Example Continued – Data Results

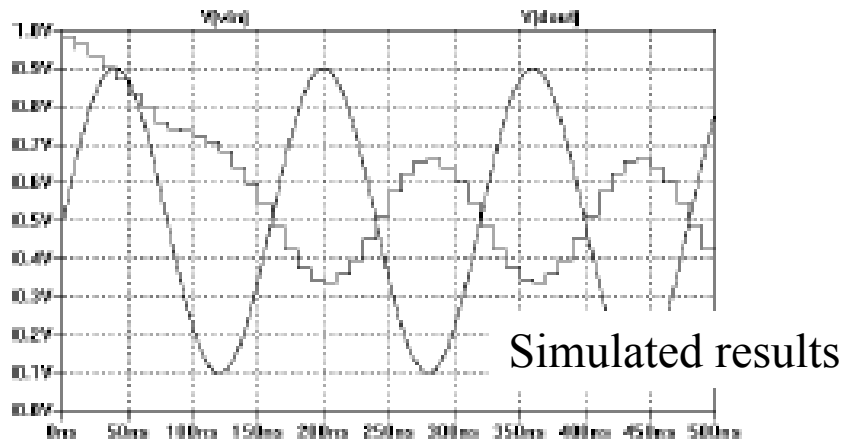
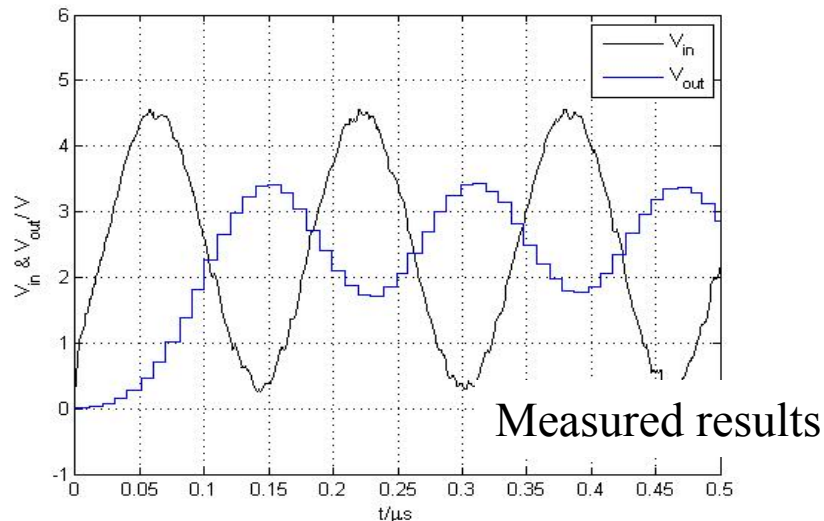


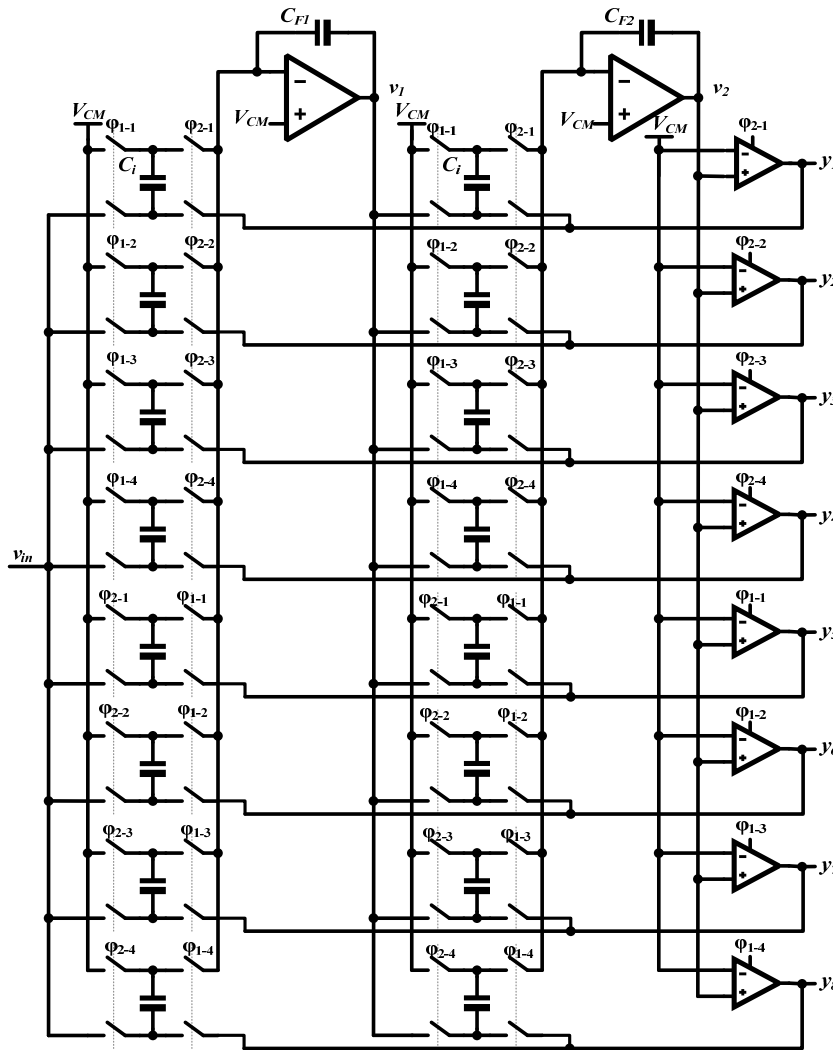
Figure 9.11 Simulating Fig. 9.10 with a 6.25 MHz input signal.



- ❑ The simulation example in Figure 9.11, seen at the left, was generated using ideal components with a VDD of 1 V.
- ❑ The data seen below this is the experimentally measured output of our data converter designed in a half-micron process with a VDD of 5 V.
 - ✓ Since the design is basically digital it's predictable
 - ✓ Note the start-up transient is the delay through the digital filter
 - ✓ Small differences are due to the sampling frequencies being different between the two sets of data

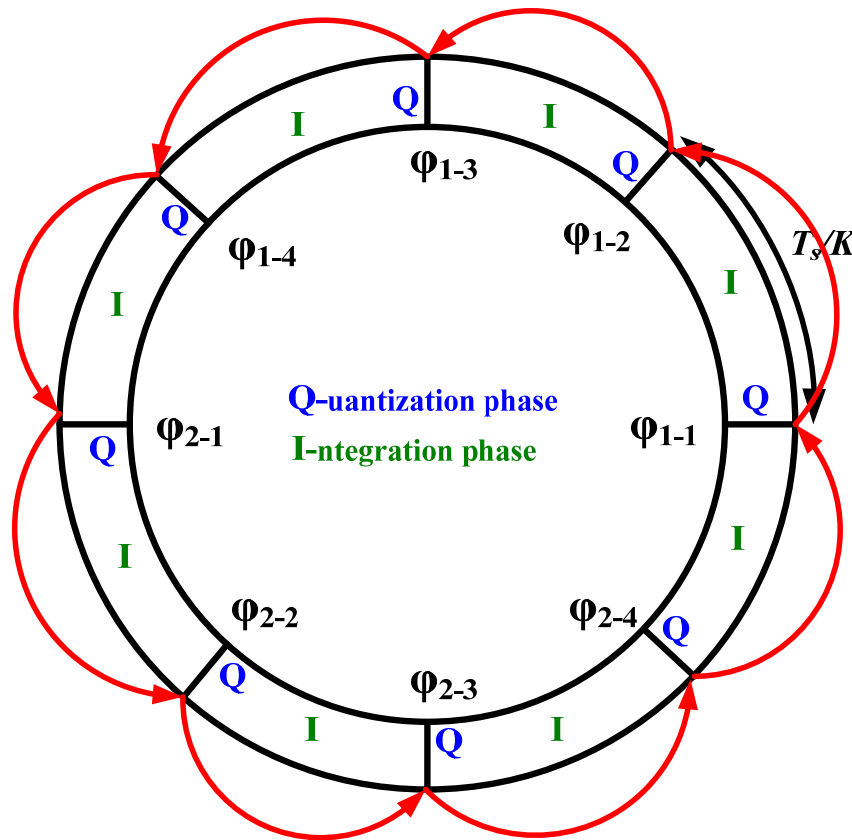
A 6.25 MHz input that is swinging from 10% to 90% of VDD

Can We Do Better? The Second Order KD1S



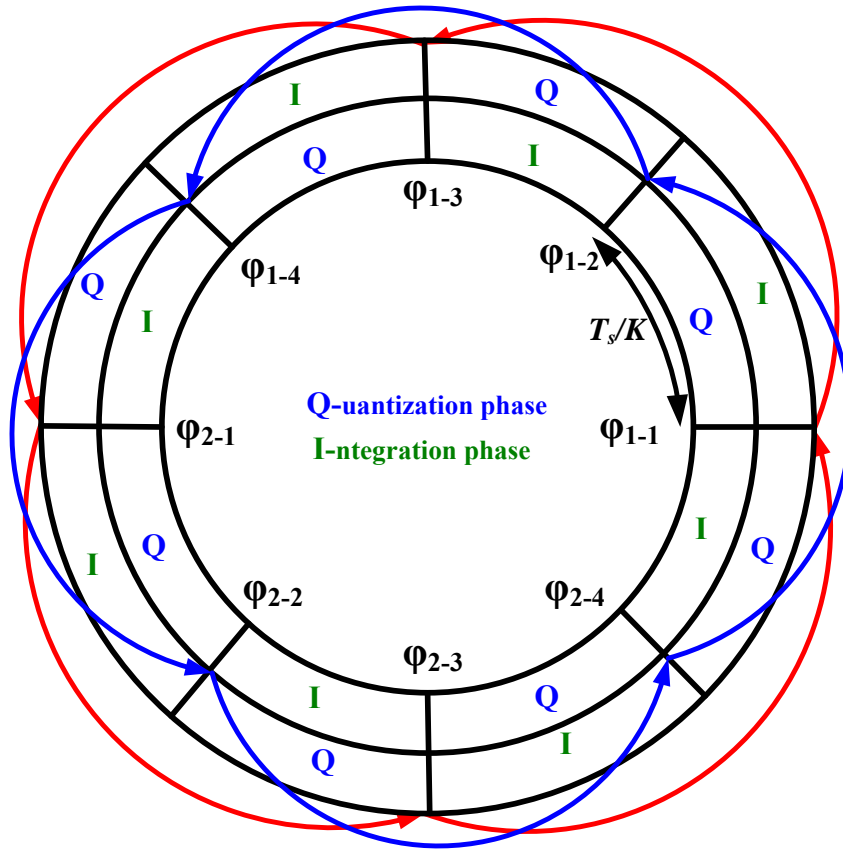
- ❑ Second-order noise shaping
- ❑ 2.5 bits increase with either doubling K_{path} or K !
- ❑ Clocking sequence is critical
 - ✓ Intuition from the circular clock phase diagram.
- ❑ Our group is designing prototypes in IBM's 130 nm process

Ideal KD1S- Circular Clock Phase Diagram (CCPD)



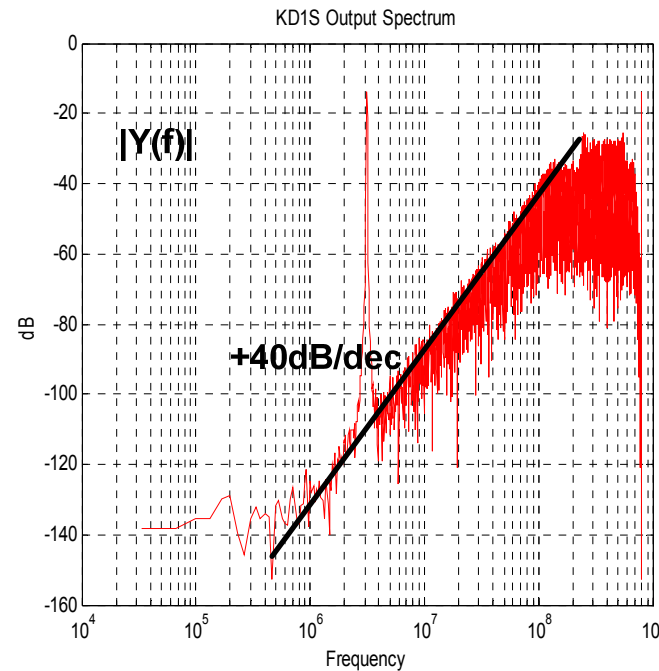
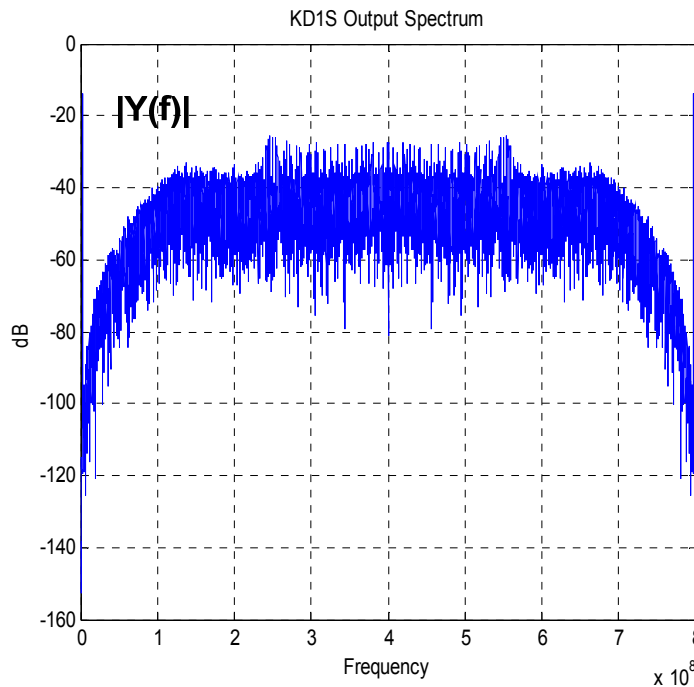
- A circular phase diagram is a convenient tool to understand the noise flow in a KD1S modulator.
- The arcs represent the cycling of v_{int} info across a path and the integrator forming a loop (T_s/K time):
 - ✓ $v_{int} \rightarrow y_i = Q(v_{int}) \xrightarrow{t} \Delta = v_{in} - y_i \rightarrow v_{int} = \Sigma(\Delta)$
- The arcs show an uninterrupted flow of noise causing differentiation of noise every T_s/K time period.
 - ✓ True first order noise shaping by K -times.

KD1S CCPD - $T_{\text{comp}} = T_s/K$



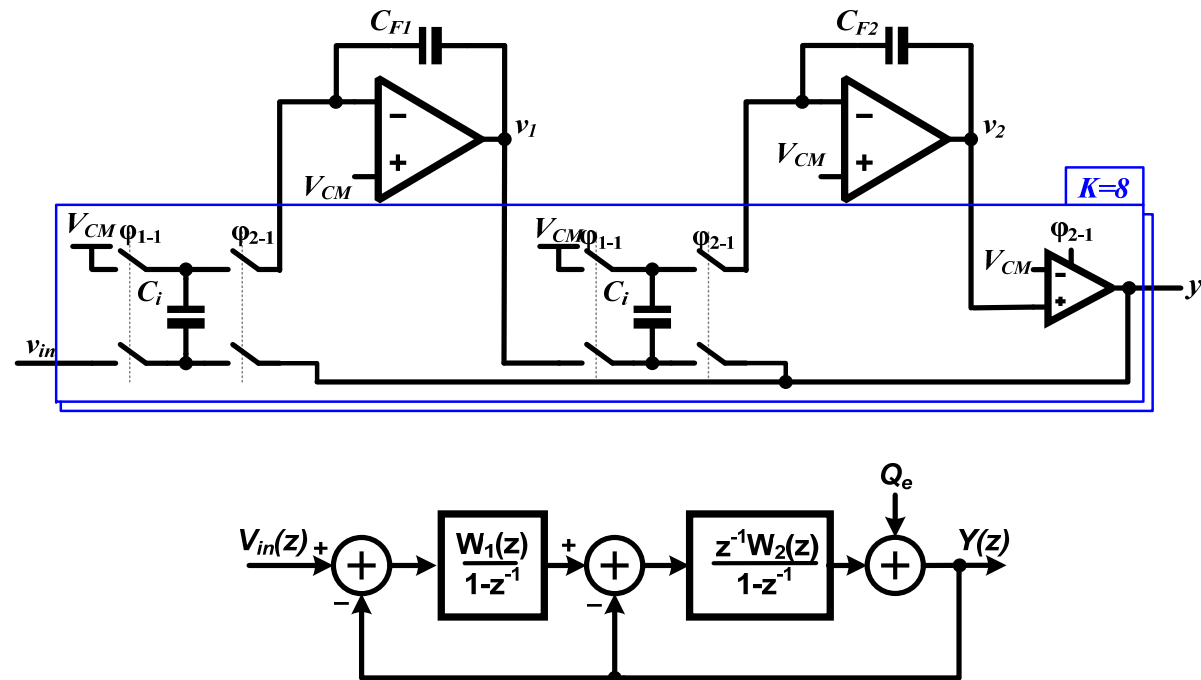
- ❑ Comparator settles in T_s/K time and is fired early by a T_s/K time slice.
- ❑ Here the noise shaping arcs get completed in $2T_s/K$ time period.
 - ✓ Formation of two distinct noise shaping loops (red and blue).
 - ✓ Noise gets differentiated in $2T_s/K$ time period.
 - ✓ $K/2$ -times noise shaping.
 - ✓ Doubling-sampling like response (two lobes in NTF) due to two distinct loops.

Second-Order KD1S Simulation



- $SNR = 71 \text{ dB}$, $N_{eff} = 11.5 \text{ bits}$
 - ✓ Ideal second-order noise shaping.
 - ✓ Reduced spurious tones.

Second-Order KD1S Concise Block Diagram



- ❑ Identical SC blocks repeated K -times.
 - ✓ Clocks follow the cyclical sequence.
 - ✓ Outputs are summed together as in KD1S topology.
- ❑ Block diagram will account for $W(z)$ for each K -path integrator.

Conclusion

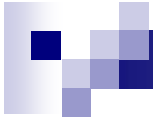
- ❑ Mismatch calibration is not the panacea for ADC design in nano-CMOS.
- ❑ K-Delta-1-Sigma Modulators combine the feedback desensitization of mismatches and inherent interleaving at low-power.
 - ✓ The KD1S is a manufacturable ADC for nano CMOS technology!
- ❑ A first-order noise shaping KD1S topology has been demonstrated.
- ❑ Simulation results for second-order KD1S are presented
 - ✓ A building block for realizing higher-order noise shaping topologies.
 - ✓ Potential for replacing Pipelined and Flash ADCs while avoiding extensive calibration.

References

- [1] Baker, R. J., "CMOS Circuit Design, Layout, and Simulation, Revised 2nd edition," *Wiley-IEEE*, 2008.
- [2] The International Technology Roadmap for Semiconductors (ITRS), 2006 [Online]. Available: <http://www.itrs.net/Links/2006Update/2006UpdateFinal.htm>
- [3] Zhao, W., Cao, Yu, "New Generation of Predictive Technology Model for sub-45nm Design Exploration" [Online]. Available: <http://www.eas.asu.edu/~ptm/>
- [4] Razavi, B., Aytur, T., Lam, C., Yang, F.-R., Yan, R.-H., Kang, H.-C., Hsu, C.-C., and Lee, C.-C. "Multiband UWB transceivers," *Proc. IEEE Custom Integrated Circuits Conference*, pp. 141-148, Sept 2005.
- [5] Floyd, B., Pfeiffer, U., Reynolds, S., Valdes-Garcia, A., Haymes, C., Katayama, Y., Nakano, D., Beukema, T., Gaudier, B., and Soyuer, M., "Silicon Millimeter-Wave Radio Circuits at 60-100 GHz," *IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, pp. 213-218, Jan. 2007.
- [6] Malla, P., Ladkawala, H., Lornegay, K., and Soumyanath, K. "A 28mW Spectrum-Sensing Reconfigurable 20MHz 72dB-SNR 70dB-SNDR DT $\Delta\Sigma$ ADC for 802.11n/WiMAX Receivers," *International Solid-State Circuits Conference*, pp. 496-497, Feb. 2008.
- [7] Gupta, S., Tang, Y., and Allstot, D. J., "Hybrid Modeling Techniques for Low OSR Cascade Continuous-Time $\Delta\Sigma$ Modulators," *International Symposium on Circuits and Systems*, pp. 2414-2417, 2008.
- [8] Verma, A., Razavi, B., "A 10b 500MHz ADC," *International Solid-State Circuits Conference*, pp. 84-86, Feb. 2009.
- [9] Baker, R. J., "CMOS Mixed-Signal Circuit Design, 2nd edition," *Wiley-IEEE*, 2009.

References

- [10] Yang, H.-K., El-Masry, E. I., “Double-Sampling Delta-Sigma Modulators,” *IEEE Trans. on Circuits and Systems - II: Analog and Digital Signal Processing*, vol. 43, no. 7, pp. 524-529, July 1996.
- [11] King, E. T., Eshraghi, A., Galton, I., and Fiez, T. S., “A Nyquist-Rate Delta-Sigma A/D Converter,” *IEEE Journal of Solid-State Circuits*, vol. 33, no. 1, pp. 45-52, Jan. 1998.
- [12] Eshraghi, A., and Fiez, T. S., “A Time-Interleaved Parallel $\Delta\Sigma$ A/D Converter,” *IEEE TCAS-II: Analog and Digital Signal Processing*, vol. 50, no. 3, Mar. 2003.
- [13] Eshraghi, A., and Fiez, T. S., “A Comparative Analysis of Parallel Delta-Sigma ADC Architectures,” *IEEE TCAS-I: Regular Papers*, vol. 51, no. 3, Mar 2004.
- [14] Schreier, R., Temes, G. C., “Understanding Delta-Sigma Data Converters,” *IEEE Press*, 2009.
- [15] Maloberti, F., “Data Converters,” *Springer*, 2007.
- [16] Cherry, J. A., “Continuous-Time Delta-Sigma Modulators for High-Speed A/D Conversion: Theory, Practice and Fundamental Performance Limits,” *Kluwers*, 2002.



Questions ?