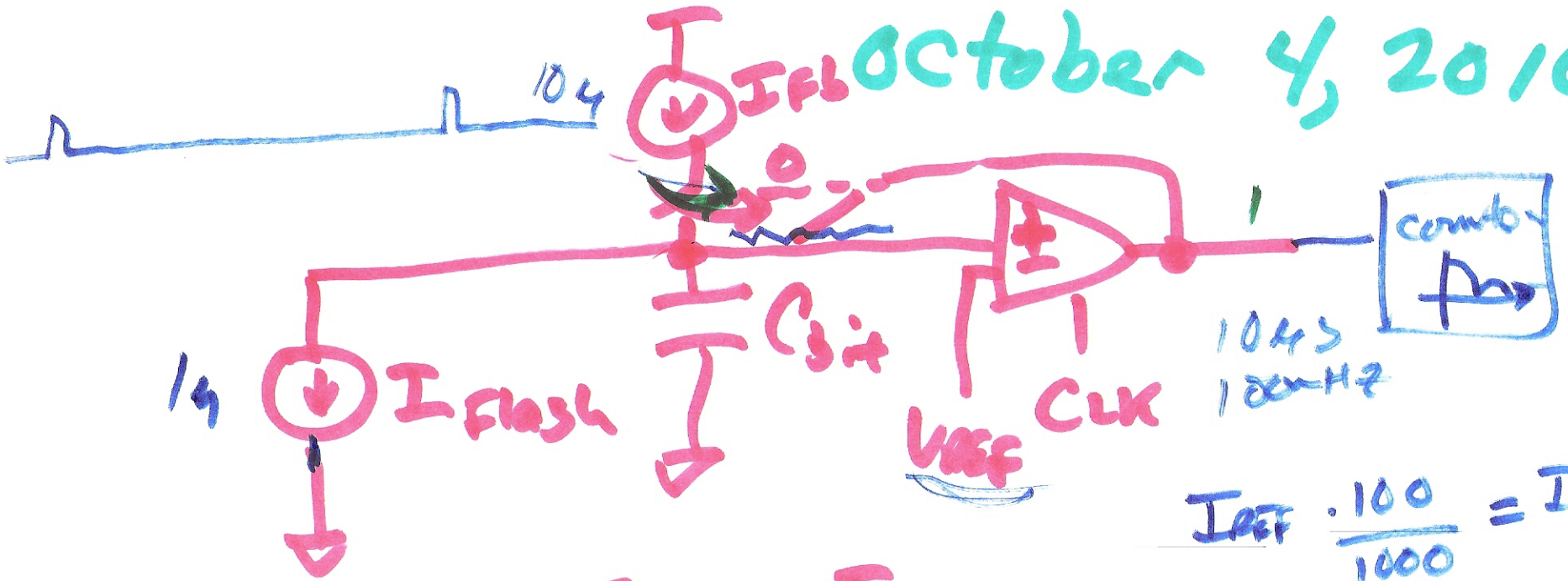
ECE 615 CMOS Mixed-Signal Circuit Design

BOISE STATE UNIVERSITY

Lecture 12

October 4, 2010



$I_{REF} \cdot \frac{100}{1000} = I_{Flash}$

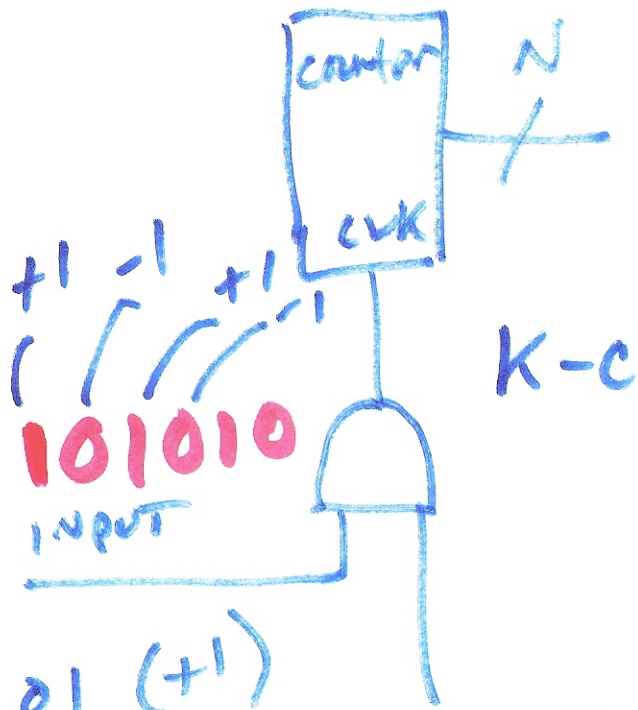
$I_{FB} > I_{Flash}$

$= 1\mu A$

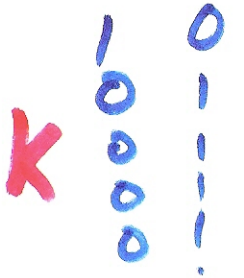
$\frac{I_{REF}}{1000}$

1)

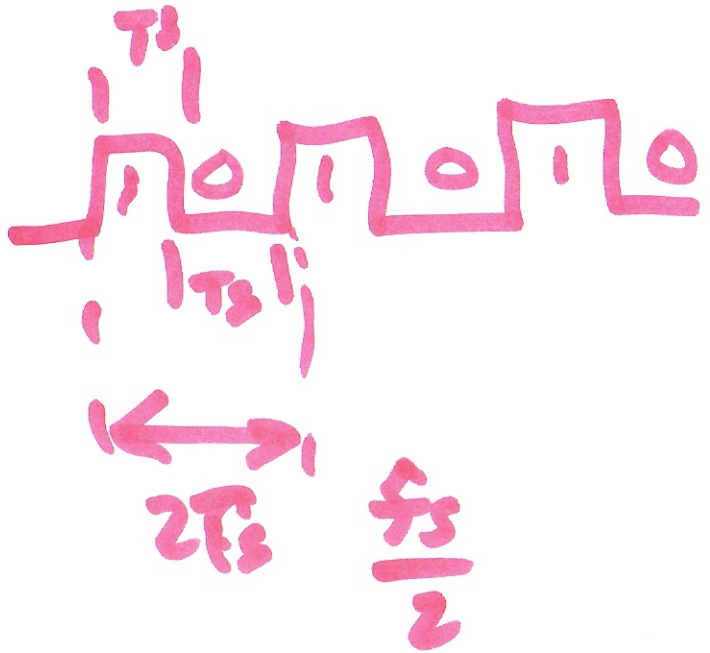
counter

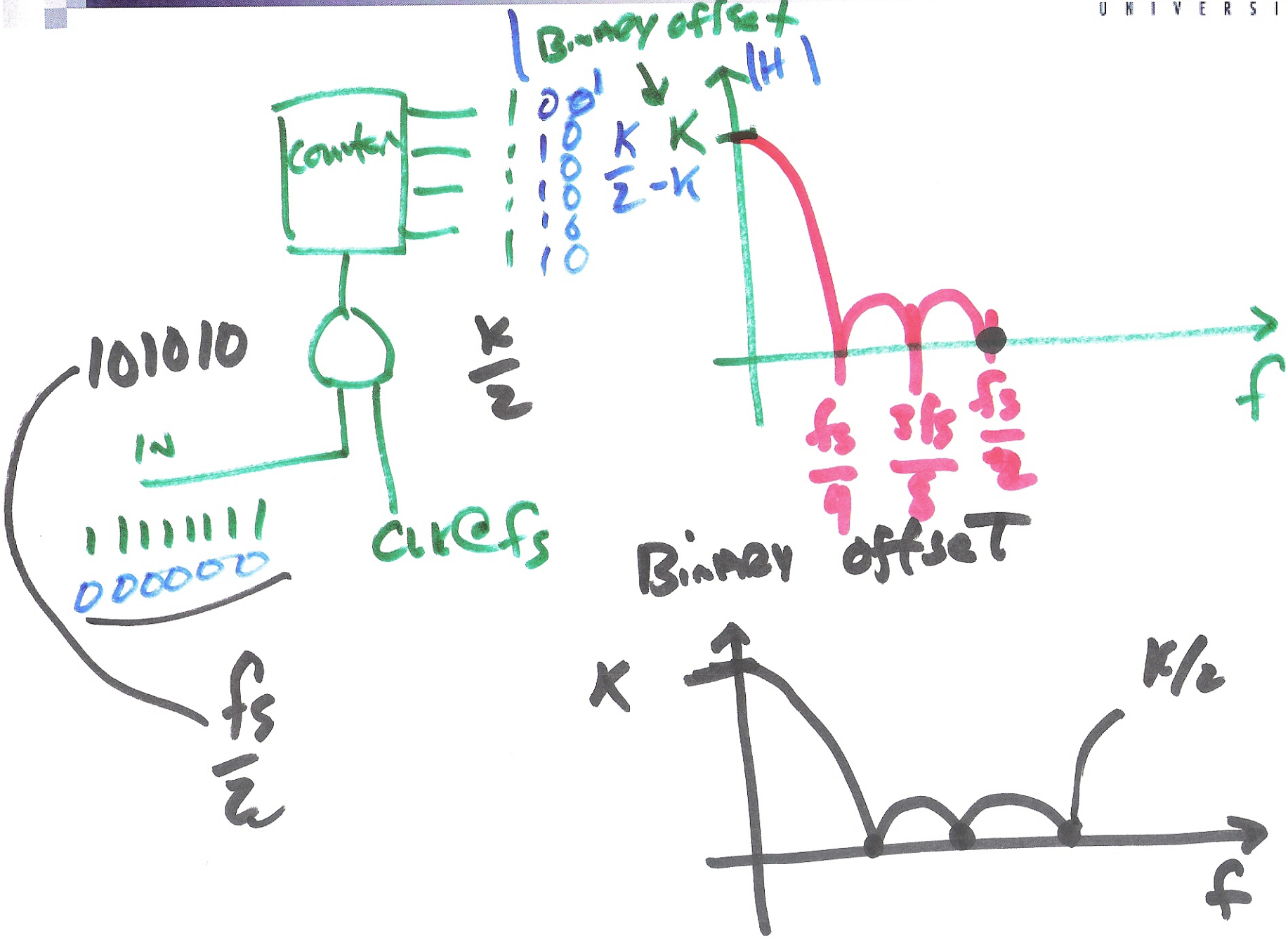


K



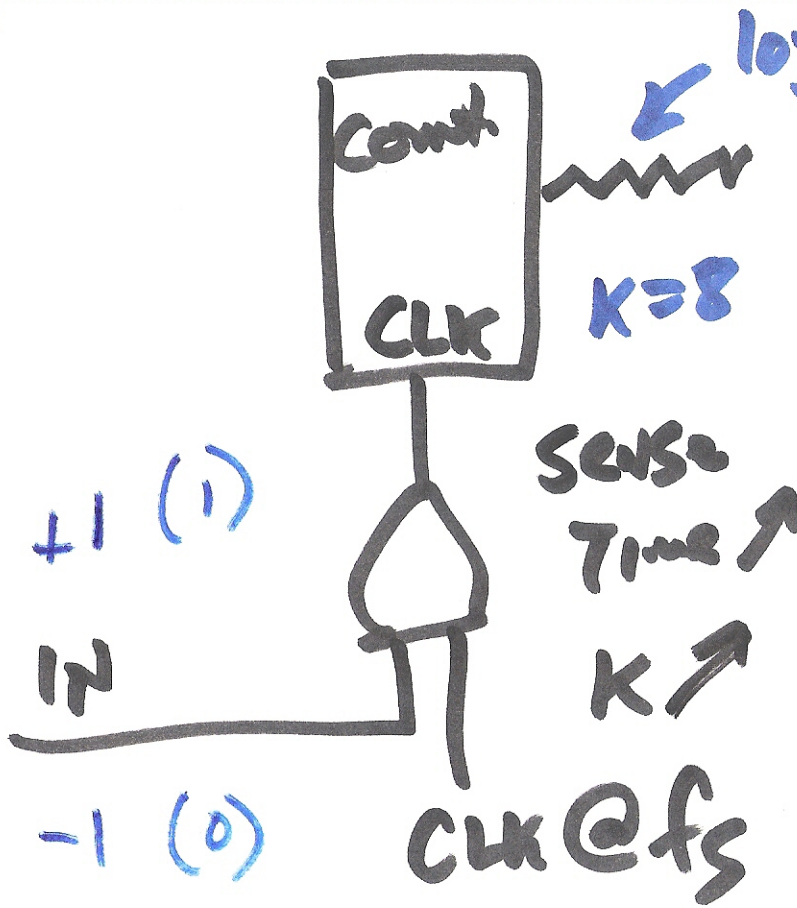
K-clock cycles

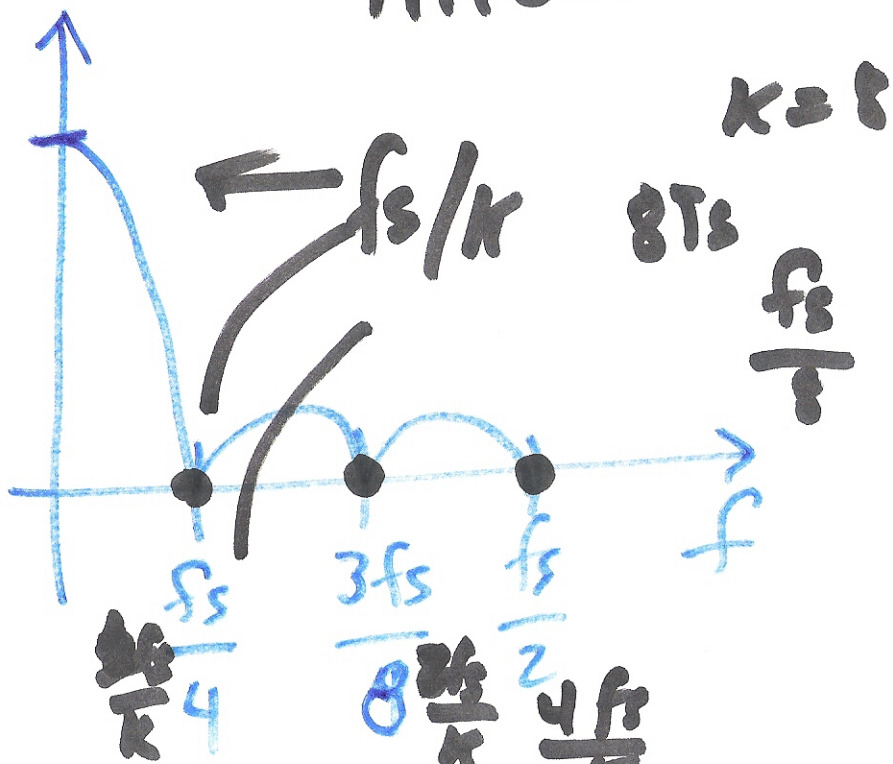



Binary offset
counter
001
010
011
100
101
110
K
2^K
101010
IN
11111111
00000000
clk@fs
K/2
fs/2
|H|
f
fs/9
3fs/9
fs/2
Binary offset
K
K/2
f

3)

Two's complement





11110000

10101010

11001100

1 1 0 0 1 1

+1 +1 -1 -1

+1 -1 +1 -1 +1

$f_s = 100\ MHz$

$\frac{300\ MHz}{8} = 36.5$

3) 4

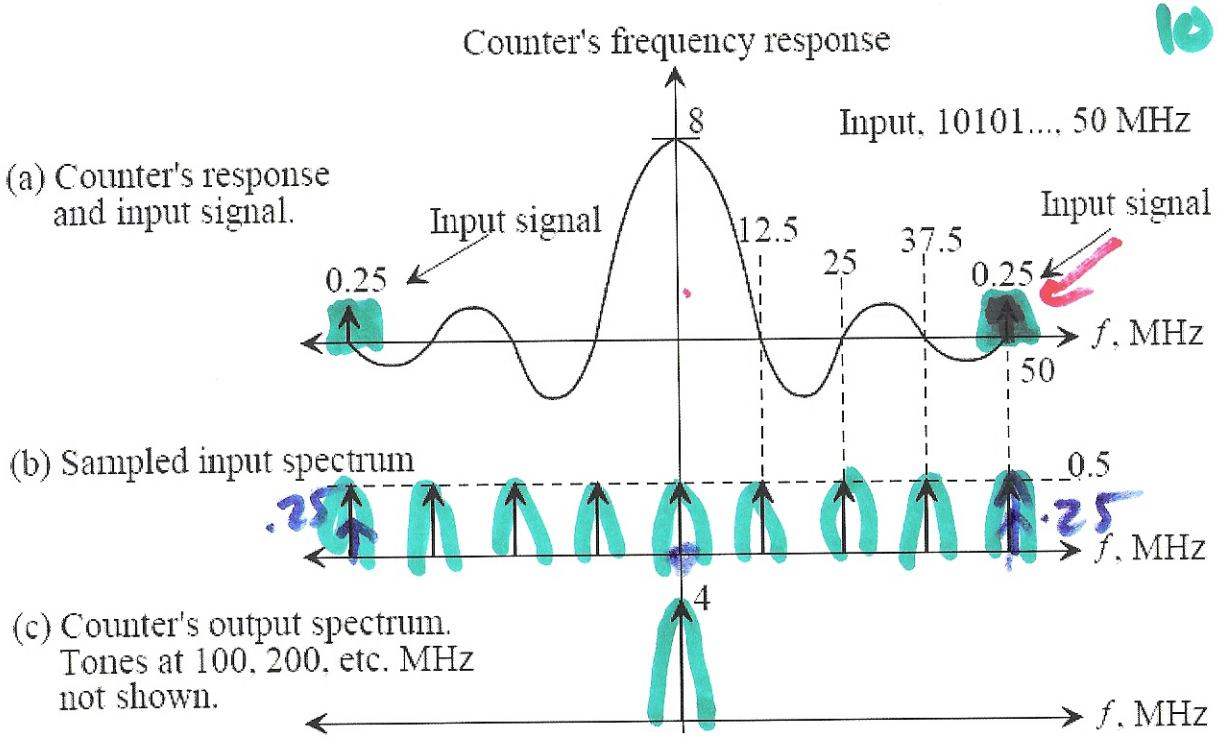


Figure 4.11 Showing how decimating using a counter results in aliasing.

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$$y[k_i \cdot T_s] = \sum_{N=k(i-1)}^{k_i - 1} x[N \cdot T_s]$$

counter output

counter inputs

3

1 1 0 0 0 0 1

$$x(0) + x(1) + x(2) + \ldots x(7)$$

$$y(z) = x(z) \sum_{N=0}^{k-1} z^{-N} = 1 + z^{-1} + z^{-2} + \ldots + z^{-7}$$

$i = 1$

6)

$$H(z) = \frac{Y(z)}{X(z)} = \frac{(1-z^{-1})}{(1+z^{-1}+z^{-2}+\cdots z^{-k})}$$

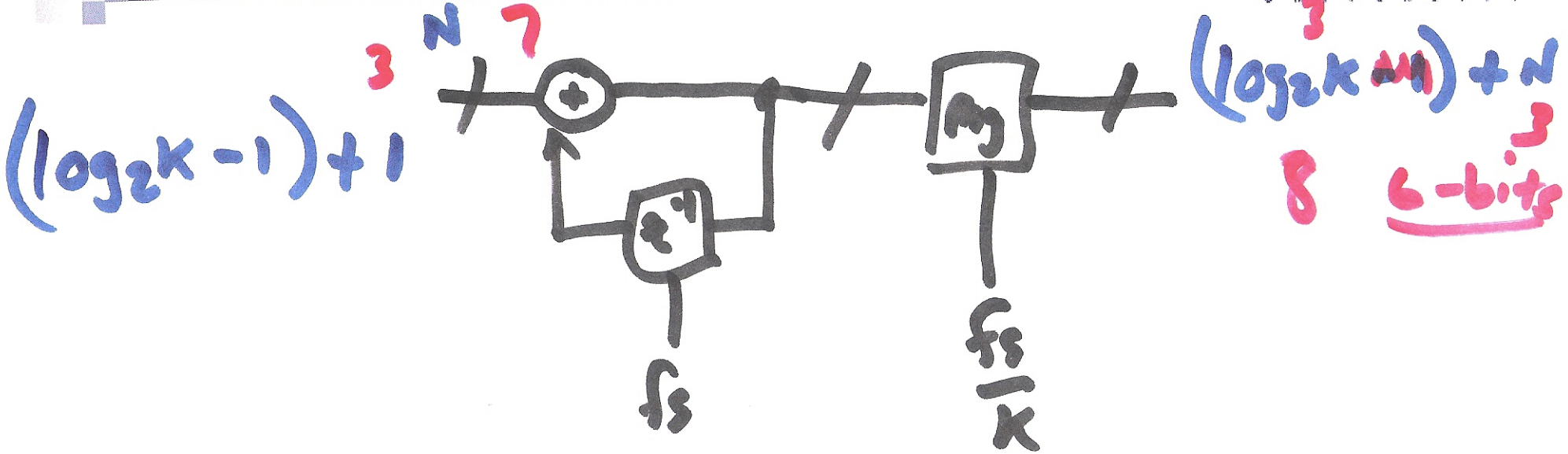
$$H(z) = \frac{1-z^{-k}}{1-z^{-1}} \qquad 1-z^{-1}$$

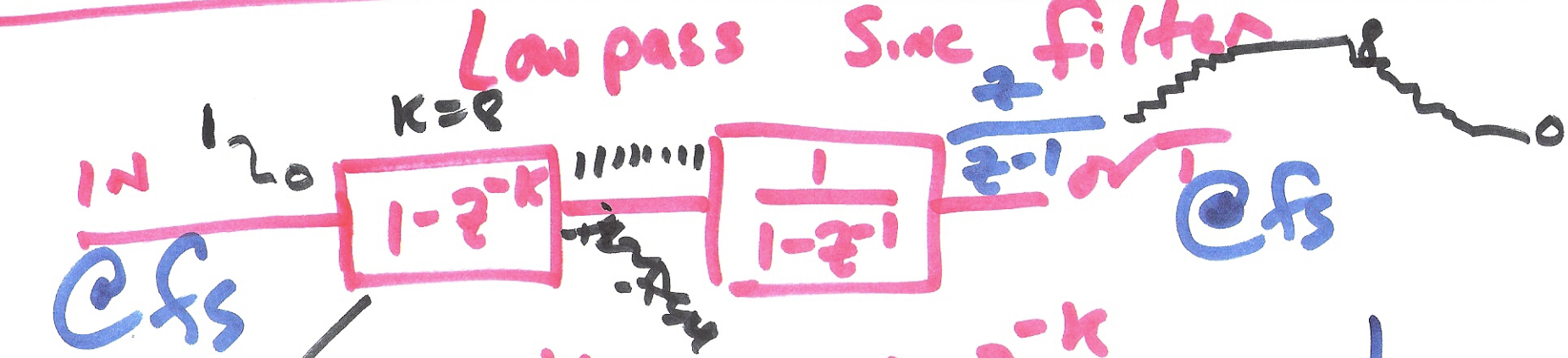
$$|H(f)| = k \cdot \left| \frac{\mathrm{Sinc}\ \pi \frac{k \cdot f}{f_s}}{\mathrm{Sinc}\ \pi f/f_s} \right|$$

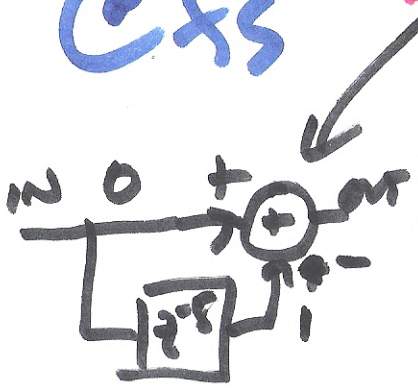
k is big $f \ll f_s$

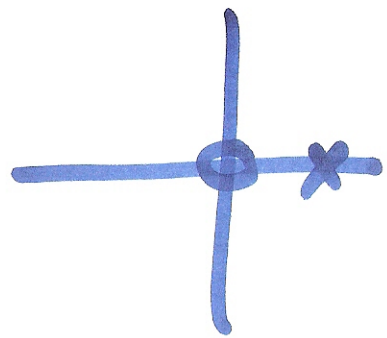
$$|H(f)| \simeq k \cdot \left| \mathrm{Sinc}\left(\pi \cdot \frac{k \cdot f}{f_s}\right) \right|$$

Accumulate & dump

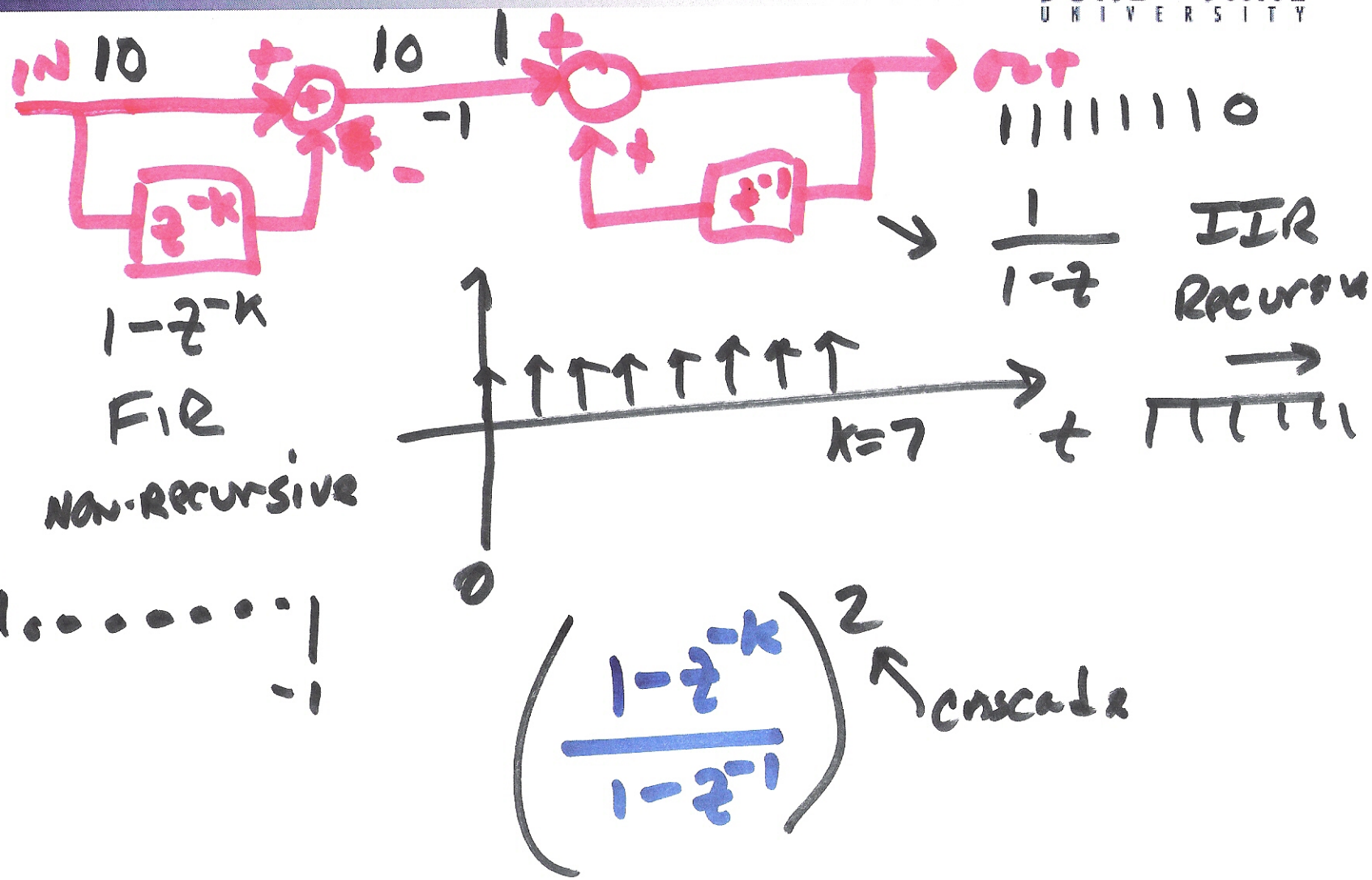


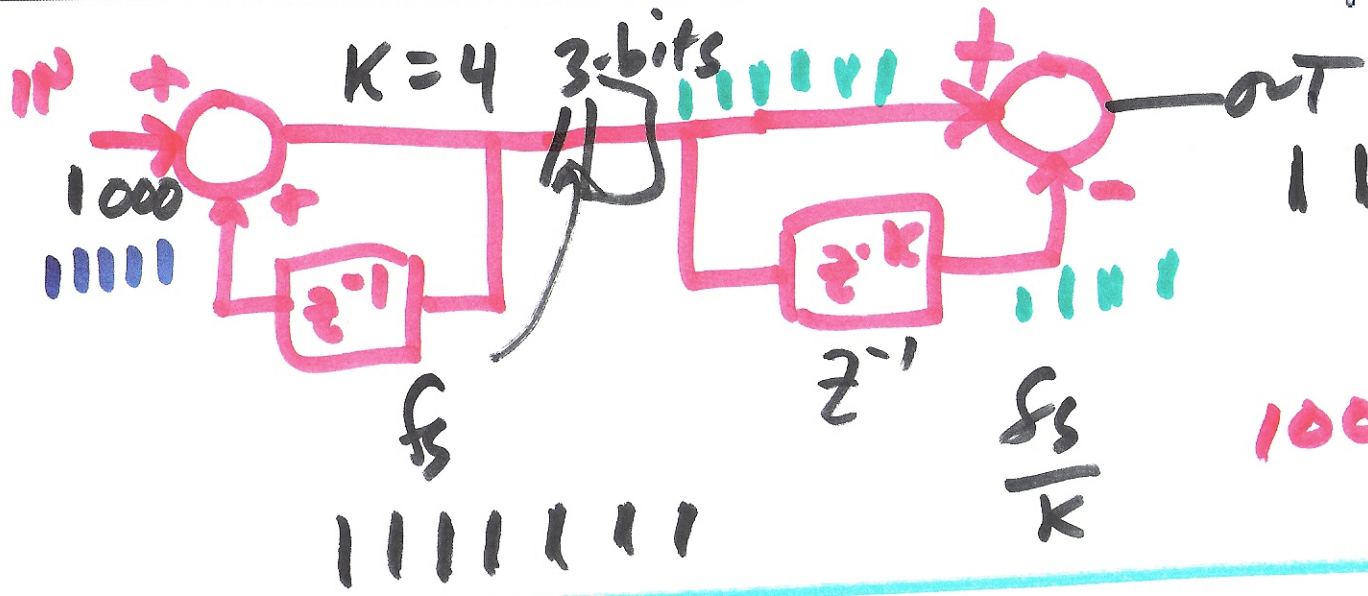






9)


IN
10
10
1
-1
z^{-K}
z^{-1}
$1-z^{-K}$
FIR
NON-RECURSIVE
$\frac{1}{1-z^{-1}}$
IIR
RECURSIVE
11111110
K=7
t
+1
-1
0
$\left(\frac{1-z^{-K}}{1-z^{-1}}\right)^2$
cascade



3 → 011
7 → 111

1, 2, 3, 4, 5, 6, 7, 0, 1, 2, 3, 4 . . .
1 2 3 4 5 6 7 0

```
  111
  011
-----
  111
  100
    1
-----
  100
```

1, 2, 3, 4, 4, 4, 4

```
  100
  000
-----
  100
  111
    1
-----
  100
```

10)