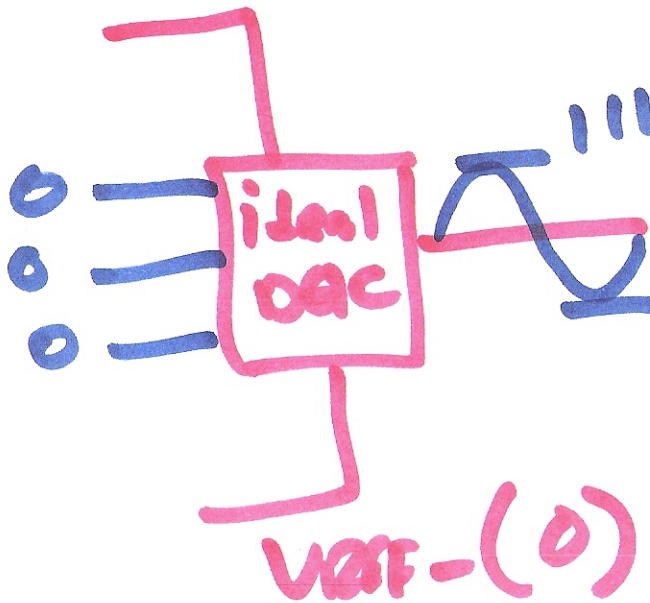
ECE 615 CMOS Mixed-signal

BOISE STATE UNIVERSITY

Sept. 29, 2010

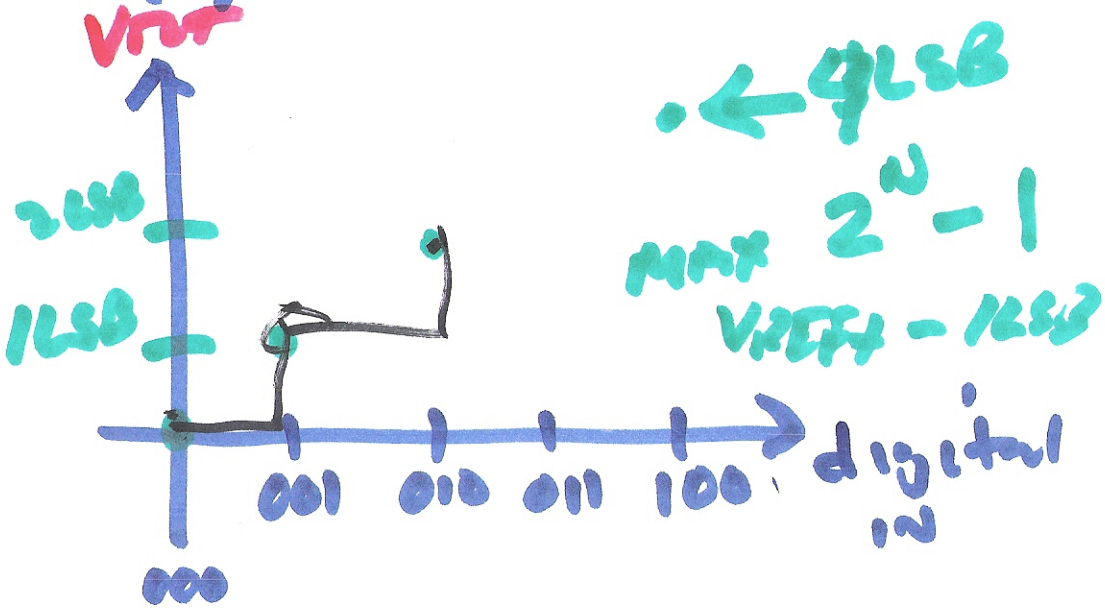
Lecture 11 Ideal ADC & DAC

V_{REF+} (V_{DD})

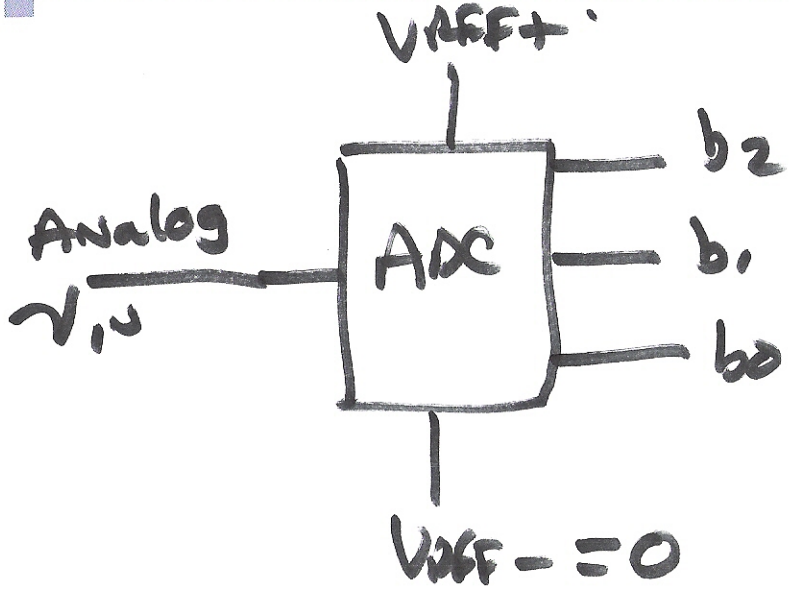


$1\,LSB = \frac{V_{REF+} - V_{REF-}}{2^N}$

$SNR = 20 \log \frac{V_S}{V_N}$



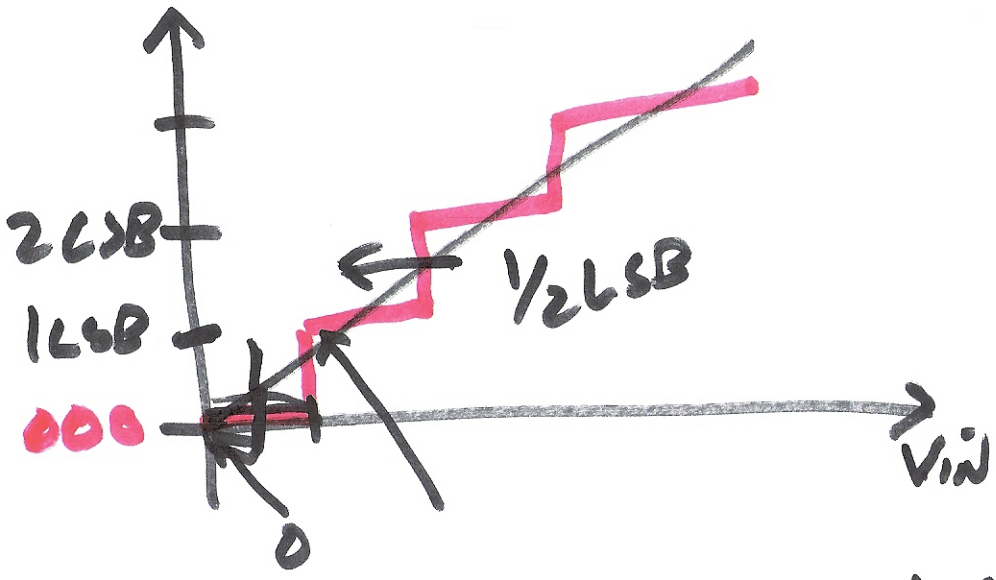
Ideal ADC



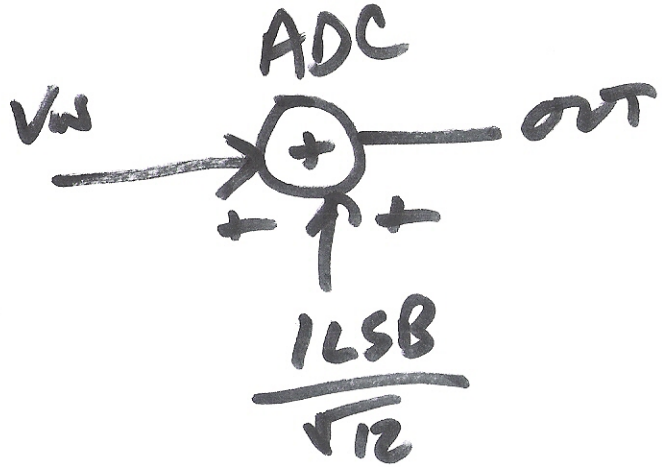
VREF-

$0 < V_{in} < 1\,LSB$ 000

$VREF- + 1\,LSB < V_{in} < 2\,LSBs$ 001



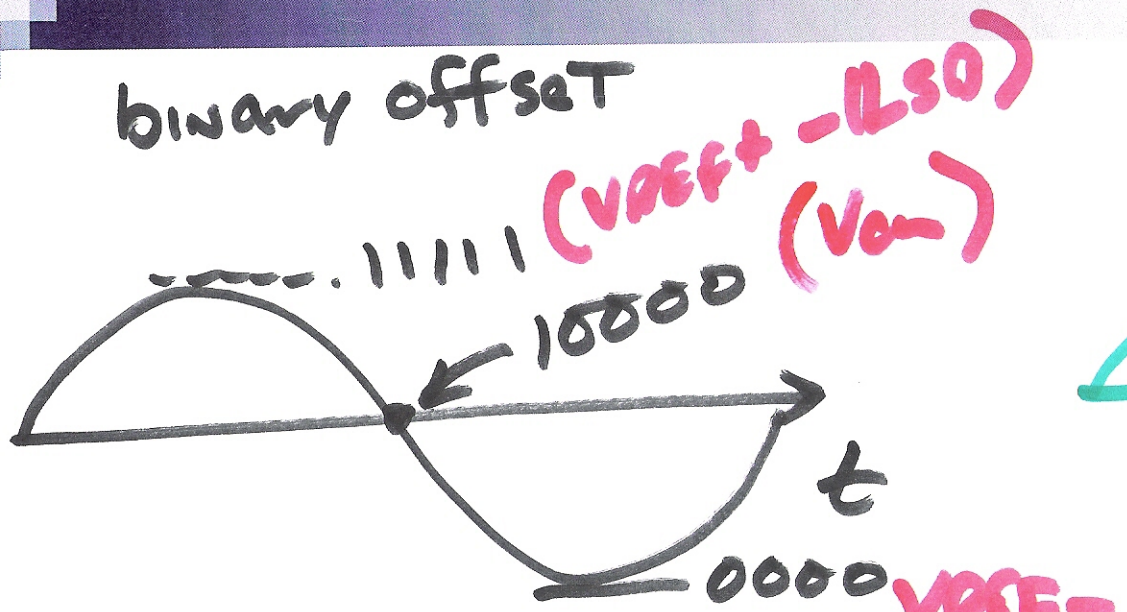
$$4\text{-}V \simeq \frac{1V}{28} = \frac{1}{256}$$



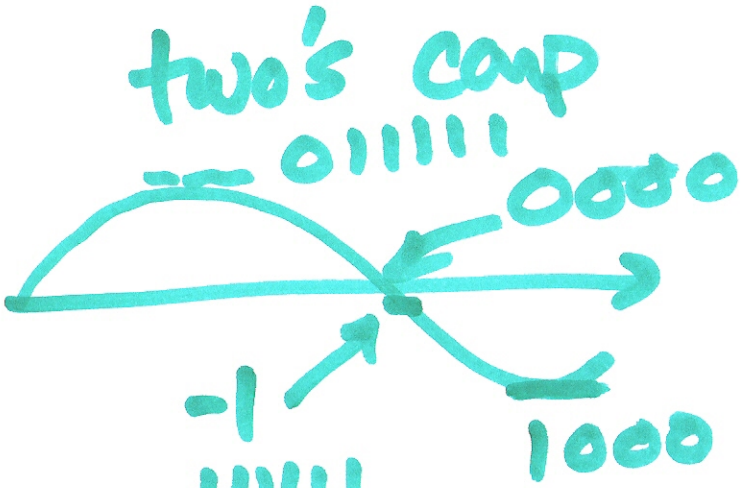
$$\frac{1LSB}{2\sqrt{3}} = \frac{1LSB}{\sqrt{12}}$$

2)

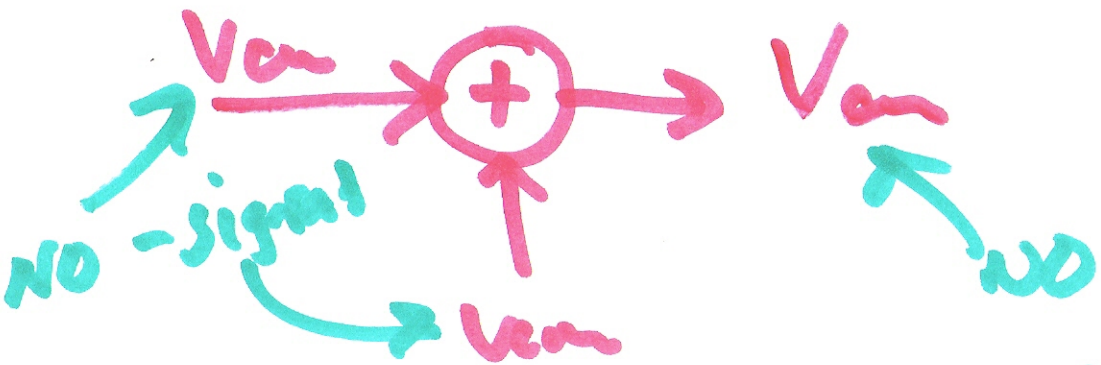
binary offset



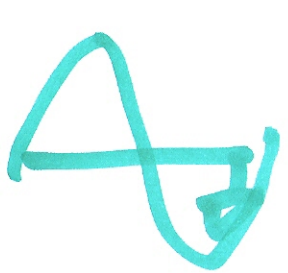
two's comp



Complement the MSB



$$V_{cm} = \frac{VDD}{2}$$



$VSS = -VDD$

3)

full Adder

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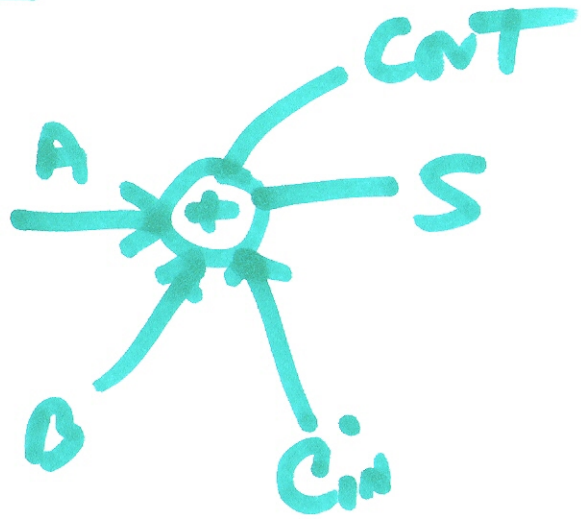
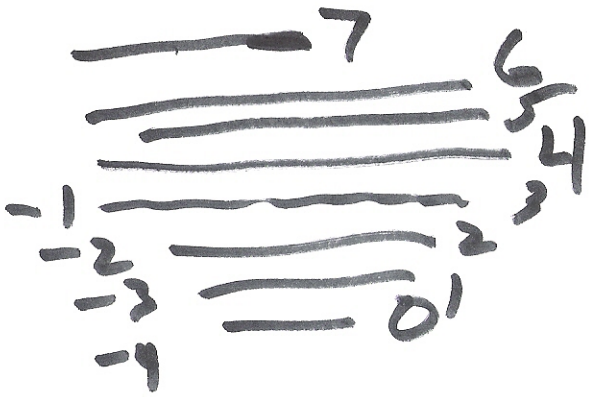
A	B	Cin	S	CnT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



3 4

011 100



111(-1) 000(0)

111
000
111 → -1

4)

110 (6)
101 (5)

6+5=7

010 (+2)
001 (+1)
---
011 (+3)

111 (7)

extend sign bit

extend sign bit

0010 (+2)
0001 (+1)

0011 (+3)

6+5=11 1011 (+11)

5)

011 (+3) → 1111

010 (+2) → 1110

B.O.) change to two's comp.

extend sign-bit

$$
\begin{array}{r}
11 \\
1111 \\
1110 \\
\hline
1101
\end{array}
$$

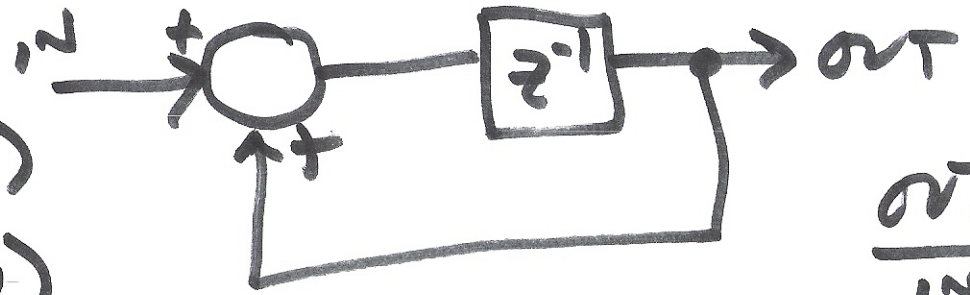
OF!

1101 — two's compl.

0101 (+5)

2+3 = 5

6)

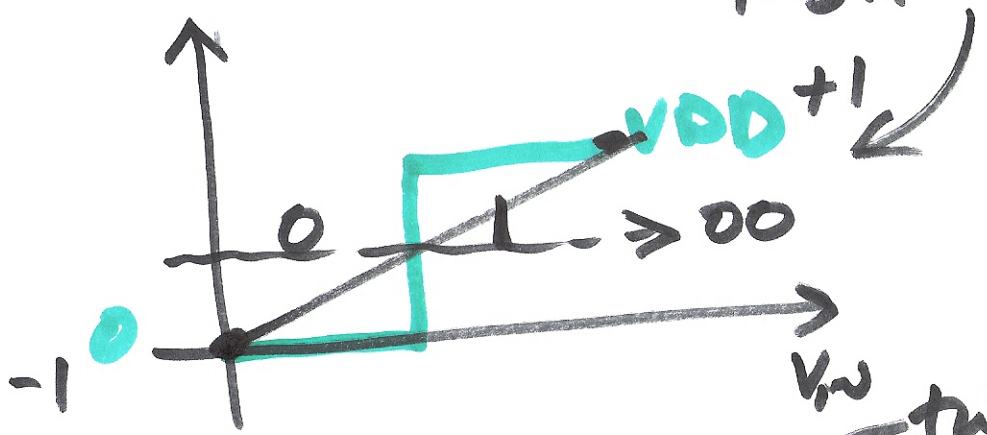


1 → 01 (+1)

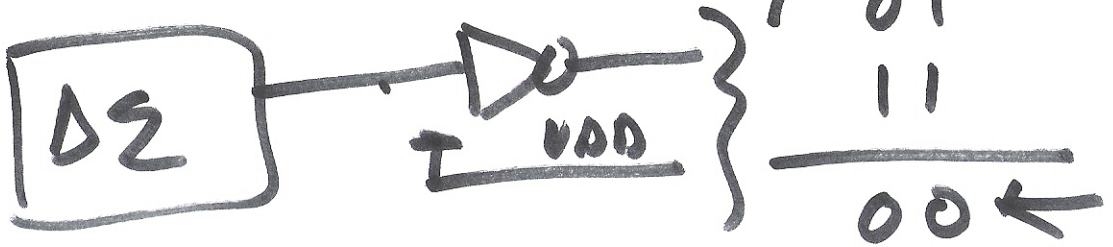
0 → 11 (−1)

$$\frac{OUT}{IN} = \frac{z^{-1}}{1-z^{-1}}$$

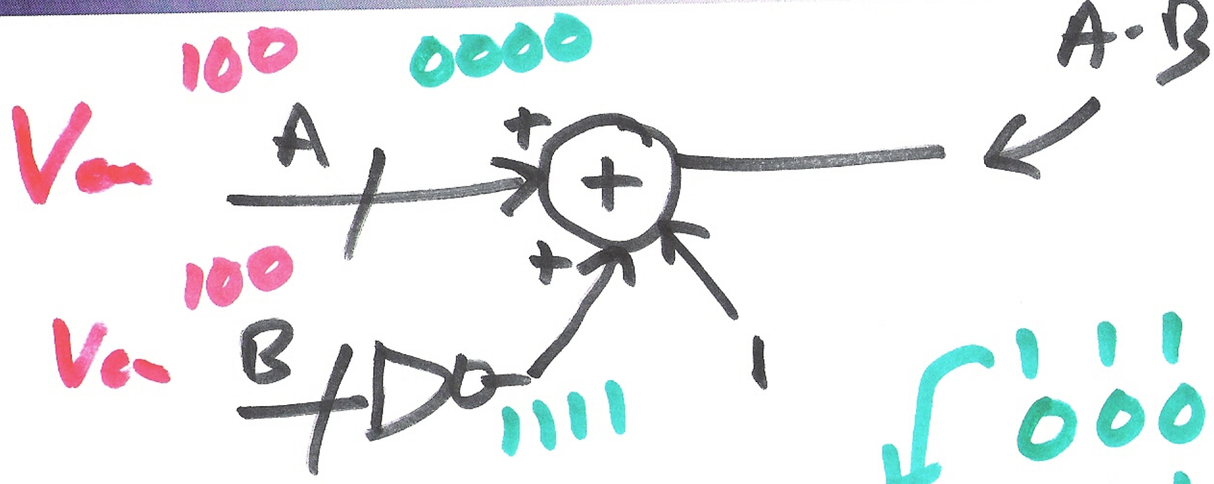
1-bit ADC



two's complement output!



SUBtraction



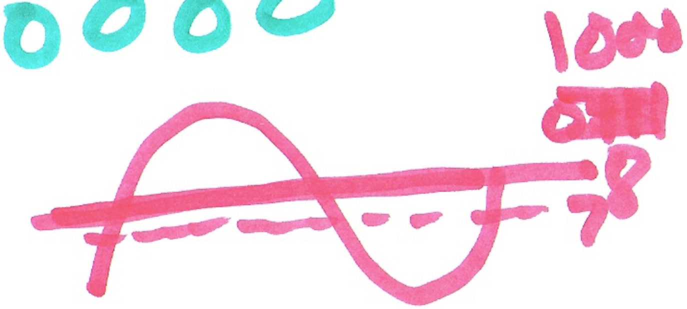
0000

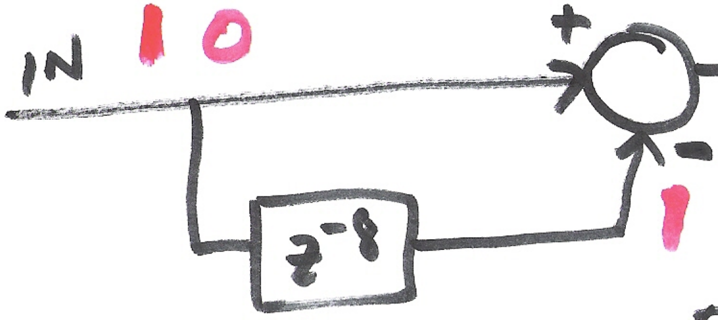
```
   2   010
 - 3   011
```

```
 1110   →    1110
 11111       0000
                1
            -----
            11111 (-1)
```

```
  111
  0000
  1111
     1
  ----
  0000
```

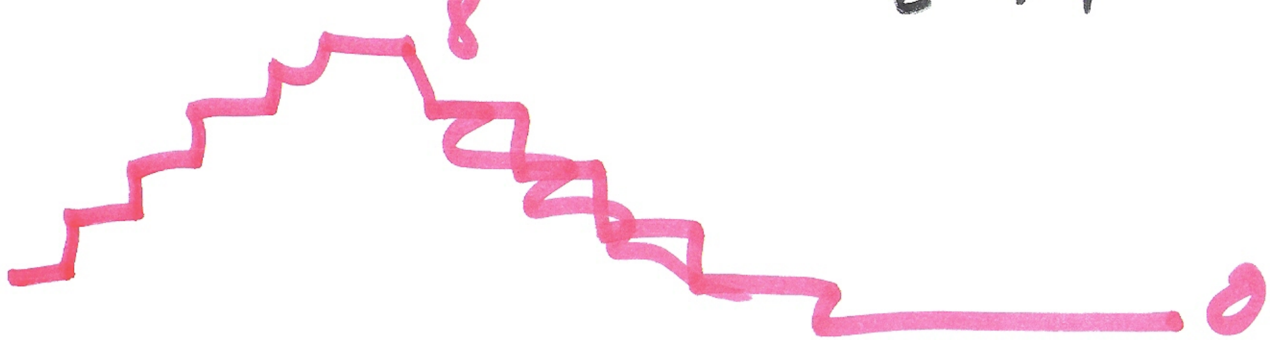
OK!





$OUT = IN(1 - z^{-8})$

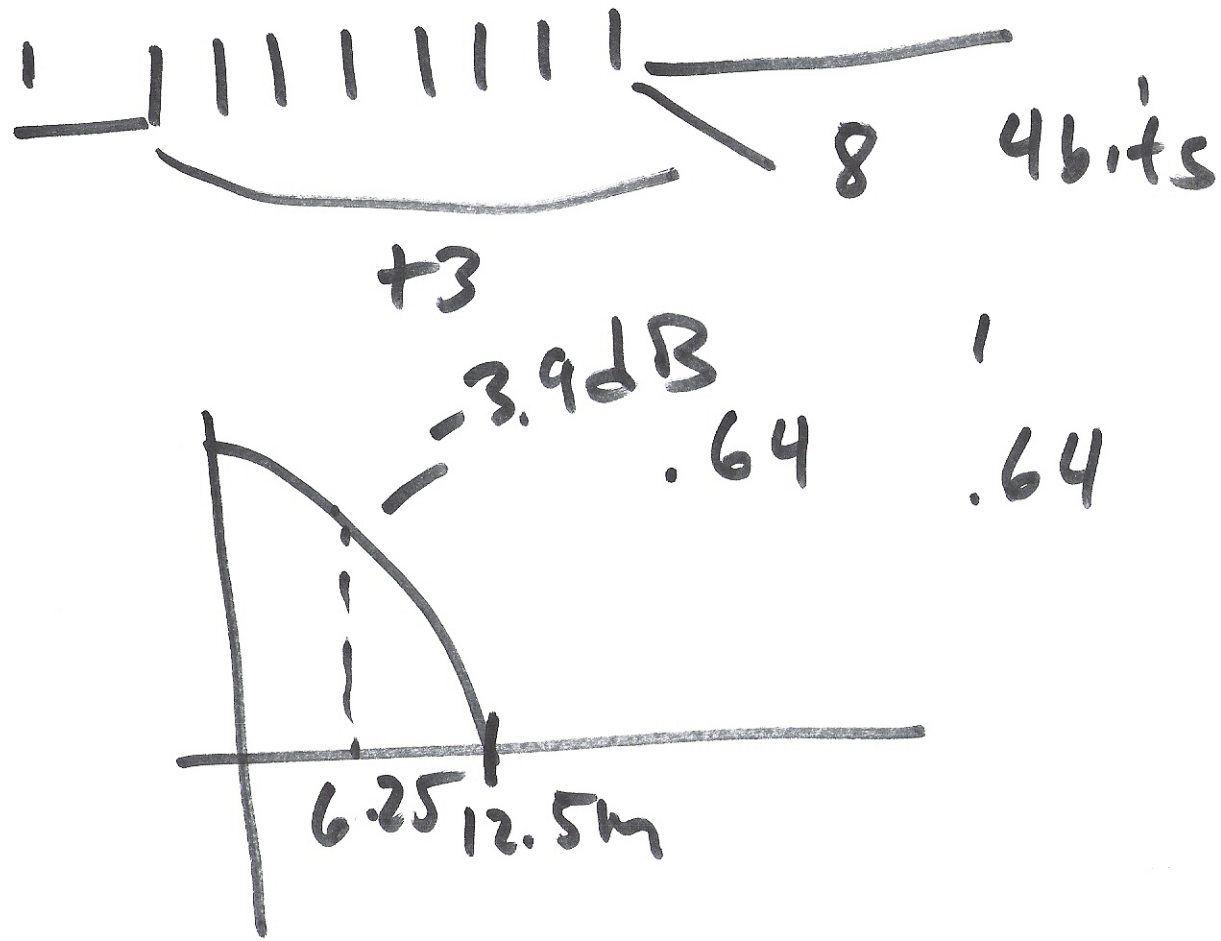
$\frac{OUT}{IN} = 1 - z^{-8}$



0 8

1 →

1 3 4


8
46.4s
+3
-3.9dB
.64
.64
6.25
12.5m