BOISE STATE UNIVERSITY

Design and Operation of Integrating ADCs

ECE614 - Advanced Analog IC Design

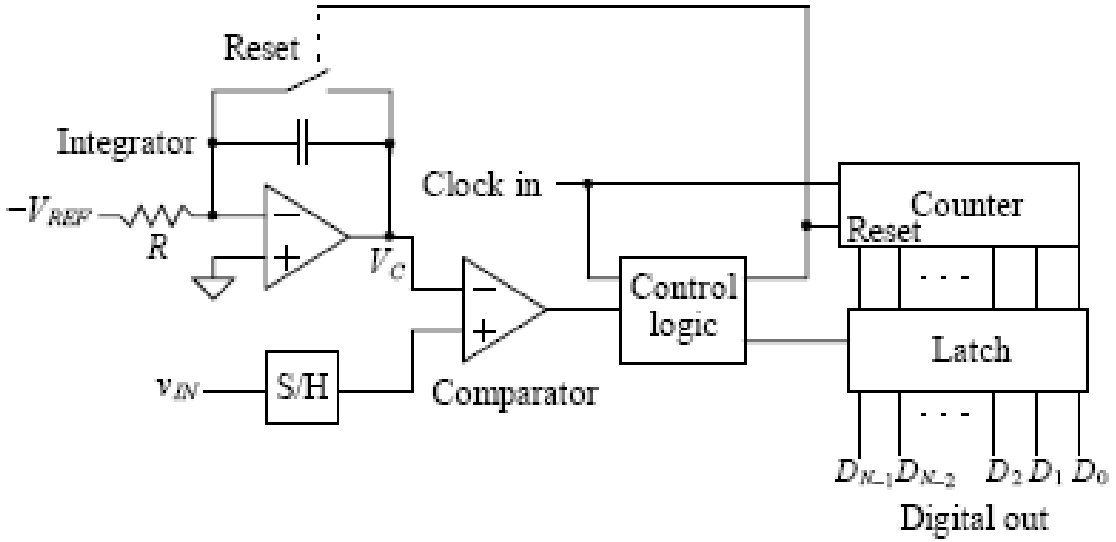
Presented by Antonio Oblea

May 7, 2008

Integrating ADC Overview

- AKA ramp and slope ADC
  - Different flavors, e.g. single-slope and dual-slope
- Strengths[1],[2]
  - High resolution
  - High linearity
  - Relatively simple circuitry
  - Low-cost
- Weaknesses
  - Slow!
- Applications
  - Sensors, voltmeters, ammeters

Single-slope ADC Operation



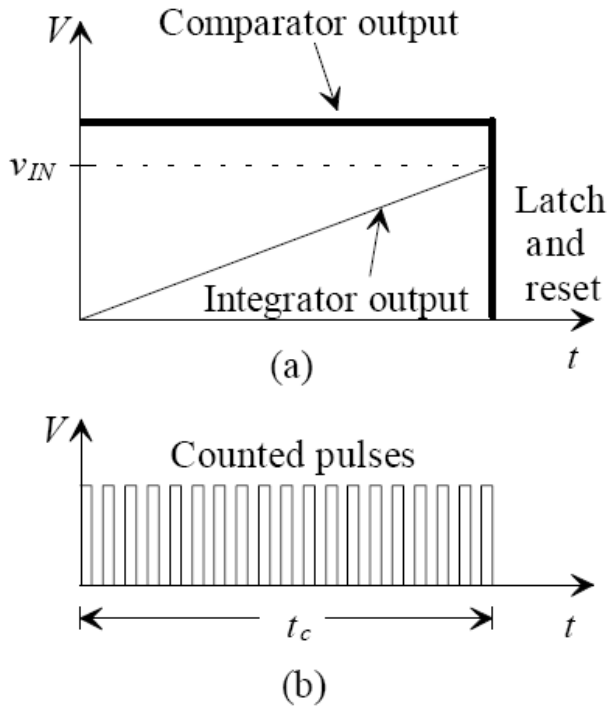
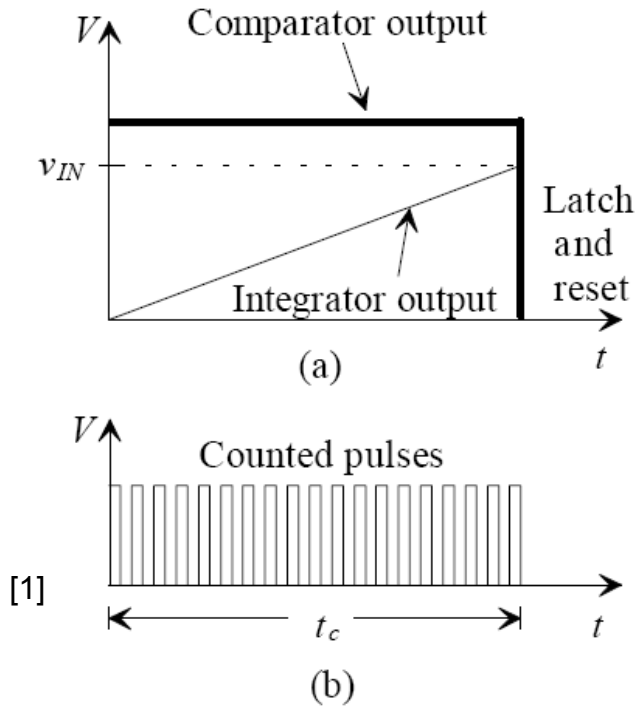


Figure 29.32 Block diagram of a single-slope ADC.

[1]

$$\frac{0-(-Vref)}{R}=C\frac{dVc}{dt}\rightarrow Vc=\frac{1}{RC}\int_0^t Vref\cdot dt=\frac{Vref\cdot t}{RC}$$

Single-slope ADC Analysis



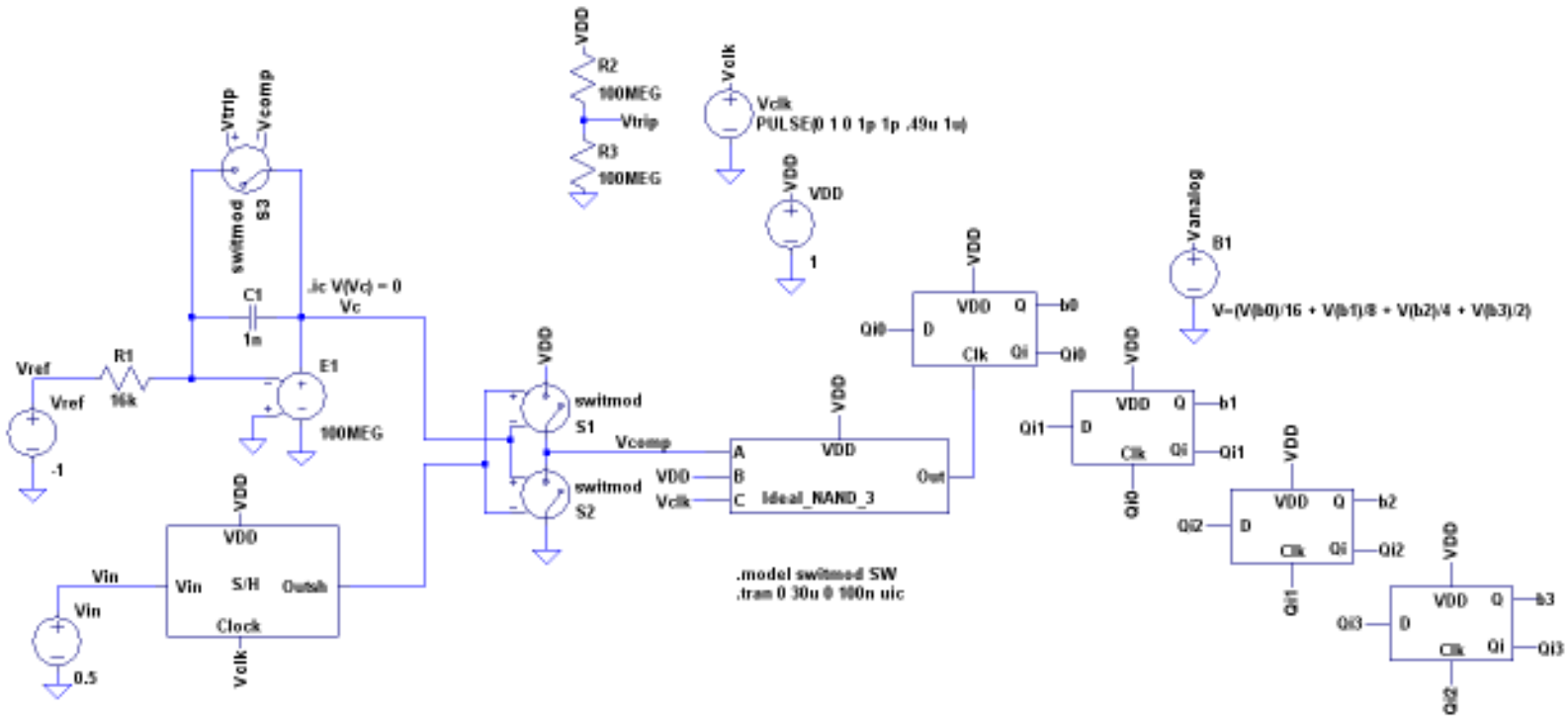
[1]

$$t_c = \frac{v_{IN}}{LSB} \cdot T_{CLK} = \frac{v_{IN}}{V_{REF}} 2^N \cdot T_{CLK}$$

(see why it's slow?)

$$Vc = \frac{V_{REF} \cdot t}{RC} = \frac{v_{IN}}{RC \cdot f_{CLK}} 2^N$$

Single-slope ADC Implementation



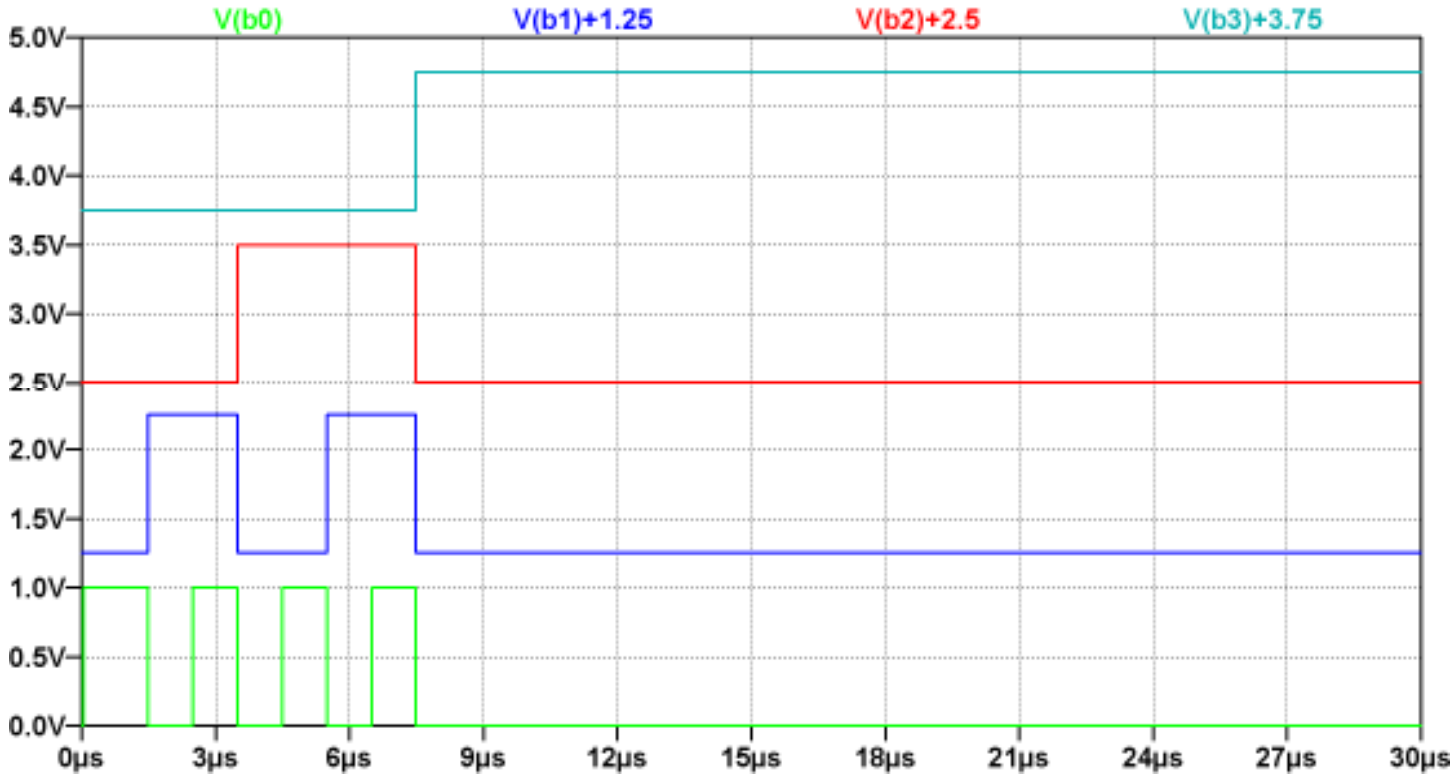
$$Vc = \frac{V_{REF} \cdot t}{RC} = \frac{v_{IN}}{RC \cdot f_{CLK}} 2^N$$

With $v_{IN} = V_c$

$N = 4$ $\quad RC = 16/10^6 = 16us$

$f_{CLK} = 1MHz$

Single-slope ADC Simulations

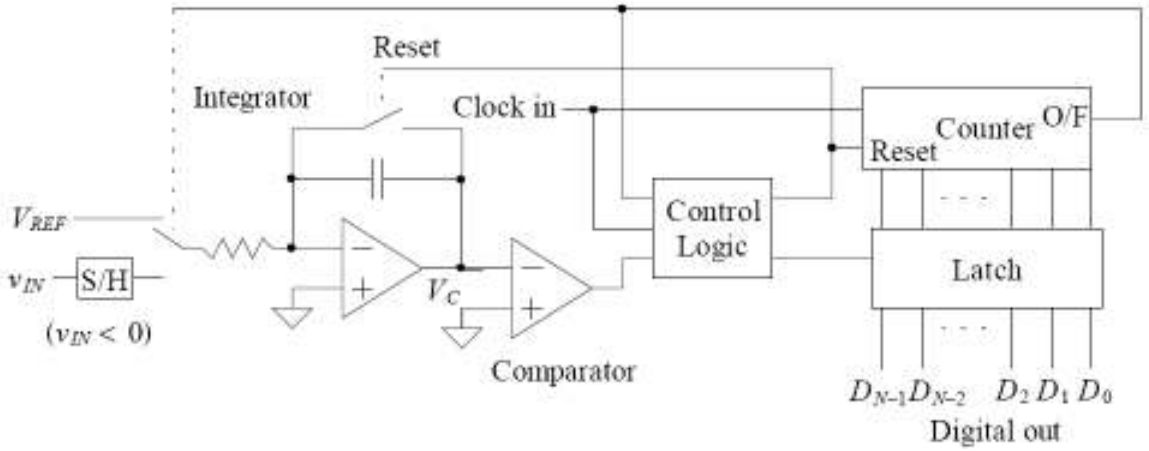


$$t_c = \frac{v_{IN}}{V_{REF}} 2^N \cdot T_{CLK} = \frac{0.5}{1} \cdot 16 \cdot T_{CLK} = 8T_{CLK}$$ ✓

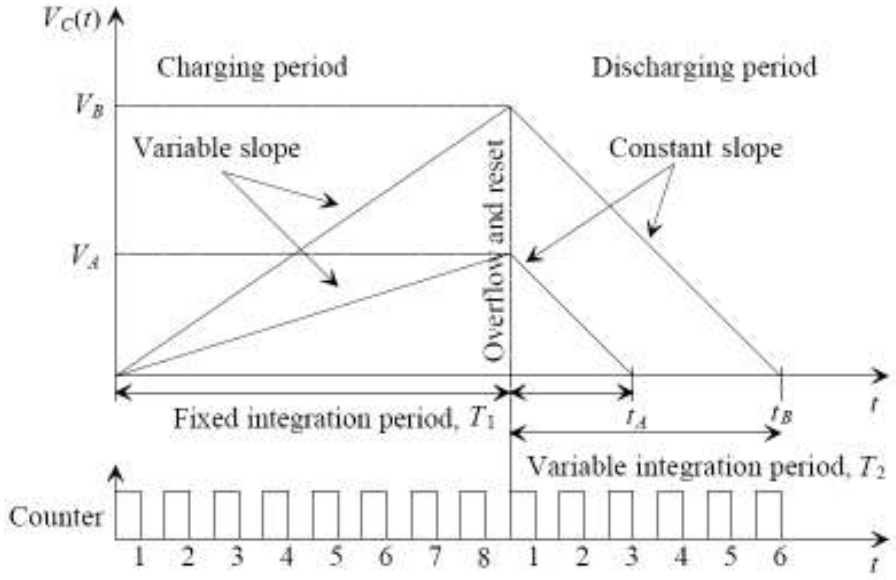
Single-slope ADC Errors

- Errors from measurement of Vc
  - Depends on CLK – jitter
  - Depends on RC – voltage coefficient, parasitic capacitances, poor processing
- Other errors
  - Offset voltage comparator, op-amp, etc.
  - Delays from non-ideal devices

Dual-slope ADC Operation

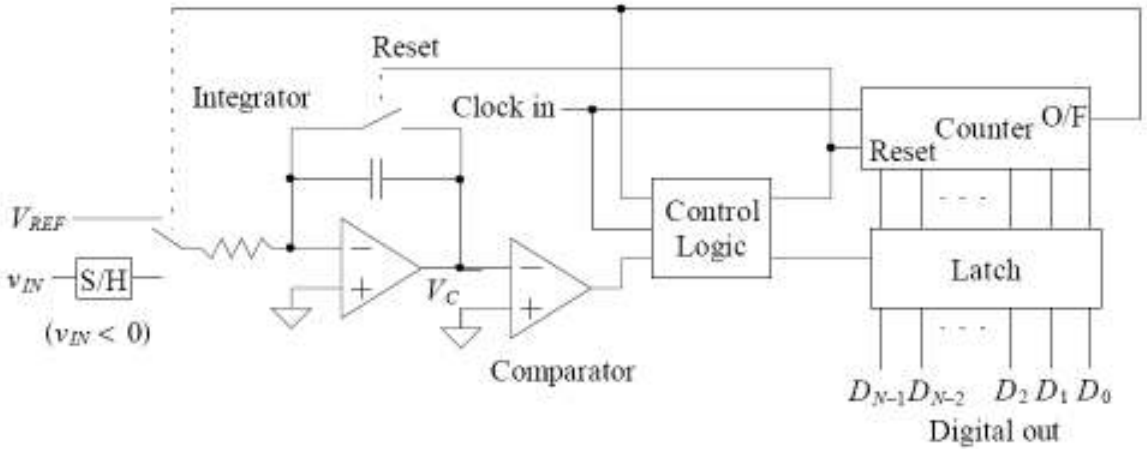


[1]



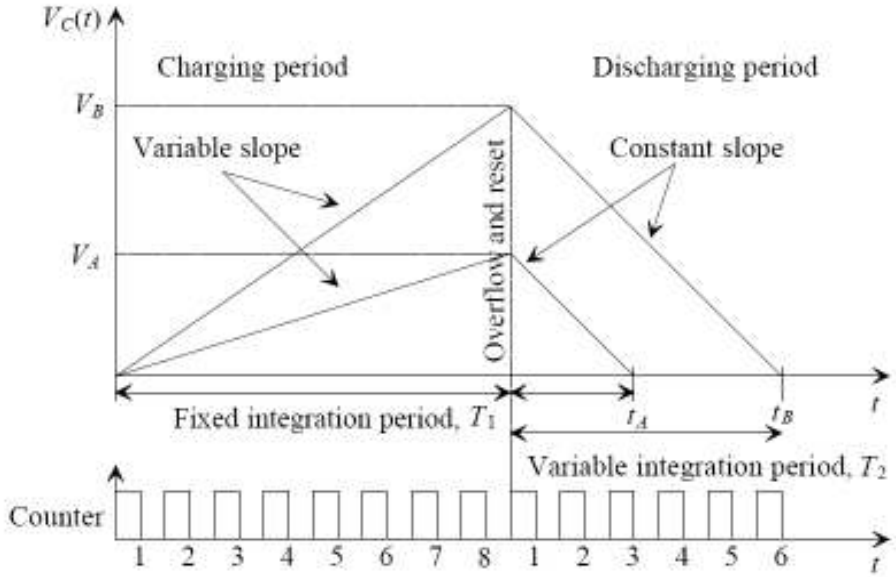
$$T_1 = 2^N \cdot T_{CLK}$$

Dual-slope ADC Operation

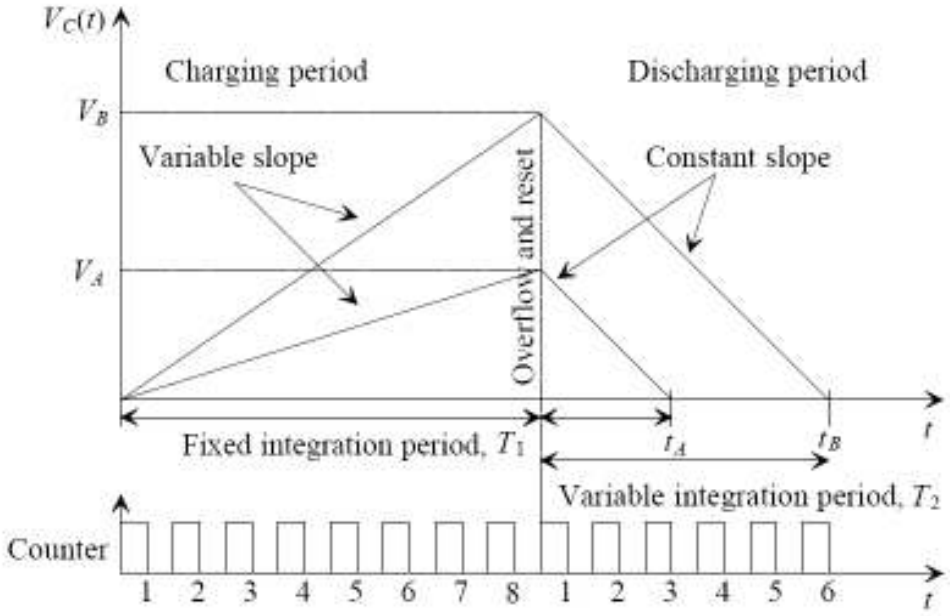


$$V_{C1} = \frac{-1}{C}\int_0^{T1}\frac{v_{IN}}{R}\,dt = \frac{v_{IN}\cdot T_1}{RC}$$

$$V_{C2} = \frac{1}{C}\int_0^{T2}\frac{V_{REF}}{R}\,dt = \frac{V_{REF}\cdot T_2}{RC}$$



Dual-slope ADC Analysis



$$V_{C1} = \frac{-1}{C}\int_0^{T1} \frac{v_{IN}}{R}\,dt = \frac{v_{IN}\cdot T_1}{RC}$$

$$V_{C2} = \frac{1}{C}\int_0^{T2} \frac{V_{REF}}{R}\,dt = \frac{V_{REF}\cdot T_2}{RC}$$

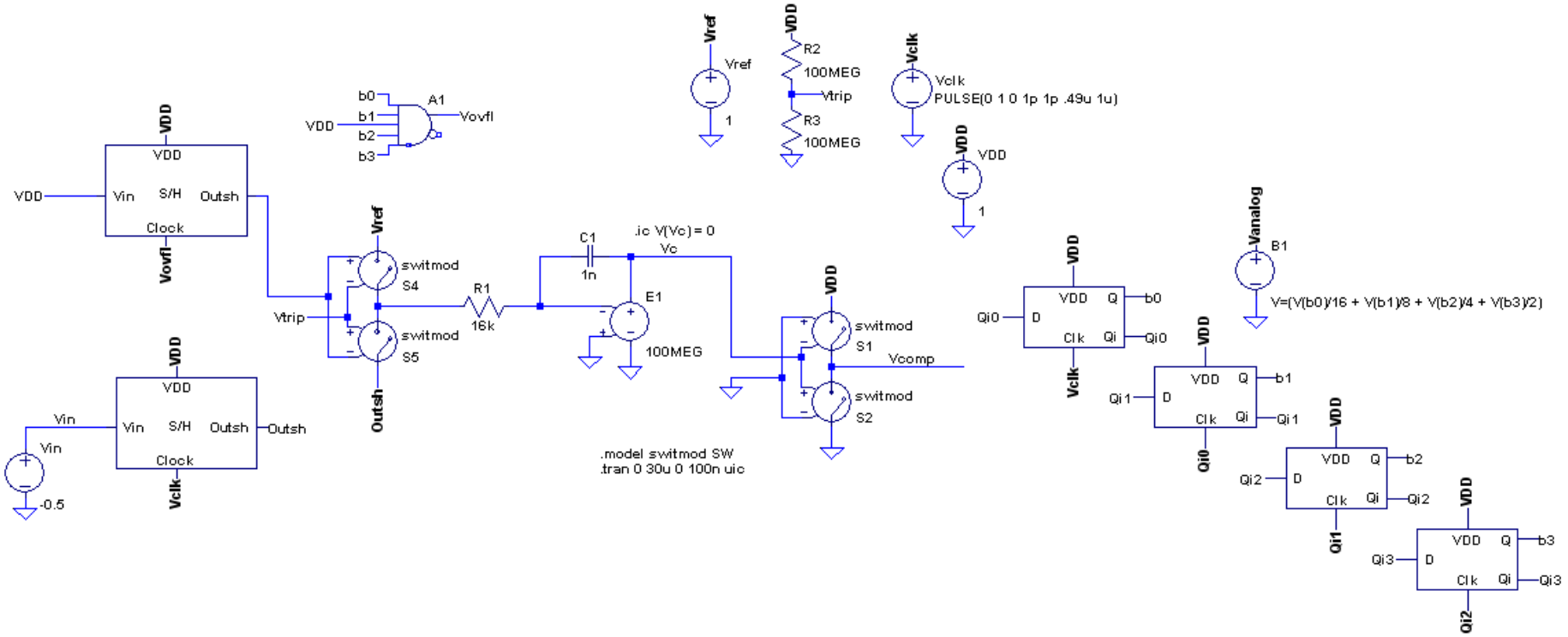
$V_C = V_{C1}\text{-}V_{C2} = (v_{IN}T_1 - V_{REF}T_2)/RC$

If $V_C = 0 \rightarrow v_{IN}T_1 = V_{REF}T_2$)

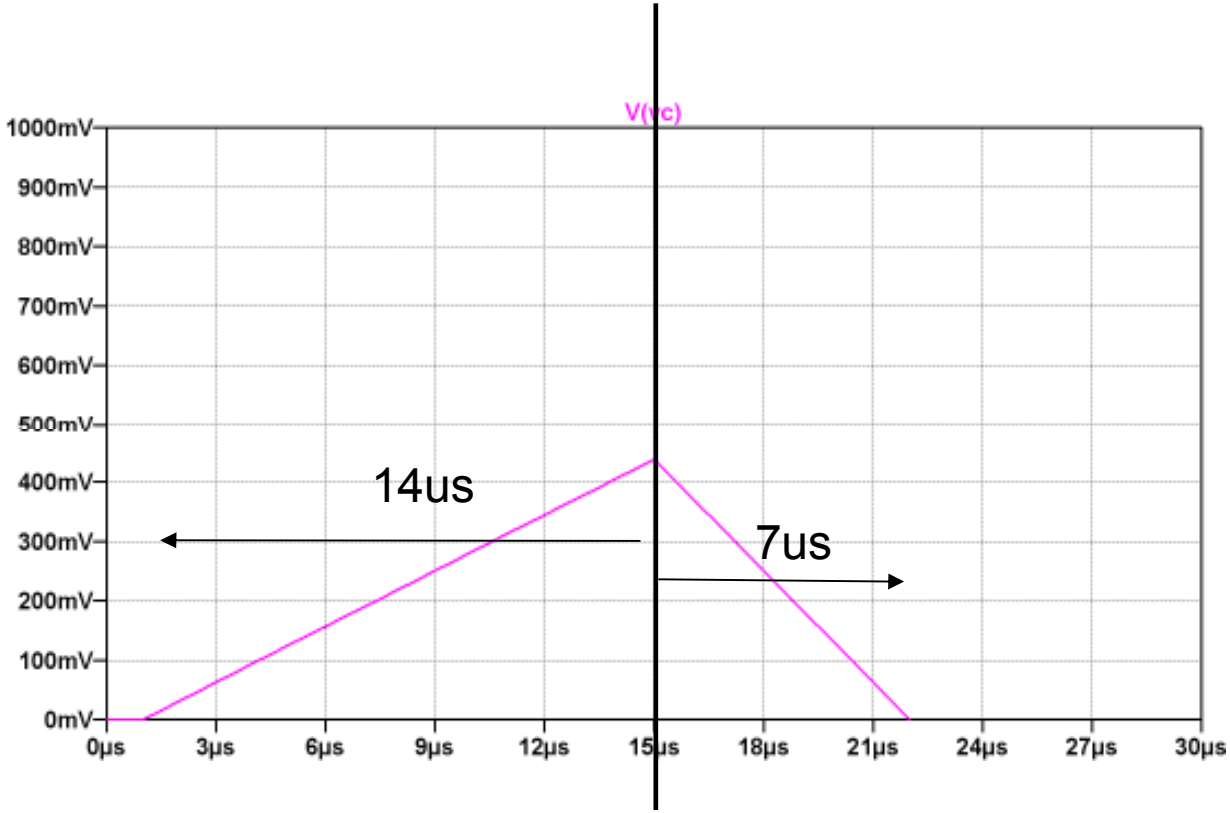
$\rightarrow$

$$\frac{v_{IN}}{V_{REF}} = \frac{T_2}{T_1}$$

Dual-slope ADC Implementation



Dual-slope ADC Simulation



$$\frac{v_{IN}}{V_{REF}} = \frac{T_2}{T_1} = \frac{7us}{14us}$$

Summary

- Integrating ADC
  - High precision
  - Slow speed
- Single-slope
  - 2^N clock cycles (worst-case)
  - Output depends on RC and clock (more error sources)
- Dual-slope
  - 2^{N+1} clock cycles (worst-case)
  - Output only depends on ratio T2/T1
  - Same integrator clock produce T2 and T1, so less error possible

References

[1] R.J. Baker, *CMOS: Circuit Design, Layout, and Simulation, 2nd ed.,* Wiley-IEEE Press, 2005

[2] W. M. C. Sansen, *Analog Design Essenetials*, Springer, 2006

[3] D. A. Johns and K. Martin, *Analog Integrated Circuit Design*, John Wiley and Sons, 1997

Questions?

Charge-Scaling DACs

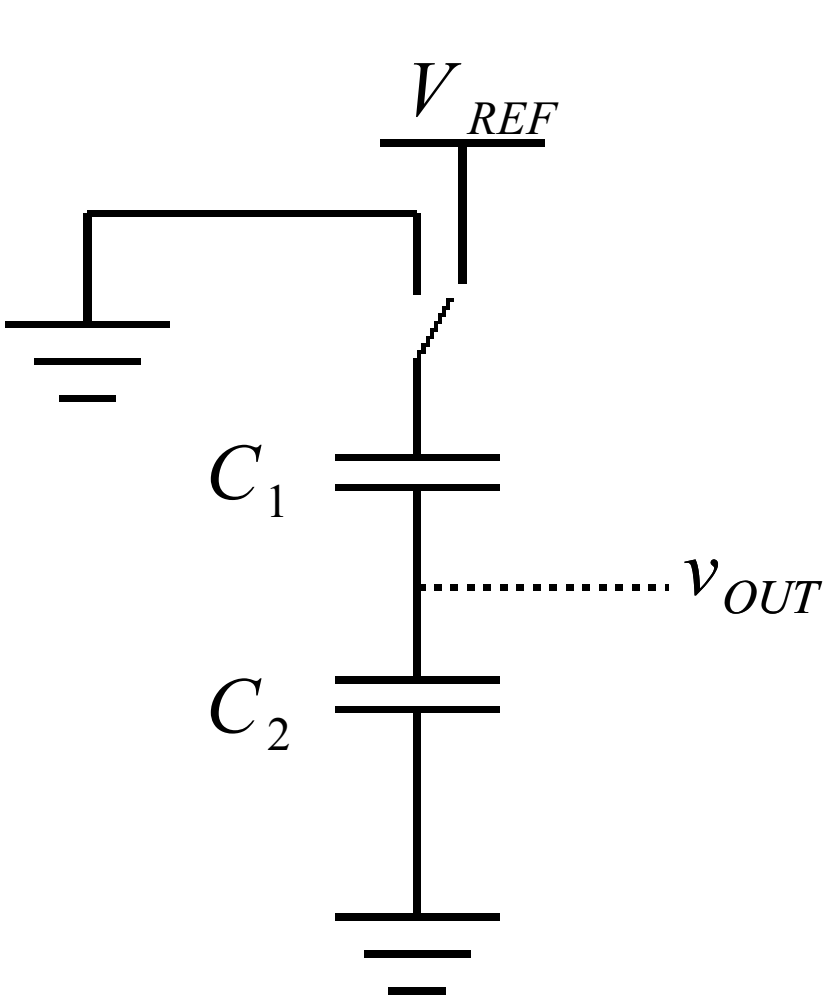
Geng Zheng

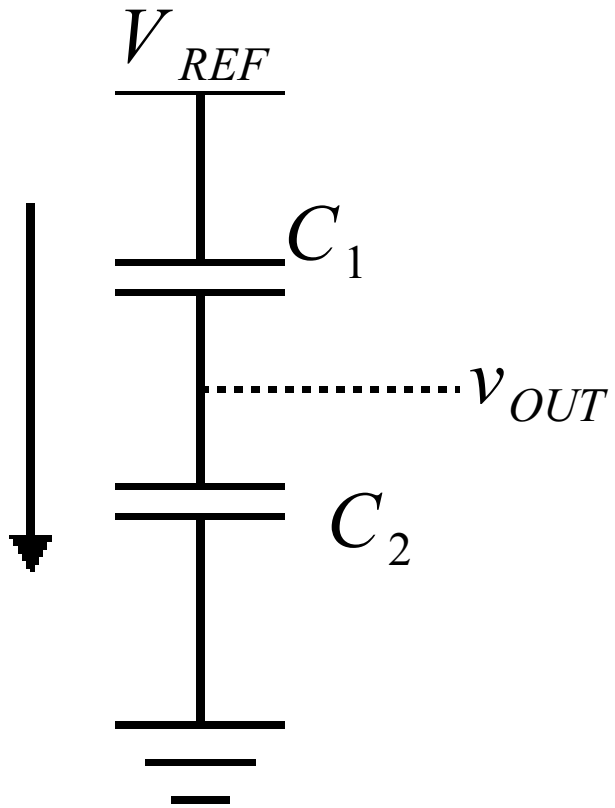
May 7, 2008

Agenda

- Operation
- Mismatch
- INL/DNL
- Topologies
- Simulation
- Summary

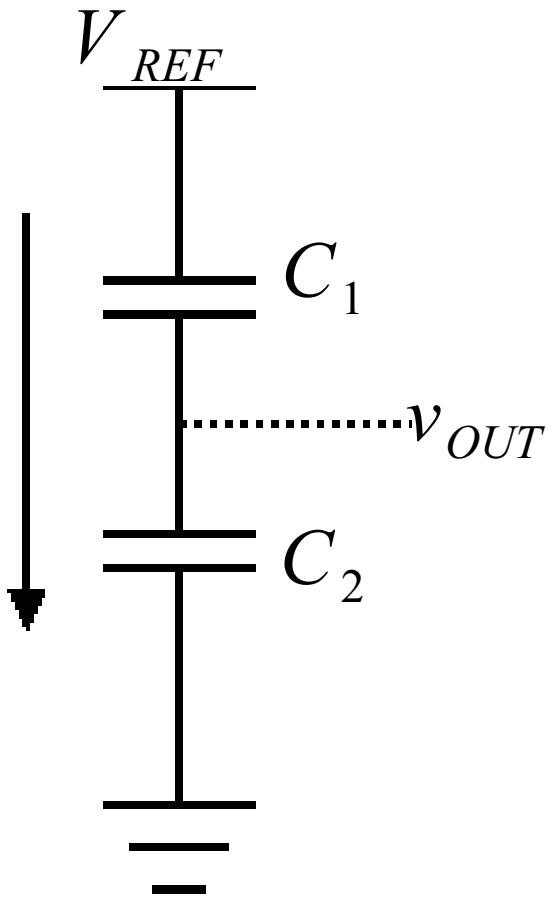
Charge-Scaling Basics





$$\Delta Q_1 = I \cdot T = \Delta Q_2$$

Charge-Scaling Basics



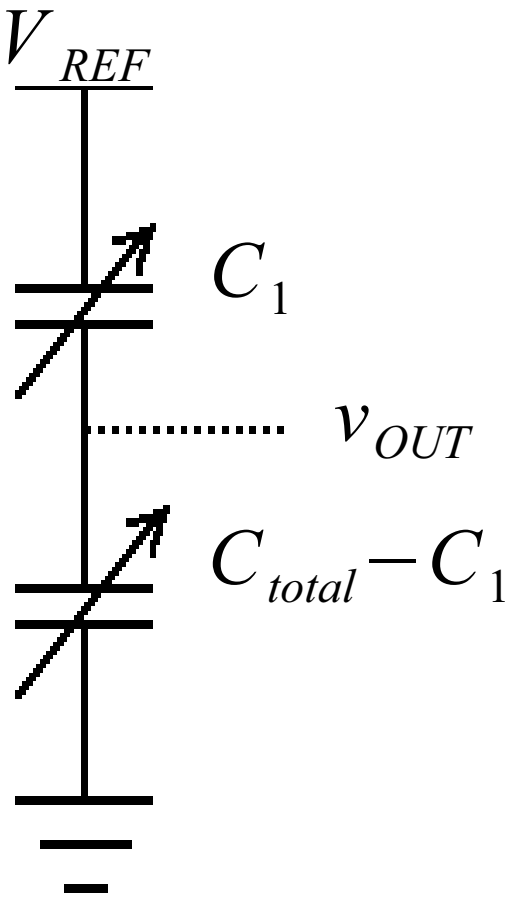
$$\Delta Q_1 = (V_{REF} - v_{OUT}) \cdot C_1 - 0$$

$$\Delta Q_2 = v_{OUT} \cdot C_2 - 0$$

$$\Delta Q_1 = \Delta Q_2$$

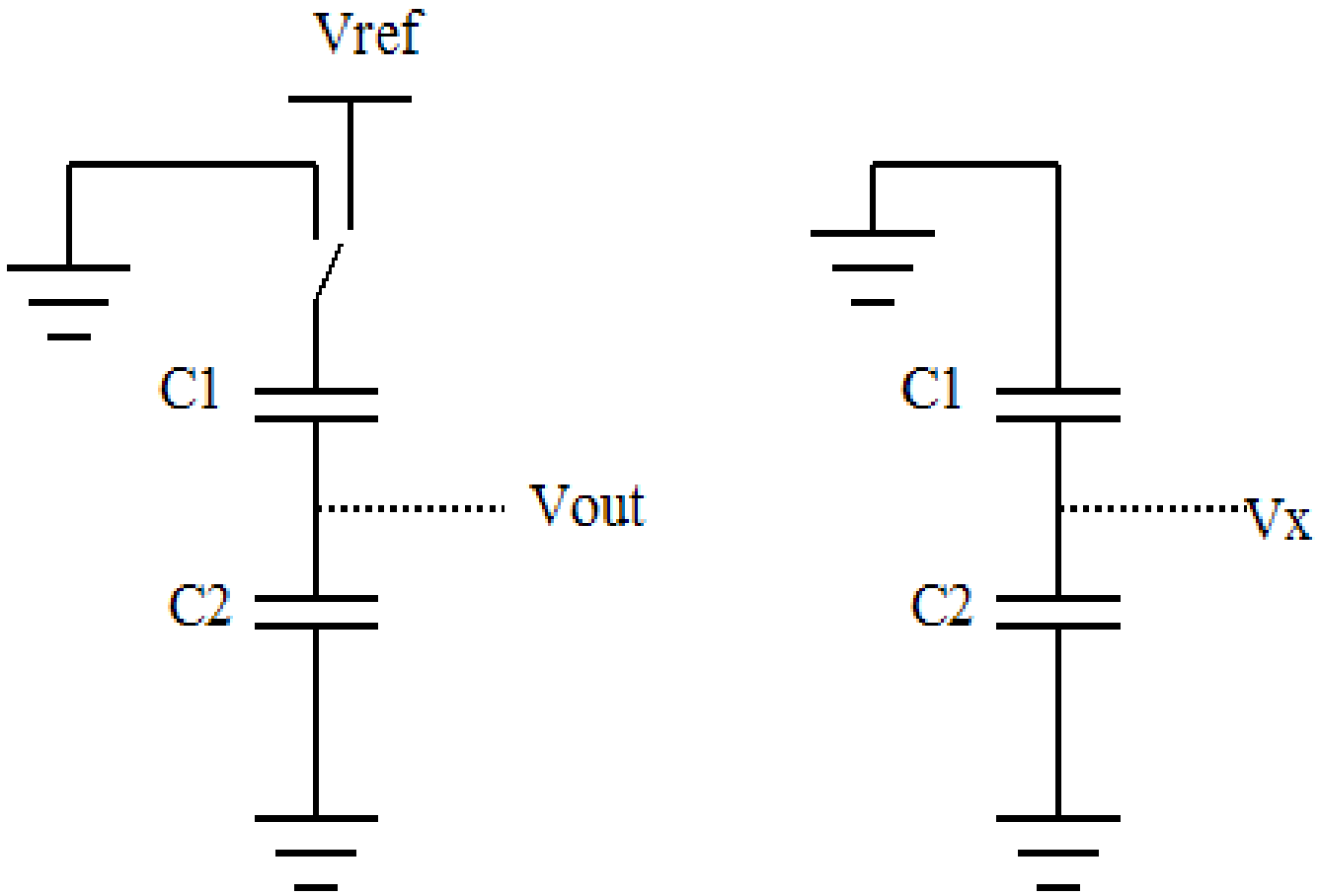
$$\rightarrow \quad v_{OUT} = \frac{C_1}{C_1 + C_2} \cdot V_{REF}$$

Charge-Scaling Basics

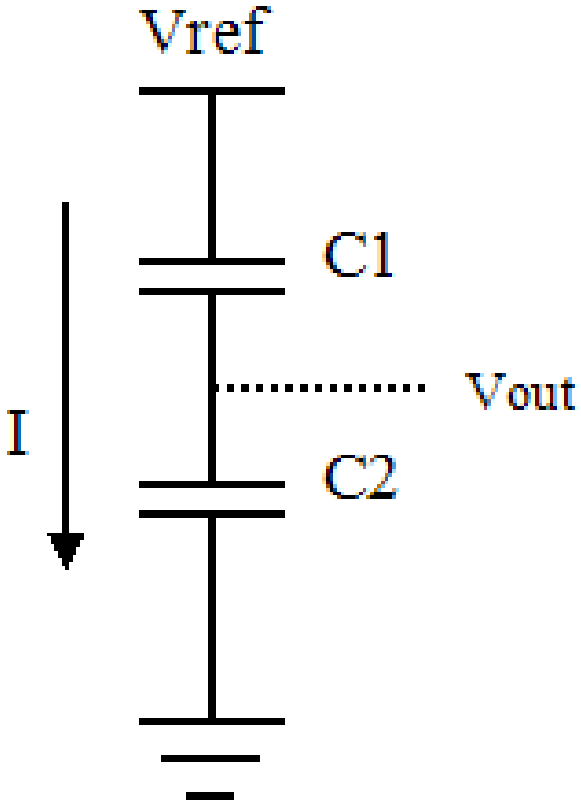


$$v_{OUT} = V_{REF} \frac{C_1}{C_{total}}$$

Charge-Scaling Basics



Charge-Scaling Basics



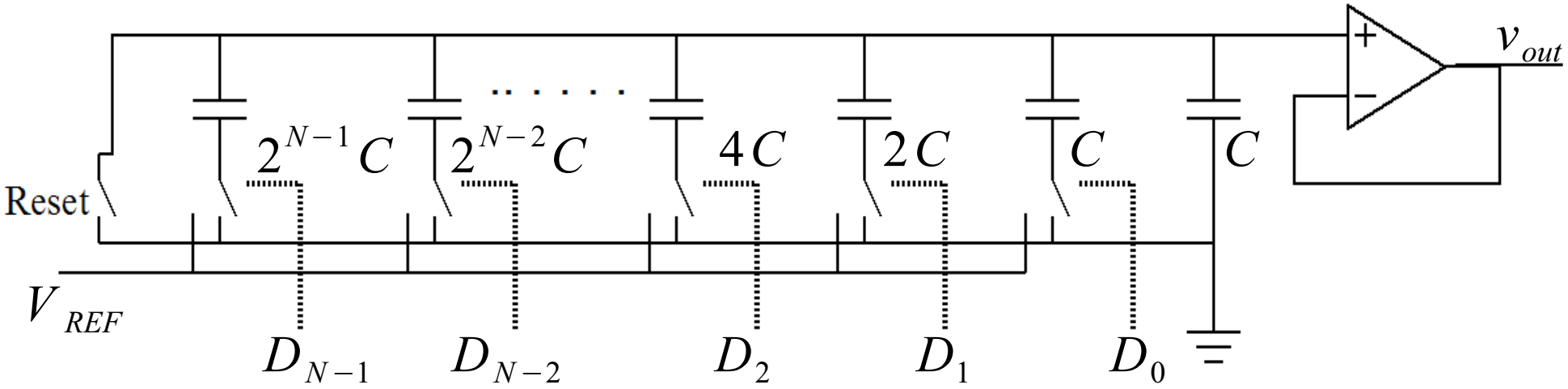
$$\Delta Q_1 = (V_{REF} - v_{OUT}) \cdot C_1 - (0 - V_x) \cdot C_1$$

$$\Delta Q_2 = v_{OUT} \cdot C_2 - V_x \cdot C_2$$

$$\Delta Q_1 = \Delta Q_2$$

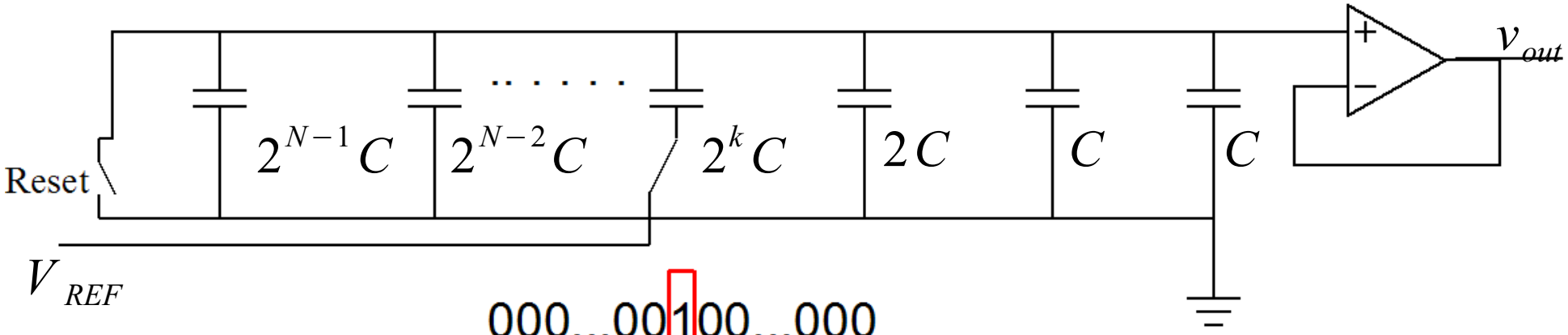
$$\rightarrow \; v_{OUT} = \frac{C_1}{C_1 + C_2} \cdot V_{REF} + V_x$$

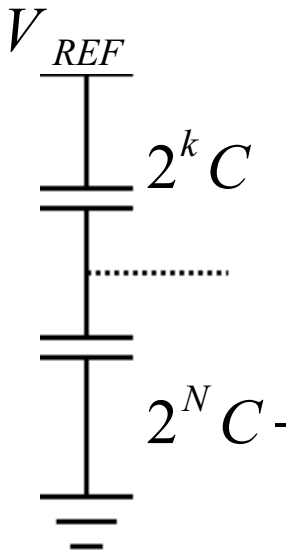
A N-bit Charge-Scaling DAC



$$\sum \text{all capacitors} = 2^N C$$

A N-bit Charge-Scaling DAC



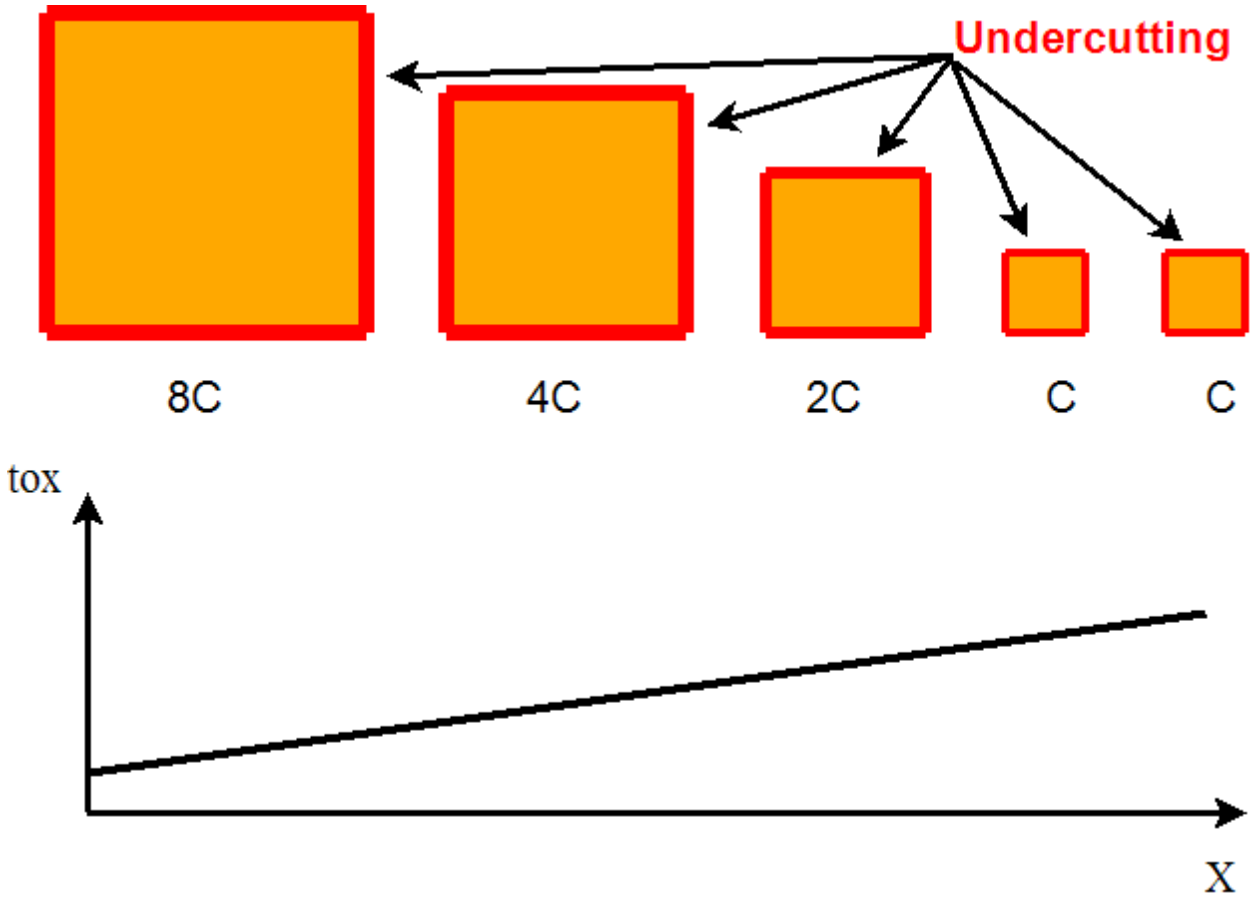


$$v_{out,k} = \frac{2^k C}{2^N C} V_{REF}$$

$$v_{out} = \sum_{k=0}^{N-1} D_k v_{out,k}$$

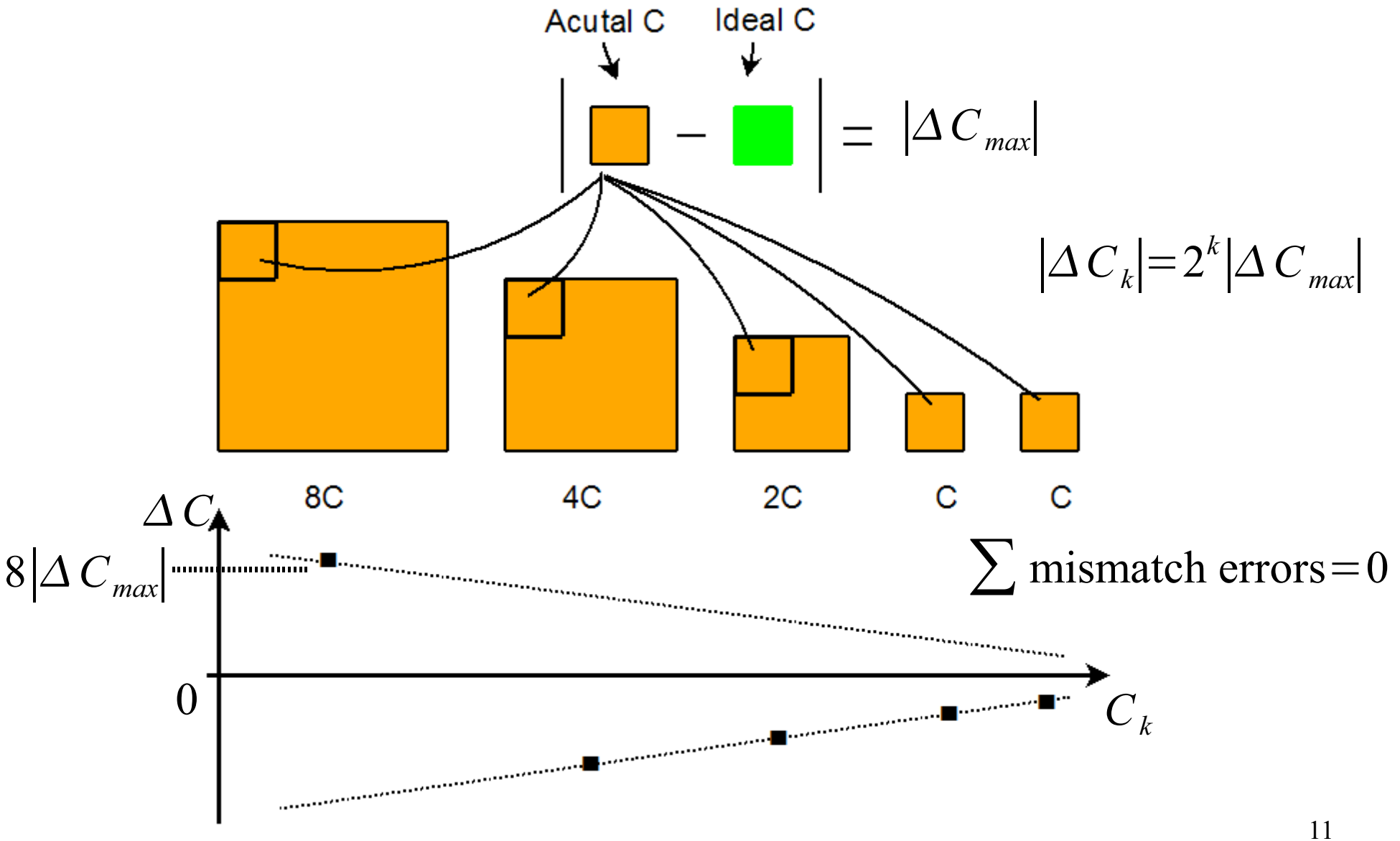
$$= \sum_{k=0}^{N-1} D_k 2^{k-N} V_{REF}$$

Capacitor Mismatch



See Ref[2] for details

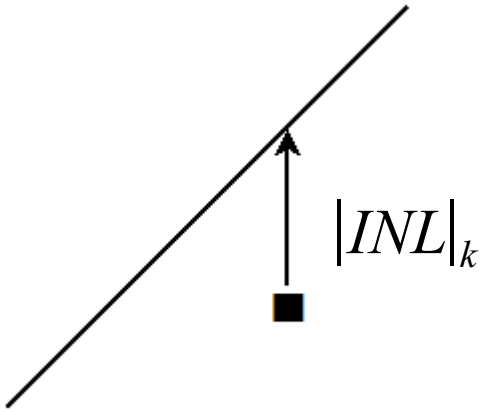
Capacitor Mismatch



INL

$$v_{out,k} = \frac{C_k}{C_{total}} \cdot V_{REF} = \frac{2^k (C \pm \Delta C_{max})}{2^N C} \cdot V_{REF}$$

$$= \frac{2^k C}{2^N C} V_{REF} \pm \frac{2^k}{2^N C} V_{REF} \frac{|\Delta C_{max}|}{C}$$



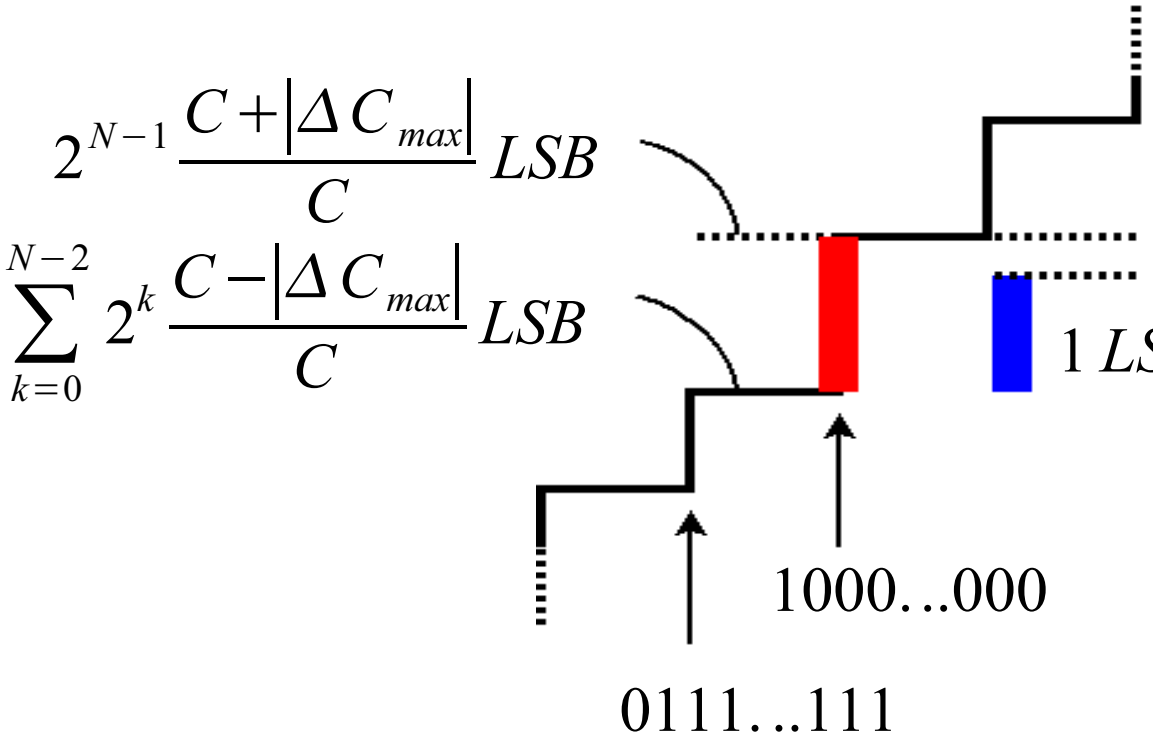
$$|INL|_k = 2^k \frac{|\Delta C_{max}|}{C} LSB$$

The worst-case occur at midpoint (k = N-1):

$$|INL|_{max} = 2^{N-1} \frac{|\Delta C_{max}|}{C} LSB \xrightarrow{|INL|_{max} \leq 0.5\ LSB} \frac{|\Delta C_{max}|}{C} \leq \frac{1}{2^N}$$

DNL

The worst-case: $0111\ldots111 \rightarrow 1000\ldots000$



$$DNL_{max} = (2^N - 1) \cdot \frac{|\Delta C_{max}|}{C} LSB$$

For $DNL_{max} \leqslant 0.5\,LSB$,

$$\frac{|\Delta C_{max}|}{C} \leqslant \frac{1}{2^{N+1} - 2}$$

The Split Array

A 12-bit DAC with C = 100 fF:

$$C_{MSB} = 2^{11} \cdot 100\ fF = 204.8\ pF$$

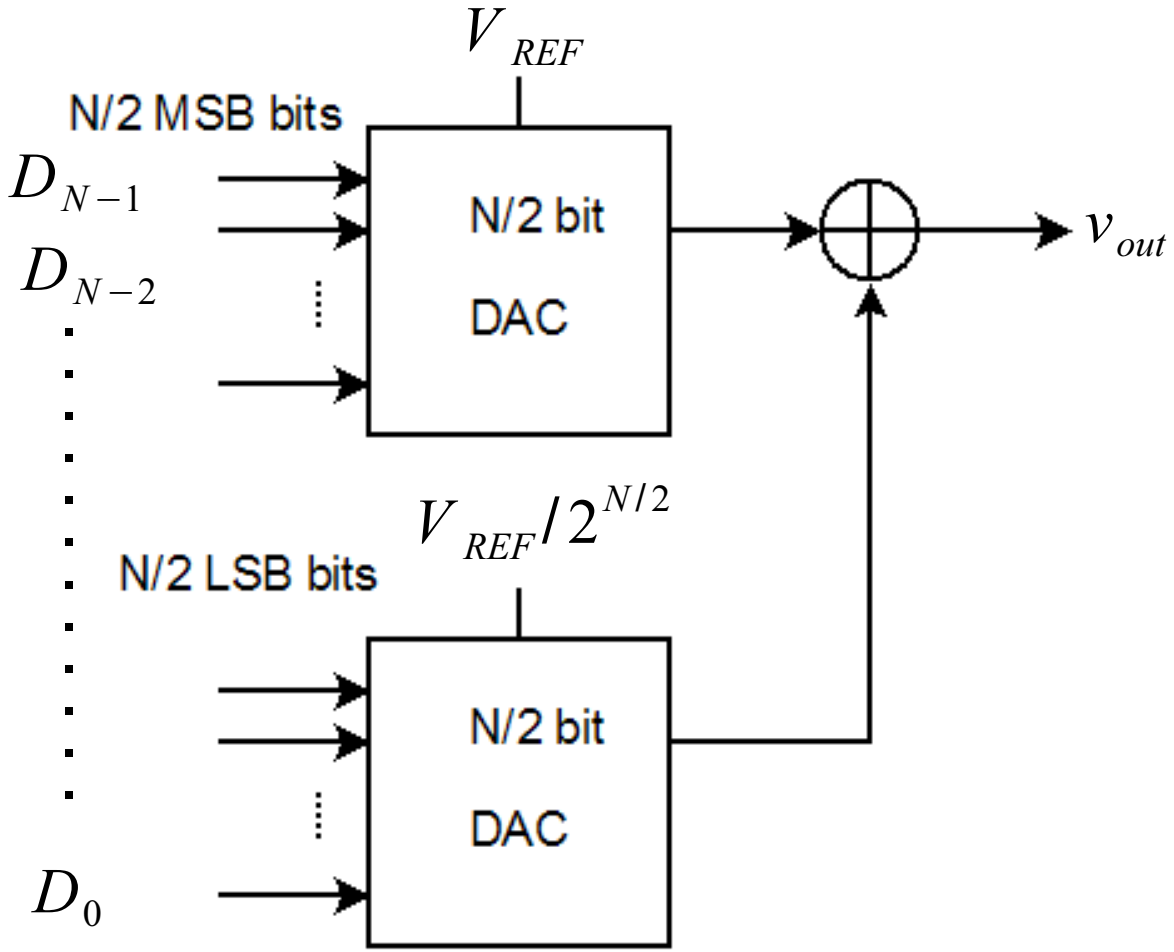
AMI's C5 (500 nm) process:

$$C_{p1-p2} \approx 900\ aF / \mu m^2$$

$$\rightarrow Area_{C_{MSB}} \approx 477 \times 477\ \mu m^2\ !\ !\ !$$

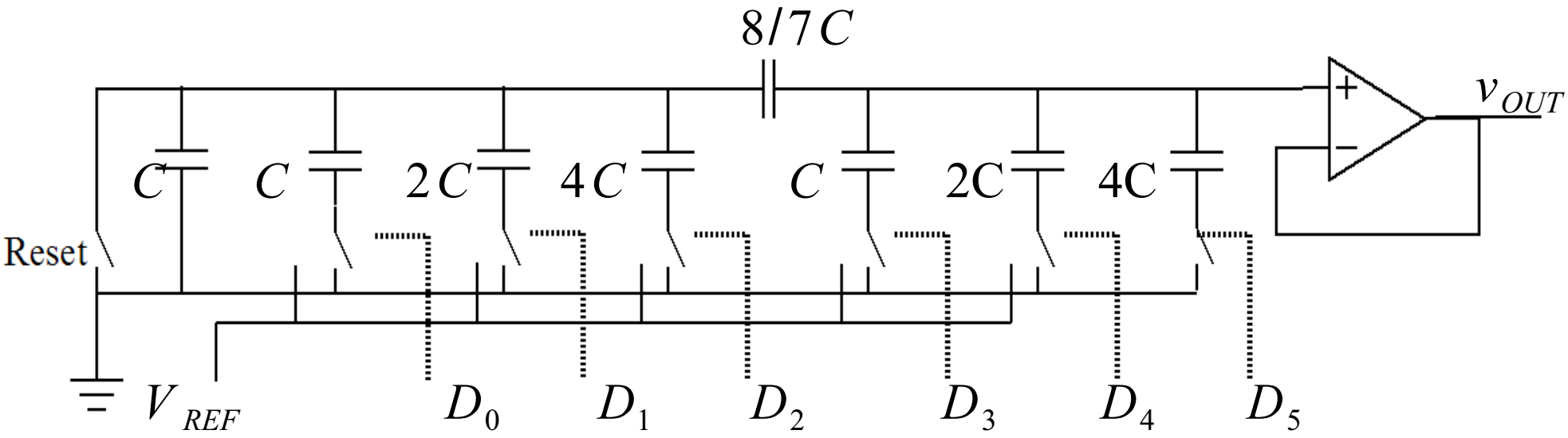
The Split Array

Subranging Topology



The Split Array

A 6-bit split array charge-scaling DAC

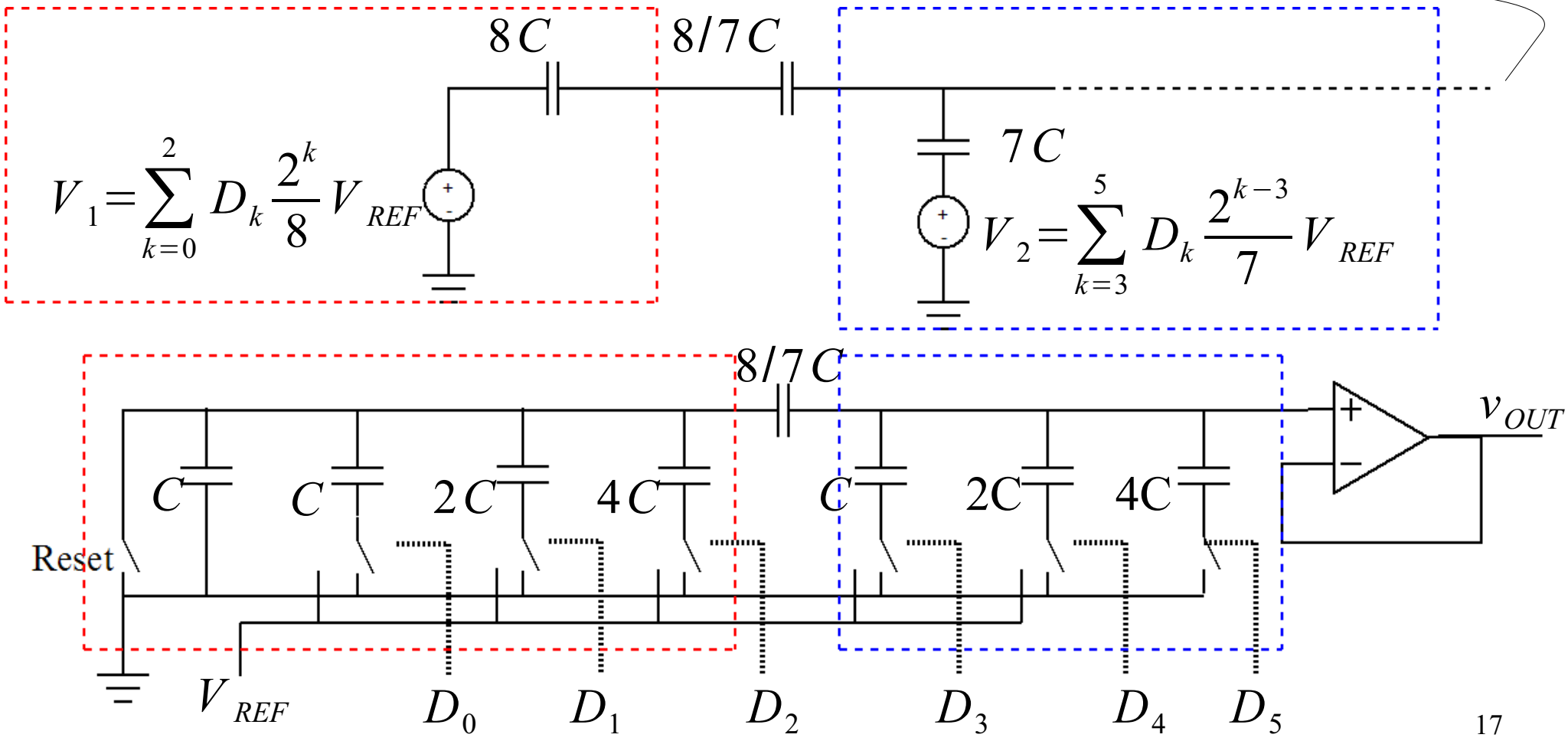


$$C_{atten} = \frac{\sum LSB\ array\ capacitors}{\sum MSB\ array\ capacitors} = \frac{C + C + 2C + 4C}{C + 2C + 4C} = \frac{8}{7}C$$

The Split Array

Thevenin equivalent circuit

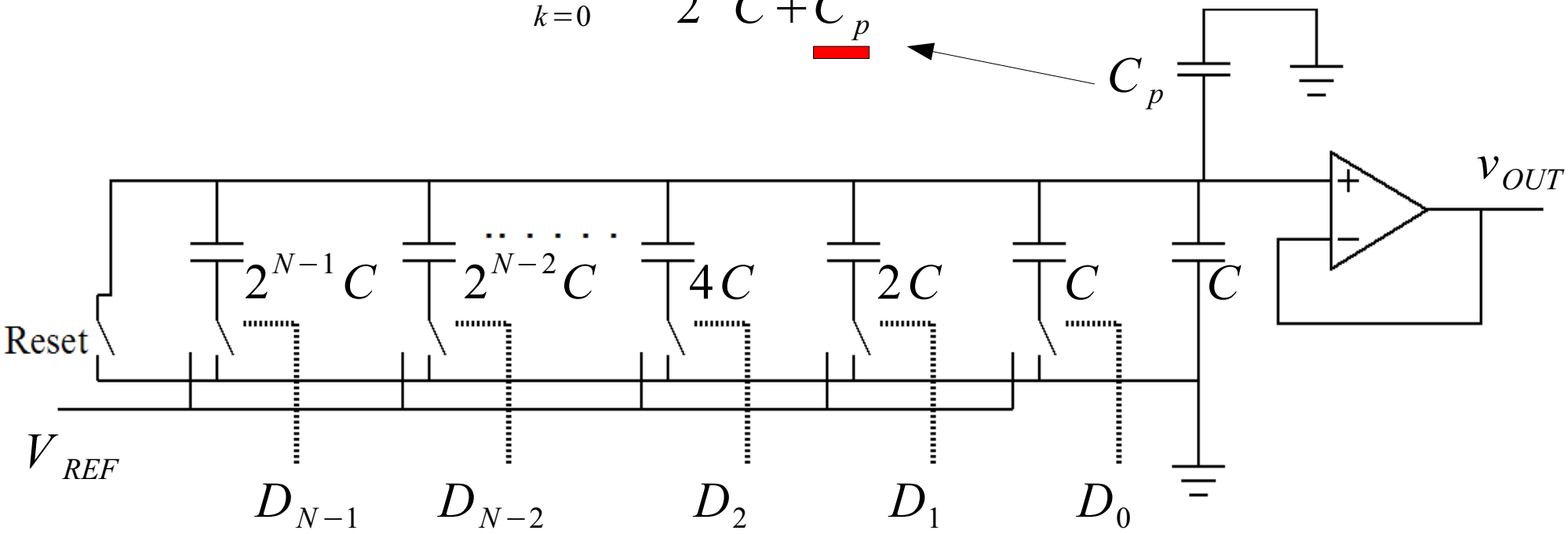
$$v_{OUT} = \frac{1}{8} V_1 + \frac{7}{8} V_2$$



Issue and Other Topologies

- Parasitic Capacitance

$$v_{OUT} = \sum_{k=0}^{N-1} D_k \frac{2^k C}{2^N C + C_p} V_{REF}$$



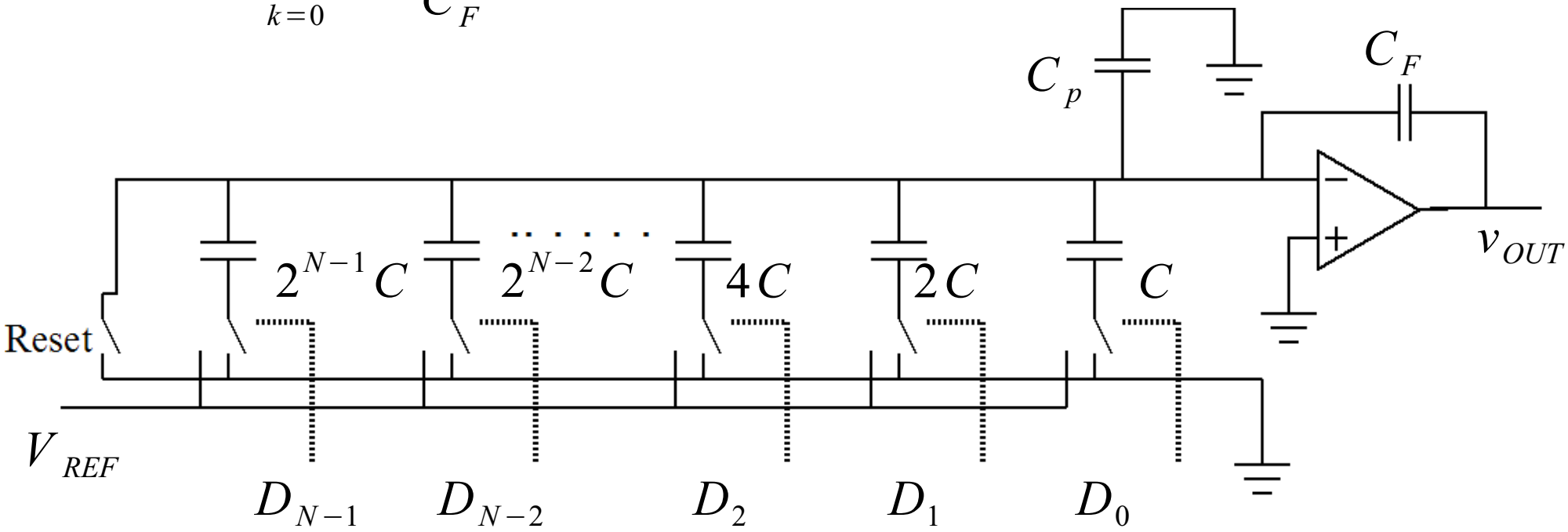
Issue and Other Topologies

- Parasitic Capacitance

$$v_{OUT} = \sum_{k=0}^{N-1} D_k \frac{2^k C}{C_F} V_{REF}$$

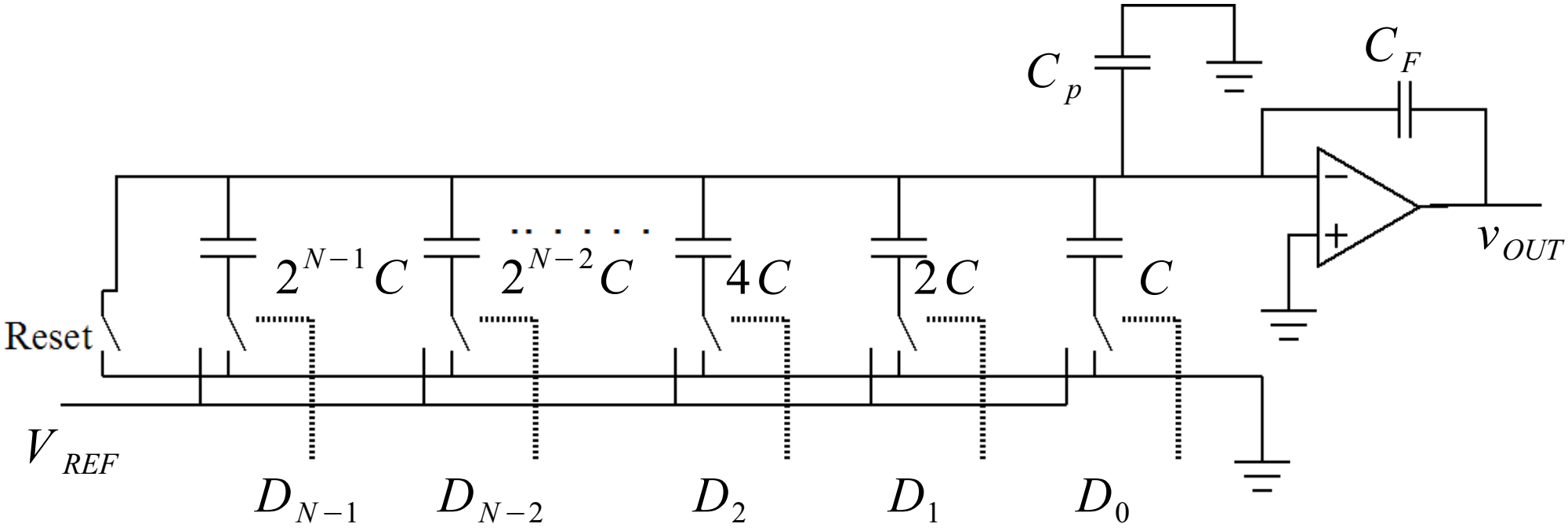
$$C_F = 2^N C$$

$$v_{OUT} = \sum_{k=0}^{N-1} D_k \frac{2^k C}{2^N C} V_{REF}$$



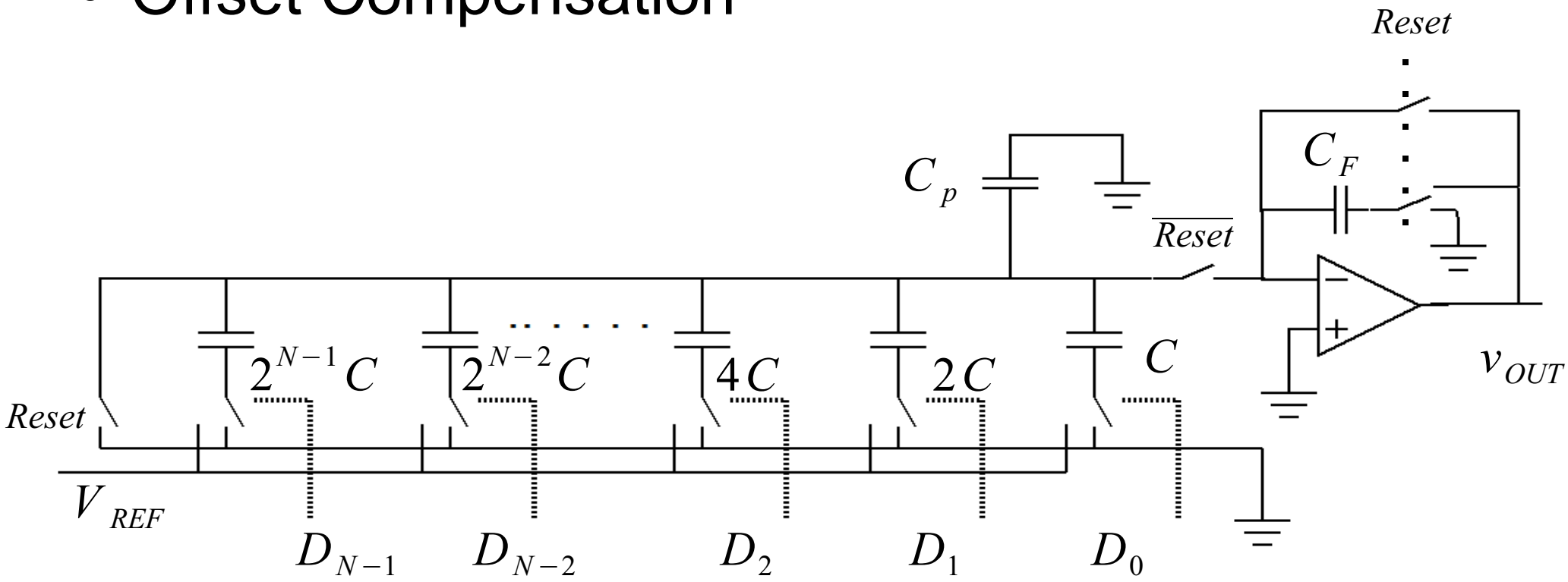
Issue and Other Topologies

- SPICE Simulation



Issue and Other Topologies

- Offset Compensation



Summary

- Large area for high resolution
- Large capacitor ratios; matching issue
- The simple topology sensitive to parasitic caps
- Offset is easy to compensate

References

1. R. J. Baker, “CMOS Circuit Design, Layout, and Simulation”, 2nd ed, Wiley-IEEE, 2005.
2. J. L. McCreary and P. R. Gray, “All-MOS Charge Redistribution Analog-to-Digital Conversion Techniques – Part I”, IEEE Journal of Solid State Circuits, vol. 10, no. 6, pp. 371-379, Dec. 1975
3. http://www.mosis.com/cgi-bin/cgiwrap/umosis/swp/params/ami-c5/t68z-params.txt
4. http://www.aicdesign.org/SCNOTES/2006notes/Chap10(12_8_06).pdf

Question?