BOISE STATE UNIVERSITY

Design and Operation of Delta-Sigma ADCs

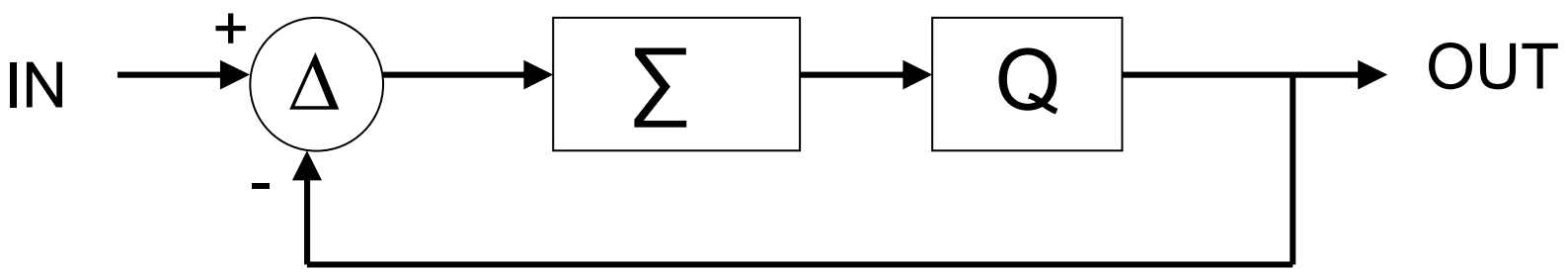
ECE614 Advanced Analog IC Design

Joshua Nekl

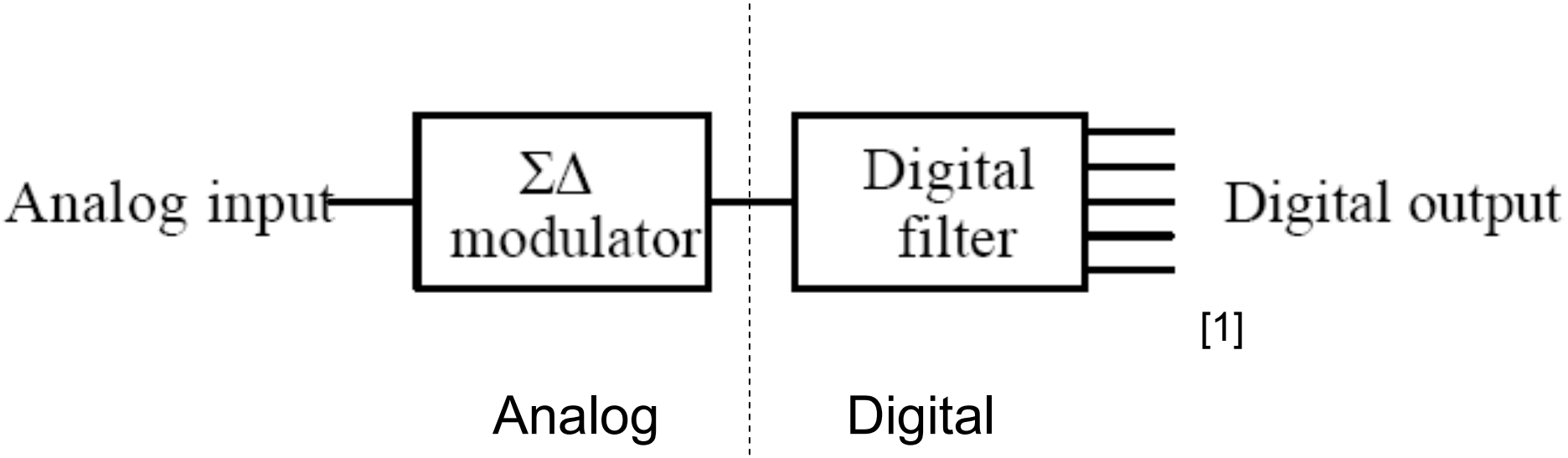
May 5, 2008

What is a Delta-Sigma ADC

- AKA Sigma-Delta ADC, over-sampling ADC, noise-shaping ADC, 1-bit ADC
- Integrates (Sigma) the difference (Delta) between the quantized output and the input



ΔΣ ADC


Analog input
ΣΔ modulator
Digital filter
Digital output
Analog
Digital

[1]

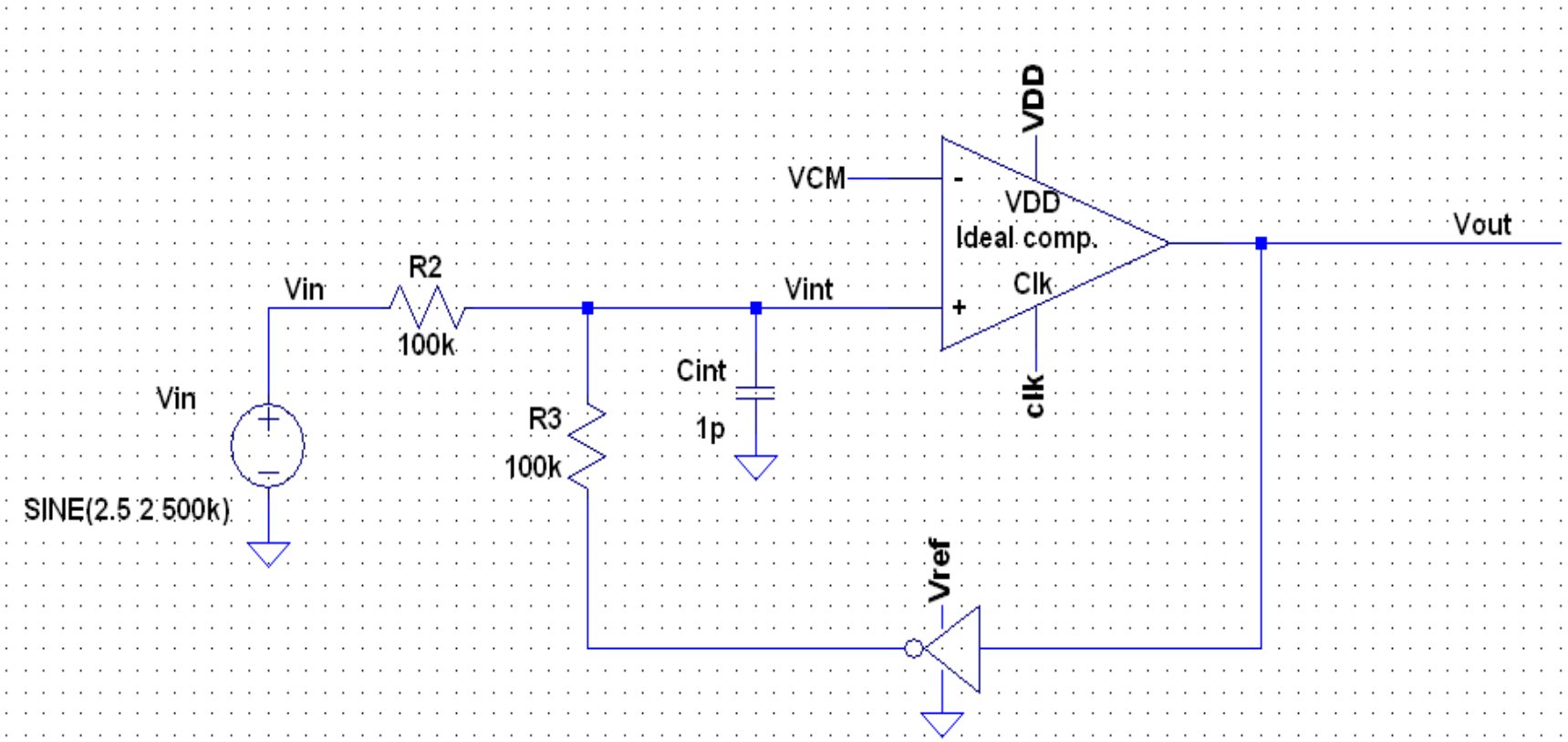
Benefits

- No precision matched analog components
- High achievable accuracy
- Low-pass filtering

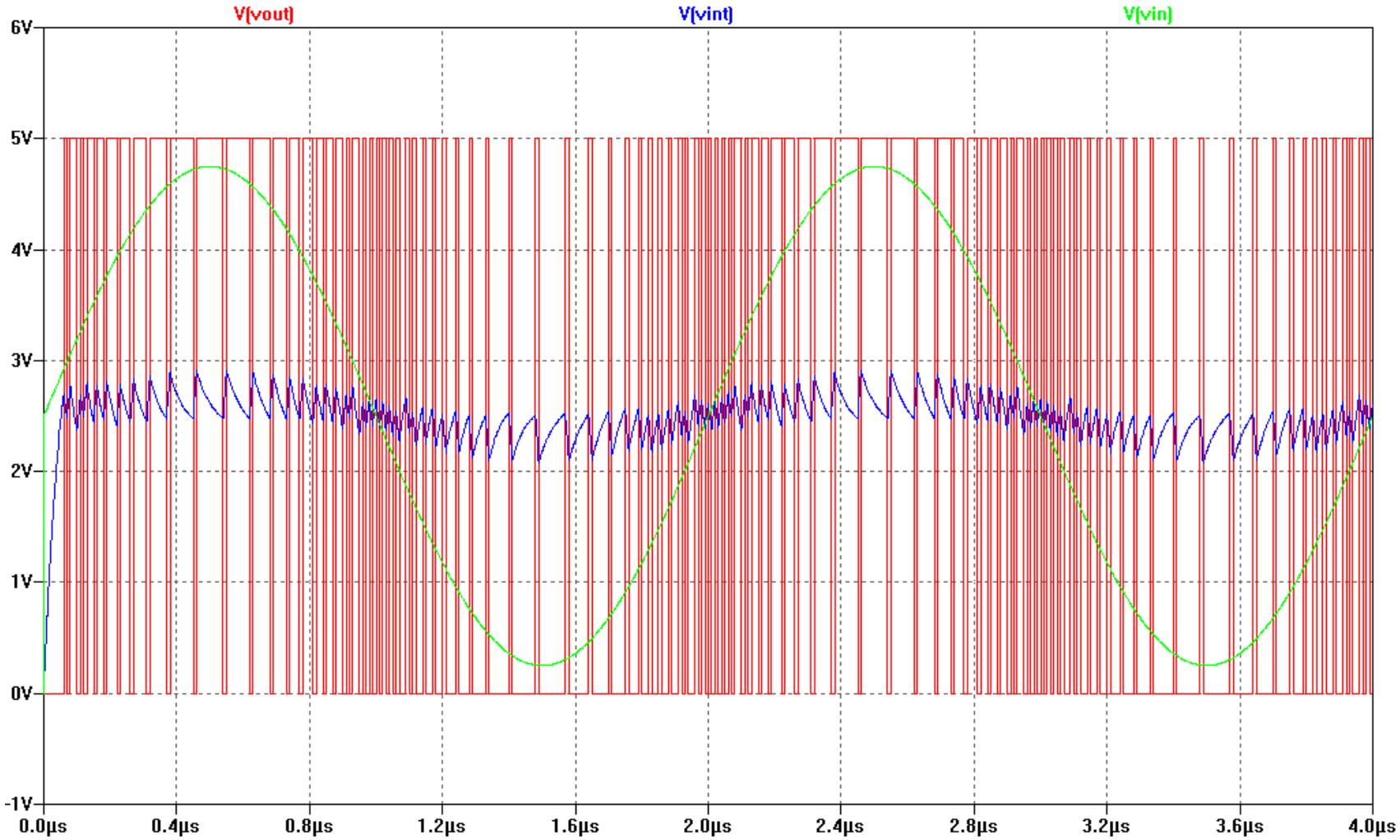
Drawbacks

- Slower conversion time
- DC input current / resistive input impedance

Simple Modulator



Modulator Output



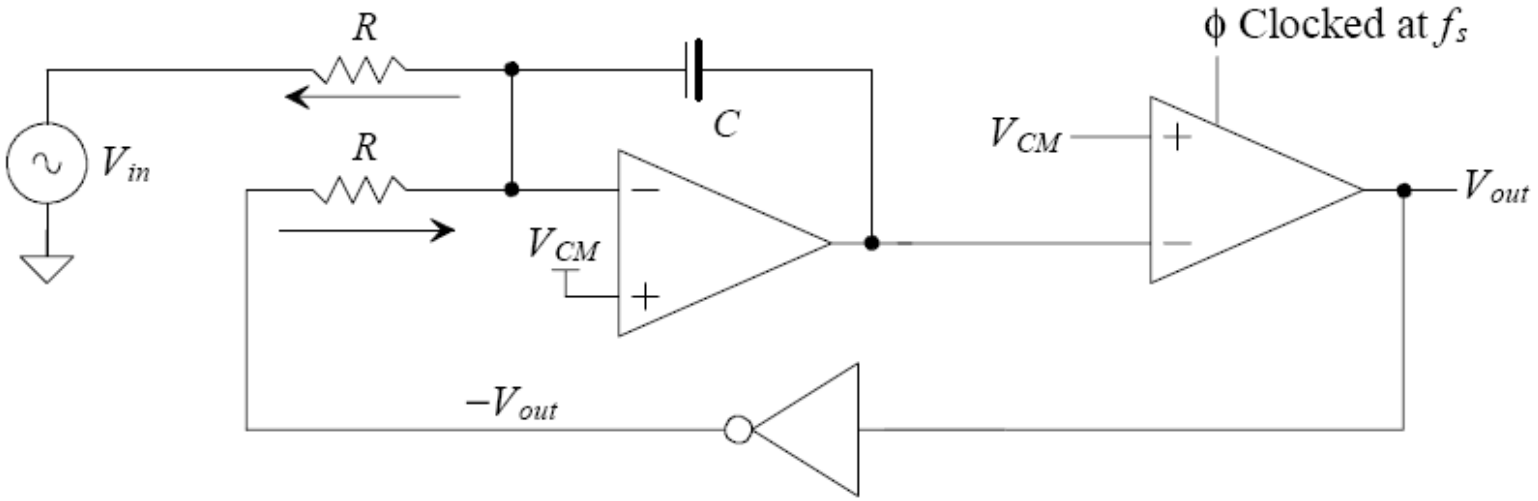
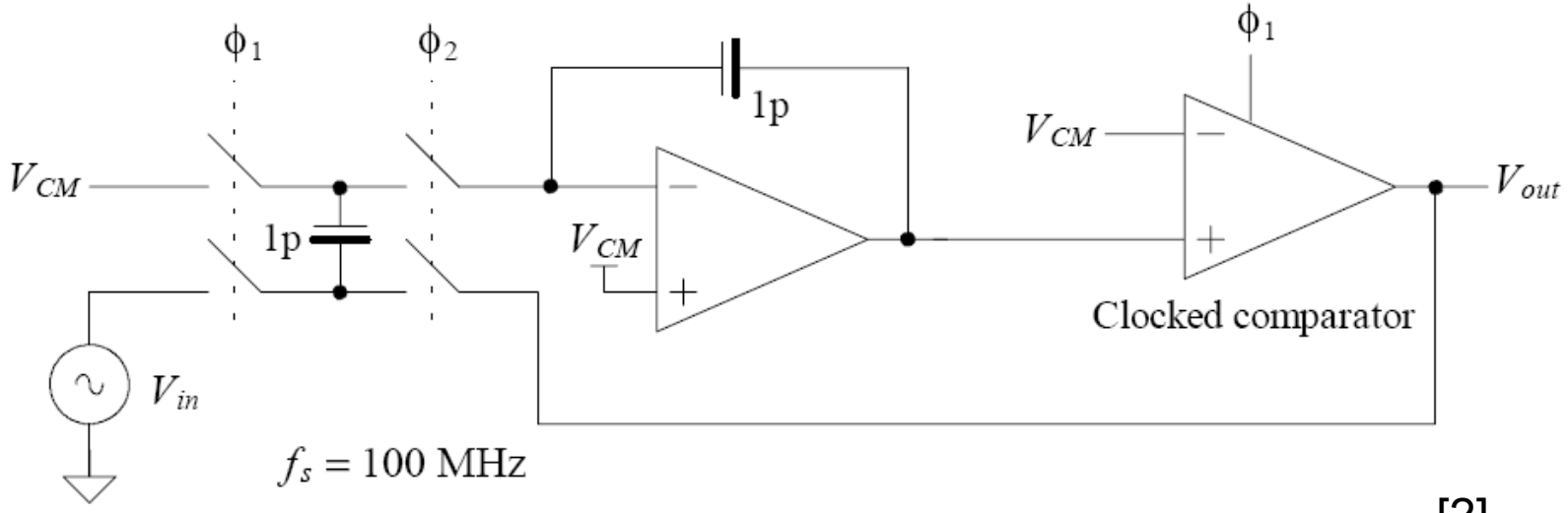


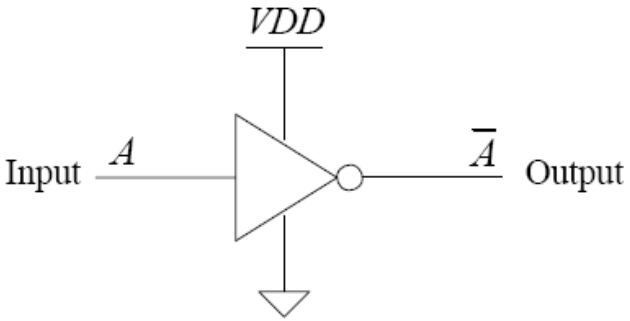
Figure 32.24 Analog circuit implementation of a first-order NS modulator. [2]

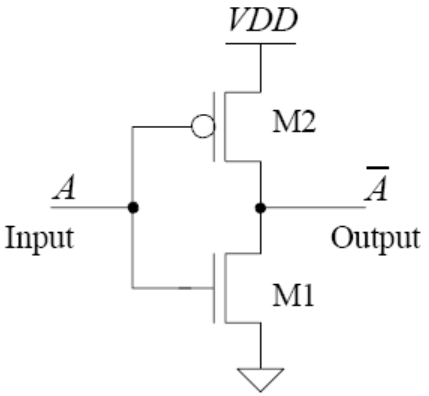


[2]

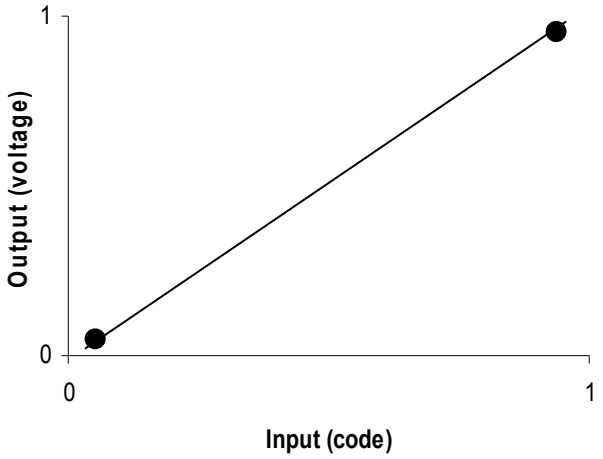
Figure 32.7 Circuit implementation of a first-order NS modulator.

Feedback DAC Transfer Curve





[1]



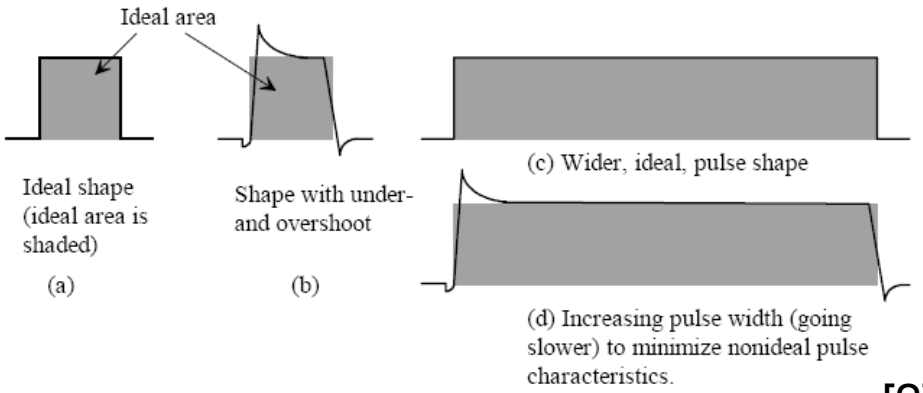
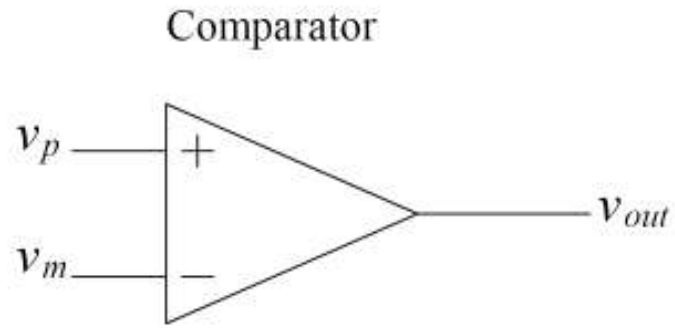


Figure 32.25 Comparator output pulse shapes, input to the integrator.

[2]

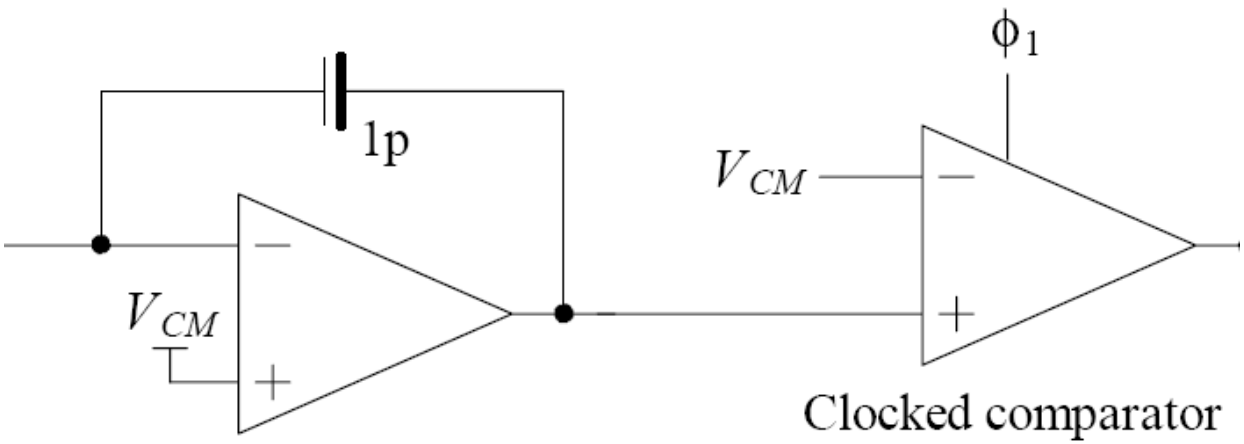
Quantizer



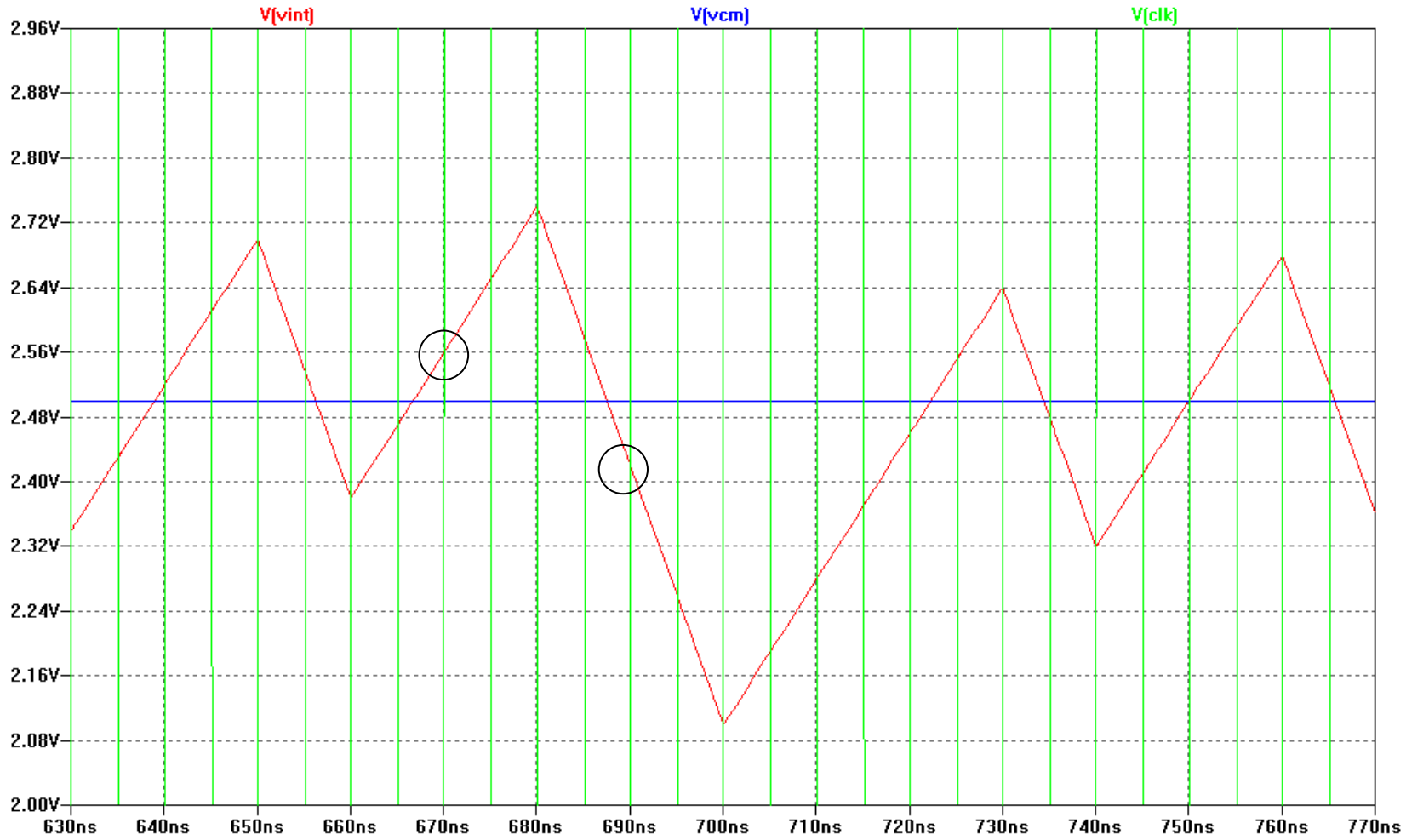
1-bit ADC

[1]

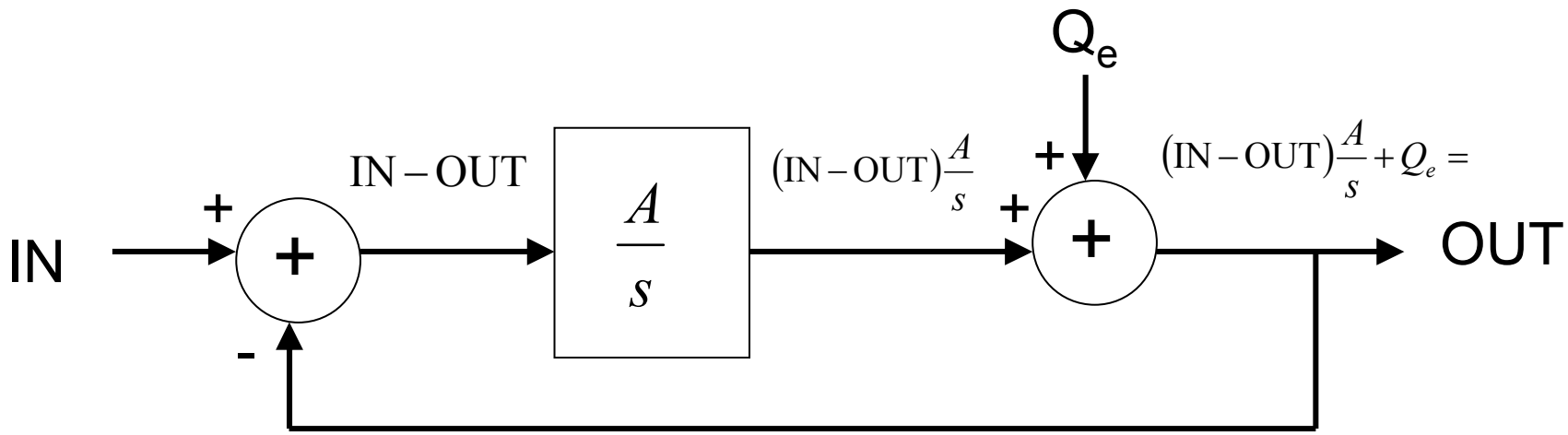
Offset Cancellation



Comparator Decision Errors

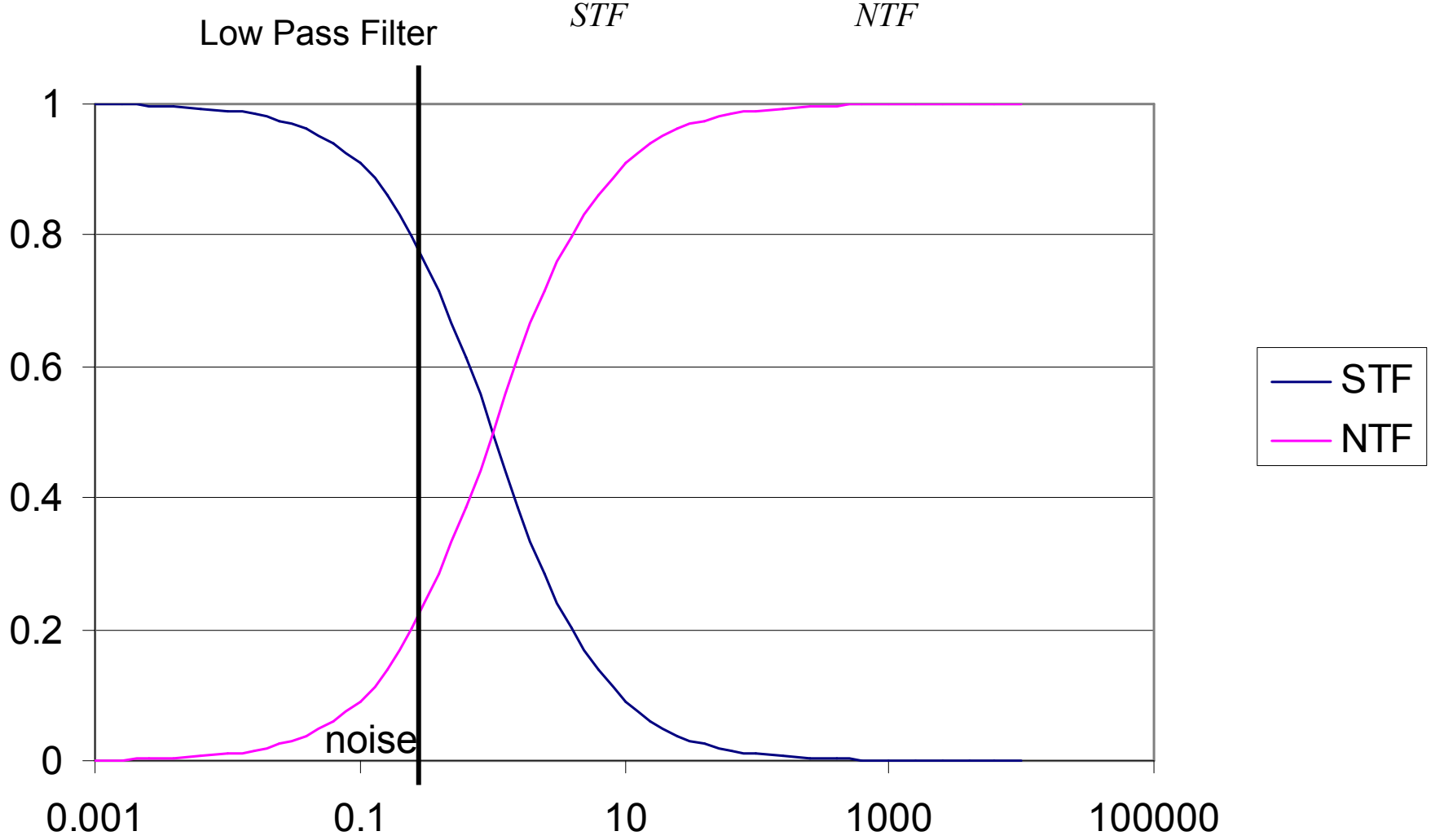


Noise Shaping

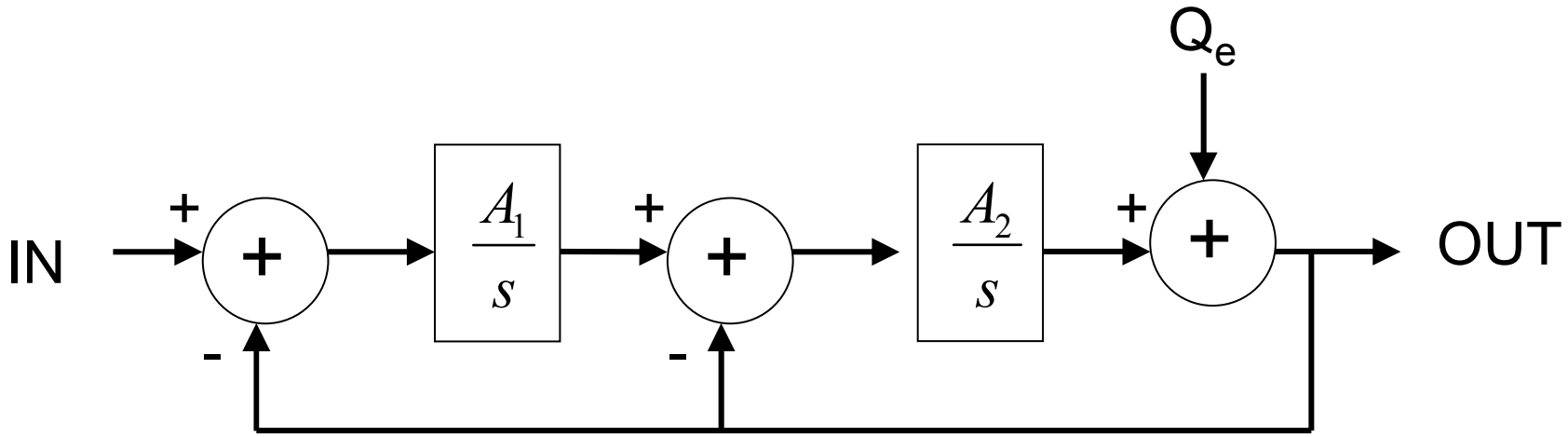


$$OUT = IN \underbrace{\frac{1}{s/A+1}}_{STF} + Q_e \underbrace{\frac{s/A}{s/A+1}}_{NTF}$$

$$OUT = IN \underbrace{\frac{1}{s/A+1}}_{STF} + Q_e \underbrace{\frac{s/A}{s/A+1}}_{NTF}$$

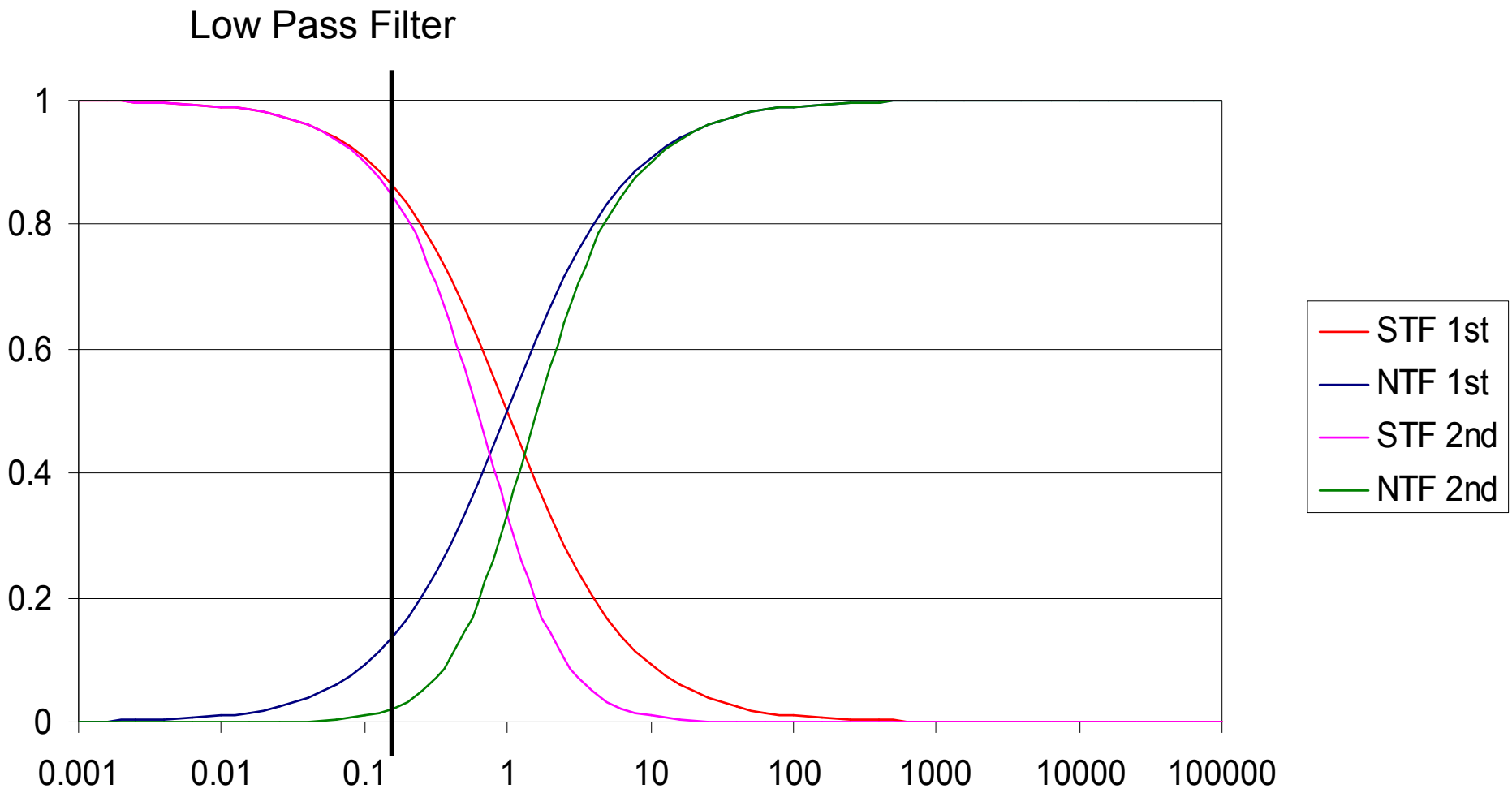


2nd order Modulator



$$OUT = IN\underbrace{\frac{1}{s^2/A_1A_2 + s/A_1 + 1}}_{STF} + Q_e\underbrace{\frac{s^2/A_1A_2}{s^2/A_1A_2 + s/A_1 + 1}}_{NTF}$$

Comparison of 1st & 2nd order modulator

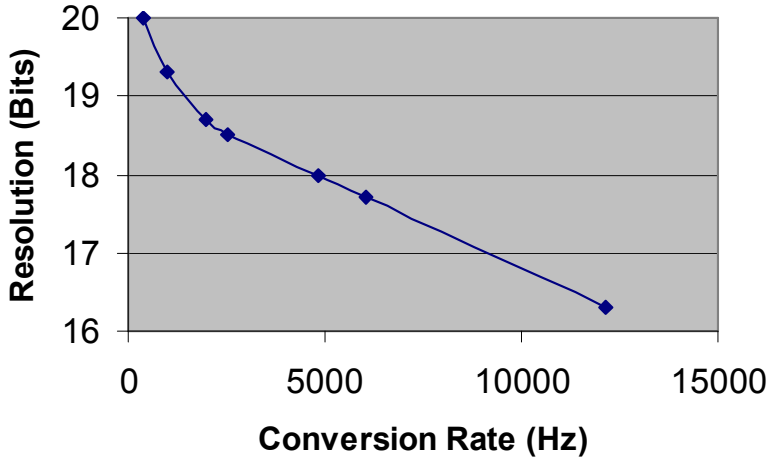


Speed vs Resolution

Analog Devices - AD7732

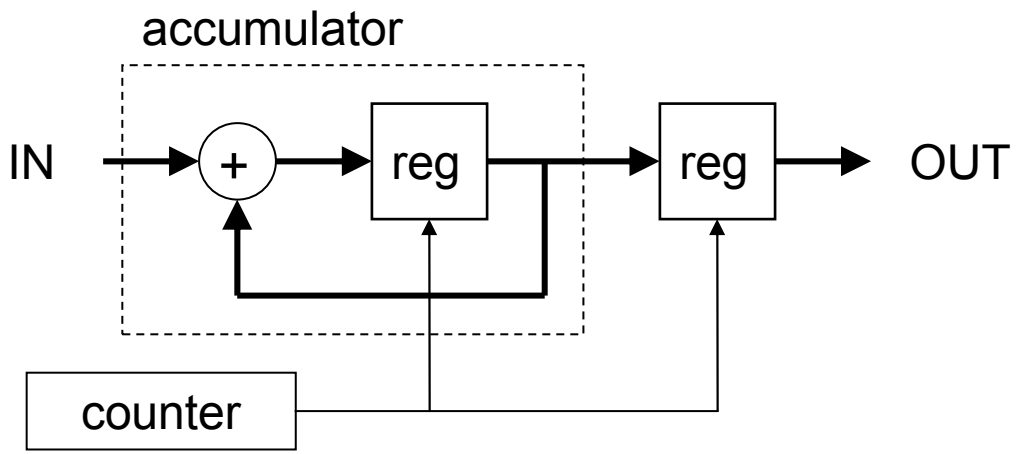
Table 5. Typical Effective Resolution in Bits vs. Conversion Time and Input Range with Chopping Enabled

FW	Conversion Time Register	Conversion Time (µs)	Output Data Rate (Hz)	–3 dB Frequency (Hz)	Input Range/Effective Resolution (Bits)			
					±10 V	0 V to +10 V	±5 V	0 V to +5 V
127	FFh	2686	372	200	21.0	20.0	20.0	19.0
46	AEh	999	1001	520	20.3	19.3	19.3	18.3
22	96h	499	2005	1040	19.7	18.7	18.7	17.7
17	91h	395	2534	1300	19.5	18.5	18.5	17.5
8	88h	207	4826	2500	19.0	18.0	18.0	17.0
6	86h	166	6041	3100	18.7	17.7	17.7	16.7
2	82h	82	12166	6300	17.3	16.3	16.3	15.3



Low Pass Digital Filter

Simple Counter



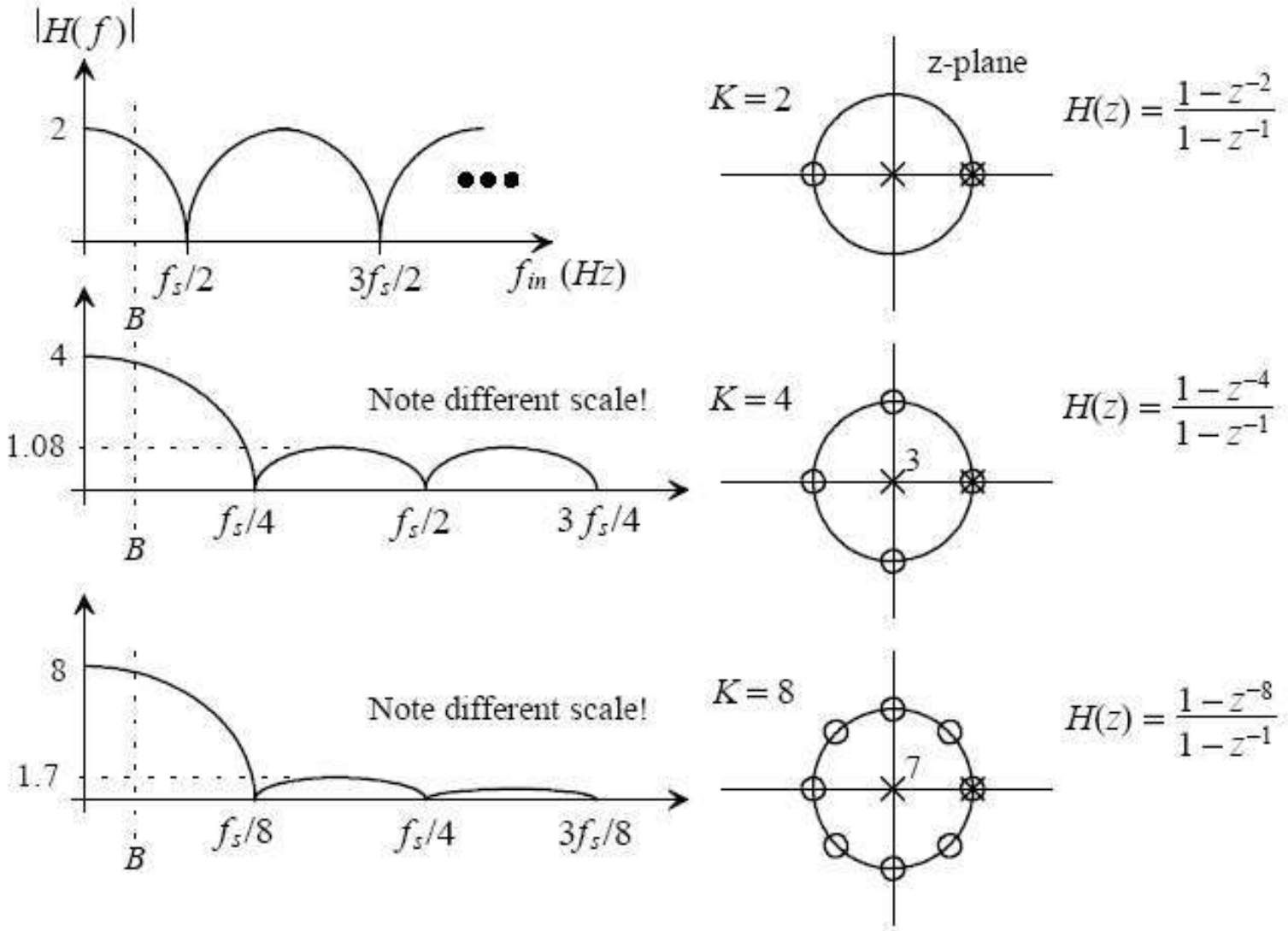
z-Transform

$$z = e^{j2\pi f T_s} = e^{j2\pi \frac{f}{f_s}}$$

$$y[n] = x[n] + x[n-1] + x[n-2] + \ldots + x[n-(K-1)]$$

$$Y(z) = X(z) \cdot (1 + z^{-1} + z^{-2} + \ldots + z^{-(K-1)}) \cdot \frac{1 - z^{-1}}{1 - z^{-1}}$$

$$H(z) = \frac{Y(z)}{X(z)} = \frac{1 - z^{-K}}{1 - z^{-1}}$$



[2]

Figure 31.40 Frequency response of the accumulate-and-dump for various values of K.

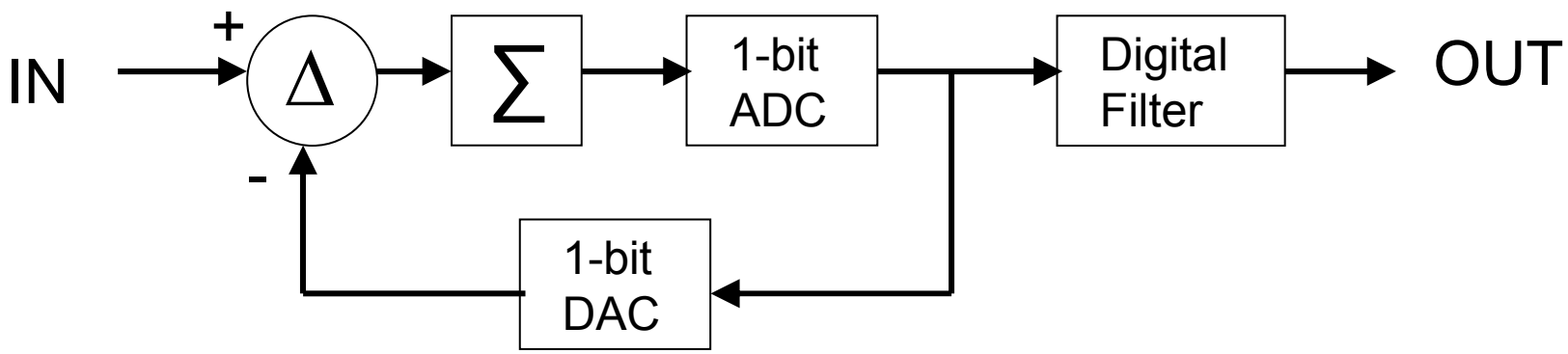
Types of Digital Filters

- Higher Order Sinc Filters
- FIR filters
- BiQuad Filters

References

[1] Baker, R. Jacob, CMOS: Circuit Design, Layout, and Simulation
[2] Baker, R. Jacob, CMOS: Mixed-Signal Circuit Design
[3] Analog Devices AD7732 Datasheet

Questions?



BOISE STATE UNIVERSITY

Design and operation of folding ADCs

ECE 614 Student Presentation

By Kaijun Li

May 5, 2008

Outline

- Miscellaneous ADC
- Interpolating ADC
- Folding ADC
- Folding & Interpolation
- Simulation
- Conclusion

Miscellaneous ADC

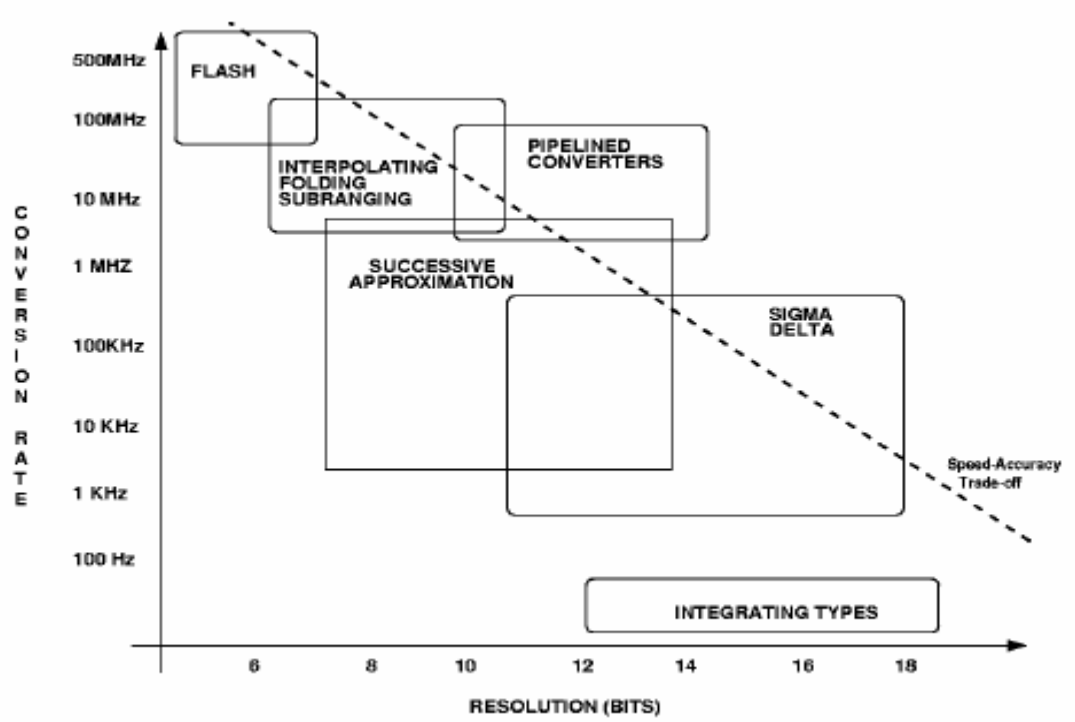


Fig. from ref.[2]

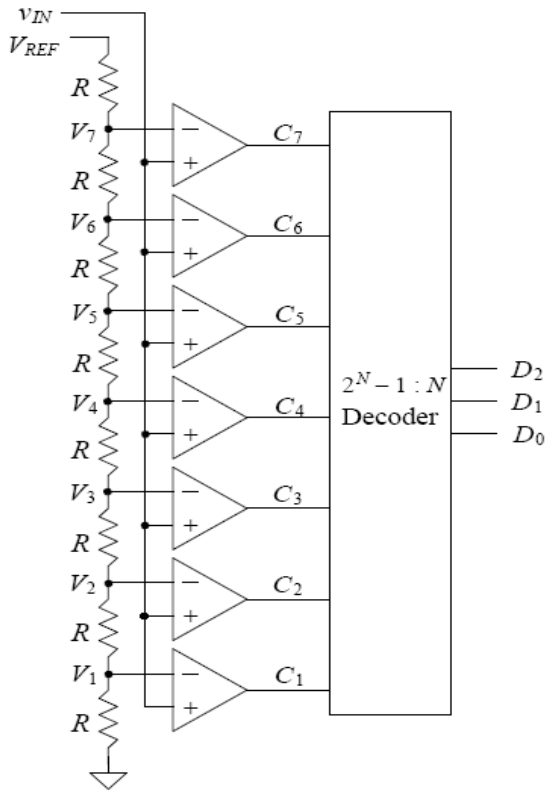
Various FOMs

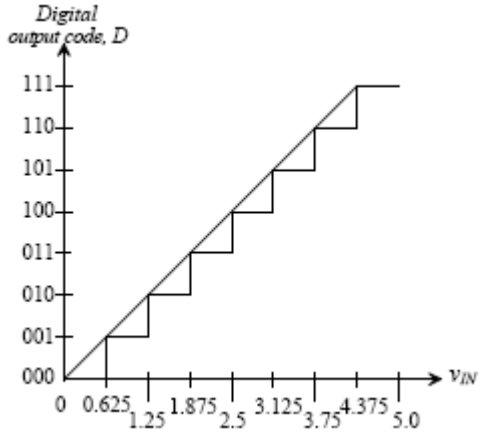
$$FOM = \frac{2^N \, 2BW}{P}$$

Miscellaneous ADC

- Trade-offs between high conversion rate and high resolution
- Latency concerns
- Complexity of the CMOS circuitry

Flash ADC

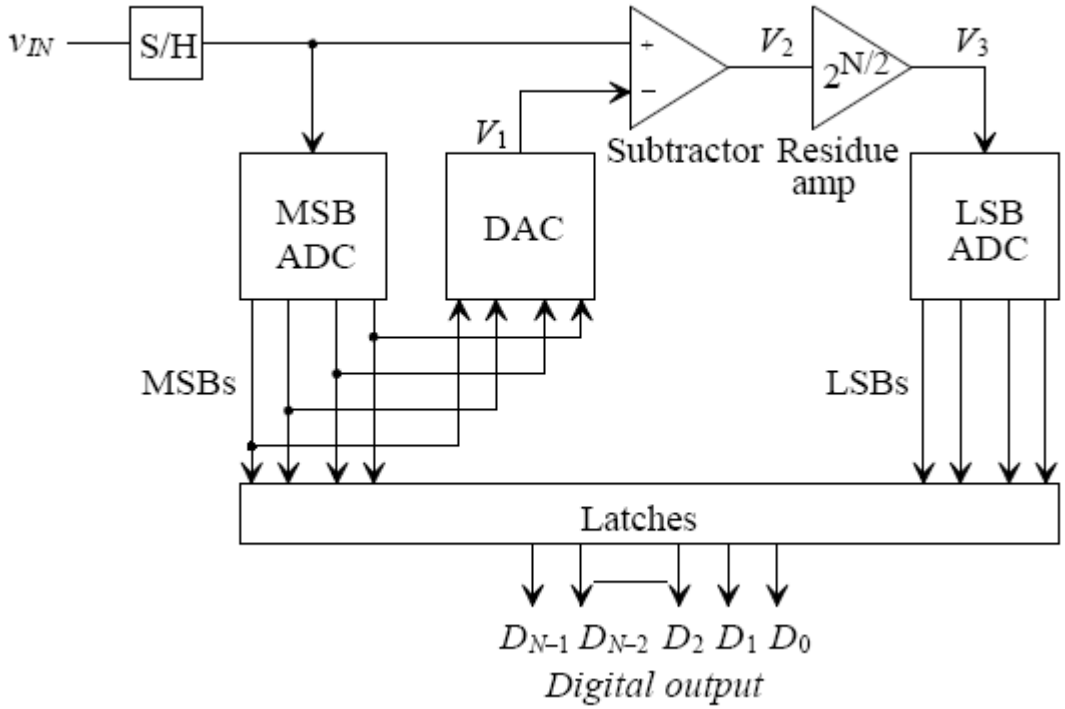




Undoubtedly the simplest ADC
Fastest conversion
Largest amount of Preamps and comparators

Figure from [1]

Subranging (or Two-step) ADC

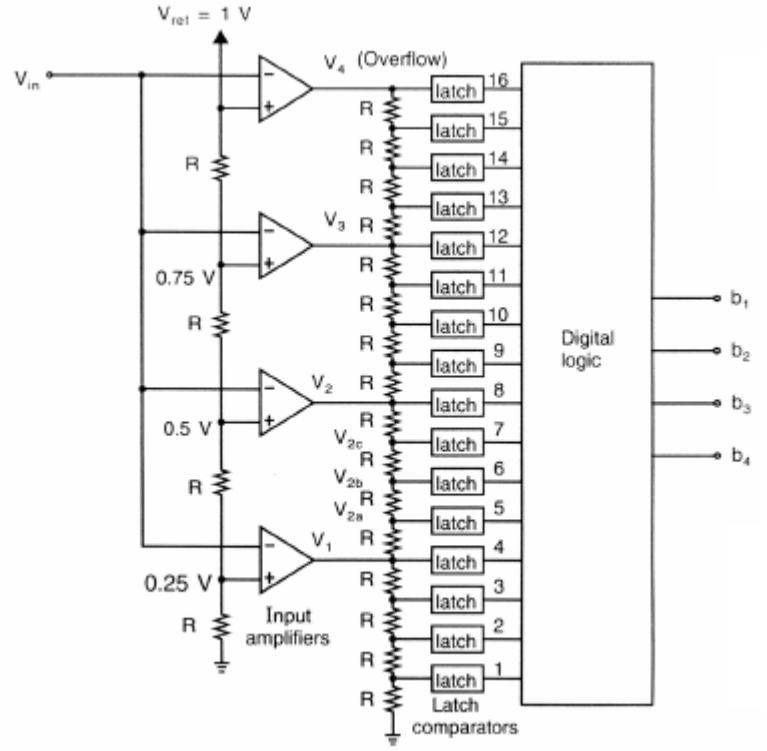


Less Comparators

2^N -> 2 $2^{N/2}$

Figure from [1]

Interpolating ADC



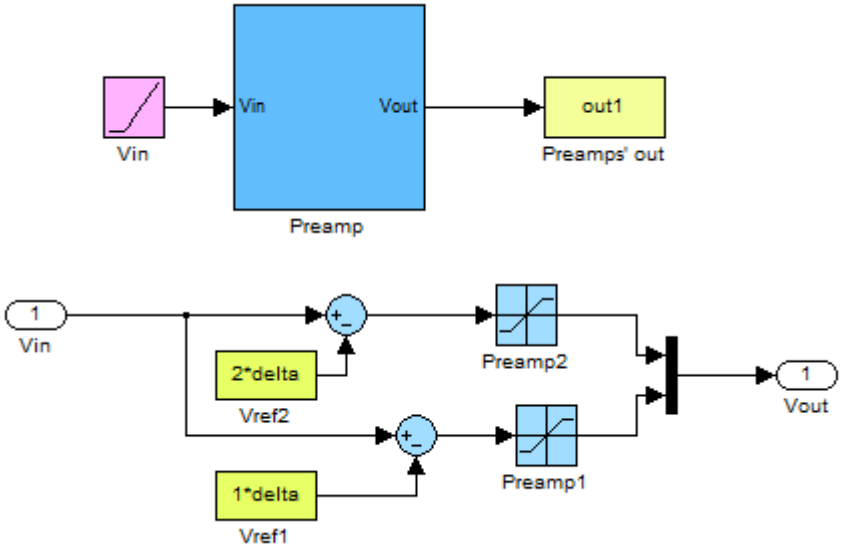
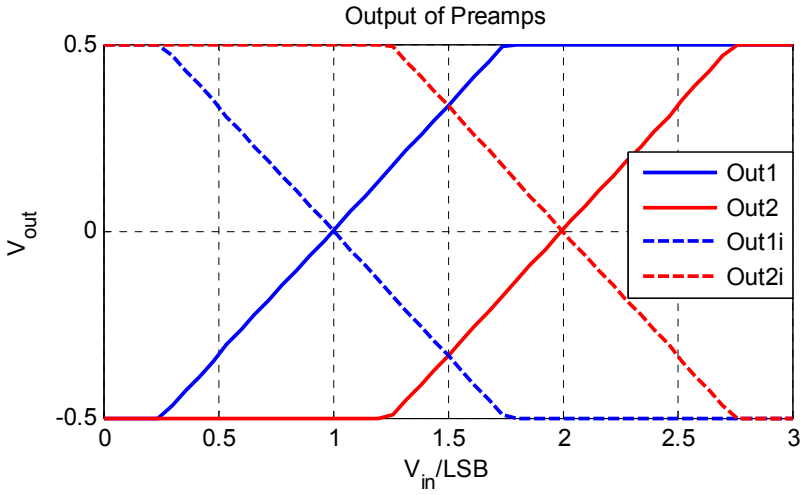
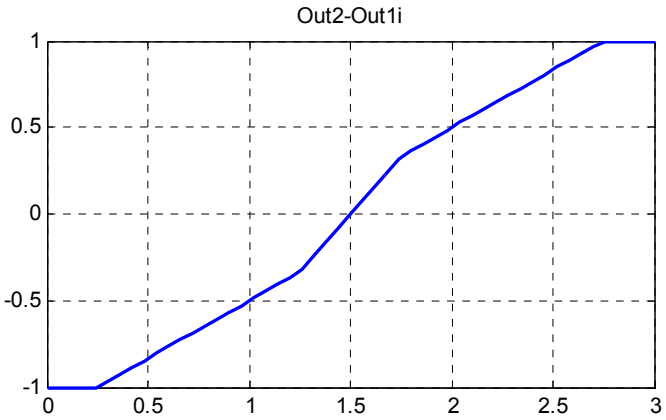
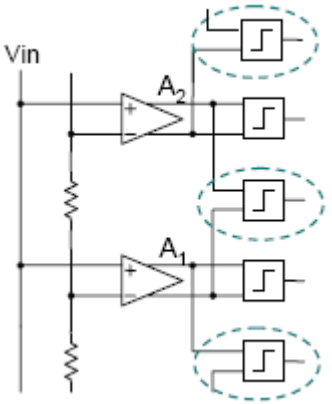


Figure from [4]

Interpolating ADC







Less Comparators
Same amount of Latches

Figure from [2]

Higher order resistive interpolation

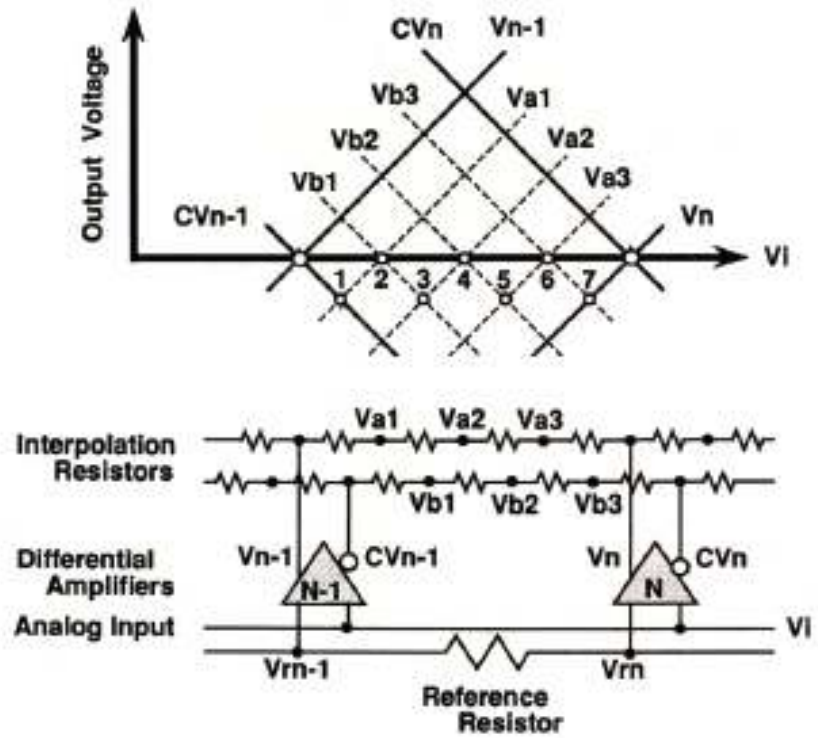
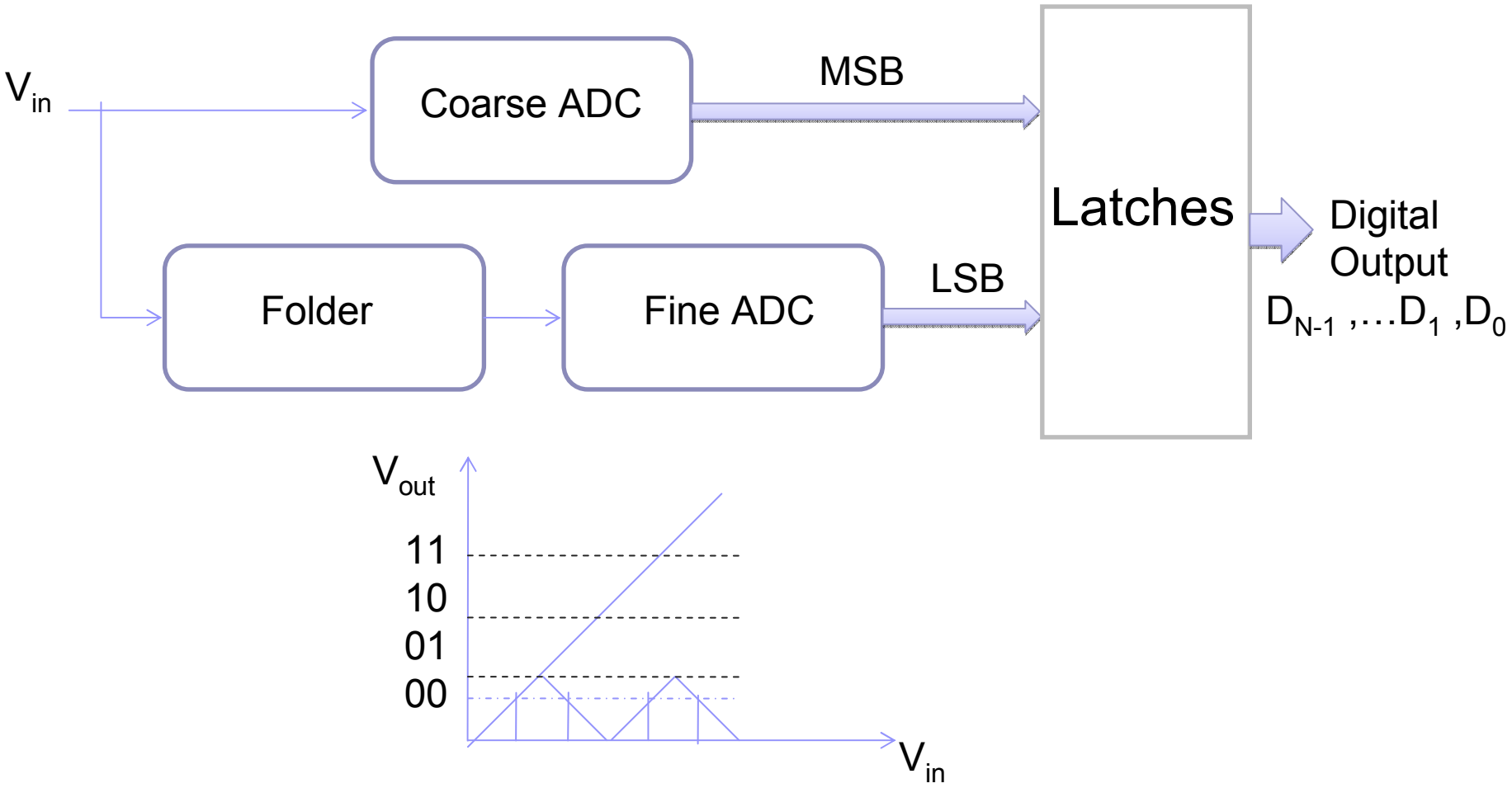
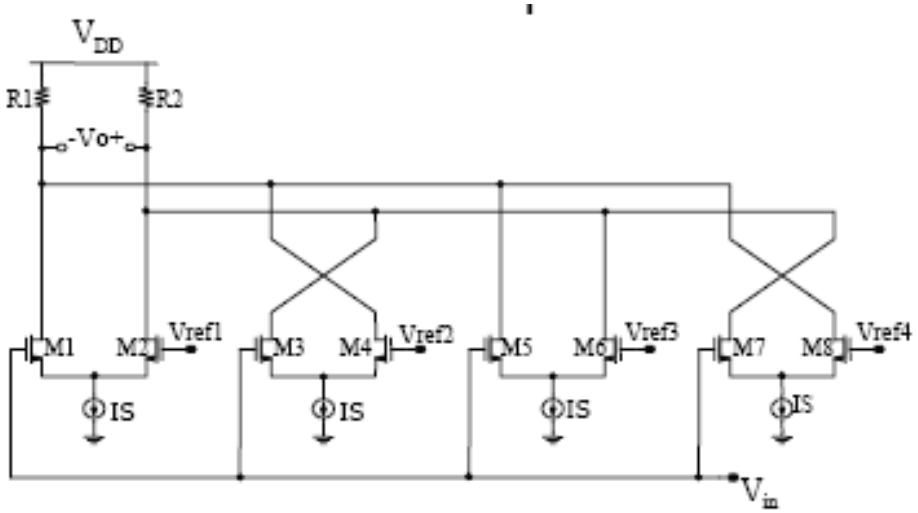


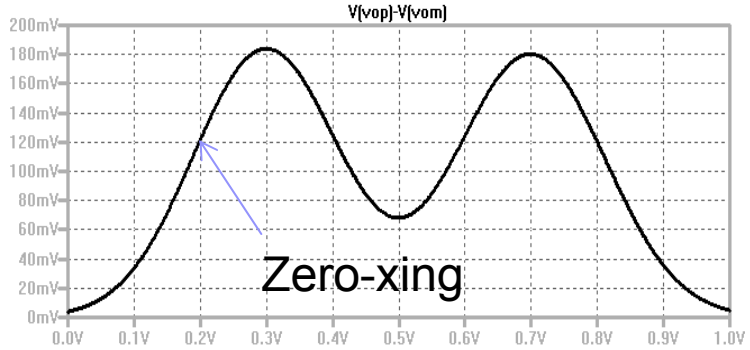
Figure from [5]

Transfer curves



Realization of Folds via Source-Couple Pairs





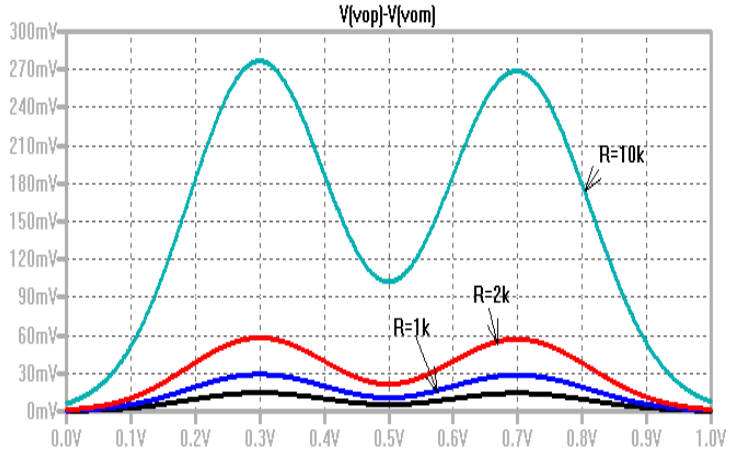
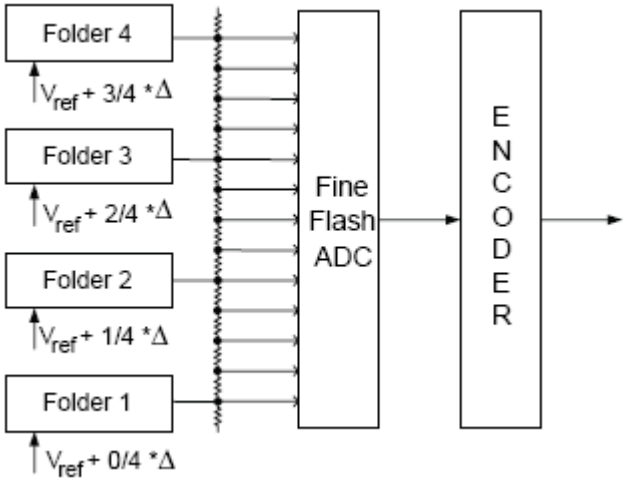


Figure from [2]

Folding & Interpolation



More practical, they are combined for application

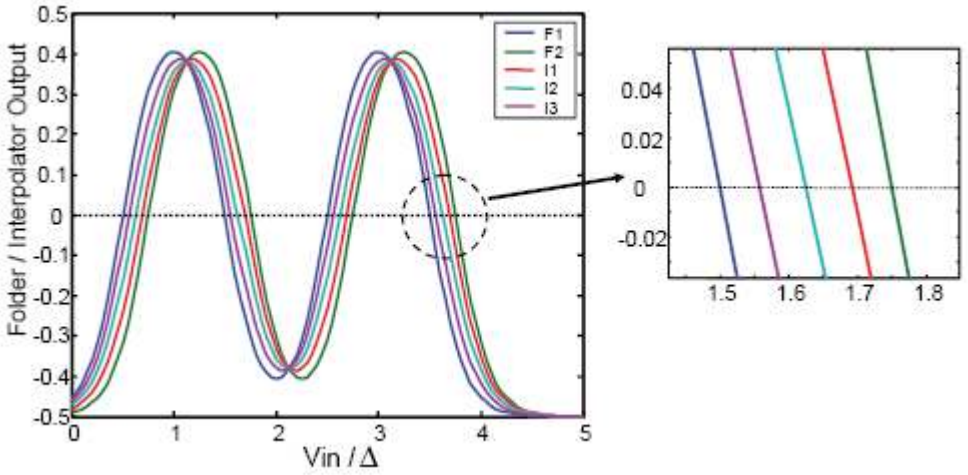
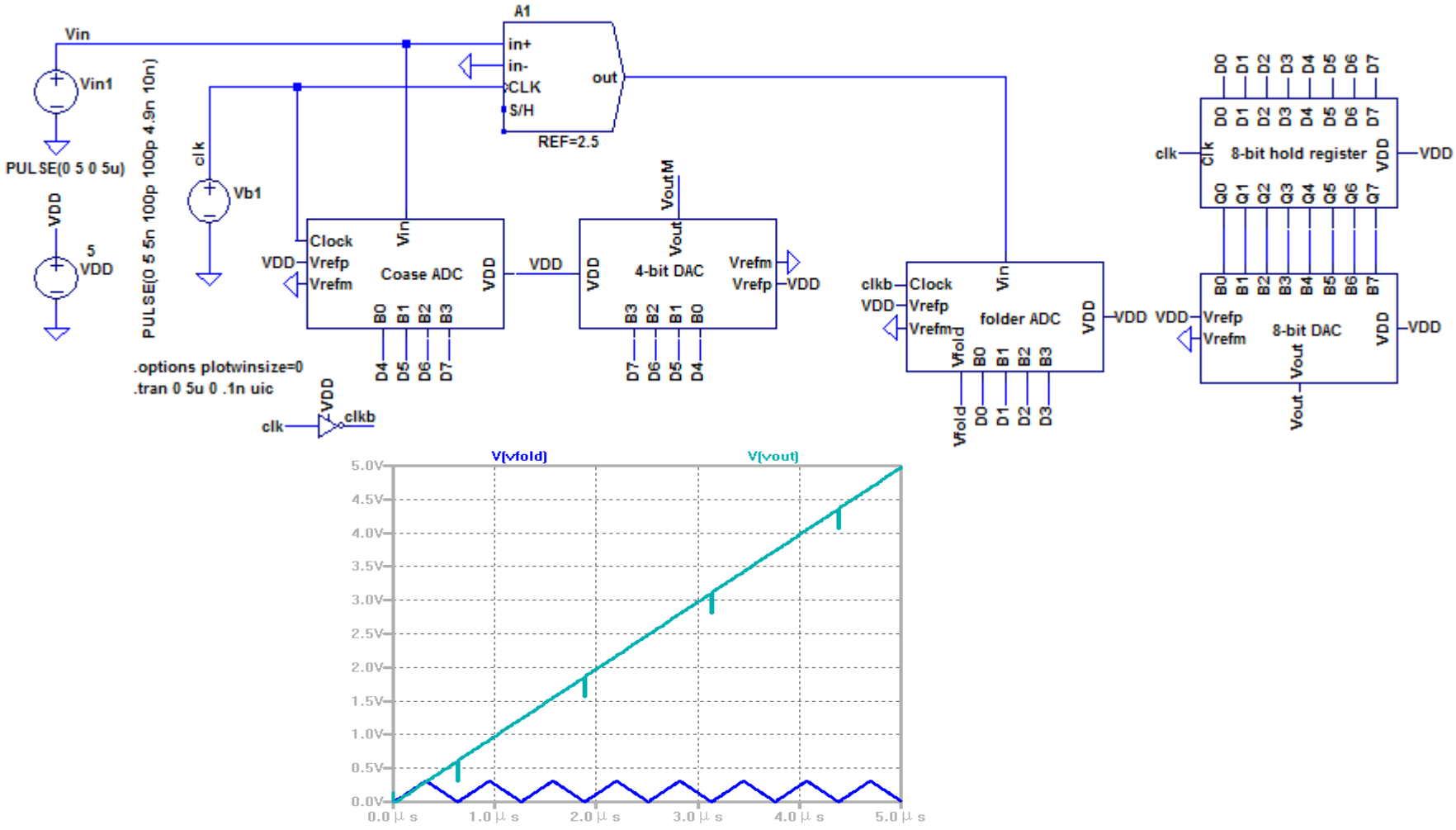


Figure from [2]

LTSpice Simulation



Conclusion

- Flash ADC, subranging (or two-step) ADC
- Interpolating and folding techniques
- Interpolating and folding ADC
- Simulation for illustration

References

- [1] R. J. Baker, CMOS Circuit Design, Layout, and Simulation, Revised Second Edition, Wiley-IEEE, 2008
- [2] http://webcast.berkeley.edu/EE 247
- [3] http://www.analog.com
- [4] Willy M.C. Sansen, Analog Design Essentials, Springer, 2006
- [5] H. Kimura et al, “A 10-b 300-MHz Interpolated-Parallel A/D Converter,” JSSC April 1993, pp.438-446

Questions