

# Tutorial presentation on Design of $\Sigma$ - $\Delta$ sensing circuits for multi-level resistive memory.

ECE 614 Advanced Analog IC Design

Spring 2008

Presented by Hemanth Ande

# Talk outline

- Delta Sigma Modulation Sensing
- DSM in Flash memory
- Resistive Memory (Types and concerns)
- Modeling Resistive memory in LT Spice
- Design development of Sensing circuit.
- Simulation Results of the DSM in Resistive Memory
- Multi Bit Sensing
- Conclusion

# Comparison of Traditional & Delta Sigma Sensing Analogy with water level.

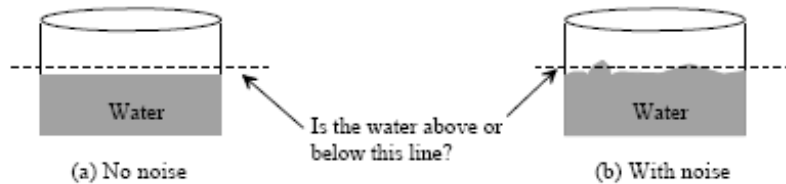


Figure from CMOSEDU.com  
**Traditional Sensing**

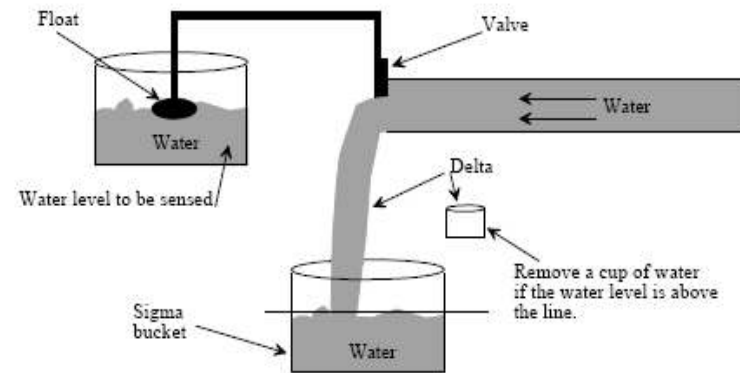


Figure from CMOSEDU.com  
**Delta Sigma Sensing**

# Example to illustrate DSM

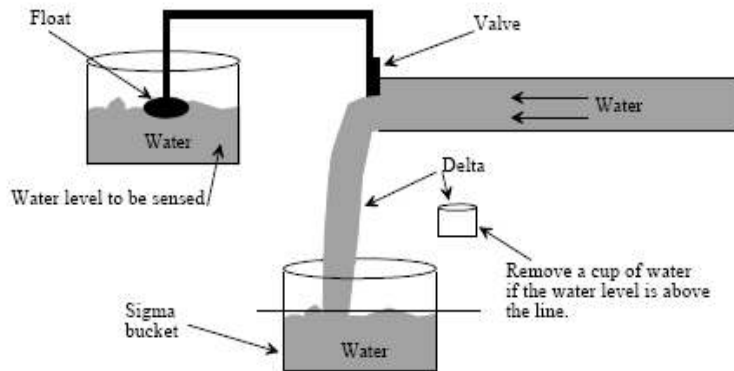
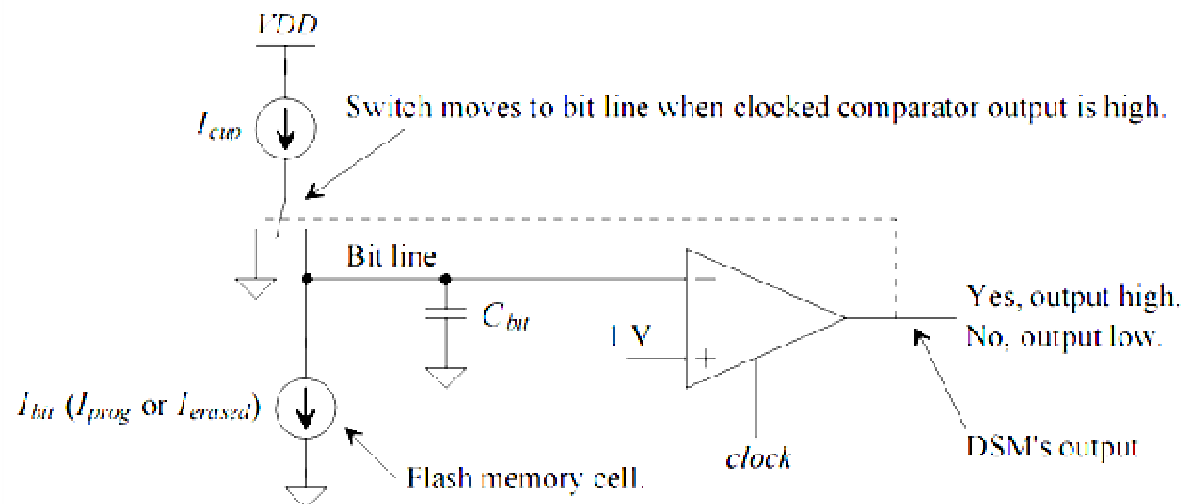


Figure from CMOSEDU.com

- Let Speed of water flowing in to the sigma bucket 1/4cup every 10sec
- Ref level of sigma bucket be 5 cups.
- Sensing at every 10sec.
- Can be found out from the table as we increase the sense time we reduce the error and the average gets close to the actual value = .25cups/10sec

Time	Water level in sigma bucket(cups)	Remove 1 cup if (water level > 5)	Running Avg
0	5		0
<b>10</b>	<b>5.25</b>	<b>1</b>	<b>1</b>
20	4.5	0	.5
30	4.75	0	.33
40	5	0	.25
<b>50</b>	<b>5.25</b>	<b>1</b>	<b>.4</b>
60	4.5	0	.33
70	4.75	0	.29
80	5	0	.25
<b>90</b>	<b>5.25</b>	<b>1</b>	<b>.33</b>
100	4.5	0	.3
110	4.75	0	.27
120	5	0	.25
<b>130</b>	<b>5.25</b>	<b>1</b>	<b>.31</b>
140	4.5	0	.29
150	4.75	0	.26
160	5	0	.25
<b>170</b>	<b>5.25</b>	<b>1</b>	<b>.29</b>
180	4.5	0	.28
190	4.75	0	.26
200	5	0	.25
<b>210</b>	<b>5.25</b>	<b>1</b>	<b>.28</b>

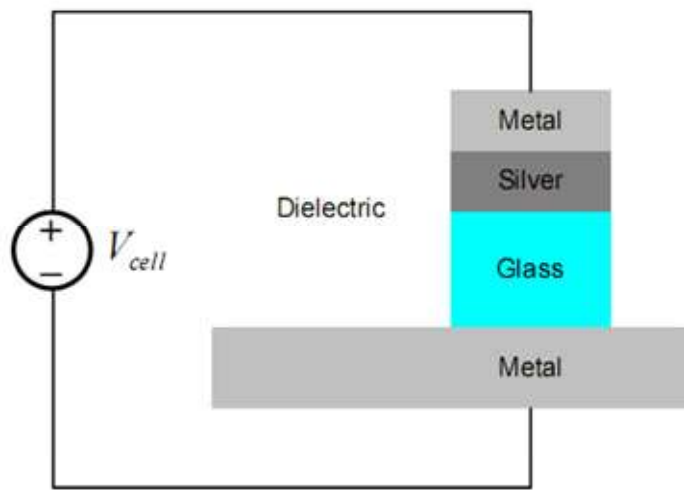
# DSM Sensing in Flash Memory



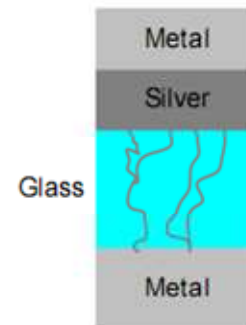
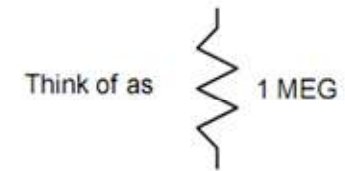
- Rate of charge removed from bit line in one clock cycle is  $I_{bit} = C_{bit} \frac{\Delta V_{bit}}{T}$
  - Amount of charge removed from bit line (which is supplied from  $I_{cup}$ )  $Q_{bit} = I_{bit} \cdot T = \Delta V_{bit} \cdot C_{bit}$
  - The rate we add charge to bitline  $Q_{bit} = I_{bit} \cdot T = Q_{cup} = I_{cup} \frac{M}{N} \cdot T$
- $$\frac{I_{bit}}{I_{cup}} = \frac{M}{N}$$

# Resistive Memory

## Programmable Resistance RAM (PRRAM)



### Erased cell



### Programmed cell

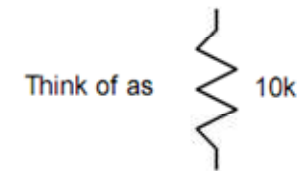
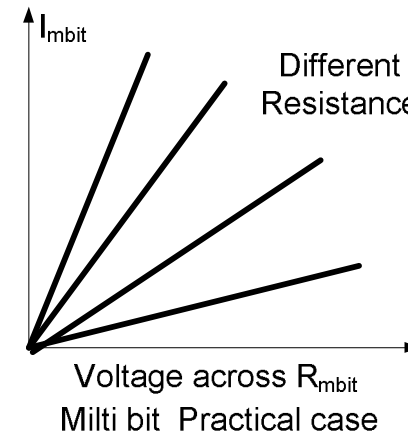
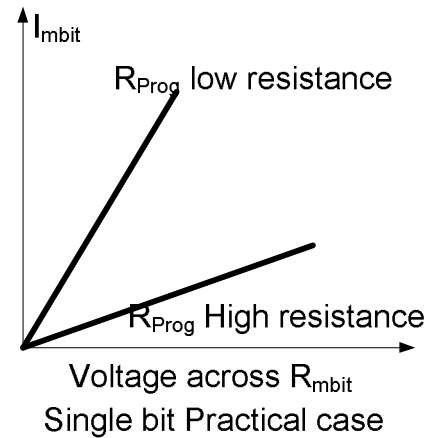
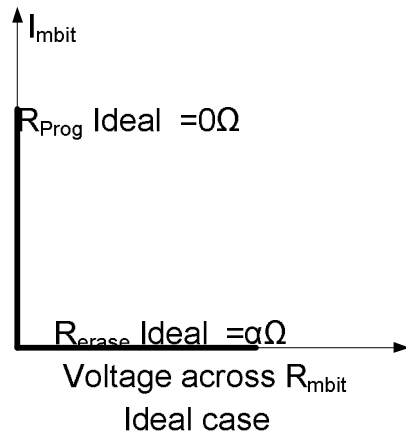
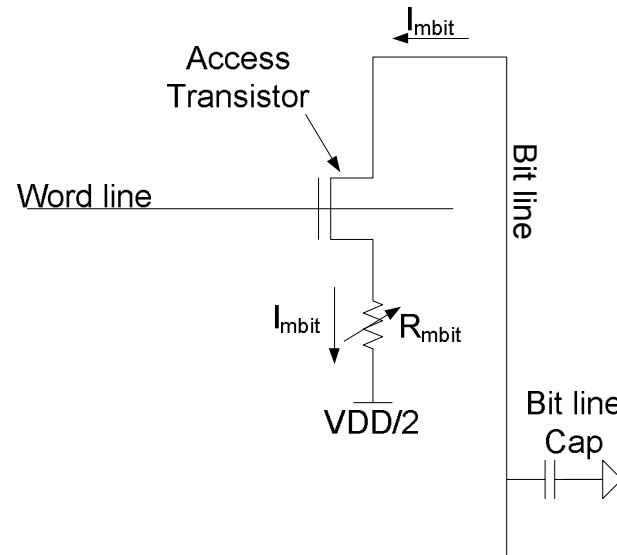
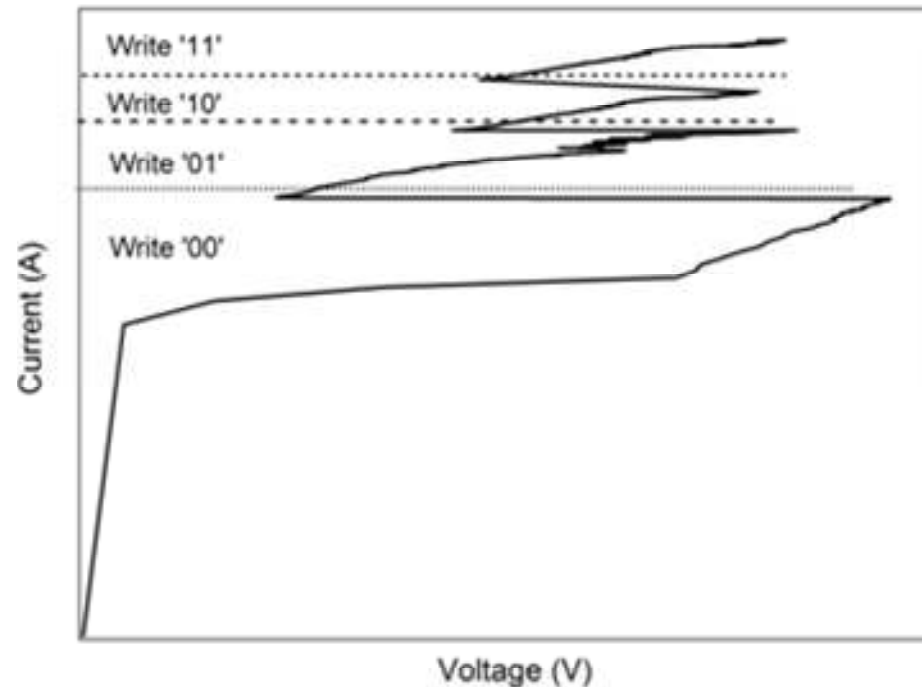
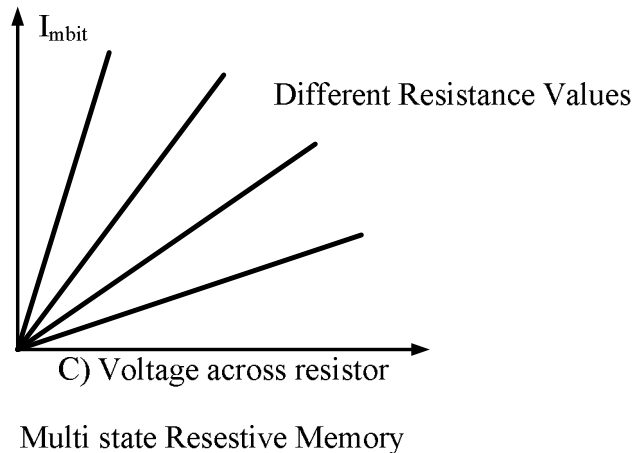


Figure from CMOSEDU.com

# Resistive Memory



# Problem with Phase change memory

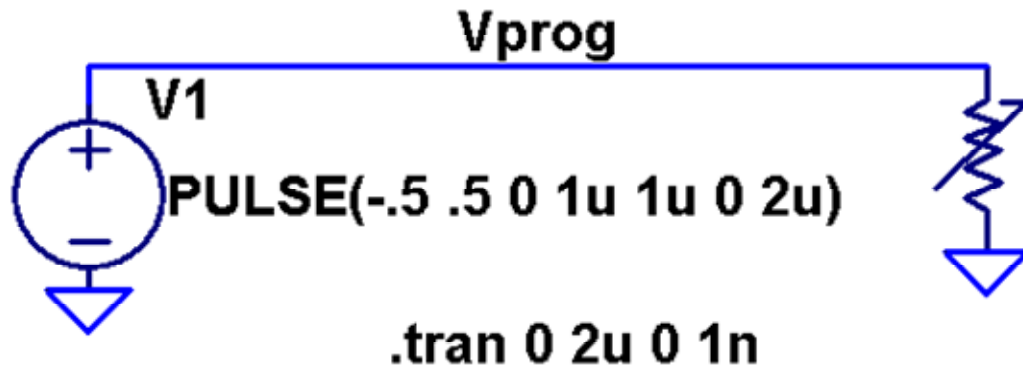


K.A Campbell and C.M. Anderson, "Phase-Change Memory Devices with Stacked Ge-Chalcogenide/Sn-Chalcogenide Layers",

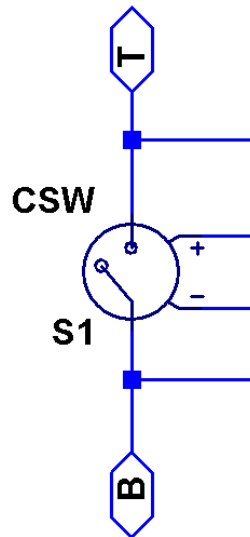
## Problems

- Not Ideal as shown
- Sensing is challenging
- Programming the Multi bit becomes more challenging

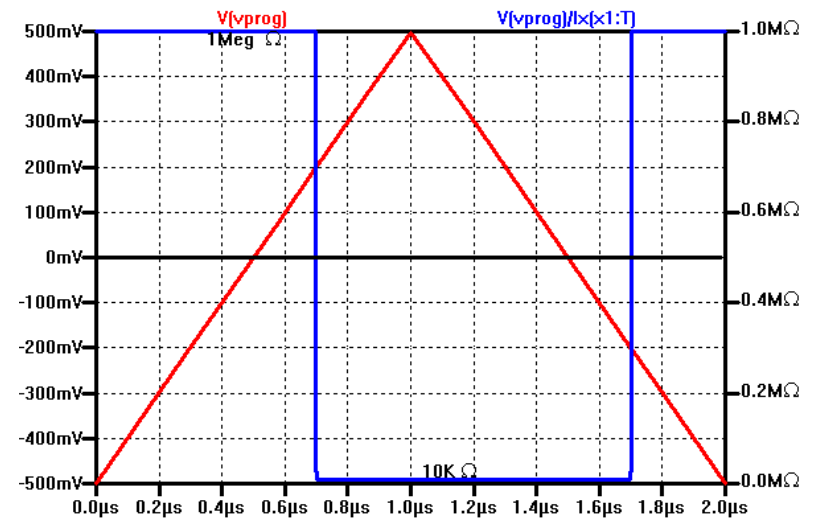
# Modeling Resistive memory



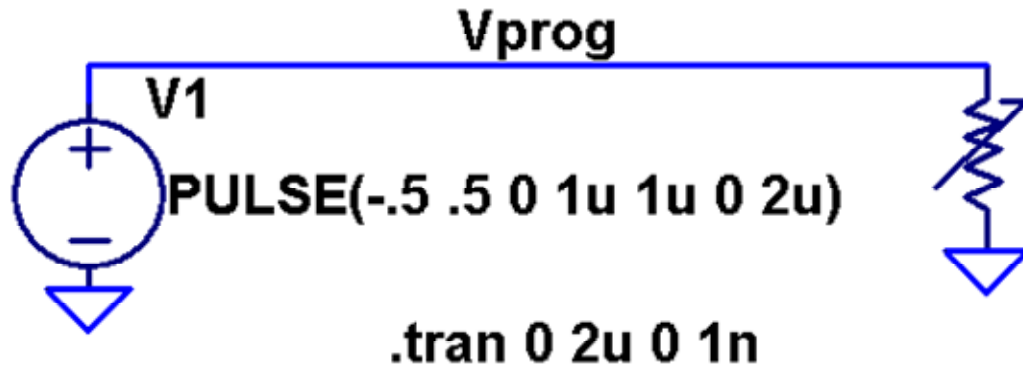
.tran 0 2u 0 1n



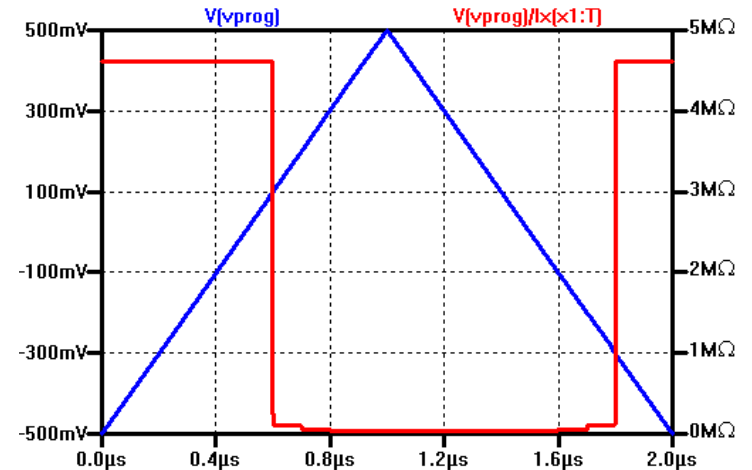
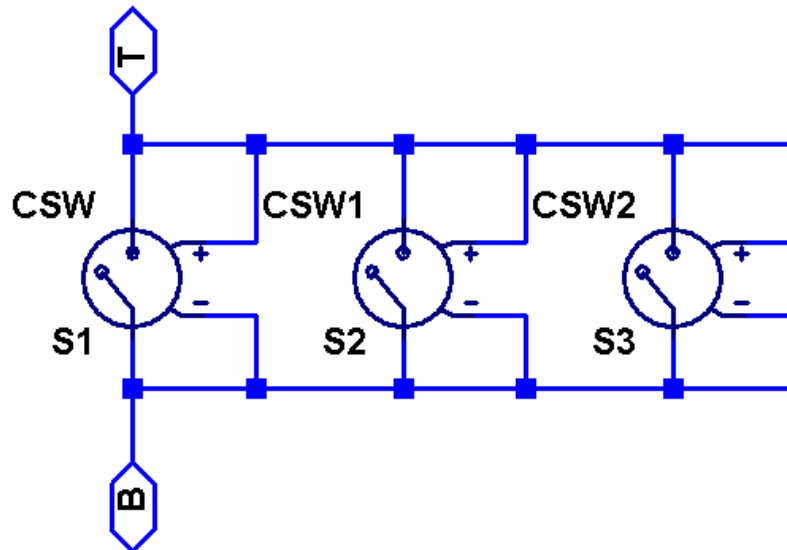
.model CSW SW(Ron=10k Roff=1Meg Vt=0 Vh=.2)



# Modeling Multi bit Resistive memory



.tran 0 2u 0 1n



```
.model CSW SW(Ron=100k Roff=10Meg Vt=0 Vh=.1)
.model CSW1 SW(Ron=100k Roff=15Meg Vt=0 Vh=.2)
.model CSW2 SW(Ron=100k Roff=20Meg Vt=0 Vh=.3)
```

# Programming single bit Phase Change Memory

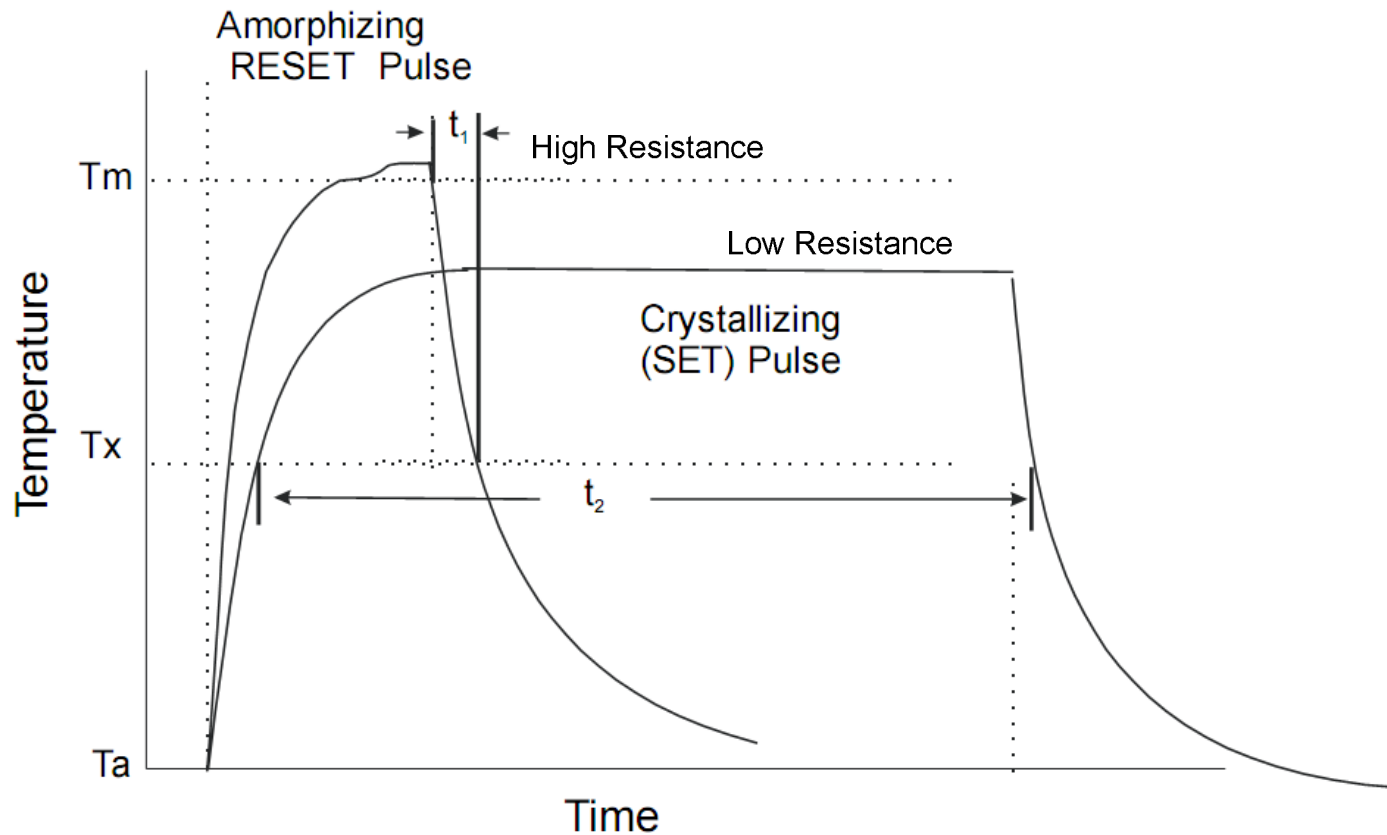
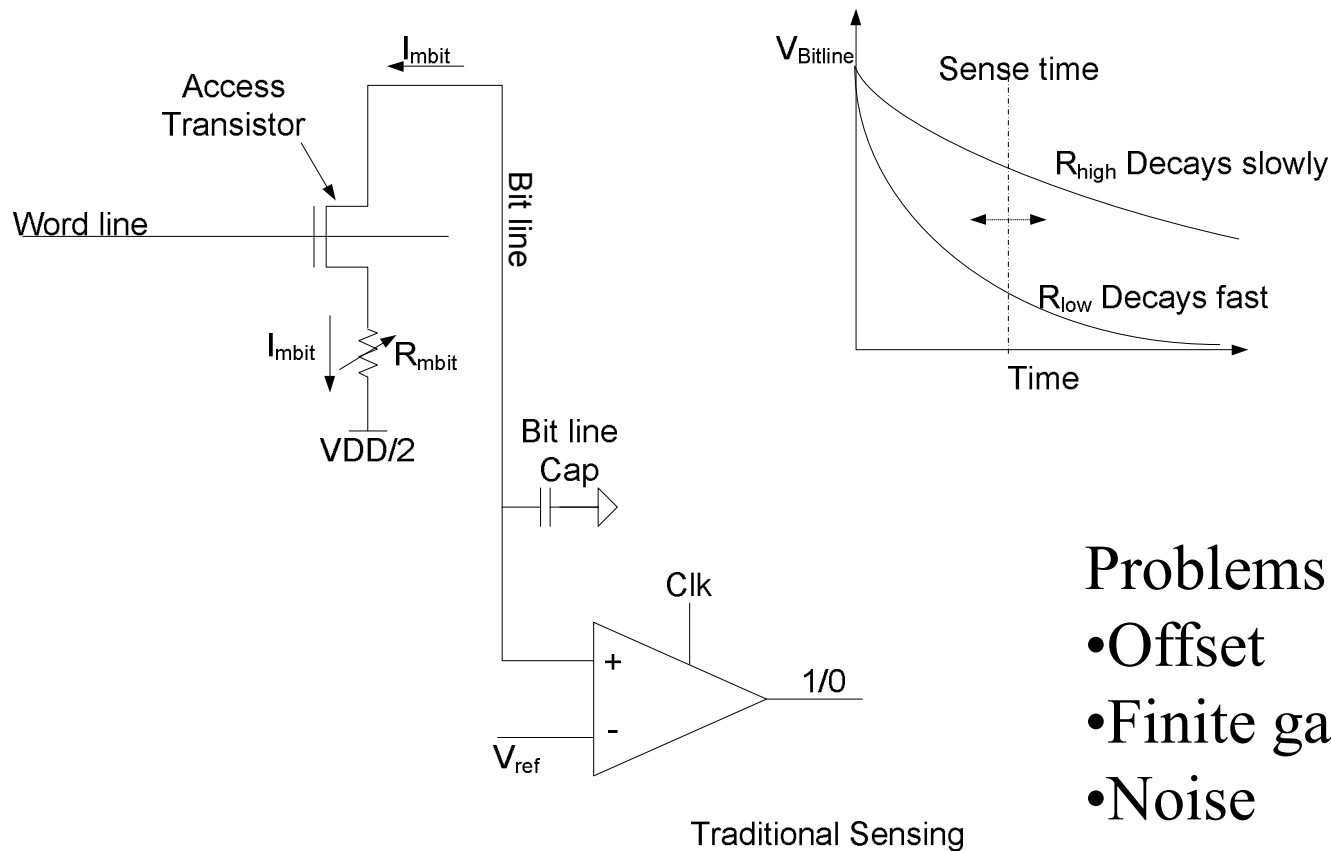


Figure from Ovonyx, Inc.

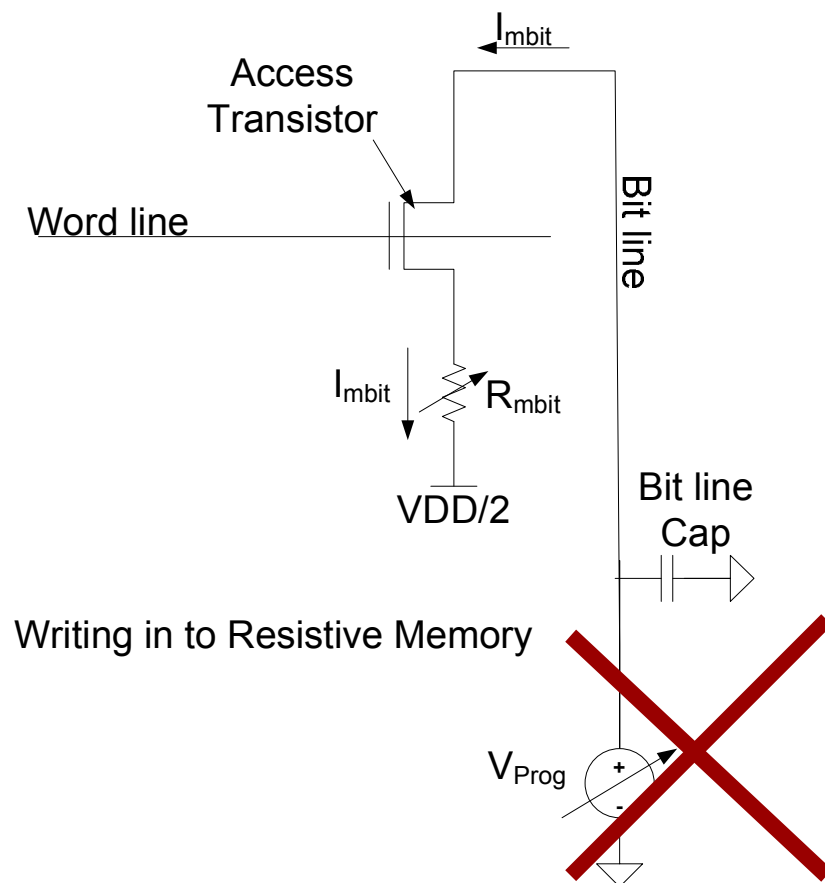
# Concept of Sensing Resistive Memory



## Problems

- Offset
- Finite gain Error
- Noise
- Timing control & sensing

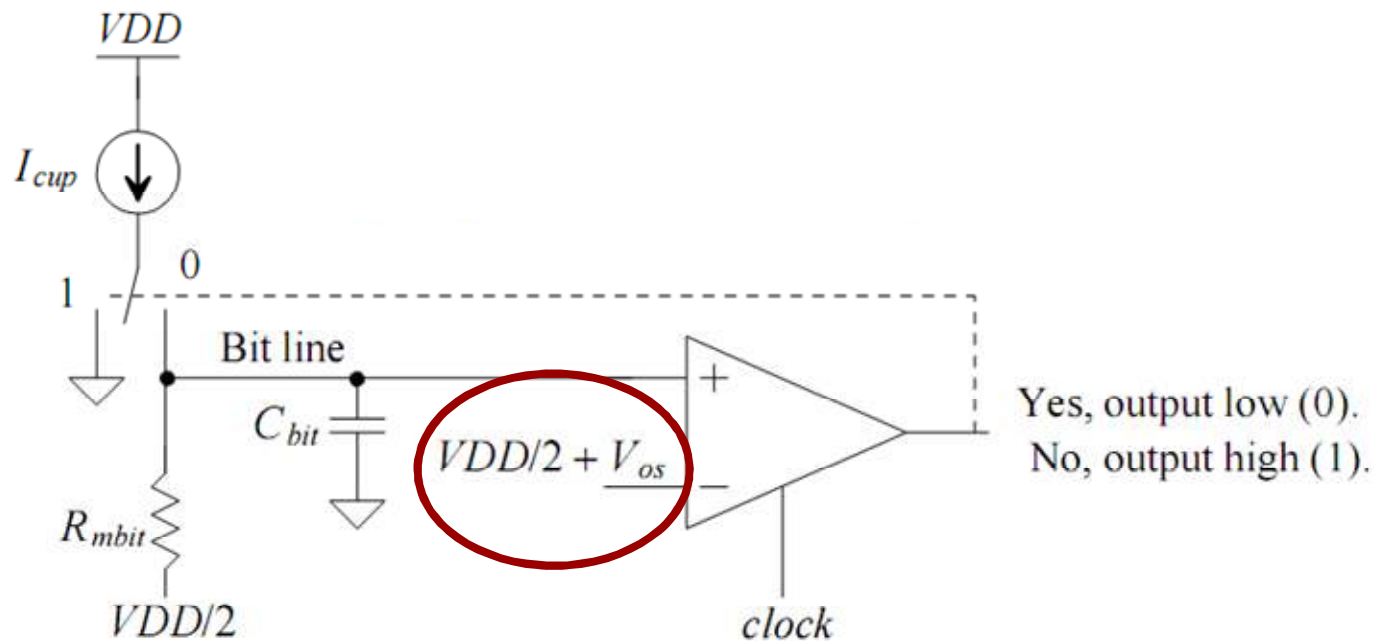
# Programming



## Problems

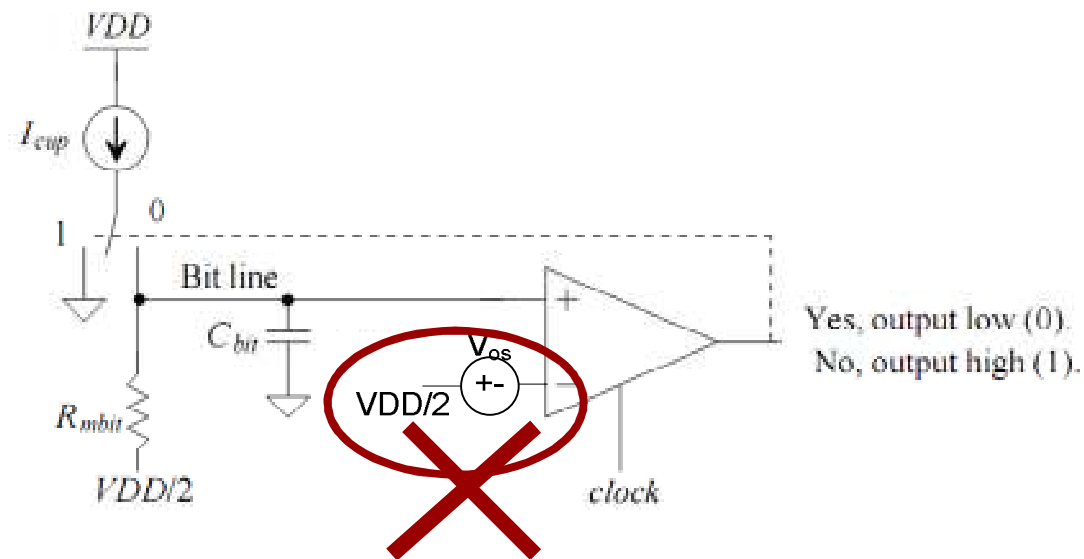
- Voltage Varies
- Process Variation
- Temperature Variation
- Noise on Word line
- Mosfet resistance comparable with  $R_{mbit}$
- Cannot Write in to Multi bit resistive memory

# DSM Sensing topologies



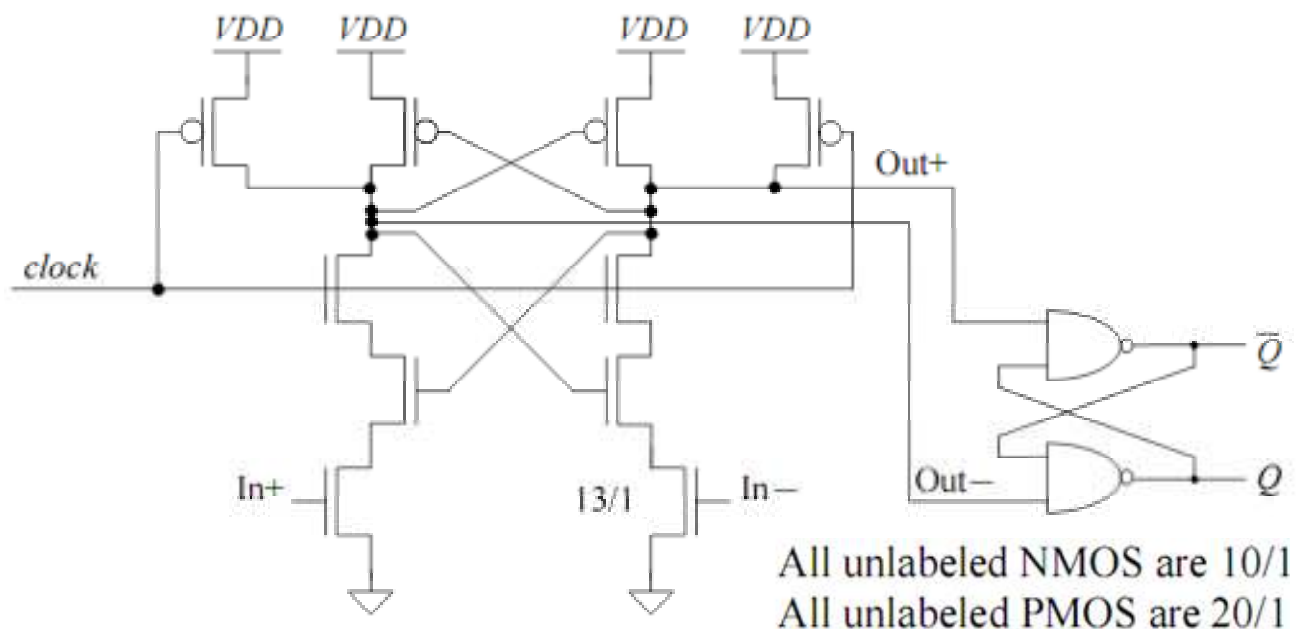
- Forcing the Current
- Holding Voltage at  $V_{ref} + V_{os}$

# DSM Sensing topologies



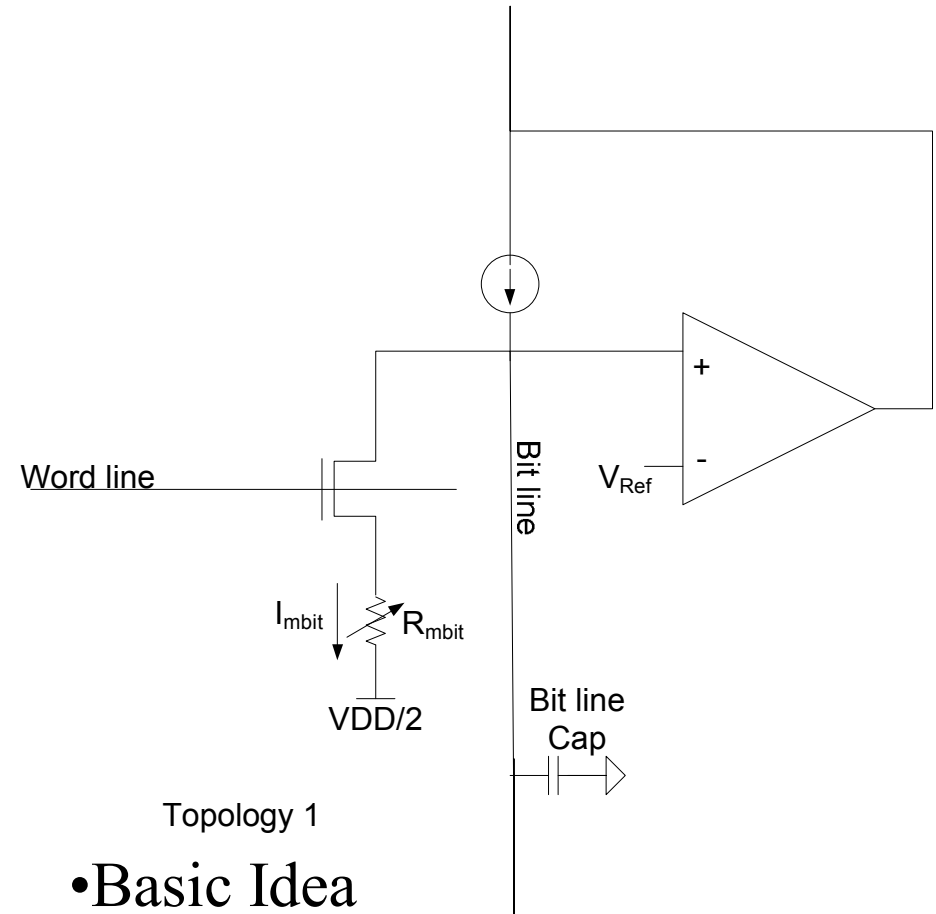
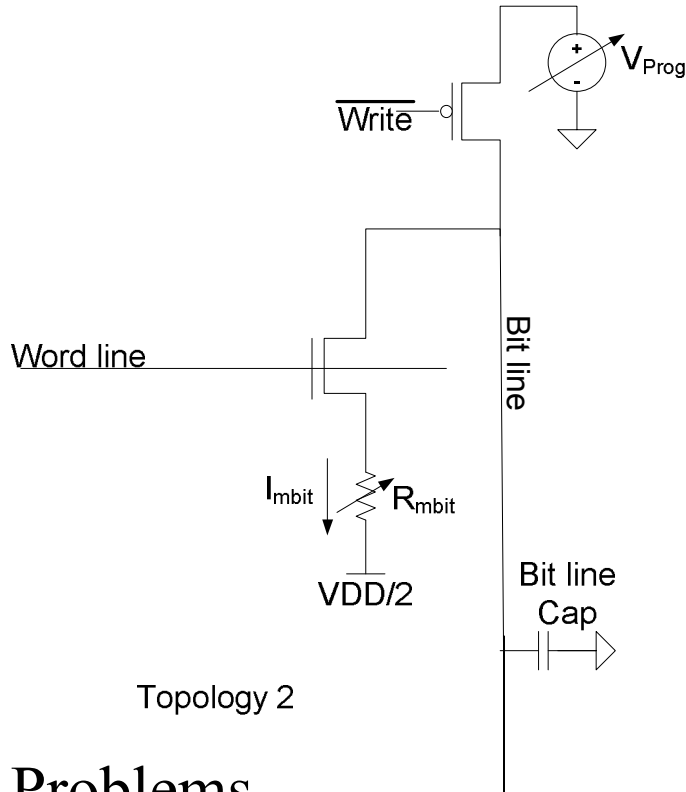
- Forcing the Current
- Holding Voltage at  $V_{ref} + V_{os}$

## Creating an offset



- Creating offset by mismatching one side of the comparator
- Very crucial to design this offset with so many variations affecting the operation (temp, process, vdd)
- Design tip: need to use some killer offset to ensure for all process run we have +offset in the direction we think.

# Writing



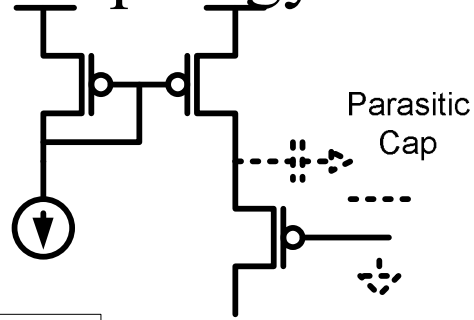
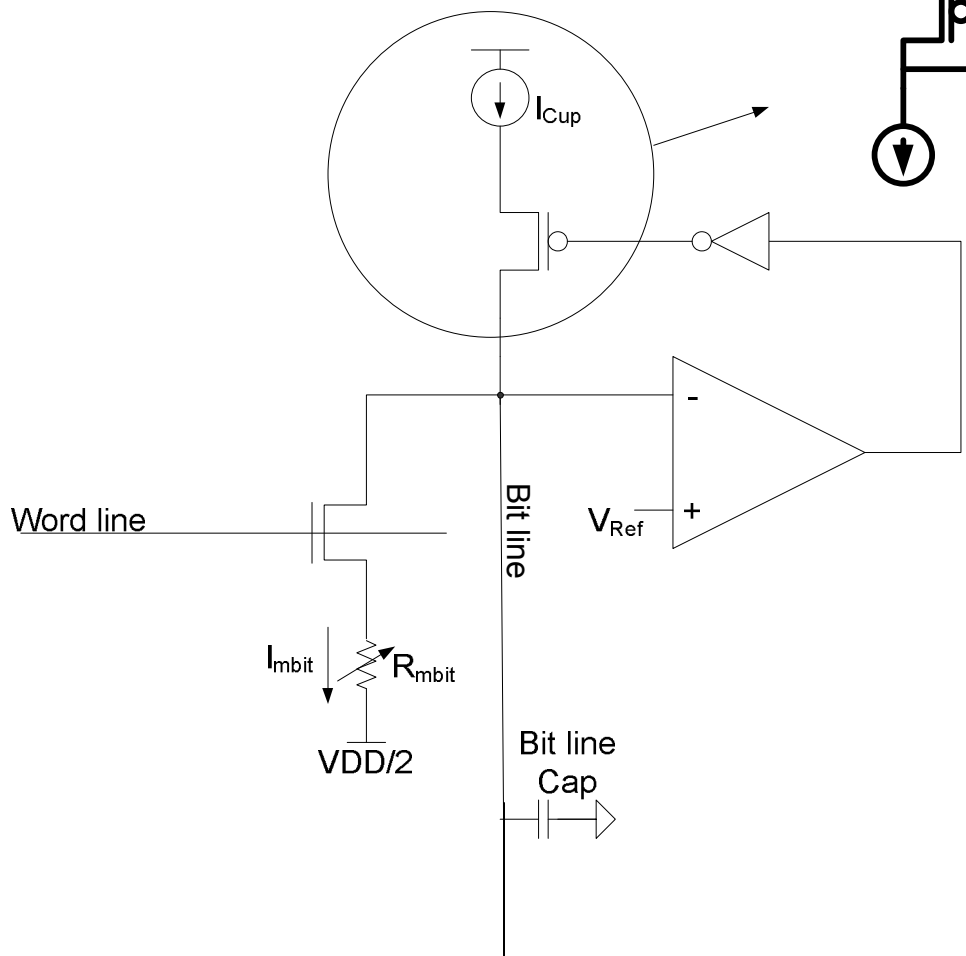
## Problems

- 2 transistors Layout concern
- Noise on wordline
- Problem with controlling

## • Basic Idea

- forcing current, and holding bit line voltage at  $V_{ref}$

# Design topology

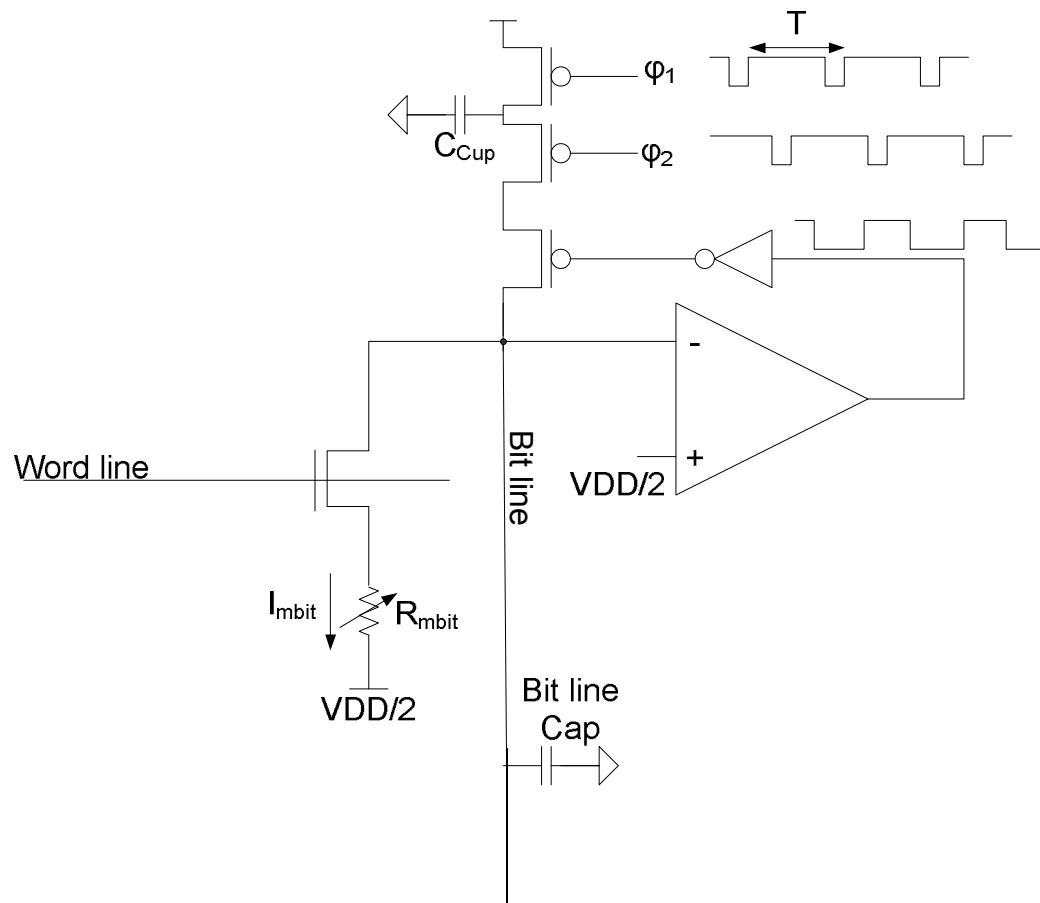


Does not change current (even bit line changes)

Cannot clock this circuit at high frequencies

- Chance of changing data
- Fundamental problem is due to the parasitic capacitance
- Doesn't start instantly PMOS has to go to saturation (takes time)
- False sensing giving rise to error

# Design topology

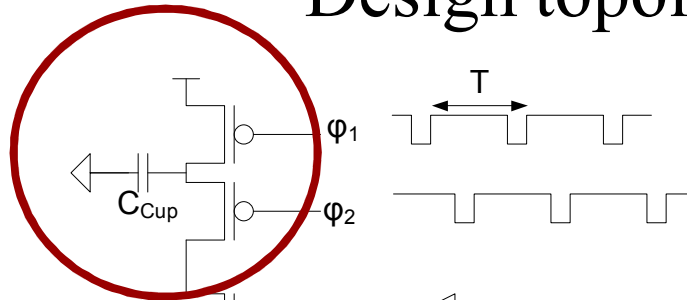


$$Q_{cup} = C_{cup} VDD$$

$$Q_{cup} = C_{cup} (VDD - V_{bit})$$

# Design topology

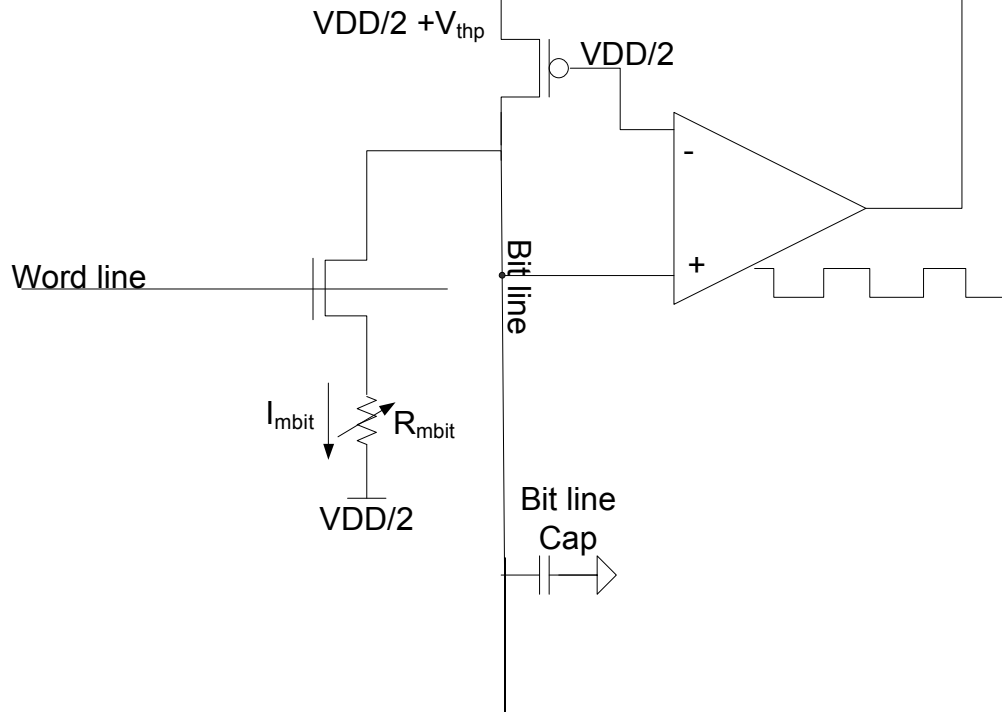
$$Q_{cup} = C_{cup} (VDD - V_{ref} - V_{Thp})$$



$$I_{Mbit} = \frac{V_{os}}{R_{Mbit}} = Q_{cup} \frac{M}{N} \frac{1}{T}$$

$$= (VDD - VDD/2 - V_{THP}) \cdot C_{cup} \frac{M}{N} \frac{1}{T}$$

$$R_{Mbit} = \frac{V_{os} \cdot T}{(VDD - VDD/2 - V_{THP}) \cdot C_{cup} \frac{M}{N}}$$



$$VDD = 1v$$

$$V_{os} = 50mv$$

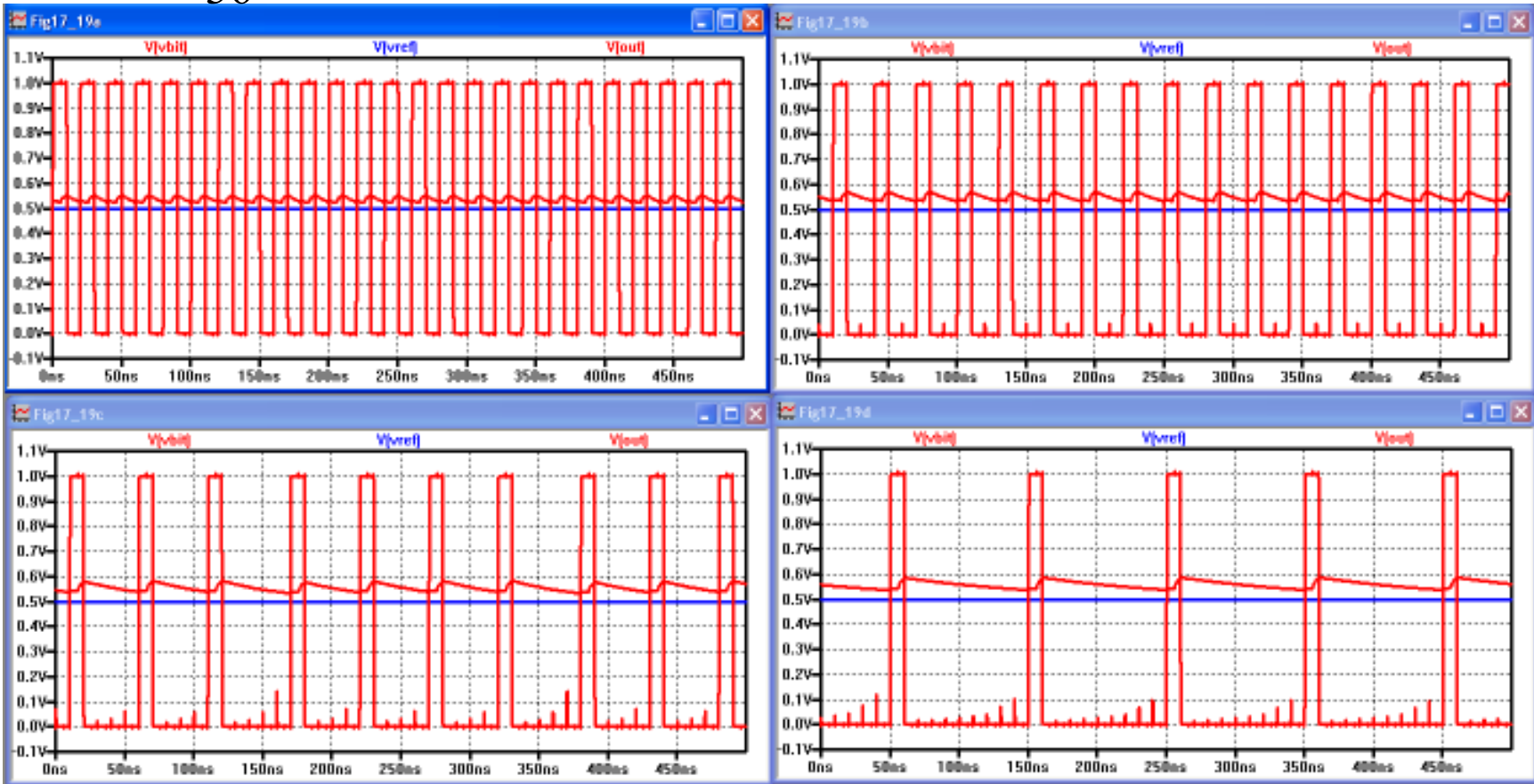
$$V_{THP} = 280mv$$

$$C_{cup} = 100fF$$

$$R_{Mbit} \approx 25K \cdot \frac{N}{M}$$

$$R_{Mbit} = 25k \cdot \frac{50}{36} = 35k (\text{actual Value } 25K)$$

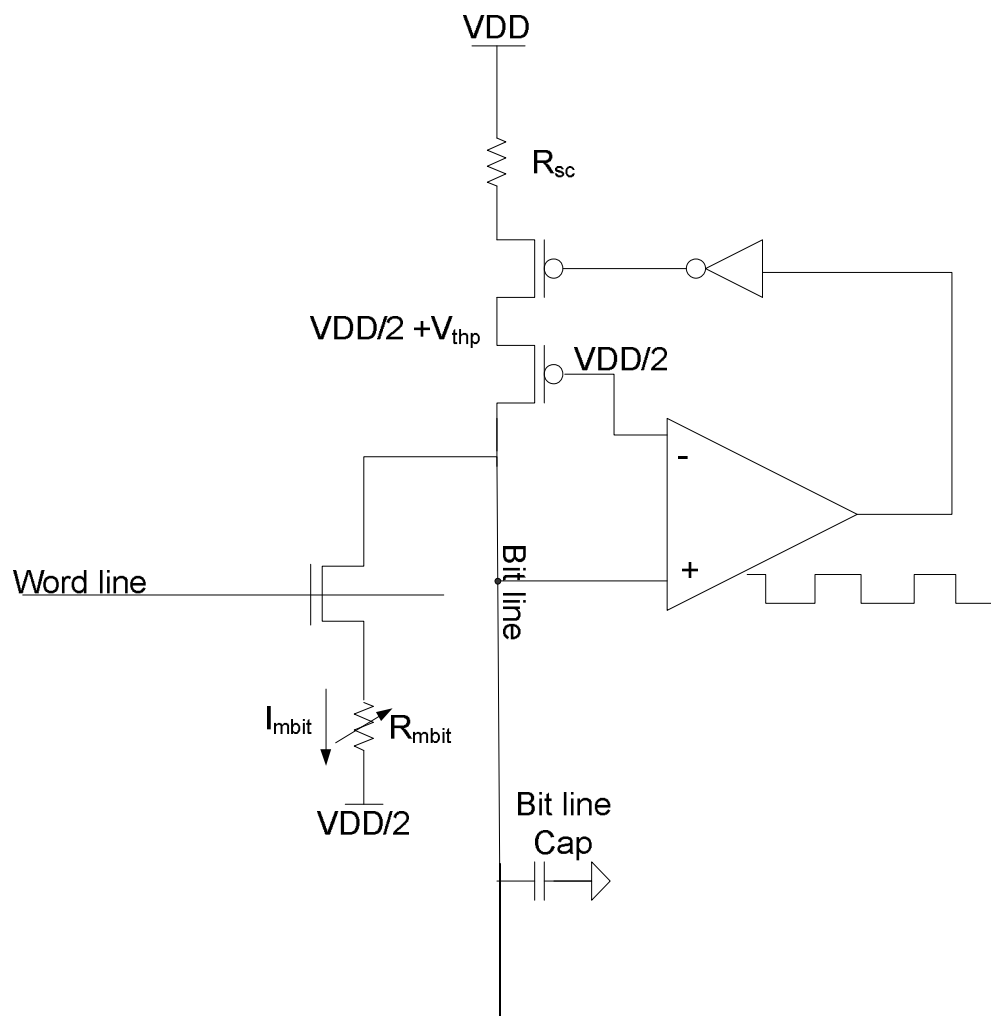
$$R_{Mbit} = 25k \cdot \frac{50}{17} = 73k (\text{actual Value } 50K)$$



$$R_{Mbit} = 25k \cdot \frac{50}{10} = 125k (\text{actual Value } 100K)$$

$$R_{Mbit} = 25k \cdot \frac{50}{6} = 208k (\text{actual Value } 200K)$$

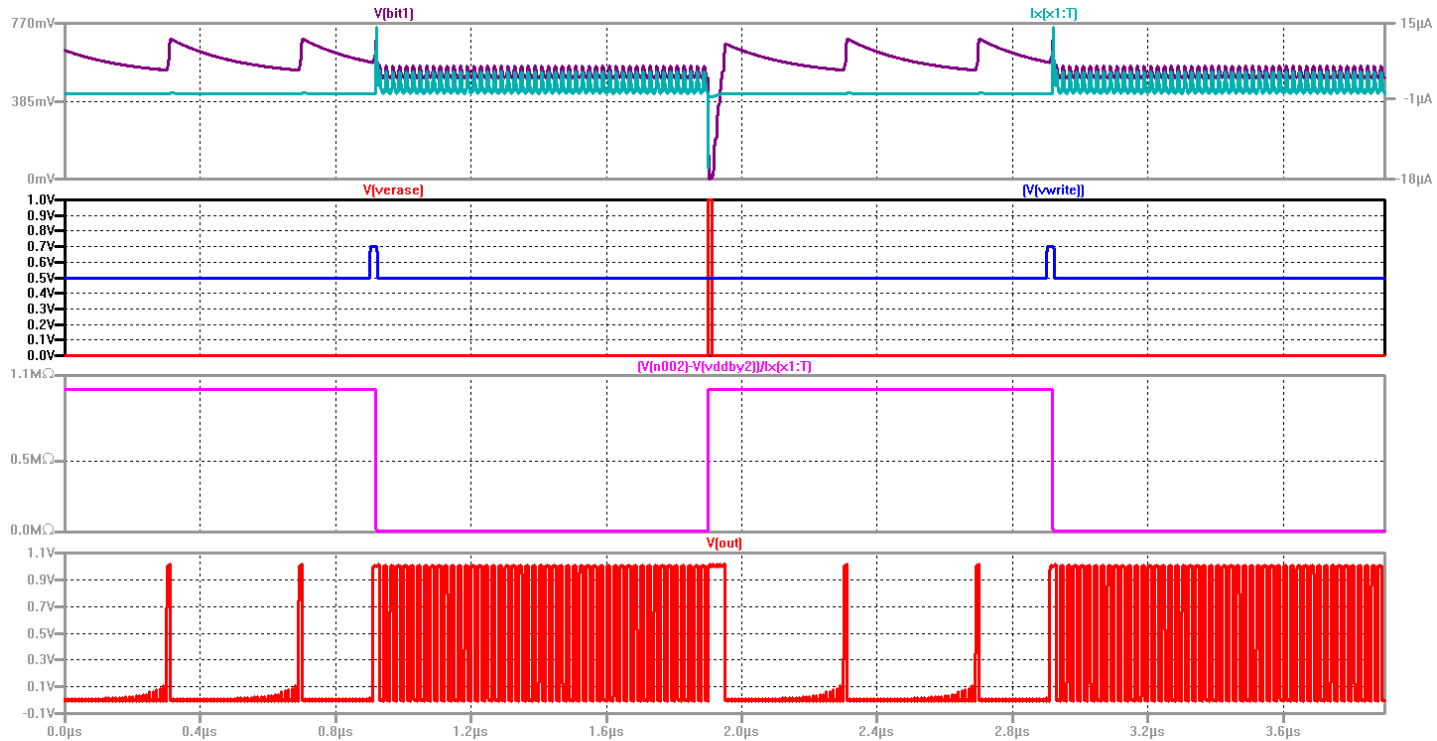
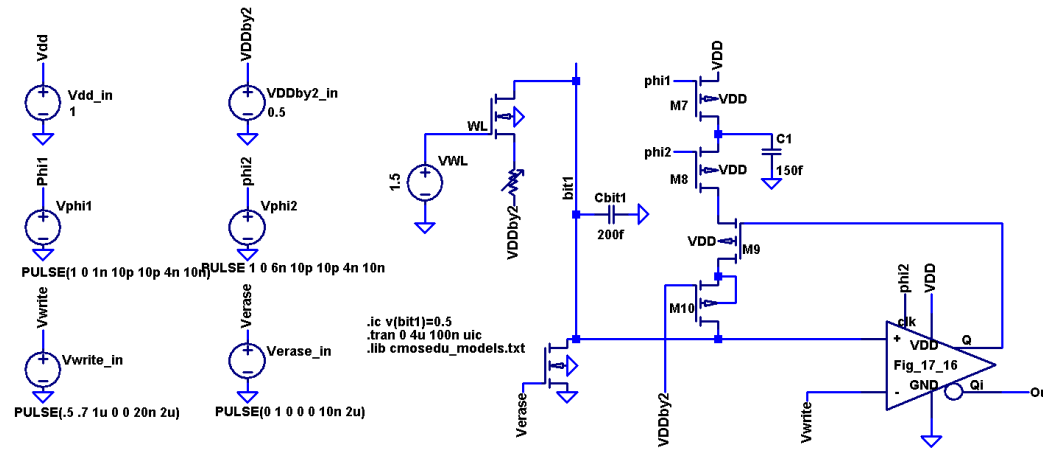
# Design topology



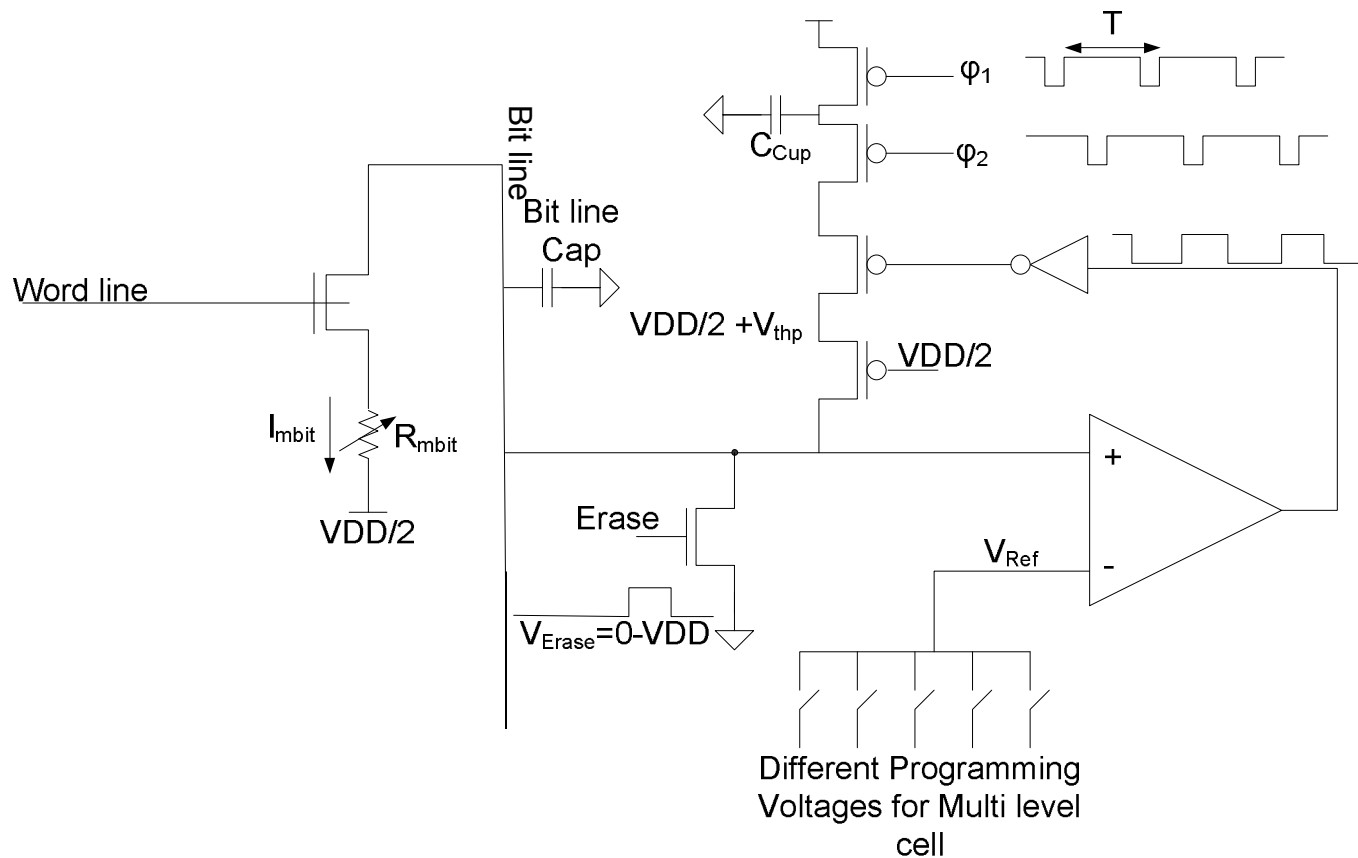
- Simple Design
- Can use 4 of the same NMOS in parallel to get the same process resistance
- Cannot be modified
- No control on the resistance
- Multi bit sensing becomes tough.



# Simulation Result



# Multi Bit Sensing and Programming.



# Conclusion

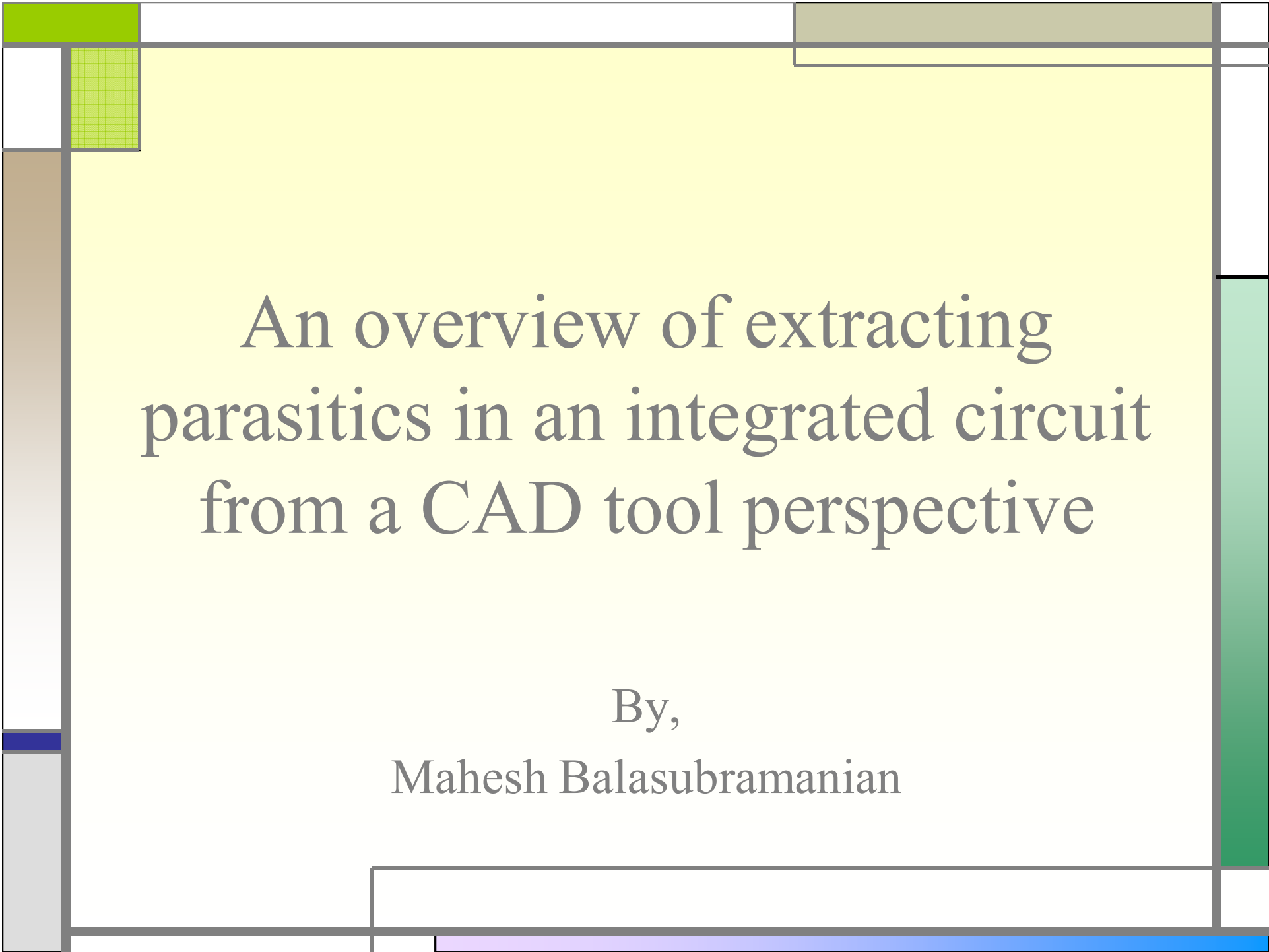
- Brief discussion about Resistive Memory Sensing and Programming
- Modeling Resistive memory in LT Spice
- Problems with various topologies
- Design & development of multi bit DSM sensing scheme for Resistive memory

# References

- [1] R. J. Baker, *CMOS Circuit Design, Layout, and Simulation, Revised Second Edition*, Wiley-IEEE, 2008.
- [2] K.A Campbell and C.M. Anderson, “Phase-Change Memory Devices with Stacked Ge-Chalcogenide/Sn-Chalcogenide Layers”, *Microelectronics Journal* **38** (2007), pp. 52-59.
- [3] <http://ovonyx.com/technology/>
- [4] H. K. Ande, P. Busa, M. Balasubramanian, K. A. Campbell, and R. J. Baker “*A New Approach to the Design, Fabrication, and Testing of Chalcogenide-Based Multi-state Phase-Change Nonvolatile Memory*” submitted for publication

# Questions ?





# An overview of extracting parasitics in an integrated circuit from a CAD tool perspective

By,  
Mahesh Balasubramanian

# Outline

- Need for Layout Parasitic Extraction (LPE).
- Parasitics to be addressed
  - ✓ Proper representation of parasitics.
  - ✓ Parasitic resistance and capacitance in interconnects .
    - ‘Lumped C’ where the coupling capacitances are grounded.
    - ‘Lumped Coupled C’ where only capacitances (coupling and to-ground) are extracted.
    - ‘Distributed RC’ where wire resistances and capacitance are extracted but coupling capacitance are grounded.
    - ‘Distributed Coupled RC’ where wire resistance and capacitance are extracted and the coupling capacitances are not grounded.
  - ✓ Device parasitics
    - Gate to Source and Gate to Drain parasitic capacitance.
    - Source/Drain to Substrate parasitic capacitance.
    - Well and Substrate resistance
    - Parasitic Diodes.
    - Junction capacitances.

# Outline Continued ..

- Limitation and Consideration
- Testing and Verification
- Conclusion and Future prospects

# Introduction

- Rapid advancement in the semiconductor industry.
- Scaling.
- Sensitivity to parasitics.
- High frequency circuits.
- Result : Designs that do not meet performance constraint.

# Parasitics representation

- Proper representation of parasitics
  - ✓ Netlist format a huge criteria for designers
  - ✓ Proper data representation :

```
Linear Technology LTspice/SwitcherCAD III - [Si...
File Edit View Simulate Tools Window Help
asdas.spi SimpleNet.spi
*** Via5: areacap=0.0FF/um^2, edgcap=0.6
*** Metal-6: areacap=0.0423FF/um^2, edgcap
.OPTIONS NOMOD NOPAGE

*** TOP LEVEL CELL: SimpleNet{lay}
XP0 pin@0 pin@1 RCLINE R=6.2 C=0.13FF len=39.5
.subckt RCLINE n1 n2
o1 n1 0 n2 0 TRC
.model TRC ltra R={R} C={C} len={len}
.ends RCLINE
.END
Ready
```

```
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*** Metal-6: areacap=0.0423FF/um^2, edg
.OPTIONS NOMOD NOPAGE

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** Extracted Parasitic Resistors ***
.ENDS subcell

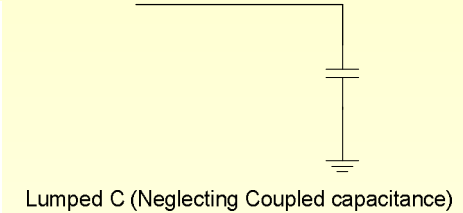
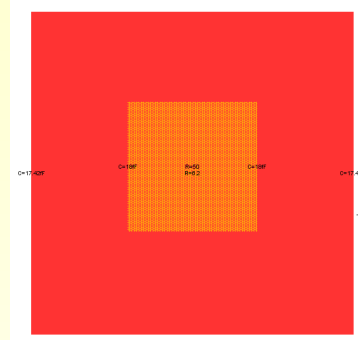
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Xsubcell@0 subcell
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C0 net@0 0 3.9FF
** Extracted Parasitic Resistors ***
.END
Ready
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File Edit View Simulate Tools Window Help
*** TOP LEVEL CELL: complexNet{lay}
** Extracted Parasitic Capacitors ***
C0 net@0 0 0.19FF
C1 net@0@pin@1 polysilicon-1 0 0.19FF
** Extracted Parasitic Resistors ***
R0 net@0 net@0@pin@1 9.73a
C2 net@0@pin@1 0 0.19FF
R1 net@0@pin@1 net@0@pin@1 9.73a
C3 net@0@pin@1 0 0.19FF
R2 net@0@pin@2 net@0@pin@2 9.73a
C4 net@0@pin@2 0 0.19FF
R3 net@0@pin@2 net@0@pin@2 9.73a
C5 net@0@pin@2 0 0.19FF
R4 net@0@pin@3 net@0@pin@3 9.73a
C6 net@0@pin@3 0 0.19FF
R5 net@0@pin@3 net@0@pin@3 9.73a
C7 net@0@pin@3 0 0.19FF
R6 net@0@pin@4 net@0@pin@4 9.73a
C8 net@0@pin@4 0 0.19FF
R7 net@0@pin@4 net@0@pin@4 9.73a
C9 net@0@pin@4 0 0.19FF
R8 net@0@pin@5 net@0@pin@5 9.73a
C10 net@0@pin@5 0 0.19FF
R9 net@0@pin@5 net@0@pin@5 9.73a
C11 net@0@pin@5 0 0.19FF
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R22 net@0@pin@12 net@0@pin@12 9.73a
C24 net@0@pin@12 0 0.19FF
R23 net@0@pin@12 net@0@pin@12 9.73a
C25 net@0@pin@12 0 0.19FF
R24 net@0@pin@12 polysilicon-1 9.73a
.END
Ready
```

# Parasitic resistance and capacitance in interconnects

## ➤ Lumped C

- $C_{\text{poly1-sub}} = 34\text{fF}$
- $C_{\text{poly2-sub}} = 36\text{fF}$



```
Linear Technology LTspice/SwitcherCAD III - [...]
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File Edit View Simulate Tools Window Help
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```
*** Metal-6: areacap=0.0423FF/um^2, edgesc
```

```
.OPTIONS NOMOD NOPAGE
```

```
*** TOP LEVEL CELL: LumpedC{lay}
```

```
** Extracted Parasitic Capacitors ***
```

```
C0 net@15 0 17.42fF
```

```
C1 net@15#1pin@26_polysilicon-1 0 17.42fF
```

```
** Extracted Parasitic Resistors ***
```

```
R0 net@15 net@15#1pin@26_polysilicon-1 6.2
```

```
.END
```

```
Linear Technology LTspice/SwitcherCAD III...
```

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File Edit View Simulate Tools Window Help
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```
*** TOP LEVEL CELL: LumpedC2{lay}
```

```
** Extracted Parasitic Capacitors ***
```

```
C0 net@15 0 17.42fF
```

```
C1 net@15#1pin@26_polysilicon-1 0 17.42fF
```

```
C2 net@18 0 18fF
```

```
C3 net@18#1pin@32_polysilicon-2 0 18fF
```

```
** Extracted Parasitic Resistors ***
```

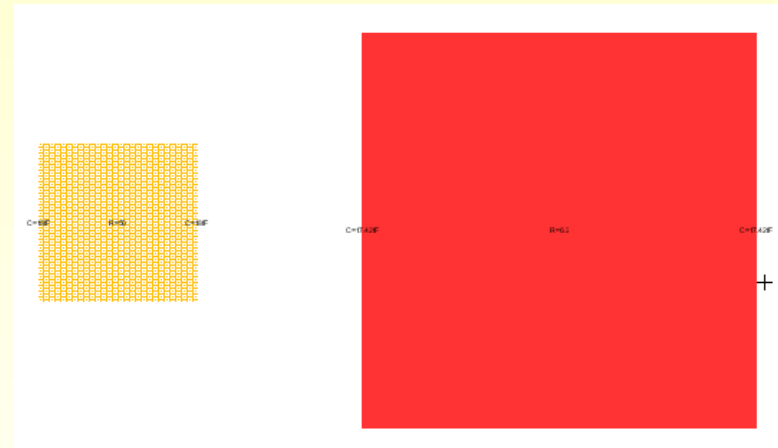
```
R0 net@15 net@15#1pin@26_polysilicon-1 6.2
```

```
R1 net@18 net@18#1pin@32_polysilicon-2 50
```

```
.END
```

# Parasitic resistance and capacitance in interconnects continued ...

- Presence of resistance for 'Lumped C'.
- Wrong estimation of capacitance of Poly2 to substrate.



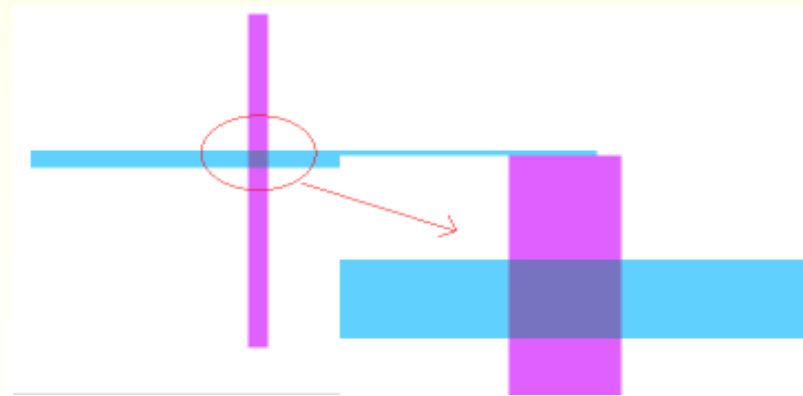
```
Linear Technology LTspice/SwitcherCAD III...
File Edit View Simulate Tools Window Help
LumpedC2.spi LumpedC3.spi
*** TOP LEVEL CELL: LumpedC3{1ay}
** Extracted Parasitic Capacitors ***
C0 net@15 0 17.42fF
C1 net@15#1pin@26_polysilicon-1 0 17.42fF
C2 net@18 0 18fF
C3 net@18#1pin@32_polysilicon-2 0 18fF
** Extracted Parasitic Resistors ***
R0 net@15 net@15#1pin@26_polysilicon-1 6.2
R1 net@18 net@18#1pin@32_polysilicon-2 50
.END
Ready
```

# Parasitic resistance and capacitance in interconnects continued ...

- Approach for 'Lumped C' parasitic extraction.
  - ✓ Simple way would be to use geometrics and find area of overlap if any and exclude it.
  - ✓ The drawback would be a slight over estimation or an underestimation when using Manhattan geometry.
  - ✓ Decide if and when to exclude area of overlap based on certain parameters.



Overestimation : Area of overlap neglected due to complications with geometry.



Overlap C Can be neglected resulting in a small over estimate of capacitance

# Parasitic resistance and capacitance in interconnects continued ...

- ✓ Decide if and when to exclude area of overlap based on certain parameters.
- ✓ The parameters : time for extraction, impact on circuit, etc.



Underestimation : Only Metal 2 Fringe to substrate capacitance considered

# Parasitic resistance and capacitance in interconnects continued ...

➤ ‘Lumped Coupled C’ where only capacitances (coupling and to-ground) are extracted.

✓ A 3D model is being considered for implementation with several applicable algorithms.

✓ The first issue would be to add inter layer parasitic capacitance in the tool.

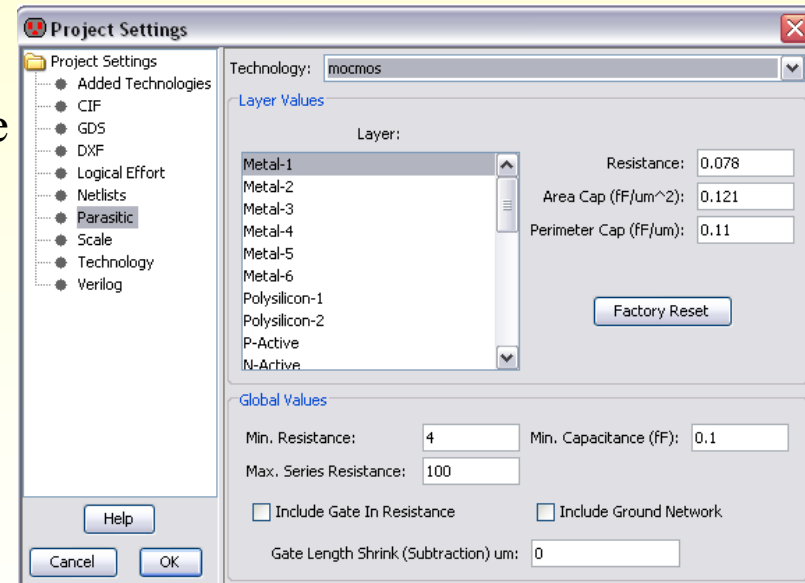
✓ Available options :

- Simple overlap Capacitance

( Low accuracy, faster)

- Pattern matching

( High accuracy, slower)

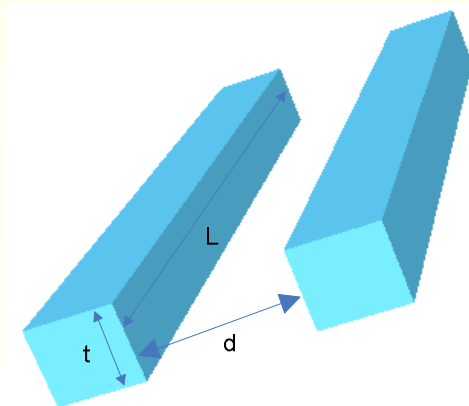


# Parasitic resistance and capacitance in interconnects continued ...

- ✓ A simple overlap capacitance as shown in the figure on left would result in a slight over estimation due to the fringe capacitance of M2-M1.
- ✓ The area of overlap can be estimated using the co-ordinates of M1 and M2.
- ✓  $Cap_{M1-M1} = \frac{\xi}{d}(t \times L)$
- ✓ The consideration here is the distance between adjacent metal lines.
- ✓ The effect of coupling capacitance on adjacent metal line increases to larger distance (d) as we move up to higher order metal layers.



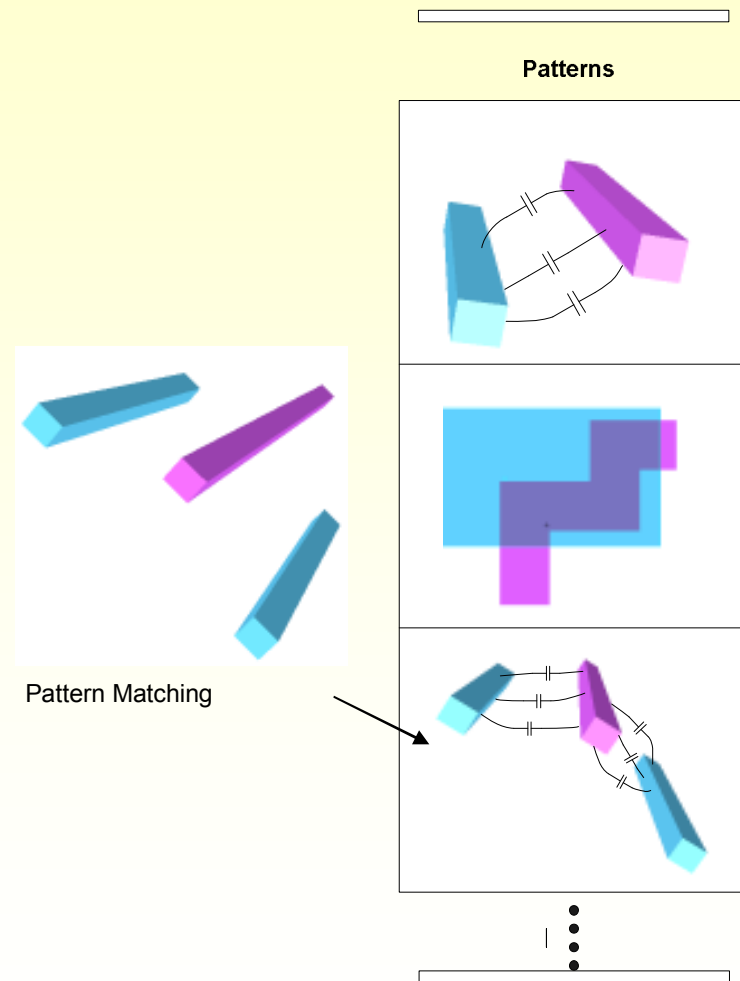
Overestimation : Simple Overlap capacitance



M1-M1 capacitance

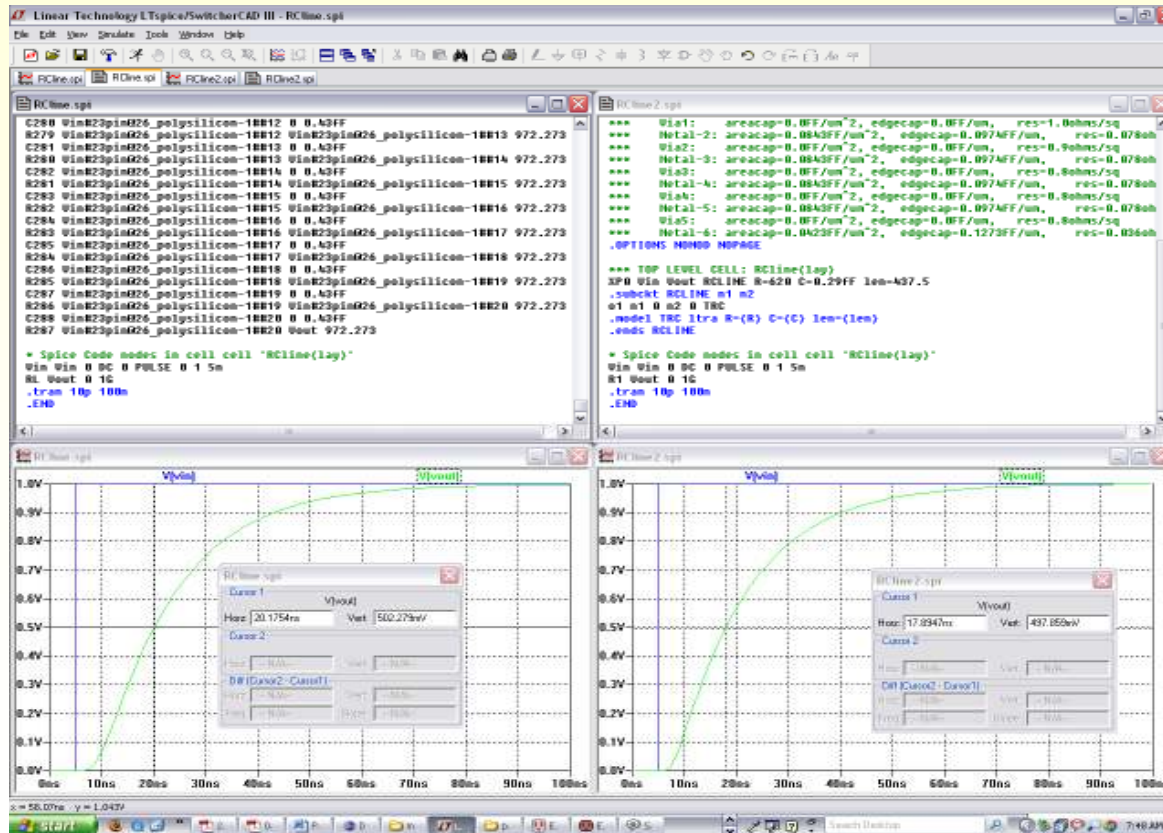
# Parasitic resistance and capacitance in interconnects continued ...

- ✓ For complex coupled parasitic capacitance extraction, pattern matching can be used.
- ✓ For any given technology, tens of thousands of test structures are enumerated and a step called pre-characterization is performed.
- ✓ The data from the tests are used to build lookup tables.
- ✓ As the geometric pattern becomes complex, i.e. more the parameters needed to describe a pattern harder it is to match.
- ✓ The matching algorithm complexity defines the speed of extraction and accuracy.



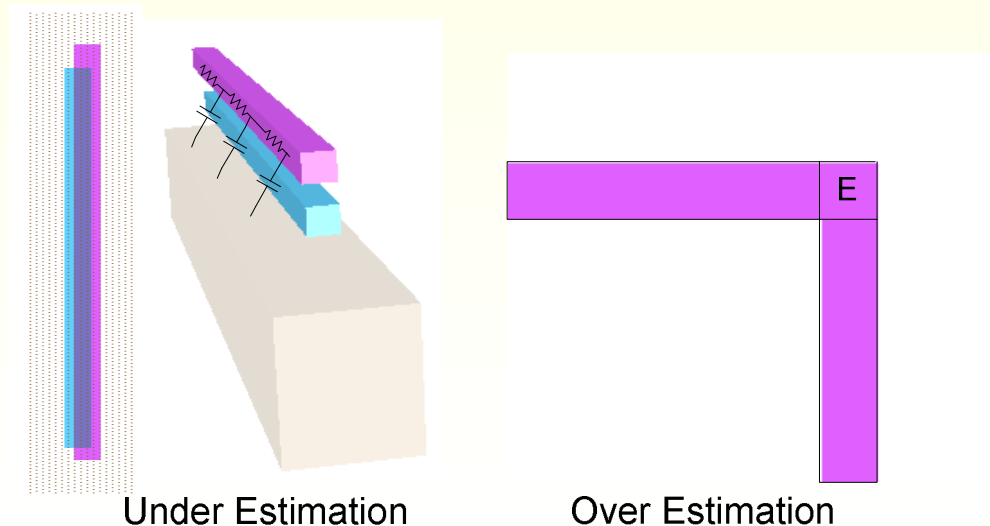
# Parasitic resistance and capacitance in interconnects continued ...

➤ ‘Distributed RC’ where wire resistances and capacitance are extracted but coupling capacitance are grounded.



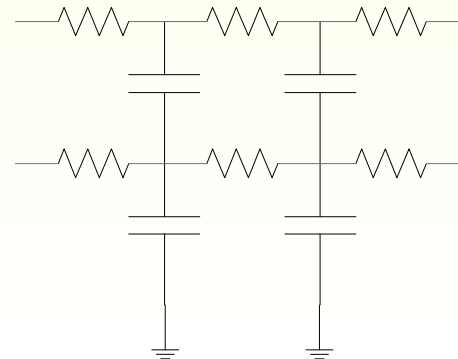
## Parasitic resistance and capacitance in interconnects continued ...

- ✓ The area of concern here is the over estimation of resistance due to the overlap of arcs at junctions/nodes. Area marked E.
- ✓ Can be addressed by merging the arcs to form one coherent metal wire before parasitic extraction.
- ✓ Again consideration and choices need to be made when two different layers overlap.



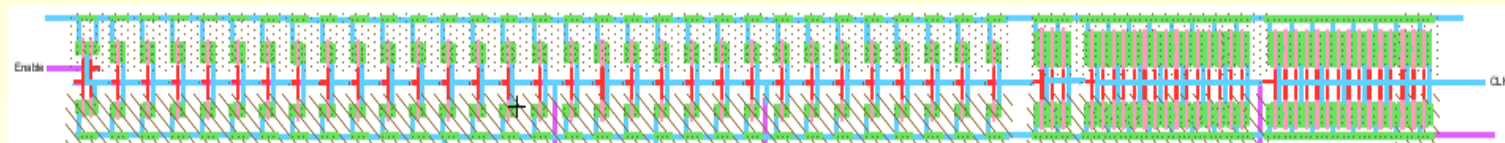
# Parasitic resistance and capacitance in interconnects continued ...

- ‘Distributed Coupled RC’ where wire resistance and capacitance are extracted and the coupling capacitances are not grounded.
  - ✓ The most complex of all interconnects parasitic extraction.
  - ✓ Network analysis algorithm required for complex networks.
  - ✓ High level of pattern matching is required for accuracy.
  - ✓ The way to tackle this situation is do a selective analysis of nodes which are of high importance and where ‘Distributed Coupled RC’ has higher prominence.



# Testing and Verification

- Using a 31 stage ring oscillator for parasitic effect due to interconnects.



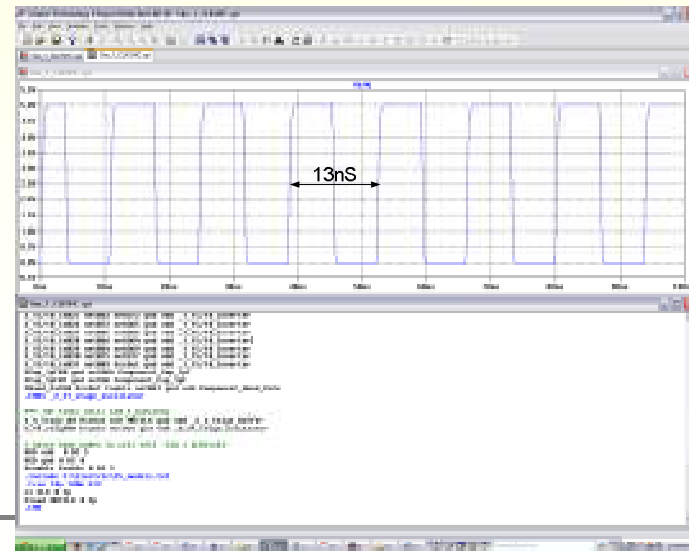
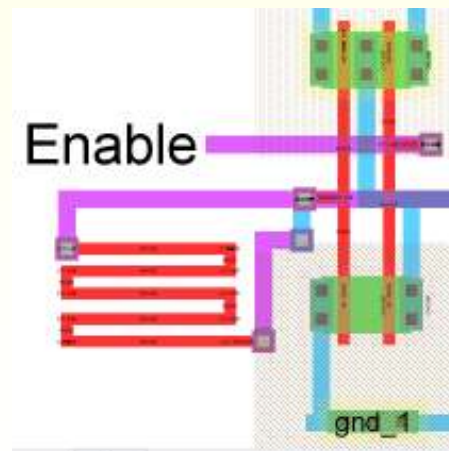
- Frequency  $f = \frac{1}{n(t_{PHL} + t_{PLH})} = 80MHz$  ;  $t = 12.5nS$

- R=7k

(Over estimation)

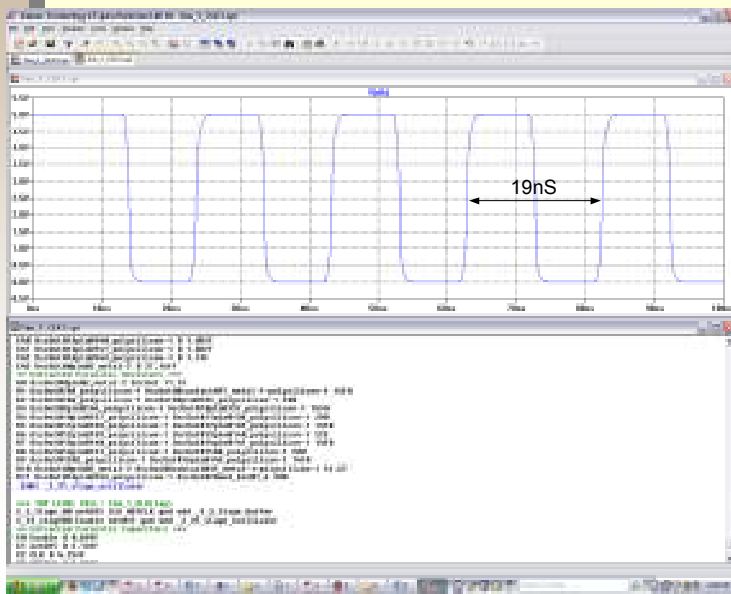
- C=20pF

- Delay=.05pS

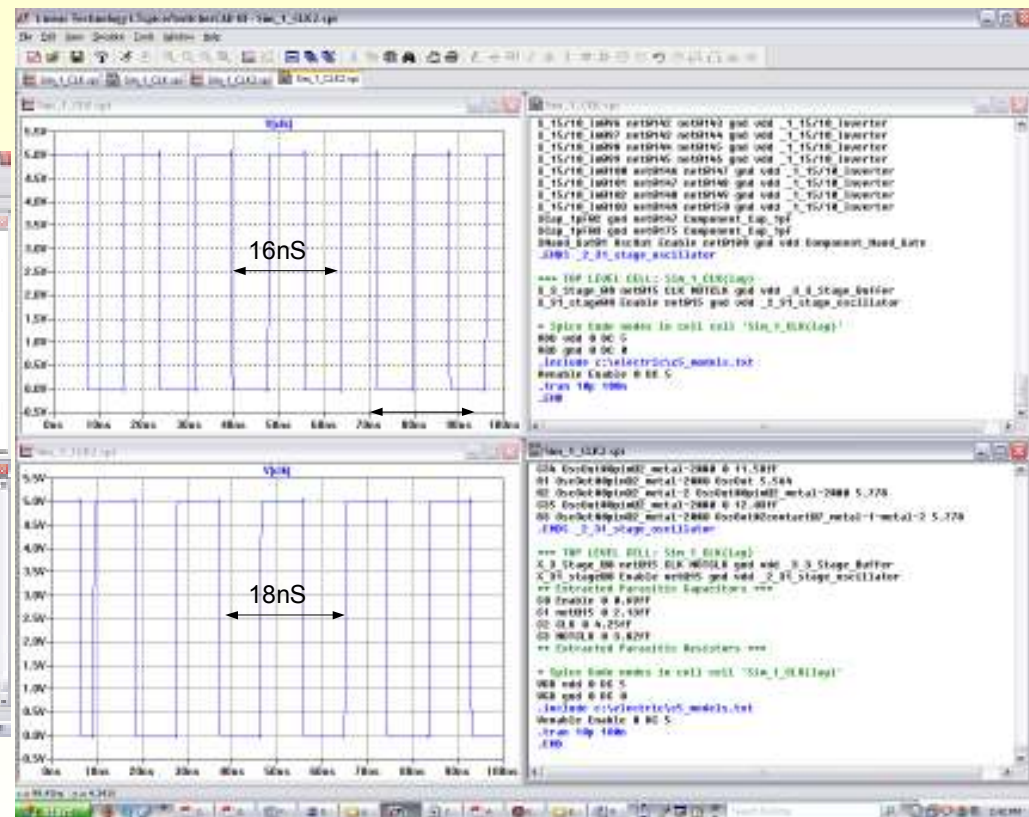


Oscillator simulation from schematic

# Testing and Verification Continued ...



Oscillator simulation with added RC



Oscillator simulation from Layout with and without parasitic

# Conclusion and Future prospects

- Considerable research and thought has been put to develop an approach for layout parasitic extraction (LPE). This could potentially be changed to better suit the requirement as and when development is done for a particular model.
- One of the first thing to consider in the future would be to include parasitic inductance.
- Increase the accuracy and speed.
- Considerable research needs to be done in extracting device level parasitics and parasitic devices.
- Develop LPE for other technologies.

# References

- [1] R. J. Baker, CMOS Circuit Design, Layout, and Simulation, Revised Second Edition, Wiley-IEEE, 2008.
- [2] William H. Kao, Chi-Yuan Lo, Raminderpal Singh, Mark Basel, “Parasitic Extraction: Current State of the Art and Future Trends”, Circuits and Systems, 2001. ISCAS 2001. vol. 5, pp. 487-490, Oct. 2001.
- [3] L.S. Dutta, T. Hillmann-Ruge, “Application of ring oscillators to characterize transmission lines in VLSI circuits”, Components, Packaging, and Manufacturing Technology, Part B: Advanced Packaging, IEEE Transactions on, vol. 18, issue: 4, pp. 651 – 657, Nov. 1995.
- [4] W. Shi, J. Liu, N. Kakani, and T. Yu, “A Fast Hierarchical Algorithm for 3-D Capacitance Extraction,” Proc. 29<sup>th</sup> ACM/IEEE DAC, pp. 2 12-2 17, San Francisco, CA, June 1998.