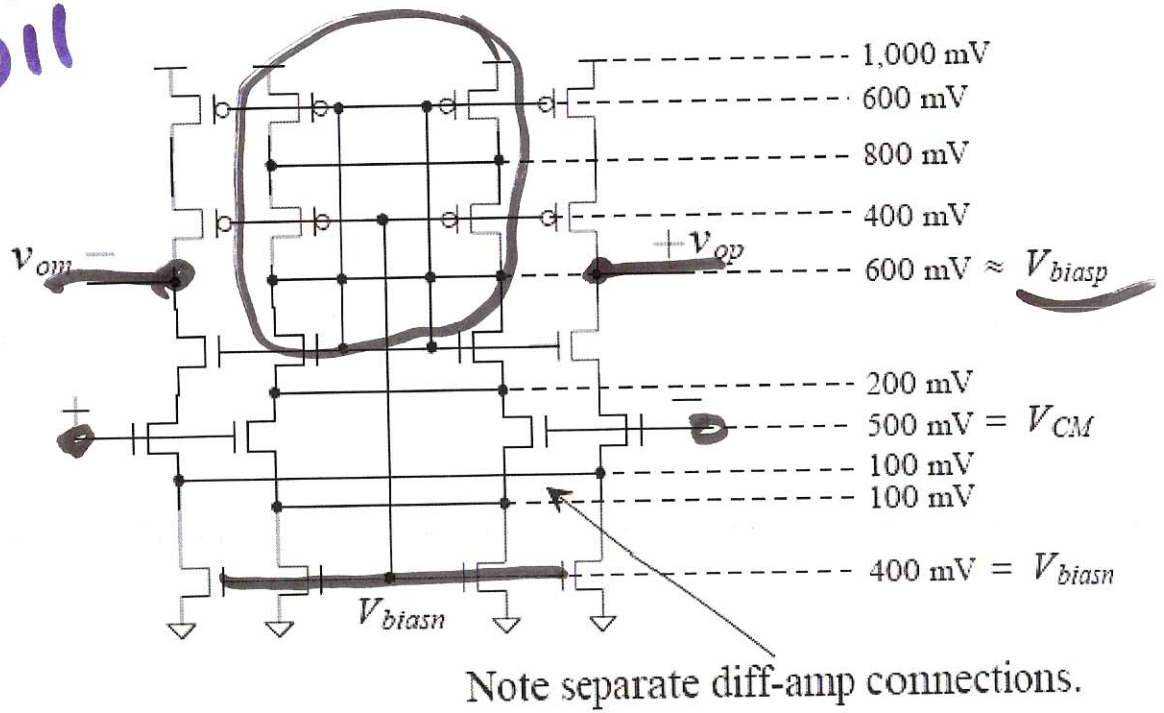
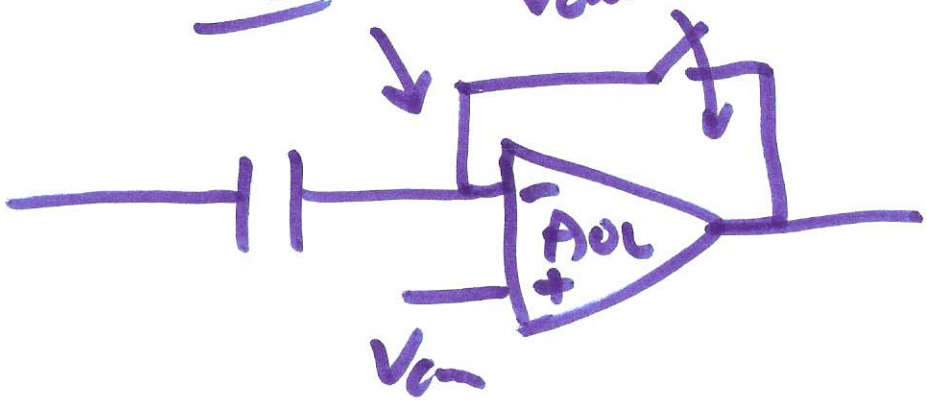
Lecture 27
Dec. 6, 2011



NMOS are 10/1
PMOS are 20/1
Bias circuit in Fig. 26.3

Figure 26.19 Fully-differential cascode diff-amp.

$V_- = -\frac{A_{OL}}{V_{cm}} + V_{cm} =$



V_-

$V_{OUT} = A_{OL}(V_+ - V_-)$

$\frac{V_{OUT}}{A_{OL}} = V_+ - V_-$

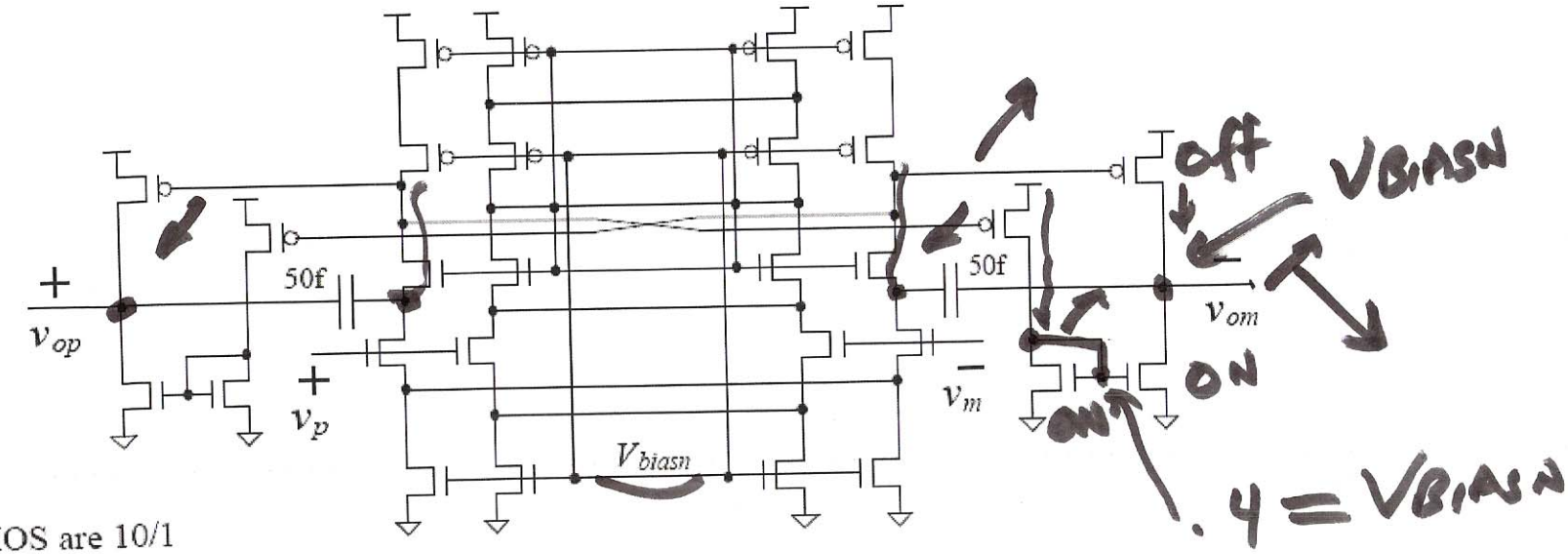
$(A_{OL}+1)V_- = V_+$

$V_- = \frac{V_{cm}}{A_{OL}+1}$

$\simeq \frac{V_{cm}}{A_{OL}}$

$\frac{V_{cm}}{A_{OL}} - \frac{V_m}{A_{OL}}$

2)



NMOS are 10/1
PMOS are 20/1
Bias circuit in Fig. 26.3

Figure 26.22 Basic two-stage op-amp without CMFB.

3)

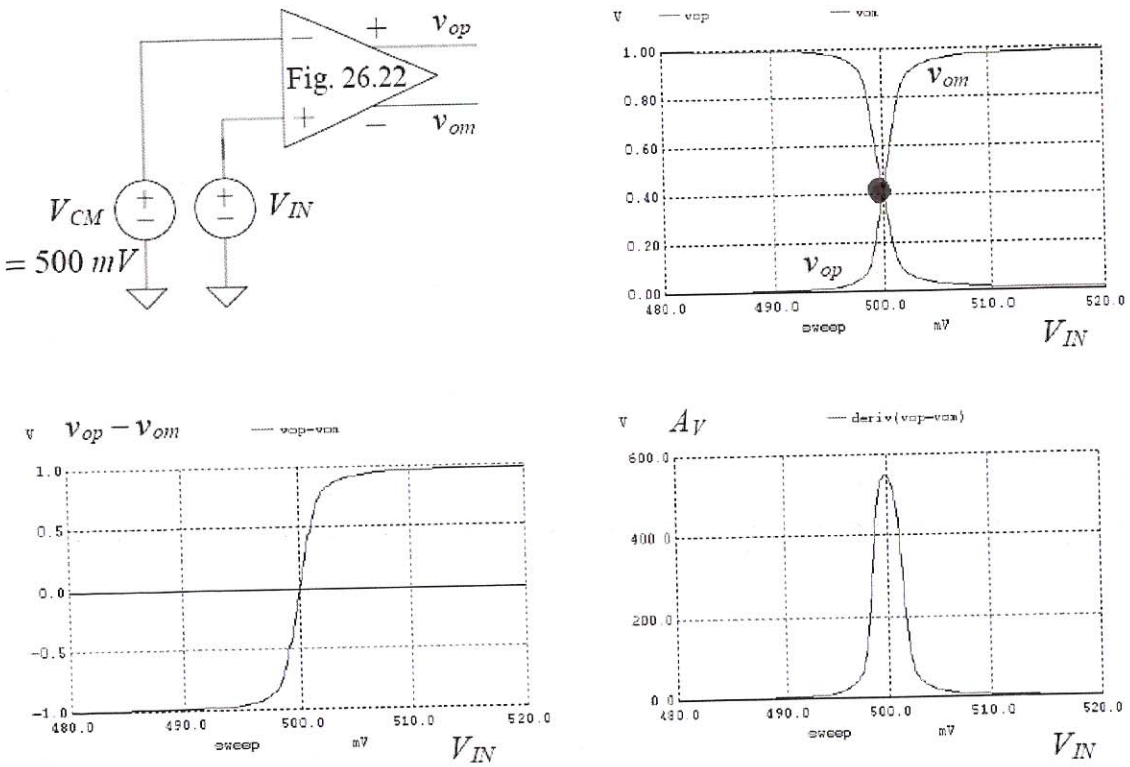


Figure 26.23 DC behavior and gain of the op-amp in Fig. 26.22.

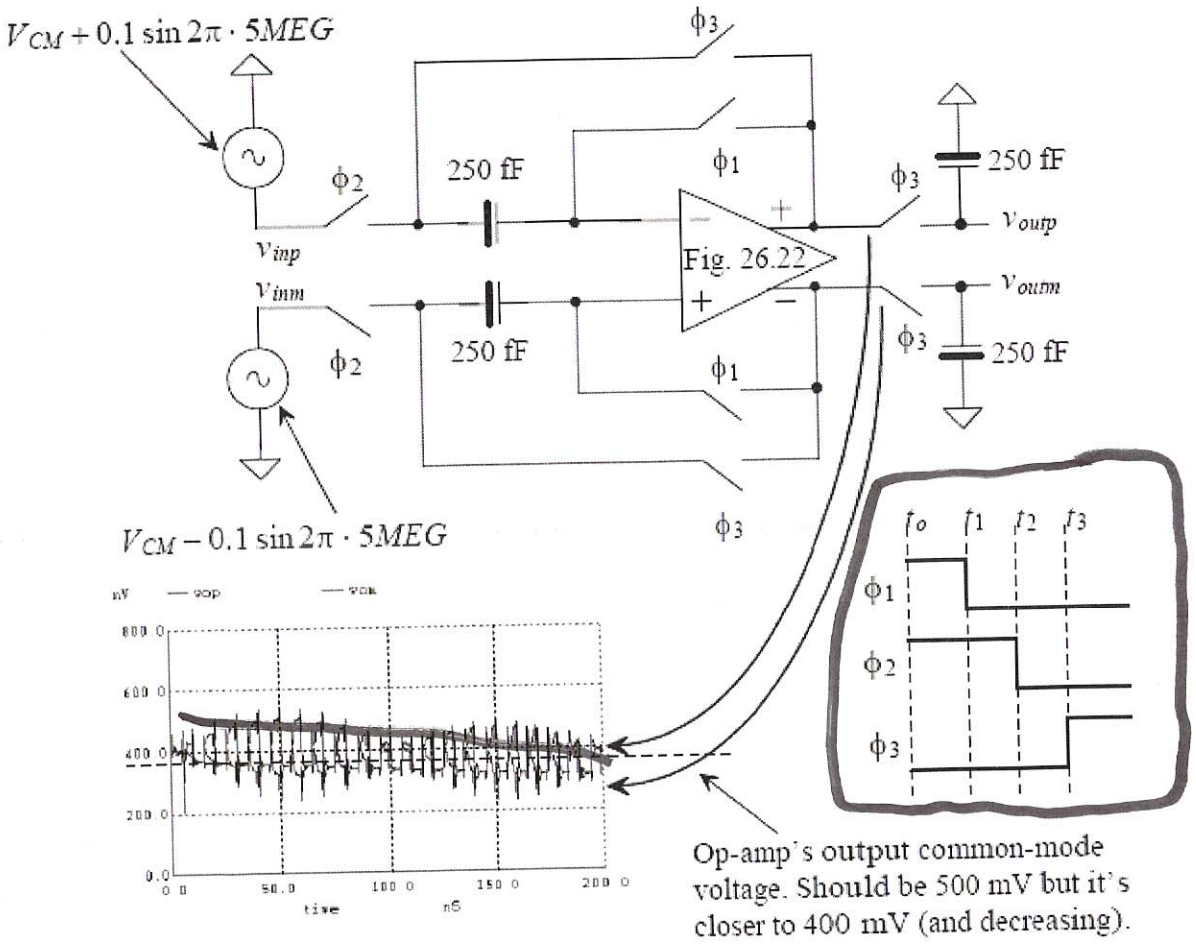


Figure 26.25 A sample-and-hold circuit. Notice how the output common-mode voltage is wandering.

5)

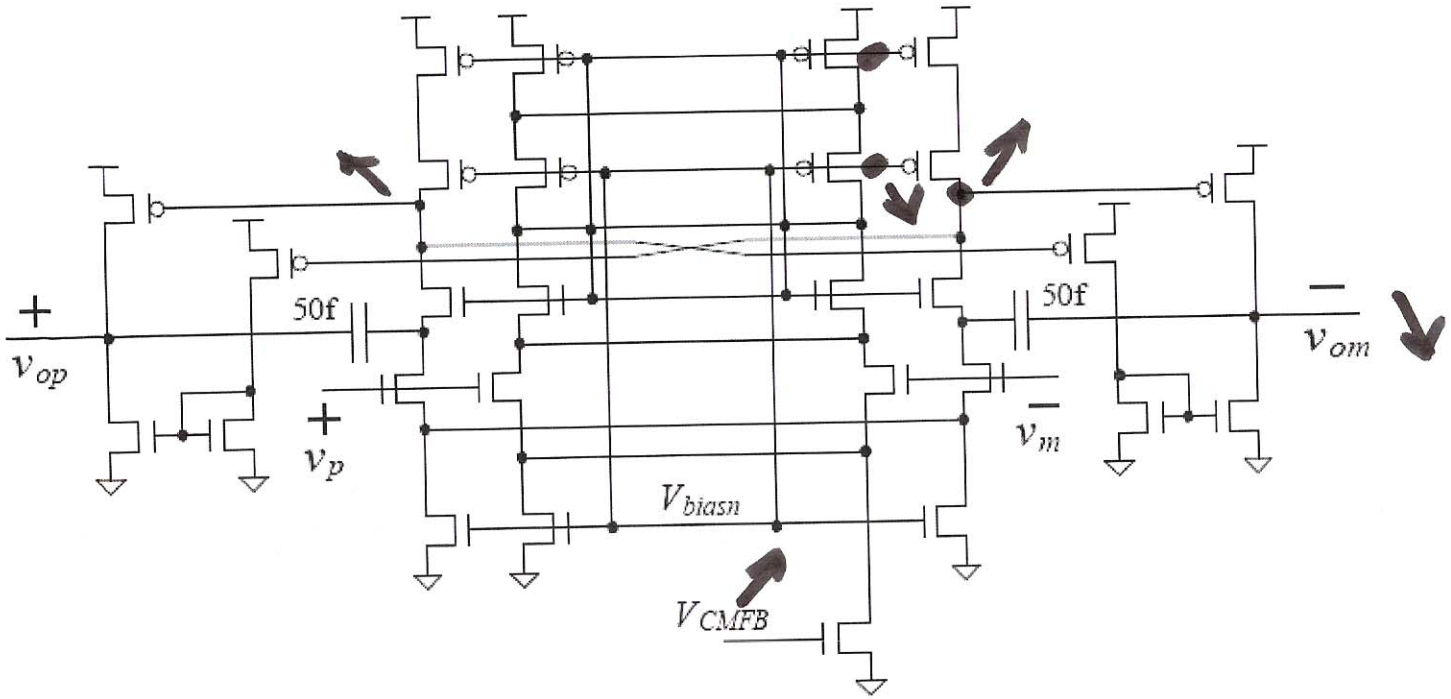


Figure 26.26 Modifying the op-amp for a CMFB input signal.

6)

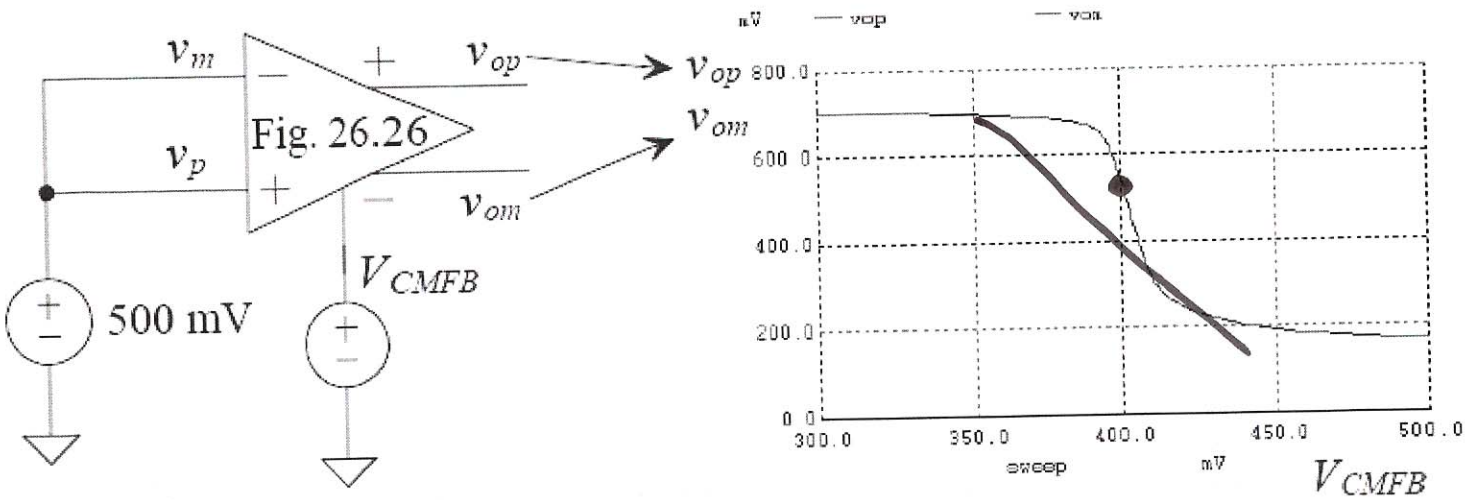
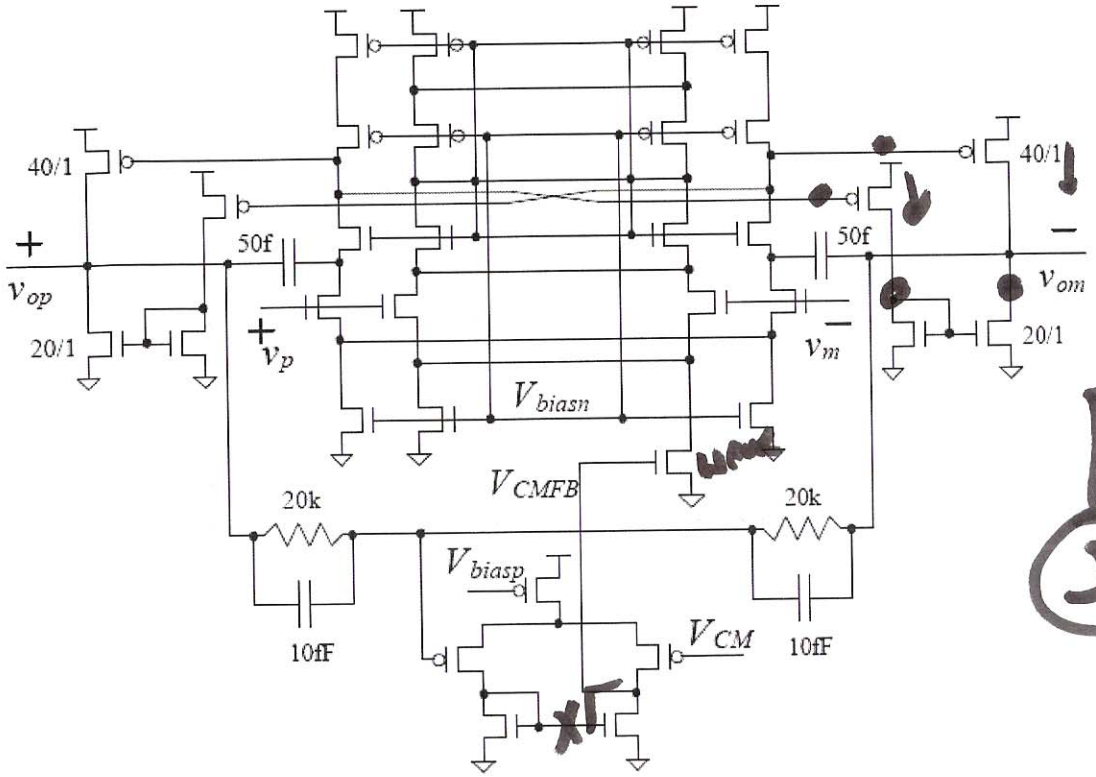


Figure 26.27 The CMFB input to output relationship. The gain is approximately 25 (considerably less than the forward differential gain).



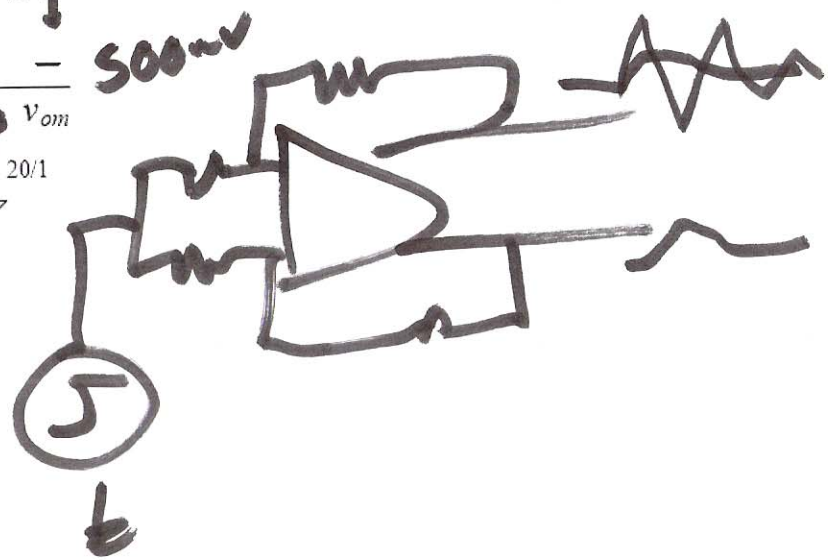


Figure 26.29 Complete schematic of op-amp with CMFB.

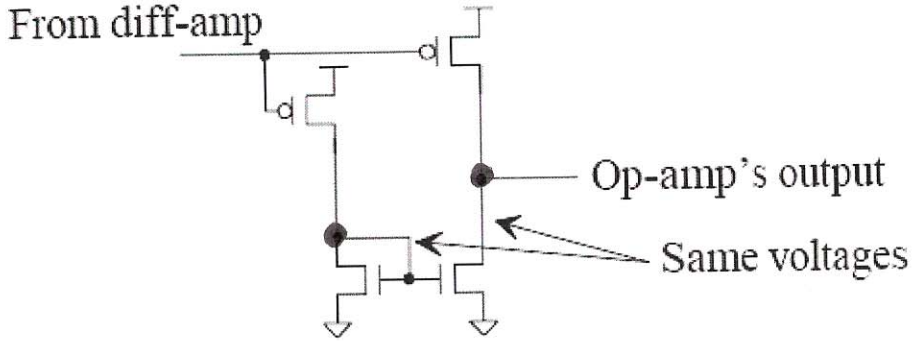


Figure 26.31 Output buffer used in the op-amp of Fig. 26.29.

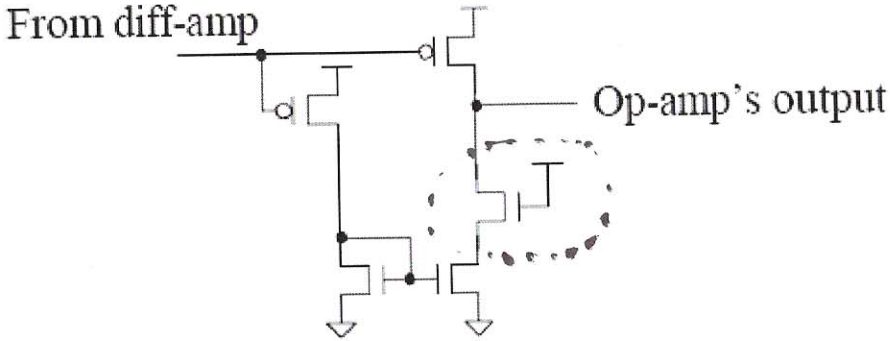


Figure 26.32 Adding a device to allow the output voltage to swing.

9)

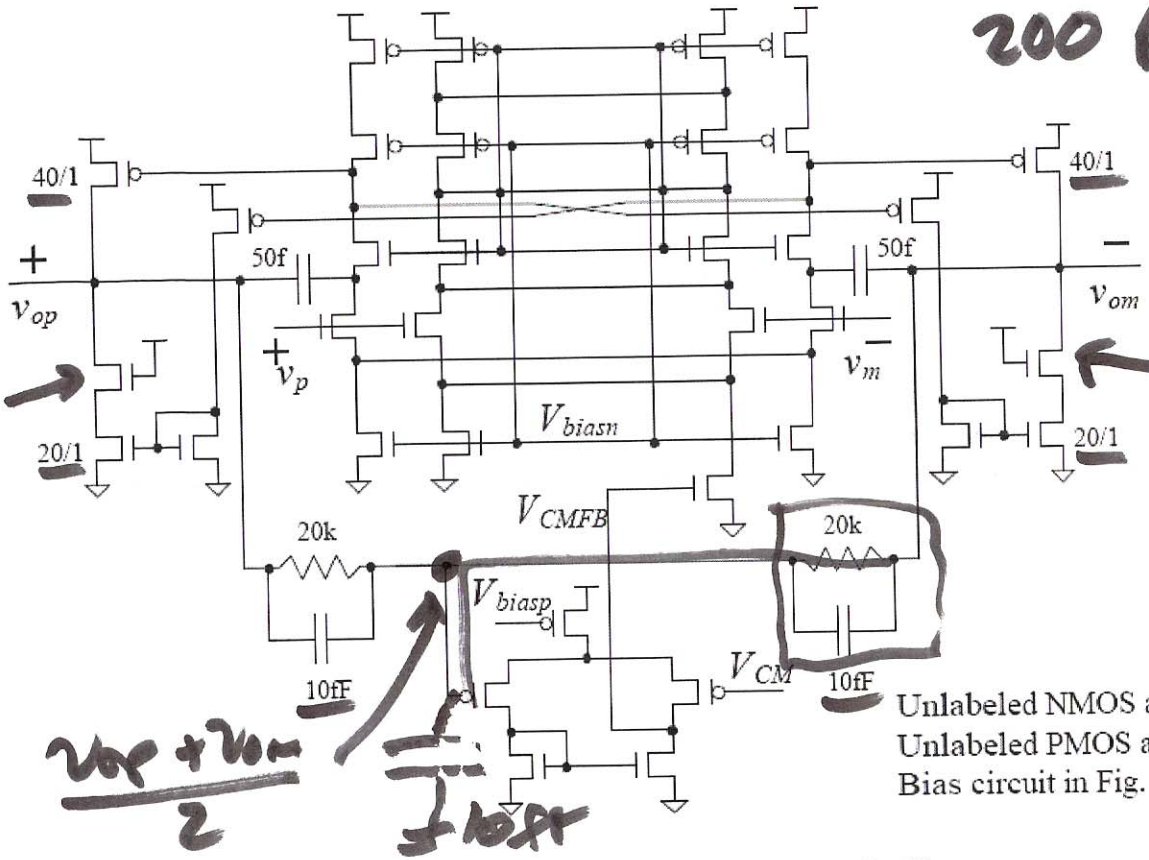
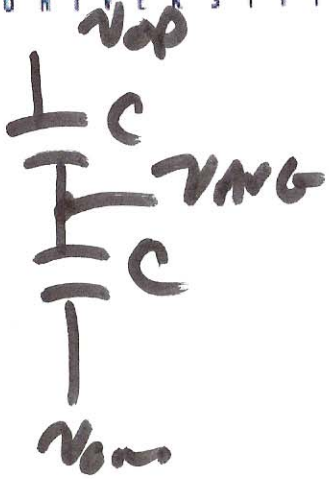


Figure 26.33 Op-amp with modified output buffer.

20k · 10fF
200 ps



added device

$$\frac{V_{op} - V_{AVG}}{\frac{1}{j\omega C}} =$$

$$\frac{V_{AVG} - V_{om}}{\frac{1}{j\omega C}}$$

$$2V_{avg} = V_{op} + V_{om}$$

$$V_{avg} = \frac{V_{op} + V_{om}}{2}$$

$\frac{V_{op} + V_{om}}{2}$

10)

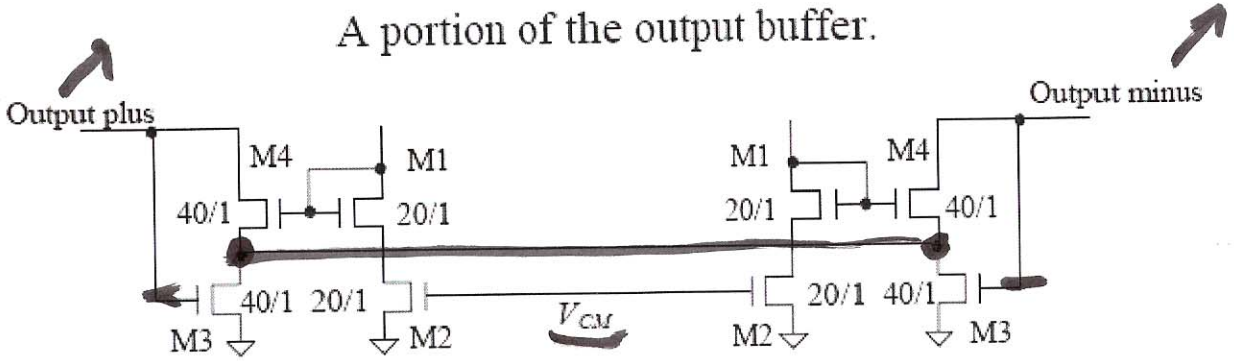


Figure 26.37 Using triode-operating MOSFETs to balance the outputs (bad).

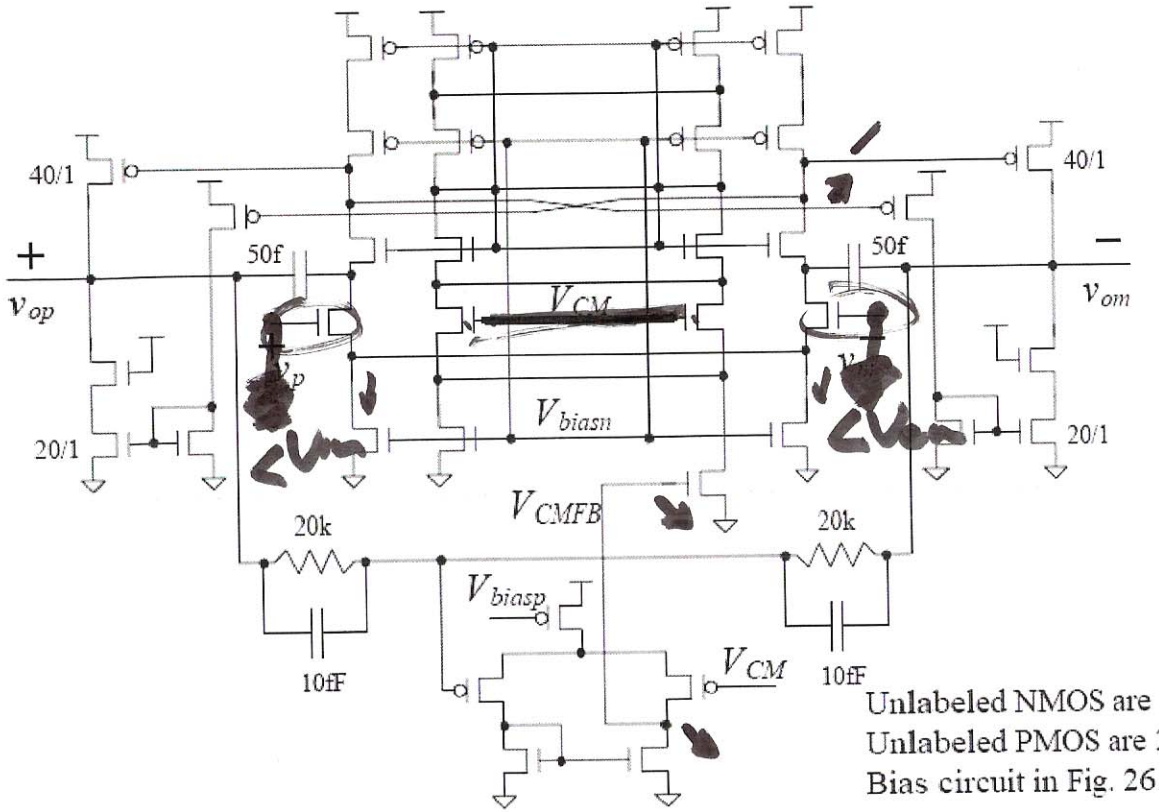


Figure 26.39 Connecting the bias circuit diff-amp's inputs to the common-mode voltage.

12

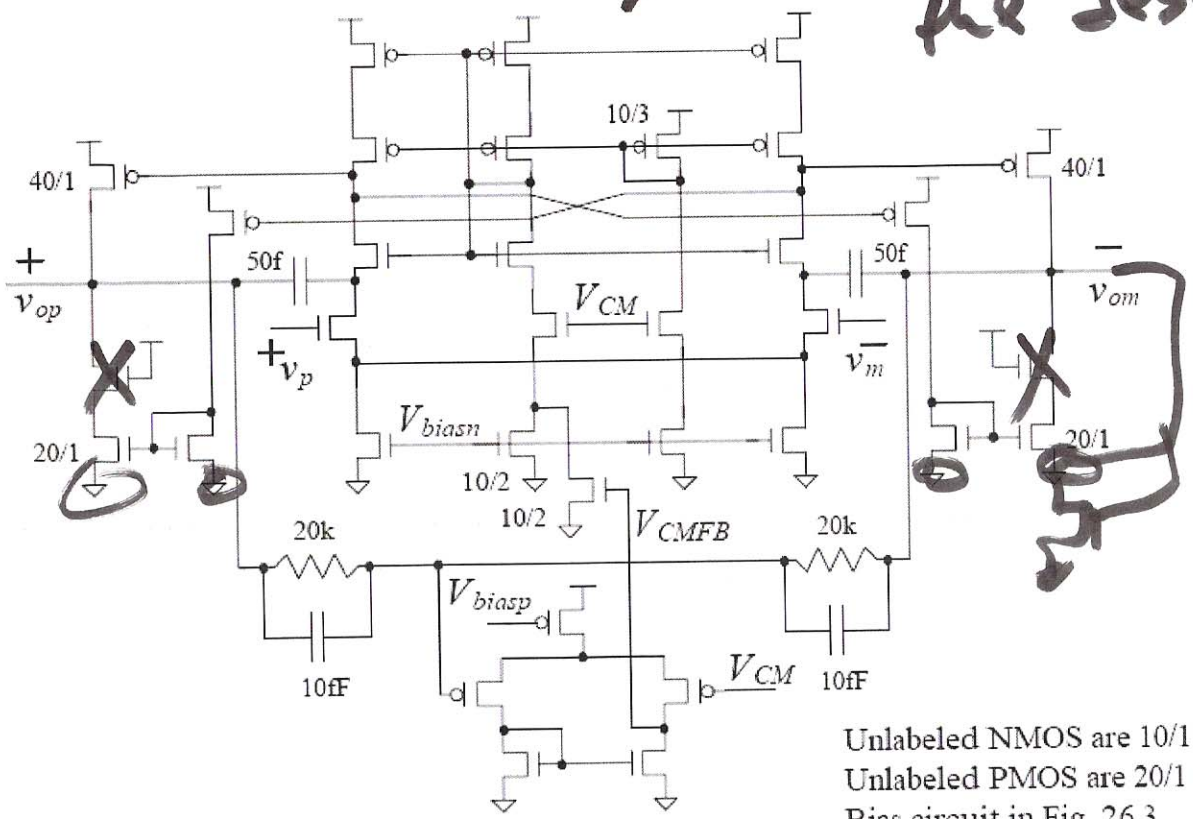
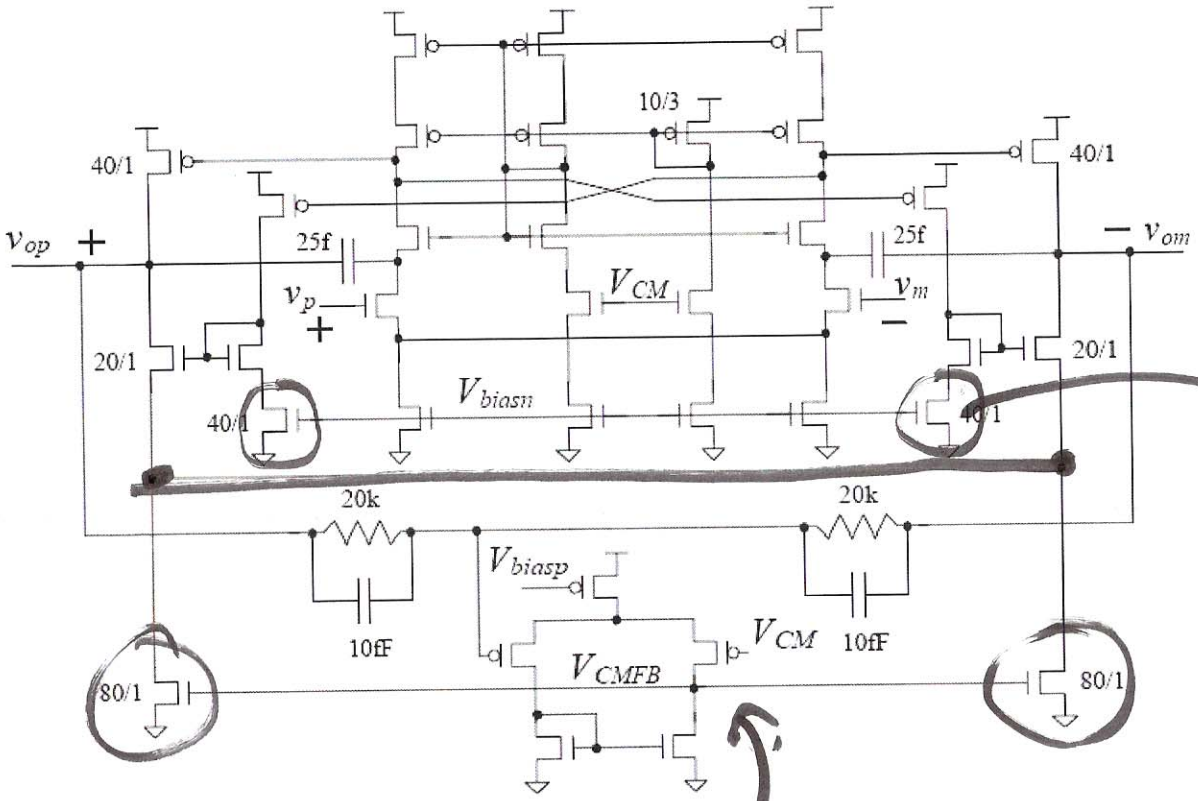


Figure 26.40 Making the op-amp more practical.



triode

Figure 26.43 Providing CMFB through just the output buffer. Using an amplifier with triode-operating MOSFETs for CMFB (good).

Amplifier with gain

14)

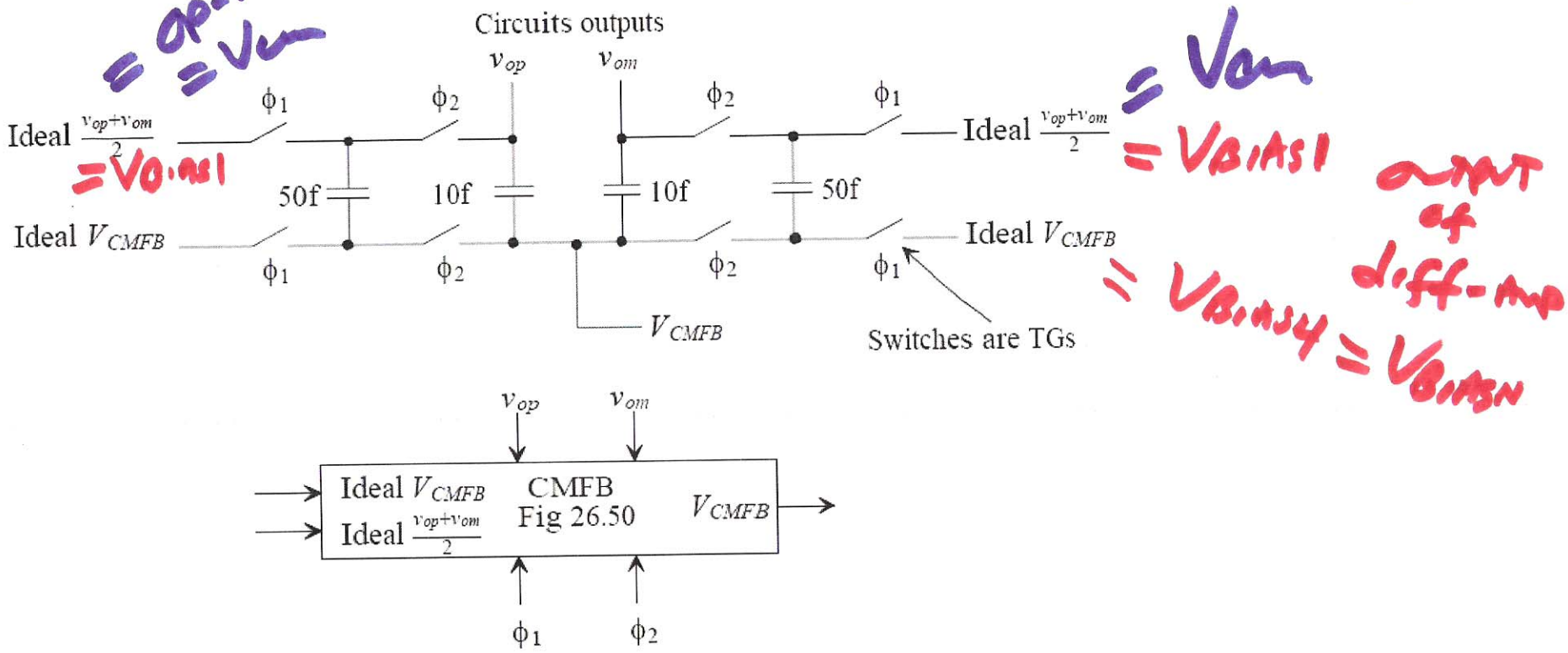


Figure 26.50 A switched-capacitor CMFB circuit (see Fig. 26.16). Switches implemented with transmission gates.

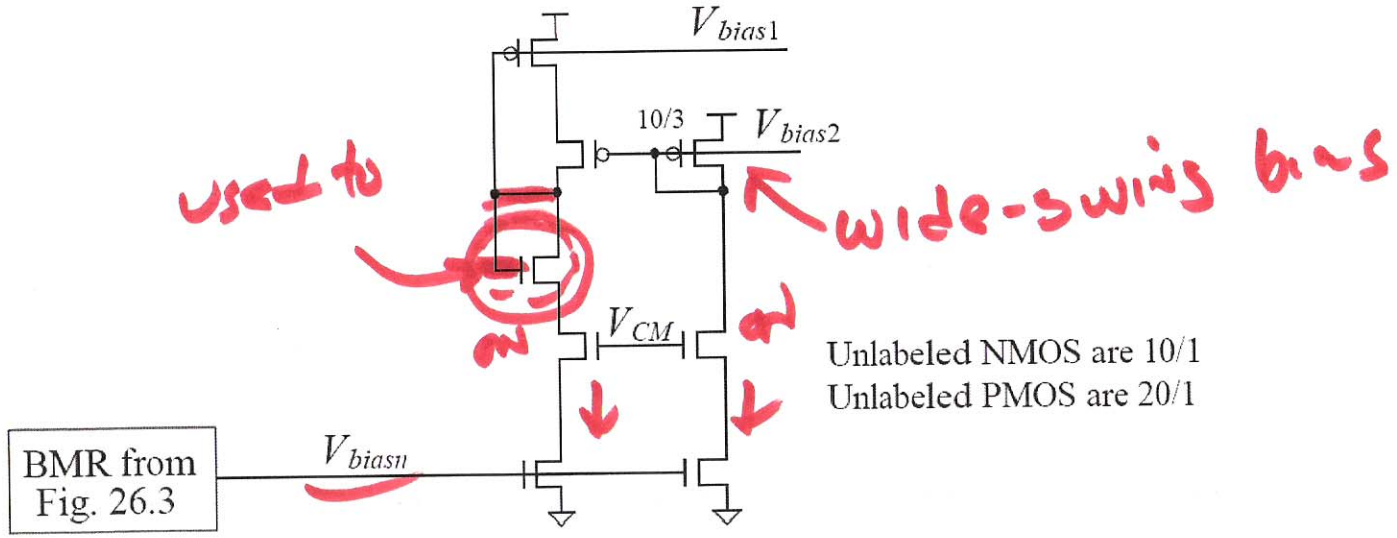


Figure 26.52 Biasing circuit for the op-amp developed in this section.

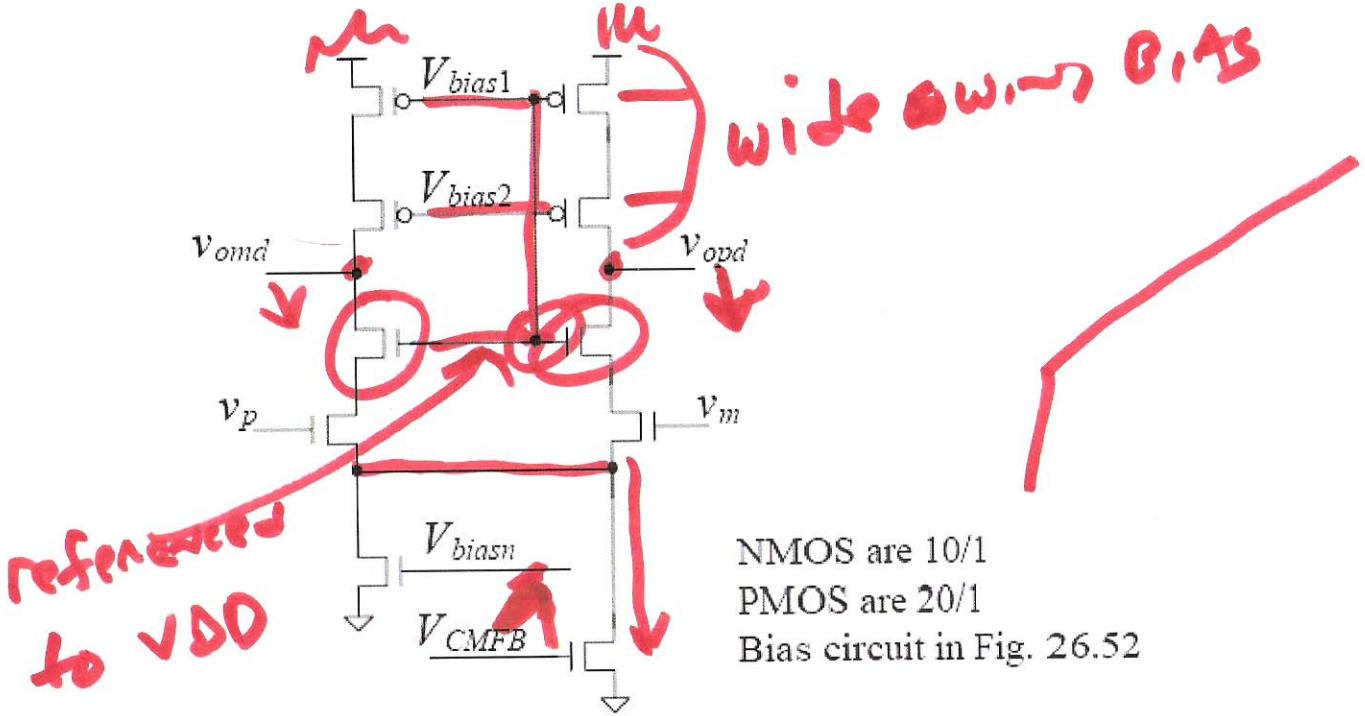


Figure 26.53 Diff-amp used with the bias circuit of Fig. 26.52.

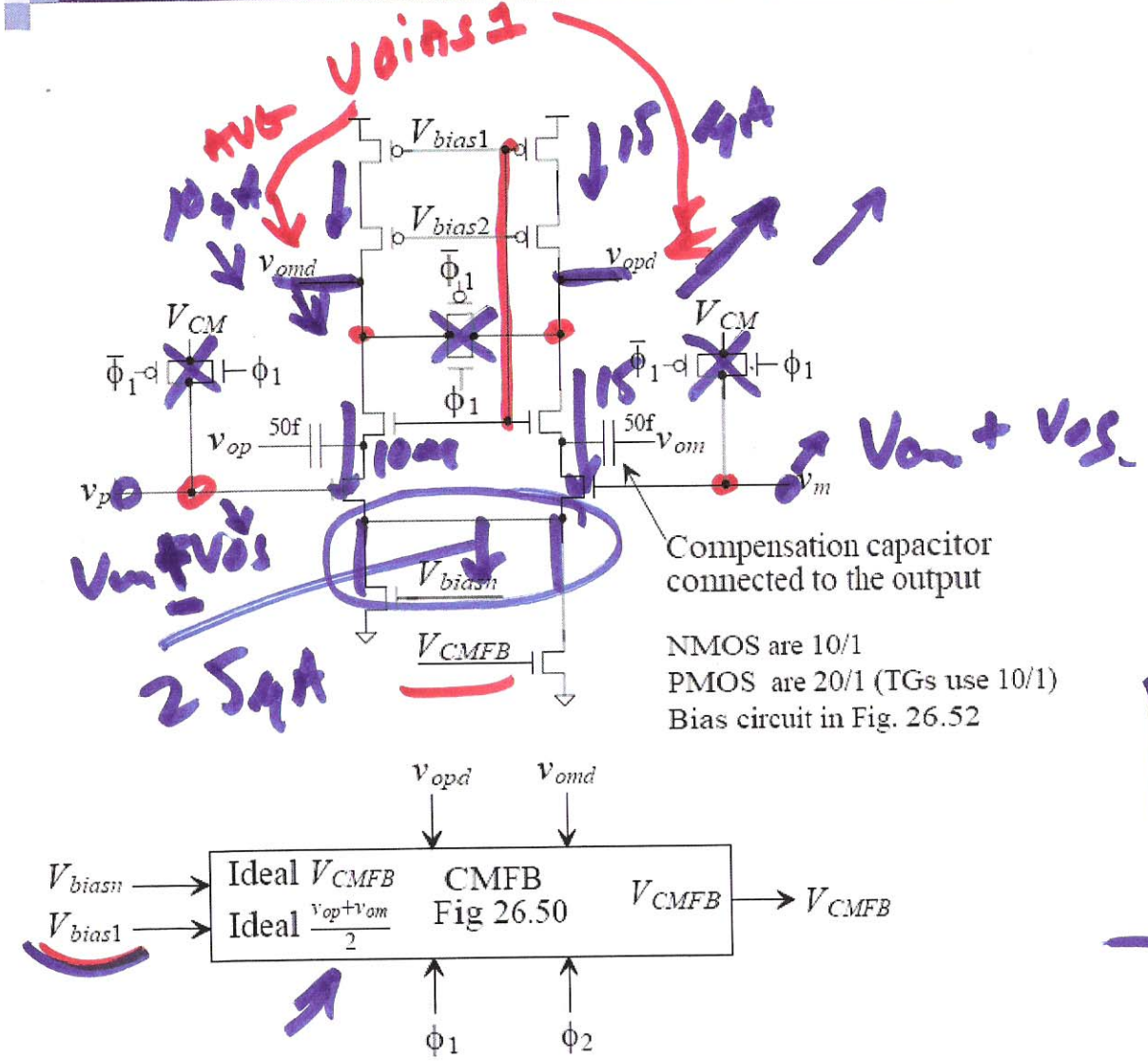
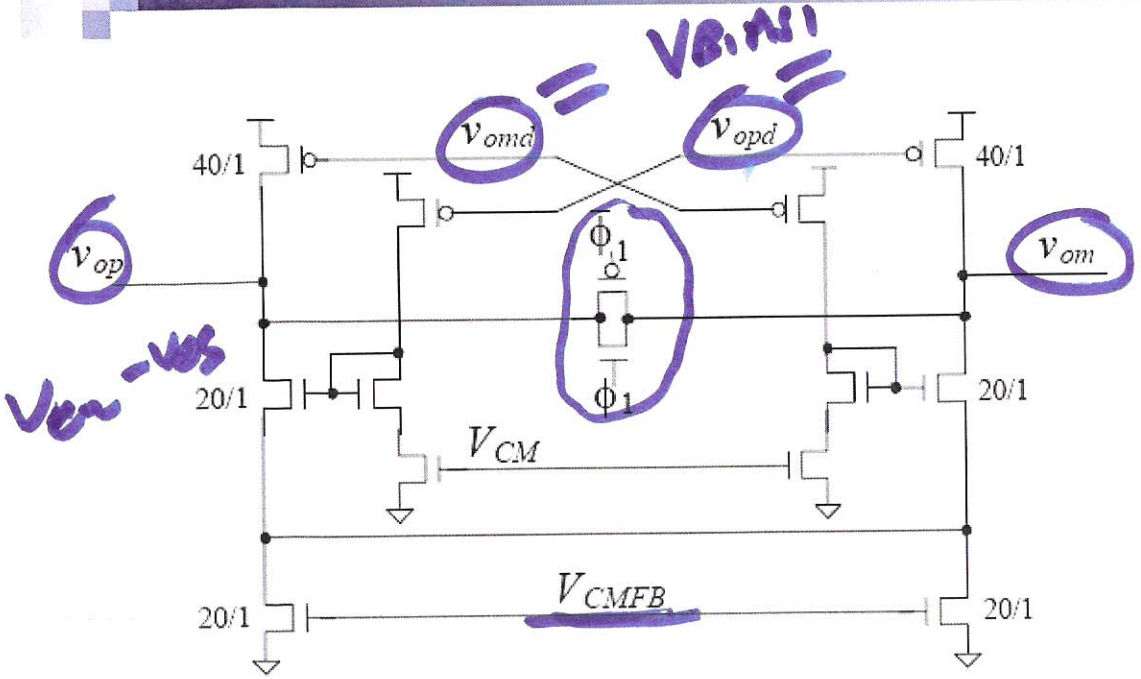


Figure 26.54 First-stage diff-amp with SC CMFB.



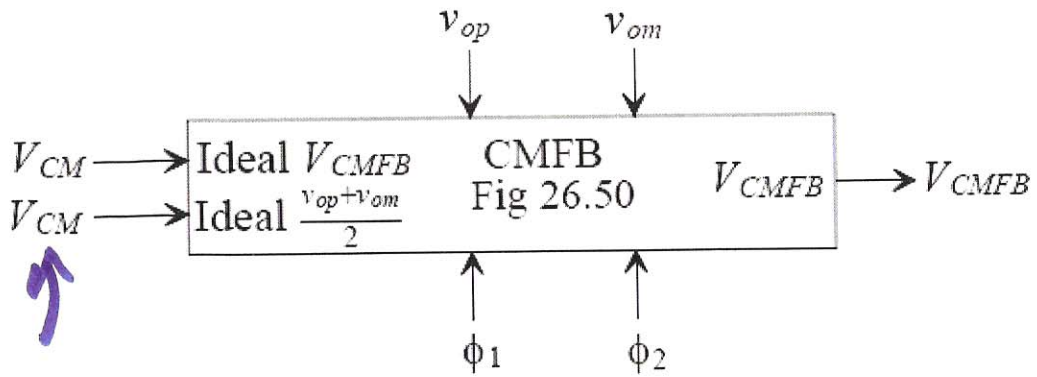


Figure 26.56 Output buffer and CMFB.

17)

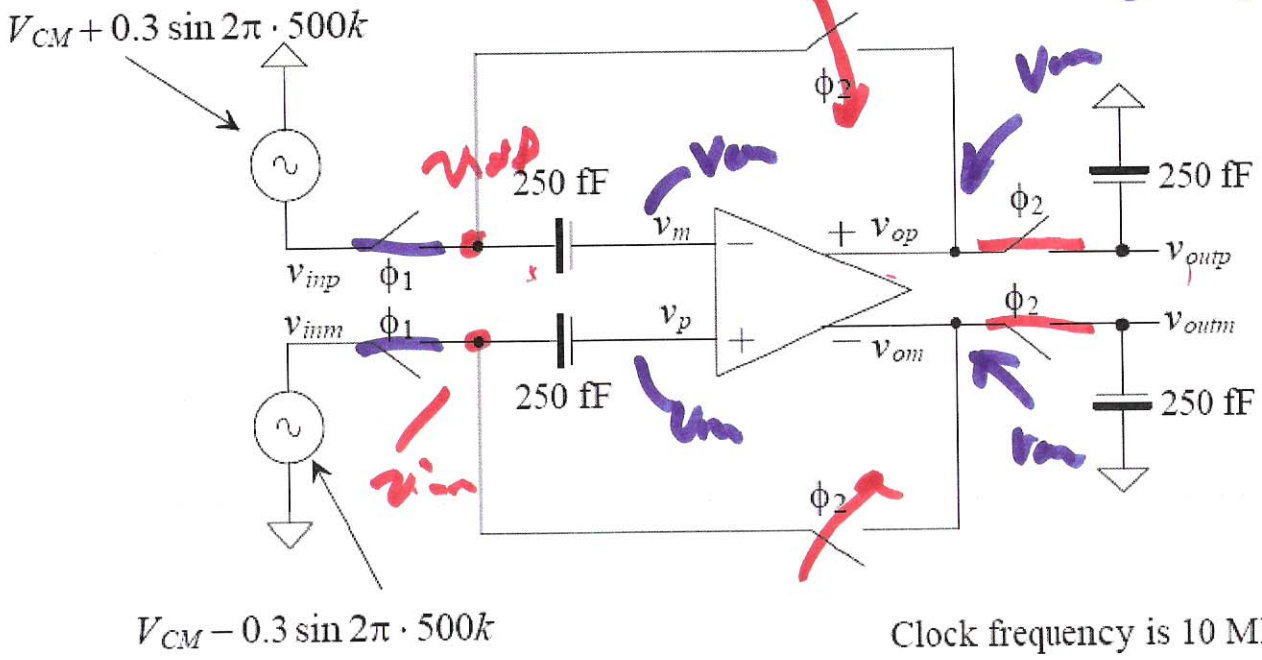


Figure 26.58 Simulating the operation of the op-amp formed with the diff-amp in Fig. 26.54 and buffer in Fig. 26.56.

Sample ϕ_1 is closed

Open ϕ_1 switches

Close ϕ_2 switches

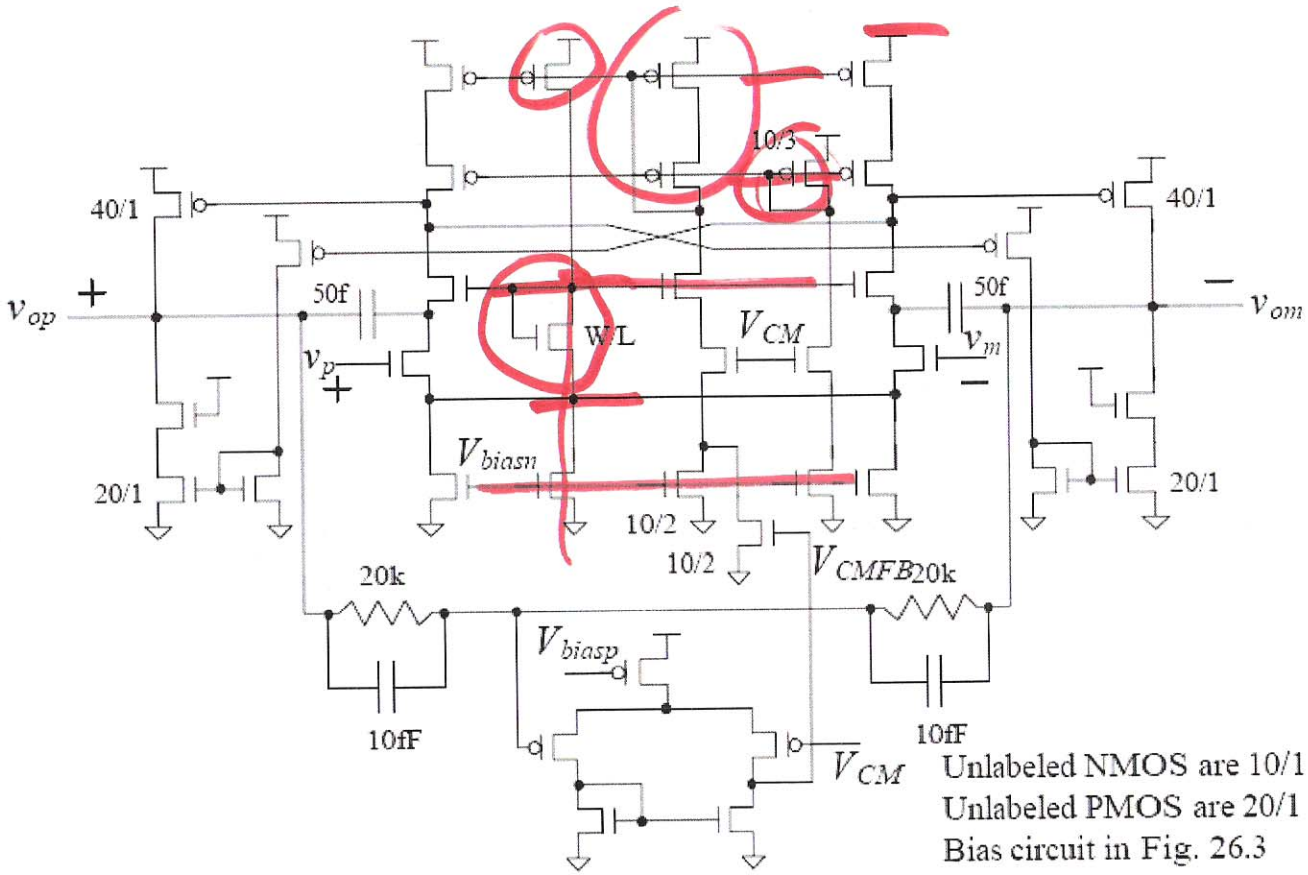
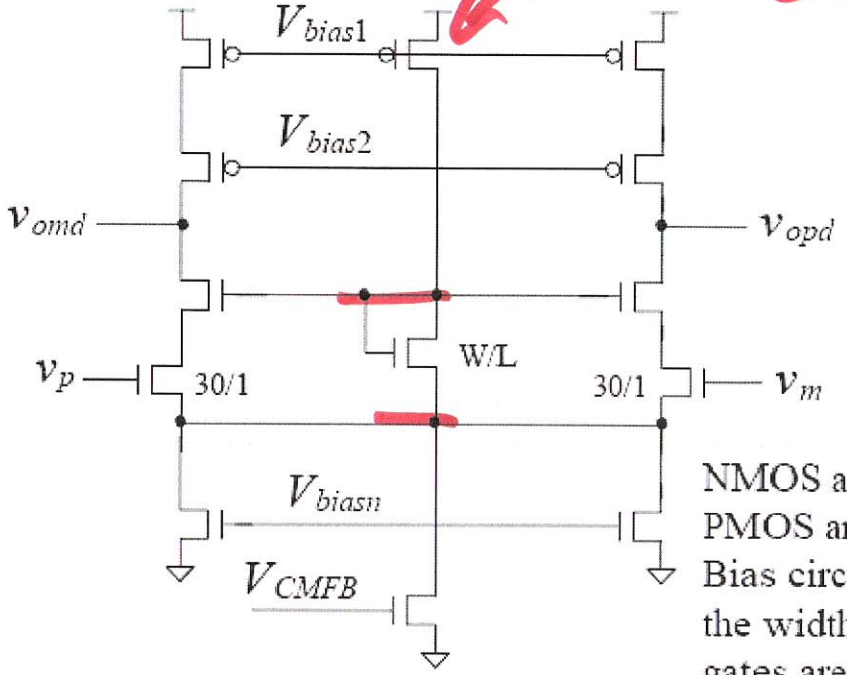


Figure 26.62 An op-amp with better biasing (but more power) for lower VDD operation.



NMOS are 10/1
PMOS are 20/1
Bias circuit in Fig. 26.52 with the widths of the NMOS whose gates are tied to Vcm increased to 30.

Figure 26.63 Modifying the diff-amp seen in Fig. 26.53 for wider swing operation.

more power dissipation

more practical!