Talk CMFB

$-x^2 - x^4$

$\sim x^2 \sim x^4$

* REjECT CM
  NOISE

* even-order $\to 0$
  harmonics subtract at T

* charge injection
  CAP. feedthrough are CM so they subtract at T.

1)

$$(V_{o+} - V_{o-}) = A_{OL}(V_+ - V_-)$$

∞

0

$V_+ \to V_-$

V_{CMFB}
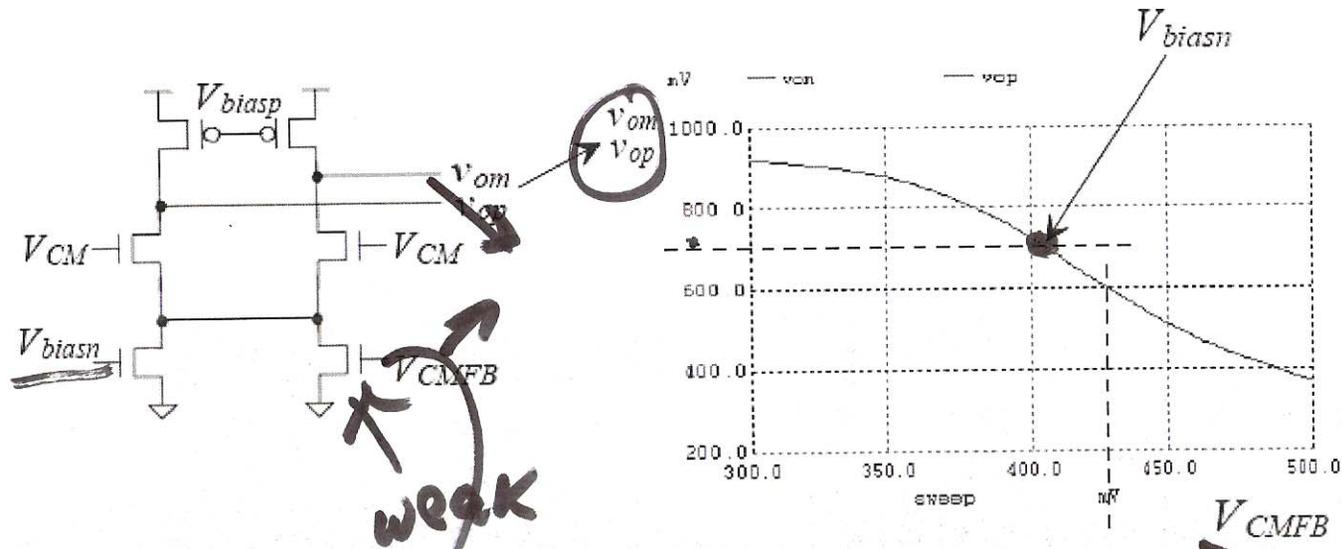
CMFB

NMOS 10/1
PMOS 20/1
Bias circuit from Fig. 26.3

WEAK

Value of CM feedback voltage
when the outputs are 600 mV.

Figure 26.17 Plotting the output voltages as a function of the CM feedback voltage.

$A_{cm} < 1$

2)

← outputs of op Amp
600mV → 580mV ← Ideal Amp
ANG. C_m voltage.

v_{op} v_{om}

ϕ_1 ϕ_2 ϕ_2 ϕ_1 V_{CM}

V_{CM}

C_1 C_2 C_2 C_1

V_{biasn} V_{biasn} 40mV

ϕ_1 ϕ_2 ϕ_2 ϕ_1

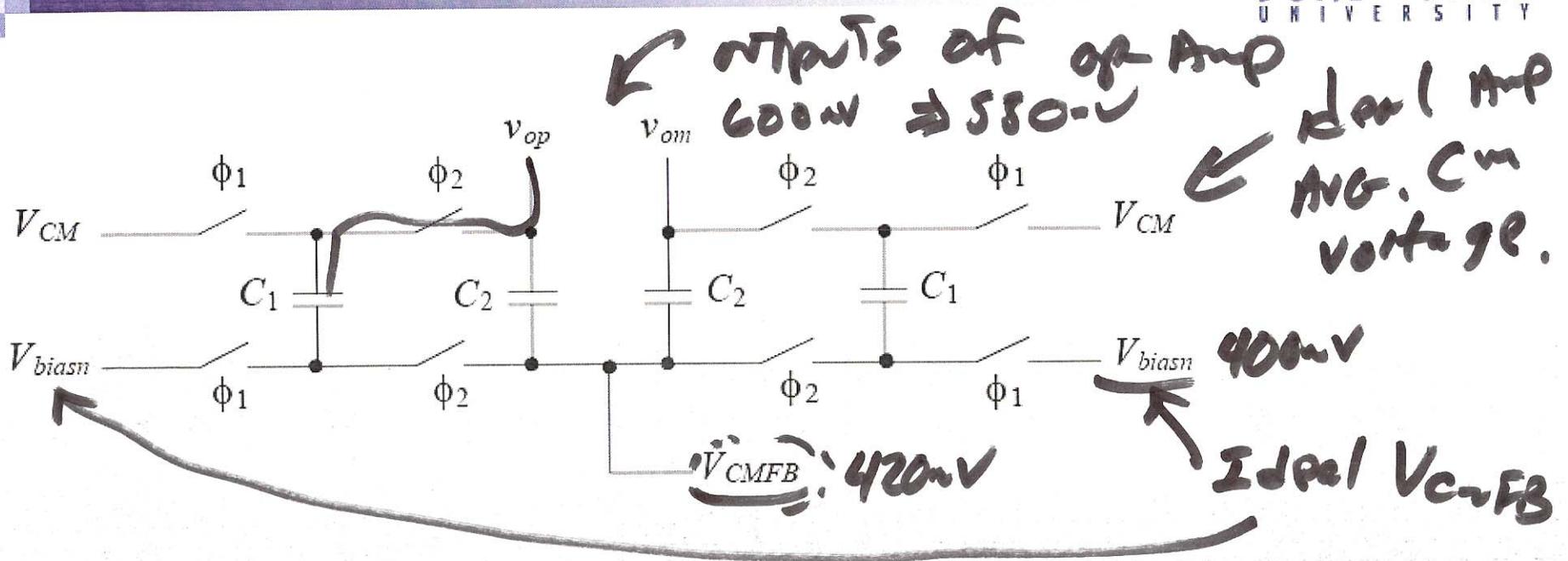$\dot{V}_{CMFB}$: 420mV ← Ideal V_{CMFB}
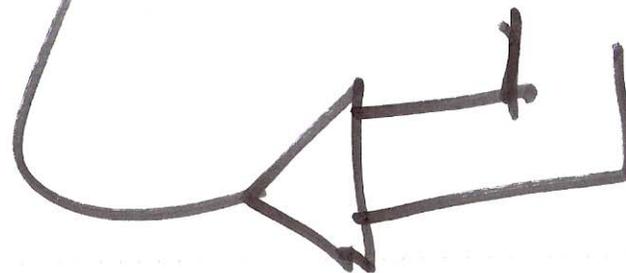
Figure 26.16 A switched-capacitor CMFB circuit.

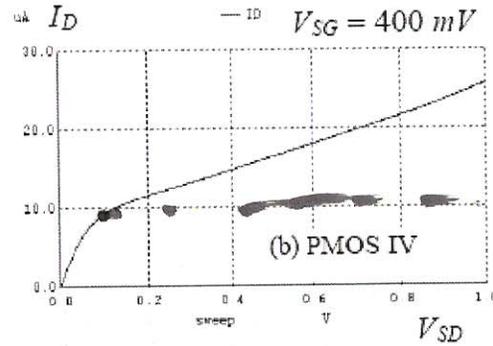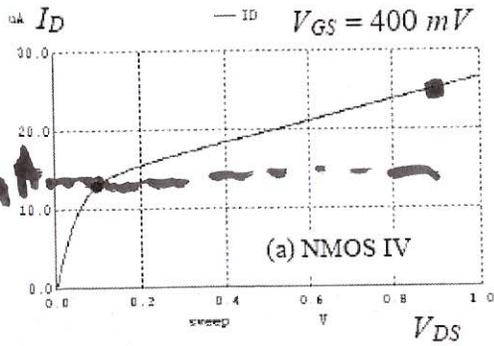ϕ_1 closed

$$q_1 = 2C_1 (V_{biasn} - V_{cm})$$

ϕ_2 closed

$$q_2 = (-V_{op} + V_{cmFB}) \cdot C_1 + C_1 (V_{cmFB} - V_{om})$$

$$\Delta V_{cmFB} = q_1 - q_2 = 2C_1 \left(V_{biasn} - V_{cmFB} + \frac{V_{op} + V_{om}}{2} - V_{cm} \right)$$
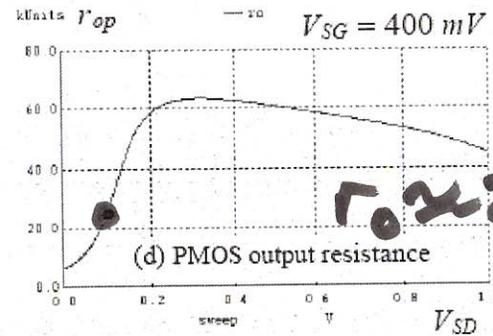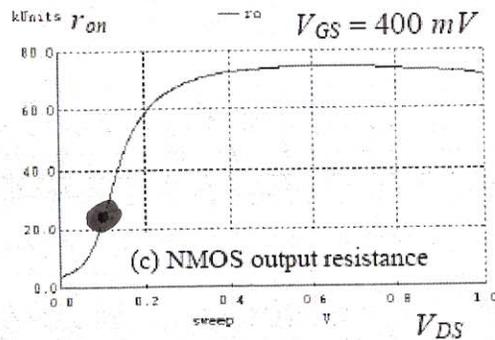
3)

Figure 26.18 Characteristics of NMOS (10/1) and PMOS (20/1) devices.

Handwritten annotations on figure:

(a) NMOS IV — $V_{GS} = 400\ mV$, I_D vs V_{DS} — "13µA"

(b) PMOS IV — $V_{SG} = 400\ mV$, I_D vs V_{SD}

(c) NMOS output resistance — r_{on}, $V_{GS} = 400\ mV$, r_o vs V_{DS}

(d) PMOS output resistance — r_{op}, $V_{SG} = 400\ mV$, r_o vs V_{SD} — "$r_o \approx 25K$"

(e) NMOS transconductance — g_{mn}, $V_{DS} = 100\ mV$ vs V_{GS}

(f) PMOS transconductance — g_{mp}, $V_{SD} = 100\ mV$ vs V_{SG}

Handwritten notes (right side):

going for speed
And low-power

V_{ov} ↗

$L \rightarrow$ minimum

$V_{DS} = 400mV$

$V_{SG} = 400mV$

$g_m = 150\ µA$

$g_m r_o = 150µ \cdot 25K$

≈ 6

4)

Vom

- - - - - - - - 1,000 mV = VDD
- - - - - - - - 600 mV
- - - - - - - - 800 mV
- - - - - - - - 400 mV

v_{om} —

$+v_{op}$ - - - - 600 mV ≈ V_{biasp}

- - - - - - - - 200 mV
- - - - - - - - 500 mV = V_{CM}
- - - - - - - - 100 mV
- - - - - - - - 100 mV

NMOS are 10/1
PMOS are 20/1
Bias circuit in Fig. 26.3

- - - - - - - - 400 mV = V_{biasn}

V_{biasn}

Note separate diff-amp connections.

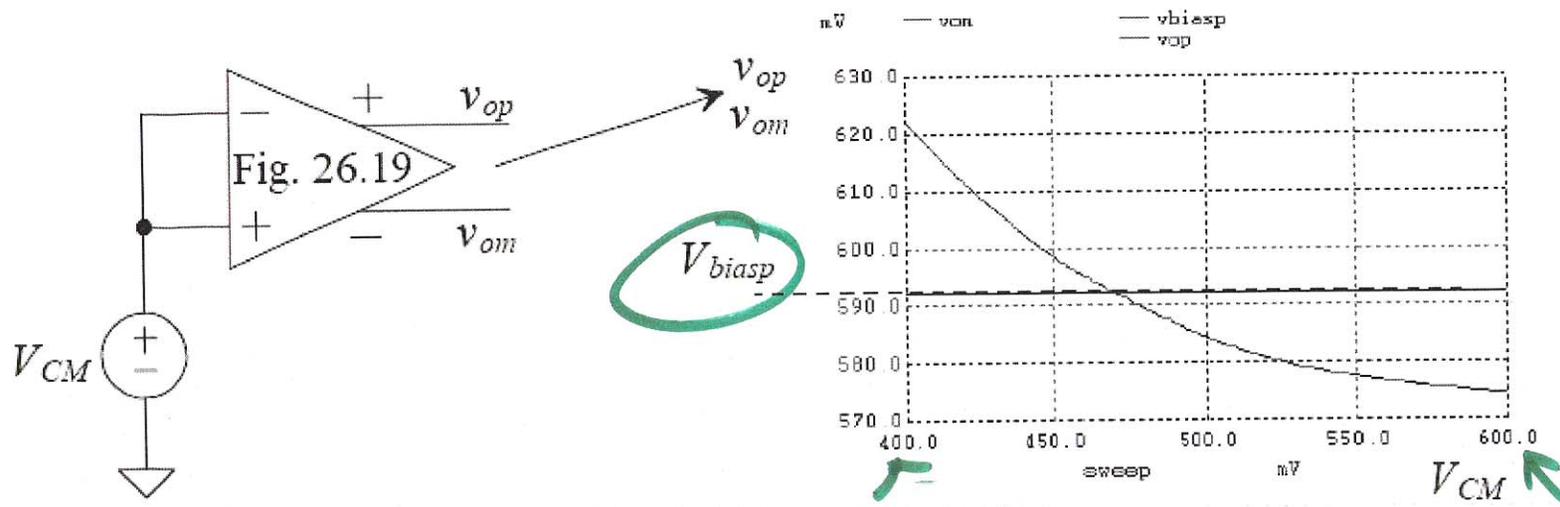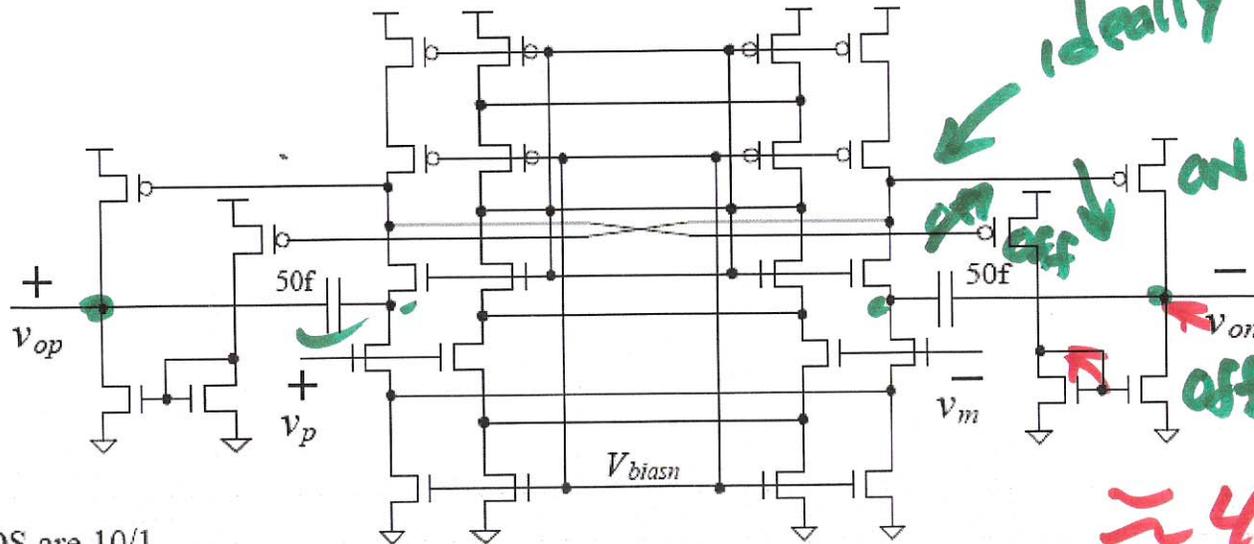**Figure 26.19** Fully-differential cascode diff-amp.

5)

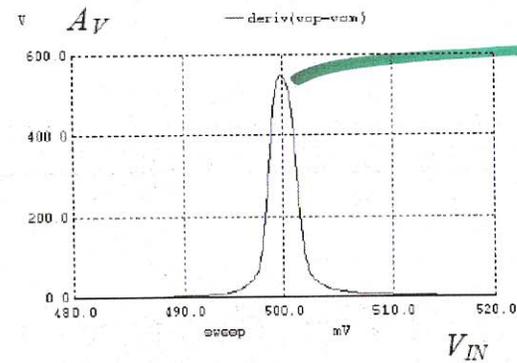**Figure 26.20** Varying the common-mode voltage and looking at the output.

b)

ideally $V_{DD} \cdot P$

on

off

Class AB operation

off

$\approx 40 cm$
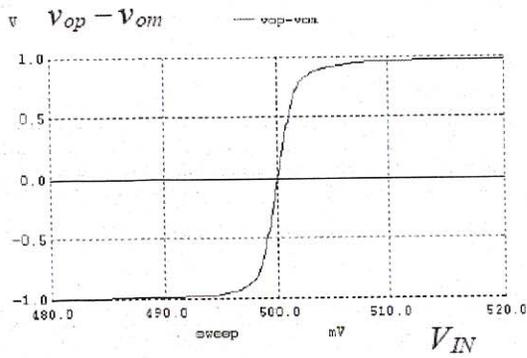
v_{op}

$+$

v_p

$+$

$50f$

$50f$

v_m

$-$

v_{om}

$-$

V_{biasn}
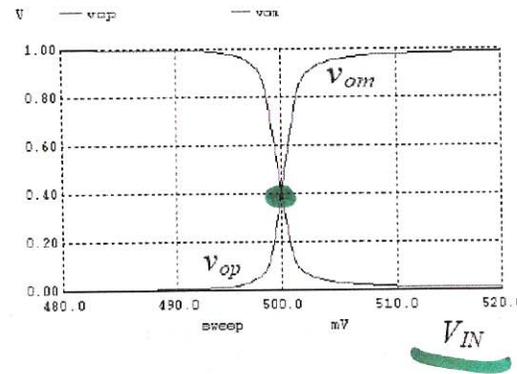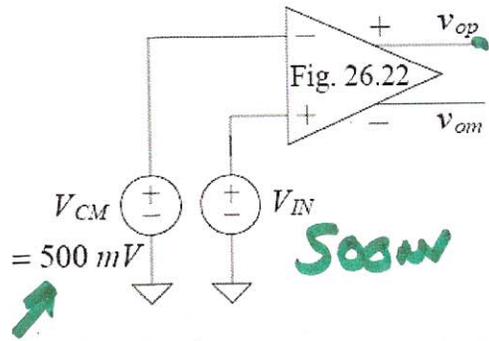
NMOS are 10/1
PMOS are 20/1
Bias circuit in Fig. 26.3

Figure 26.22 Basic two-stage op-amp without CMFB.
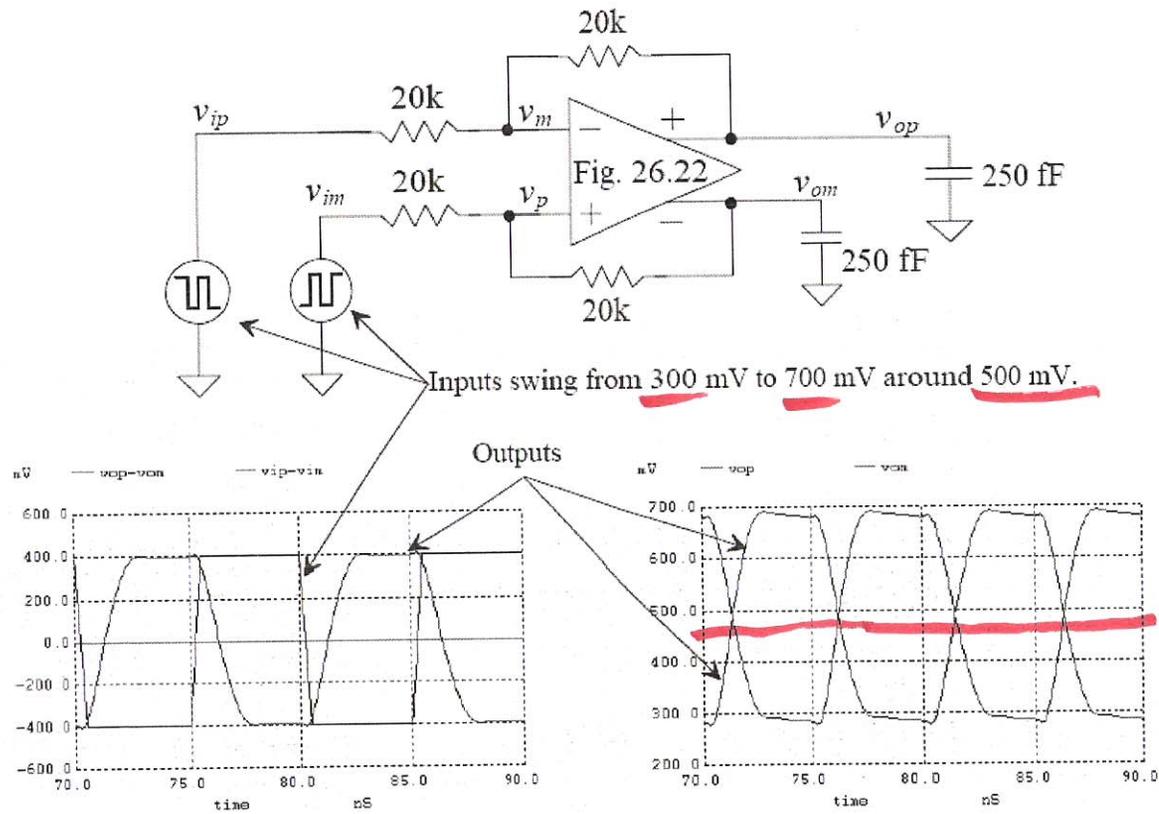
Figure 26.23 DC behavior and gain of the op-amp in Fig. 26.22.

Figure 26.24 Step response of the op-amp in Fig. 26.22 driving
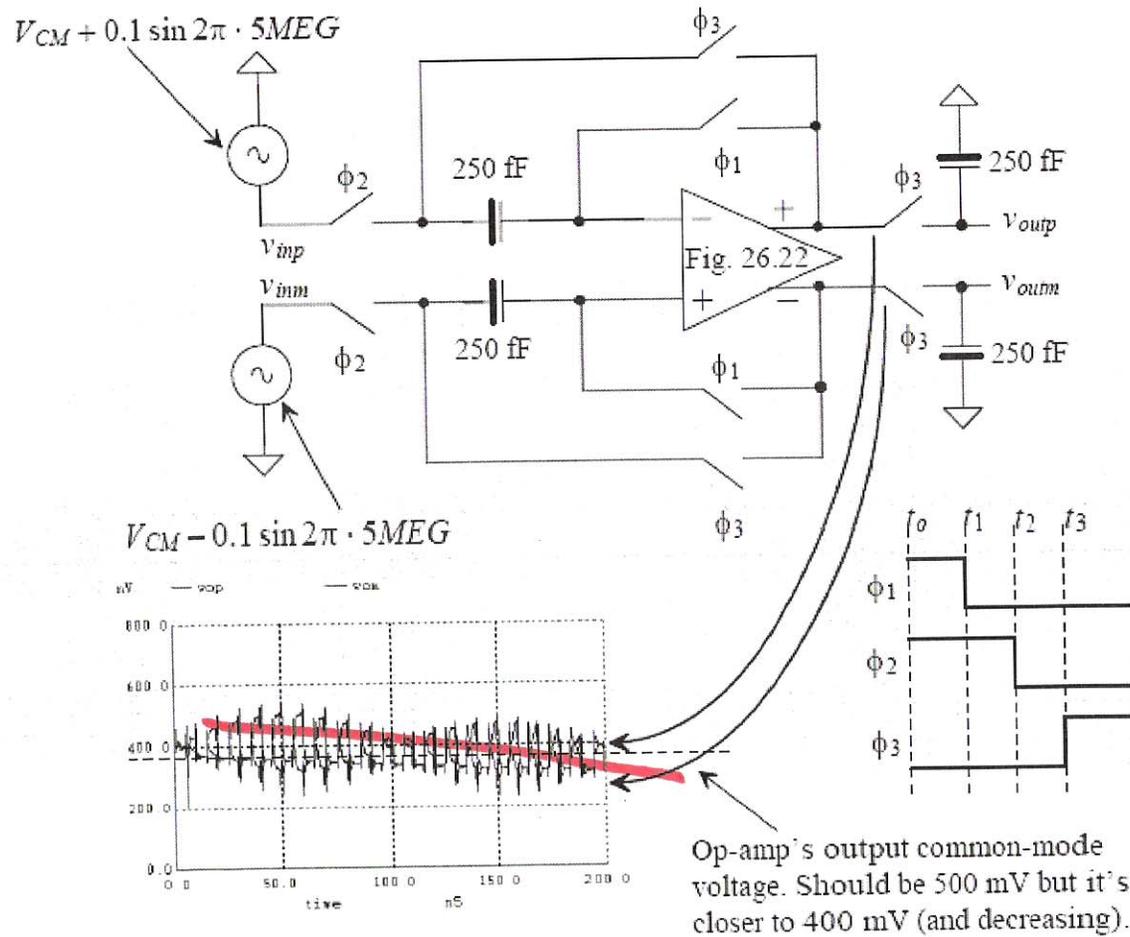250 fF load capacitors and 20k feedback resistors.

Figure 26.25 A sample-and-hold circuit. Notice how the output common-mode voltage is wandering.

Annotations on figure:

$V_{CM} + 0.1 \sin 2\pi \cdot 5MEG$

$V_{CM} - 0.1 \sin 2\pi \cdot 5MEG$

250 fF

ϕ_2

ϕ_1

ϕ_3

v_{inp}

v_{inm}

v_{outp}

v_{outm}

Fig. 26.22

Op-amp's output common-mode voltage. Should be 500 mV but it's closer to 400 mV (and decreasing).
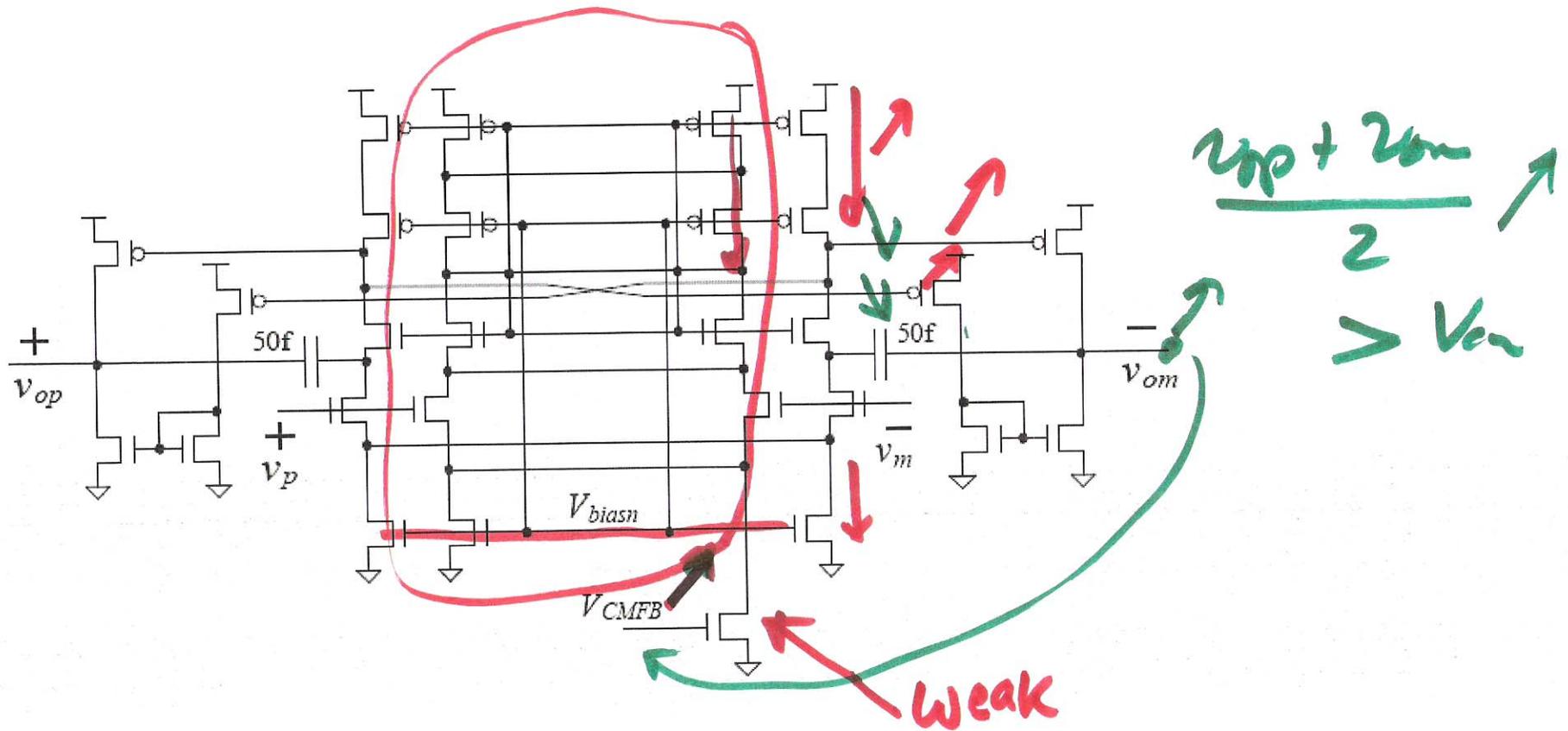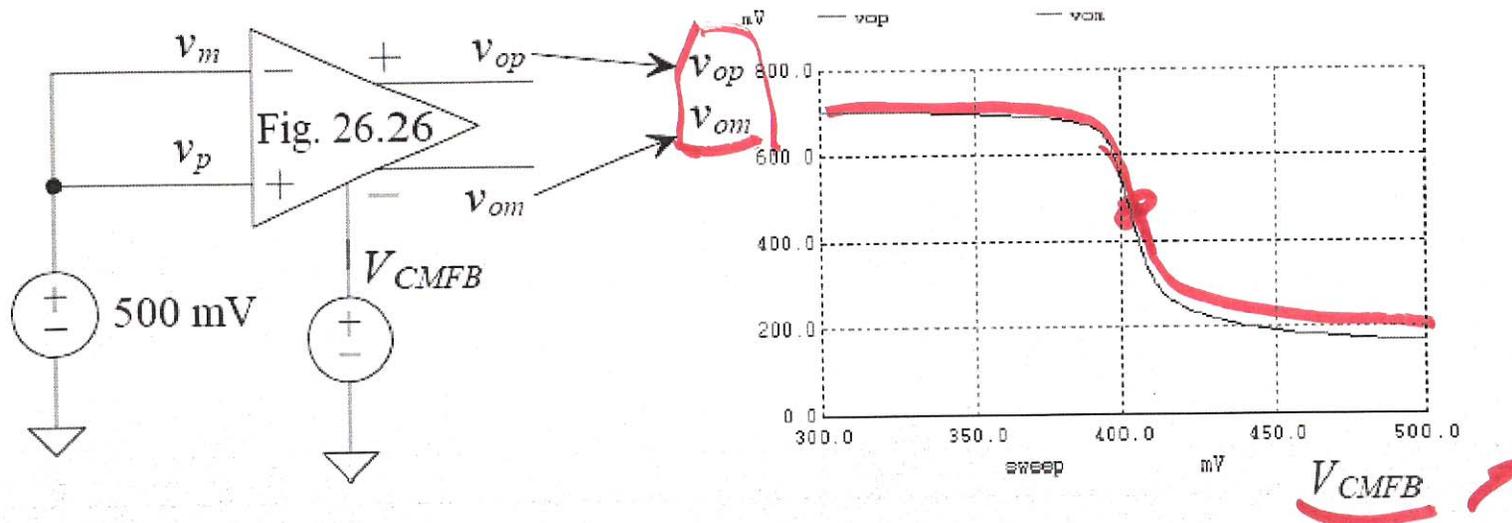
Bottom plate S/H

Figure 26.26 Modifying the op-amp for a CMFB input signal.

Figure 26.27 The CMFB input to output relationship. The gain is approximately 25 (considerably less than the forward differential gain).
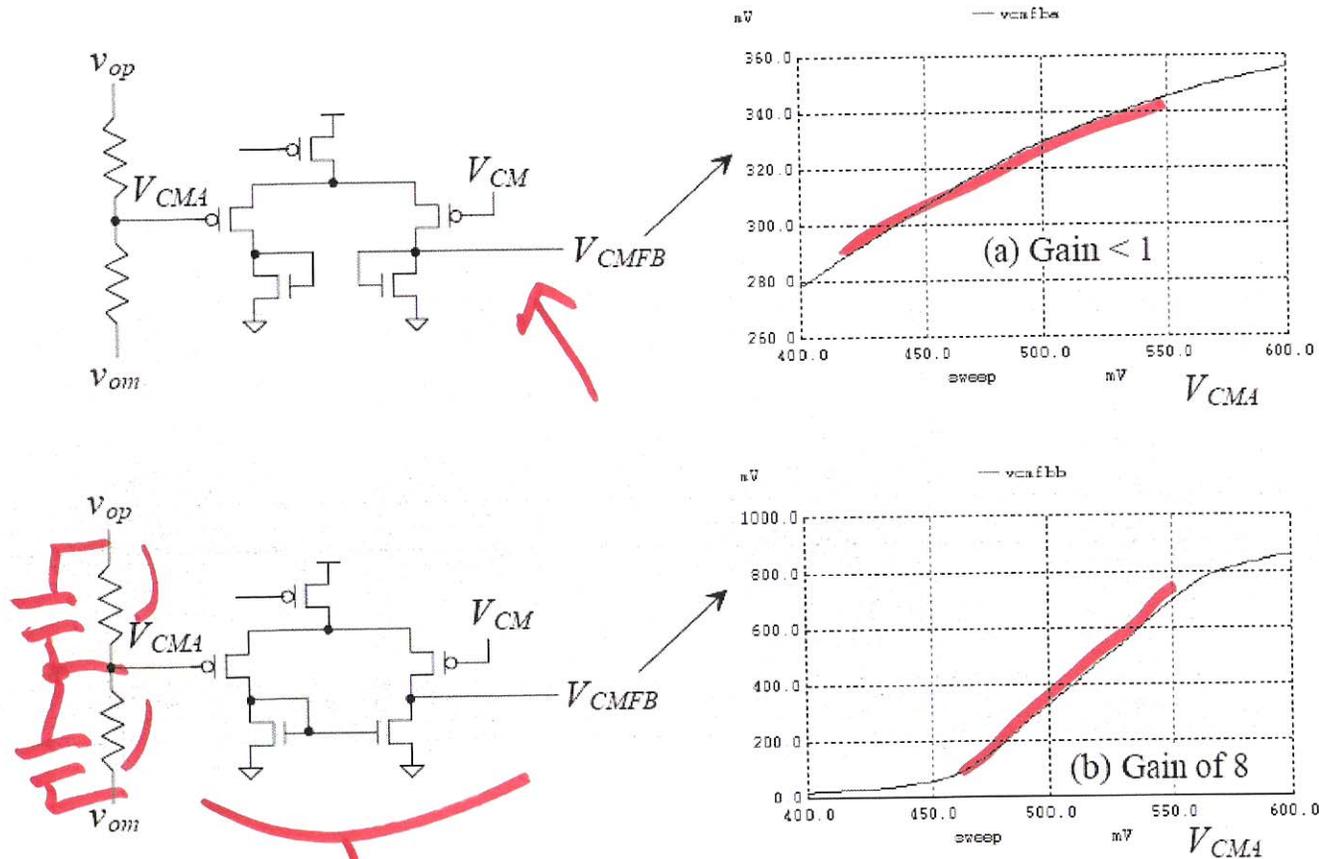
$A_{cm} < 1$

← CMFB Amplifier gain

12)

Figure 26.28 Gains of CMFB amplifiers.
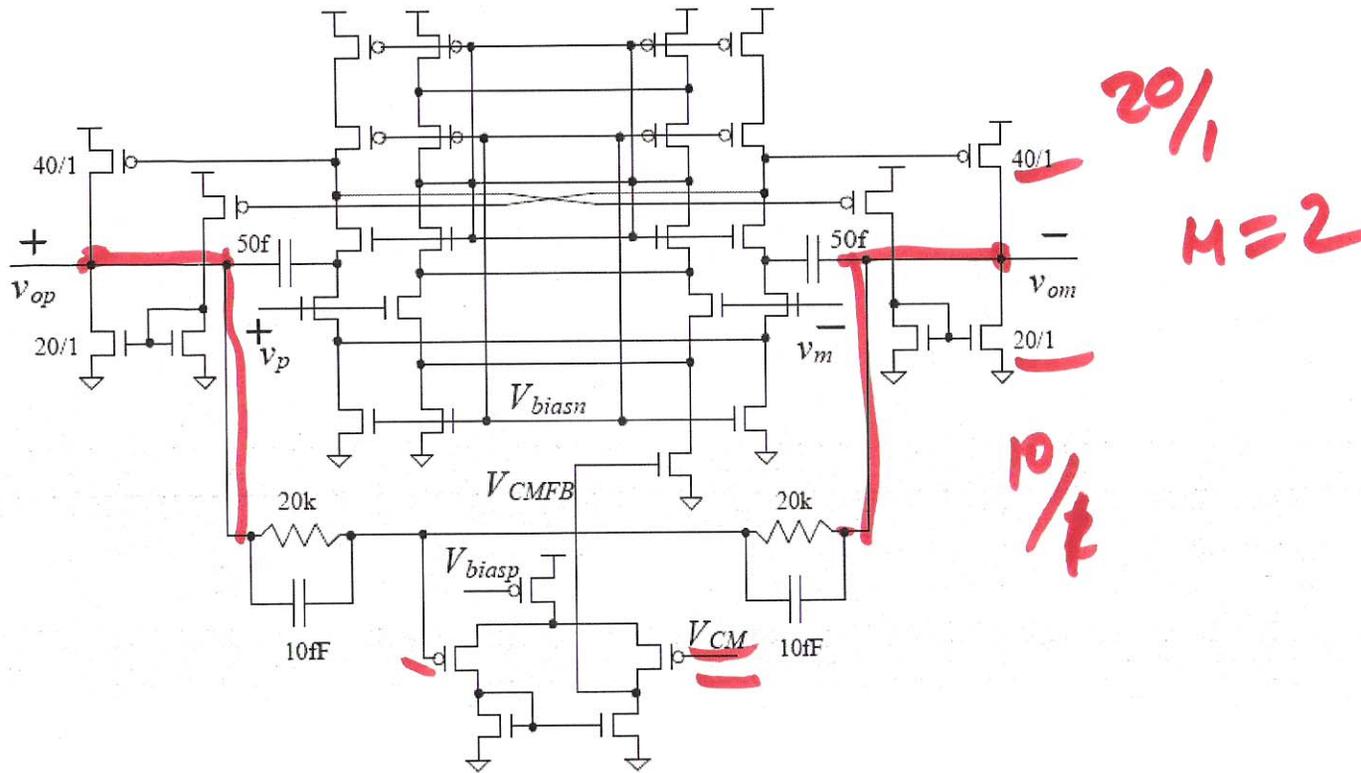
CAN use only if CMFB sigal goes to a weak transistor!

13)

Figure 26.29 Complete schematic of op-amp with CMFB.

14)