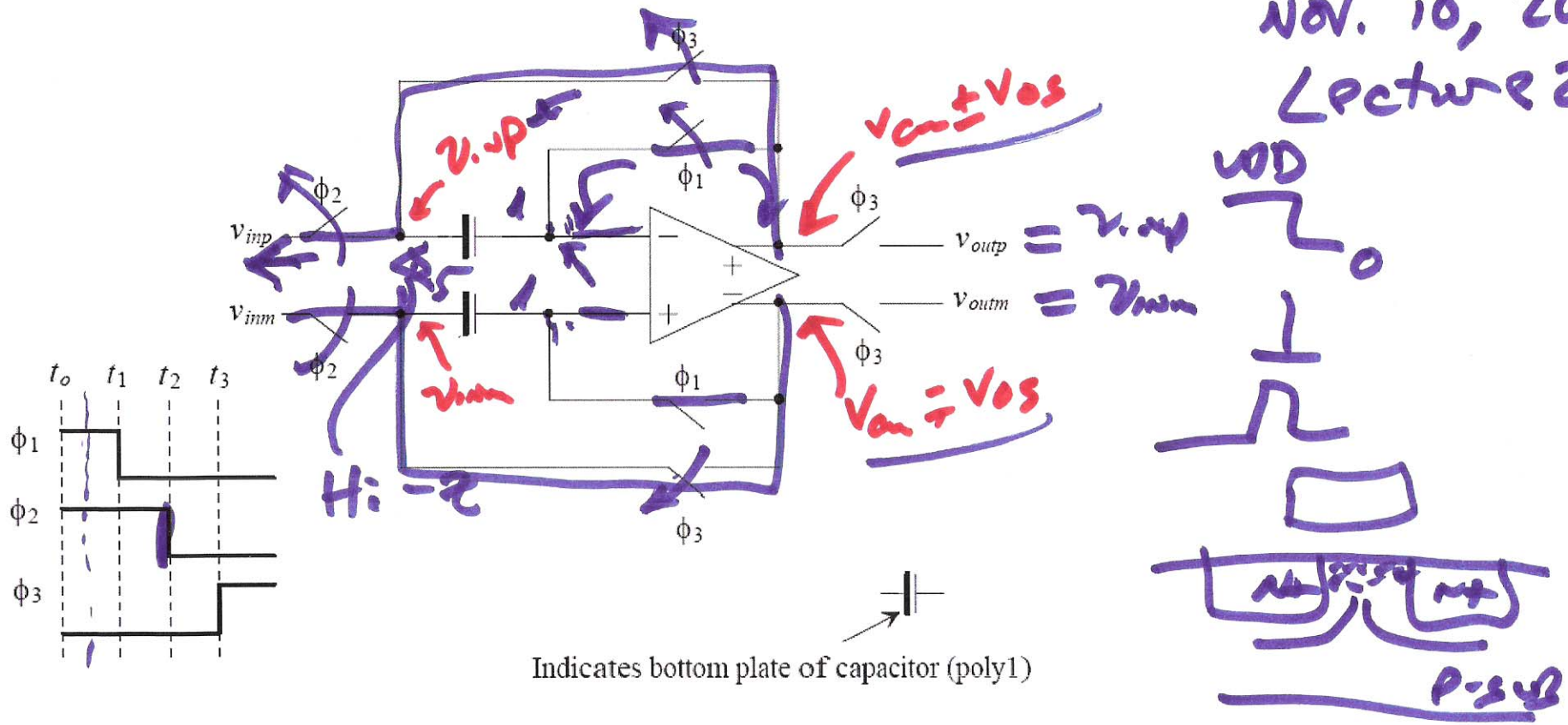
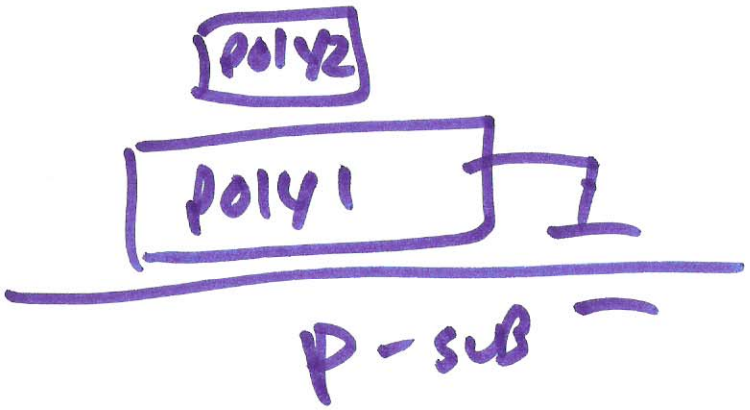


Figure 25.15 Sample-and-hold using differential topology.



1)

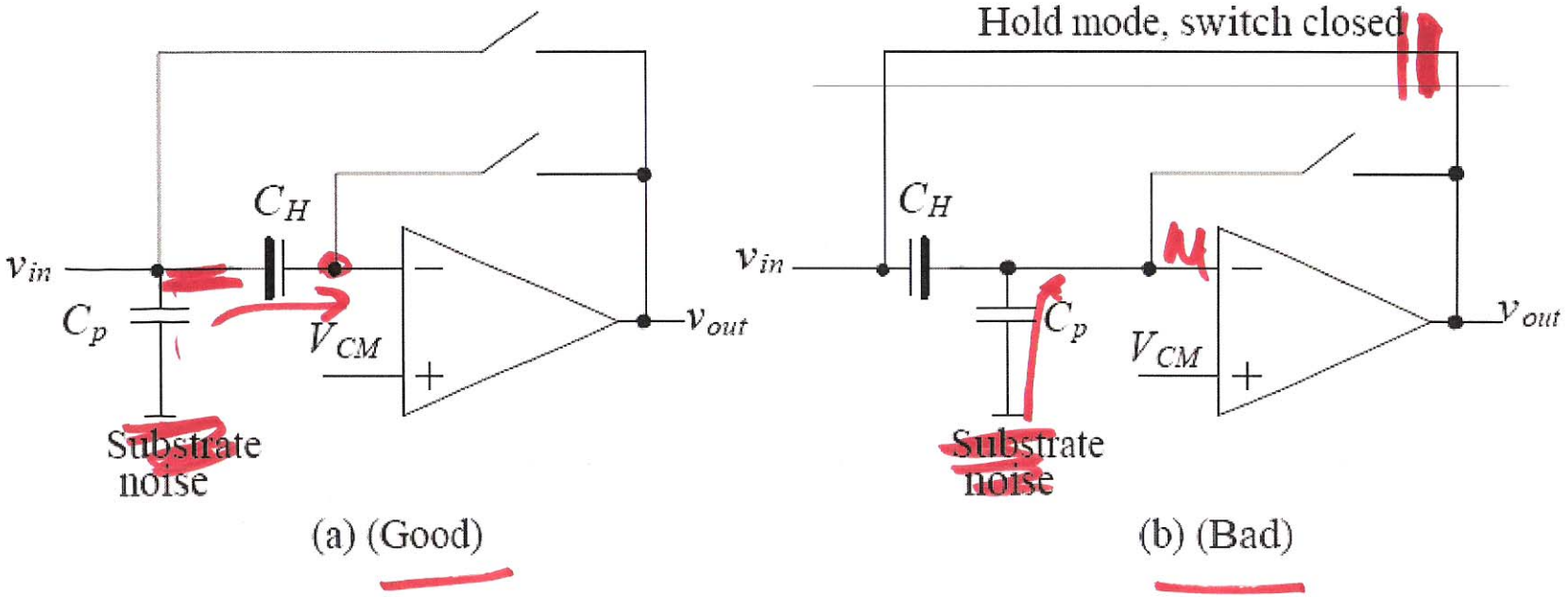
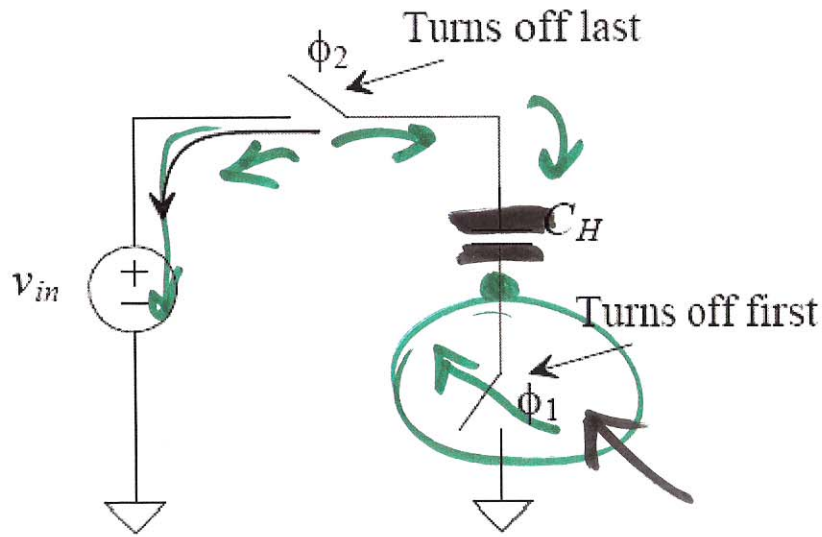


Figure 25.16 Explanation for connecting the bottom plate of the capacitor to the input.



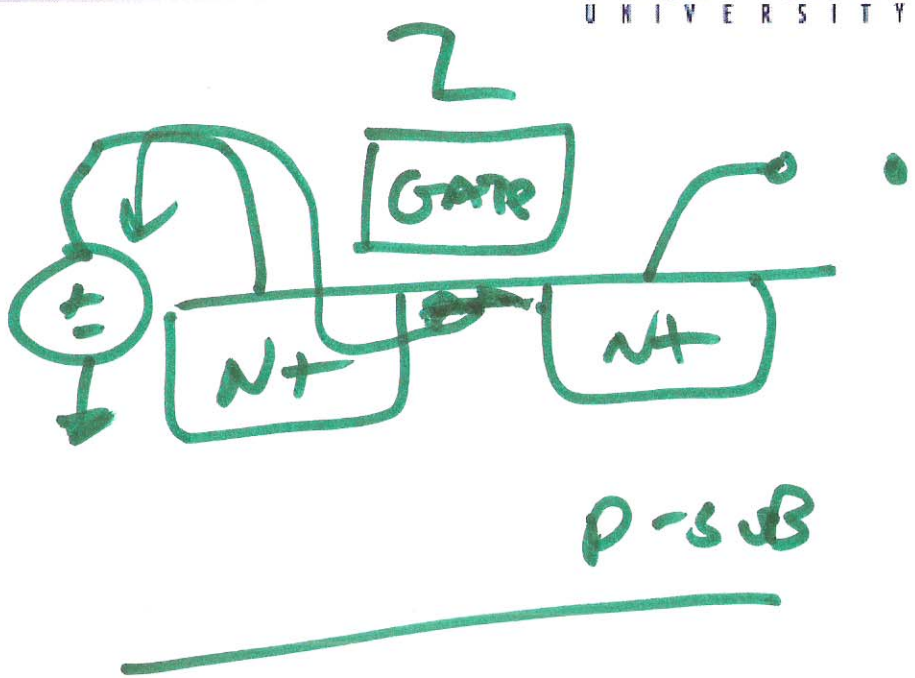
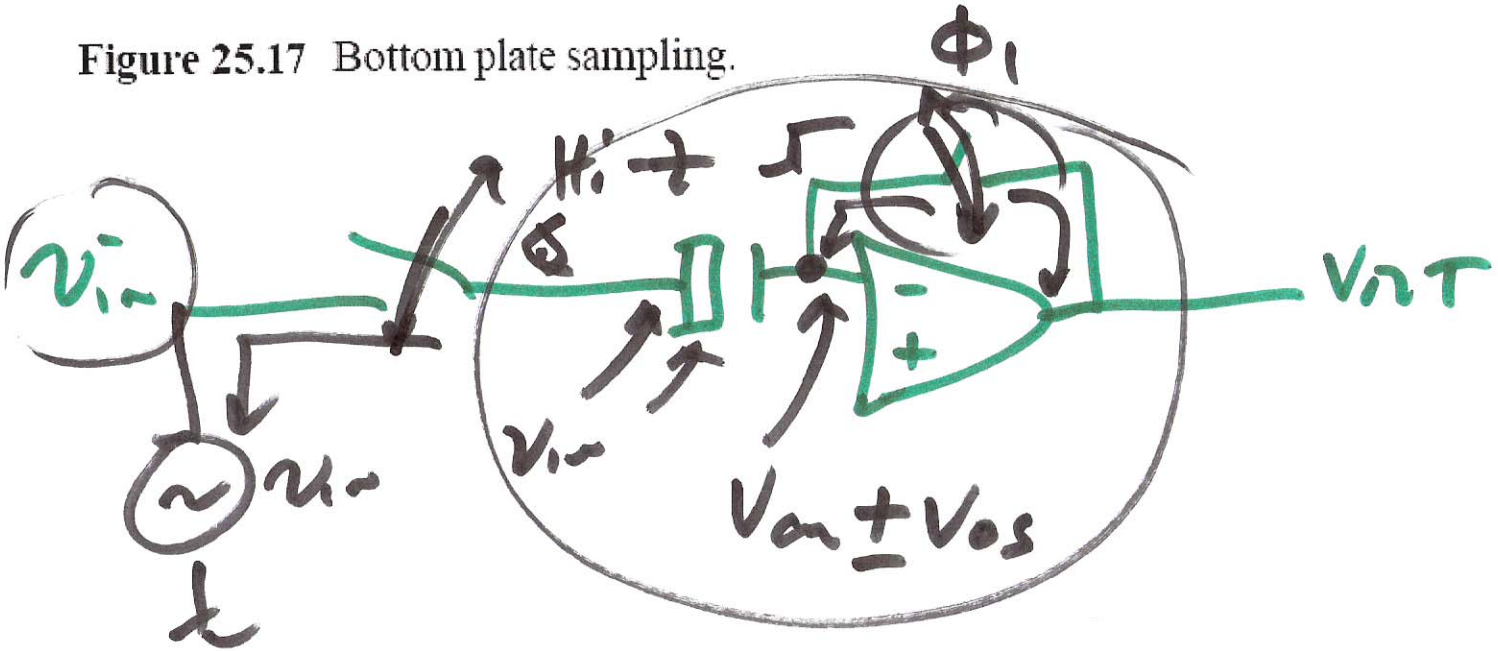


Figure 25.17 Bottom plate sampling.



3)

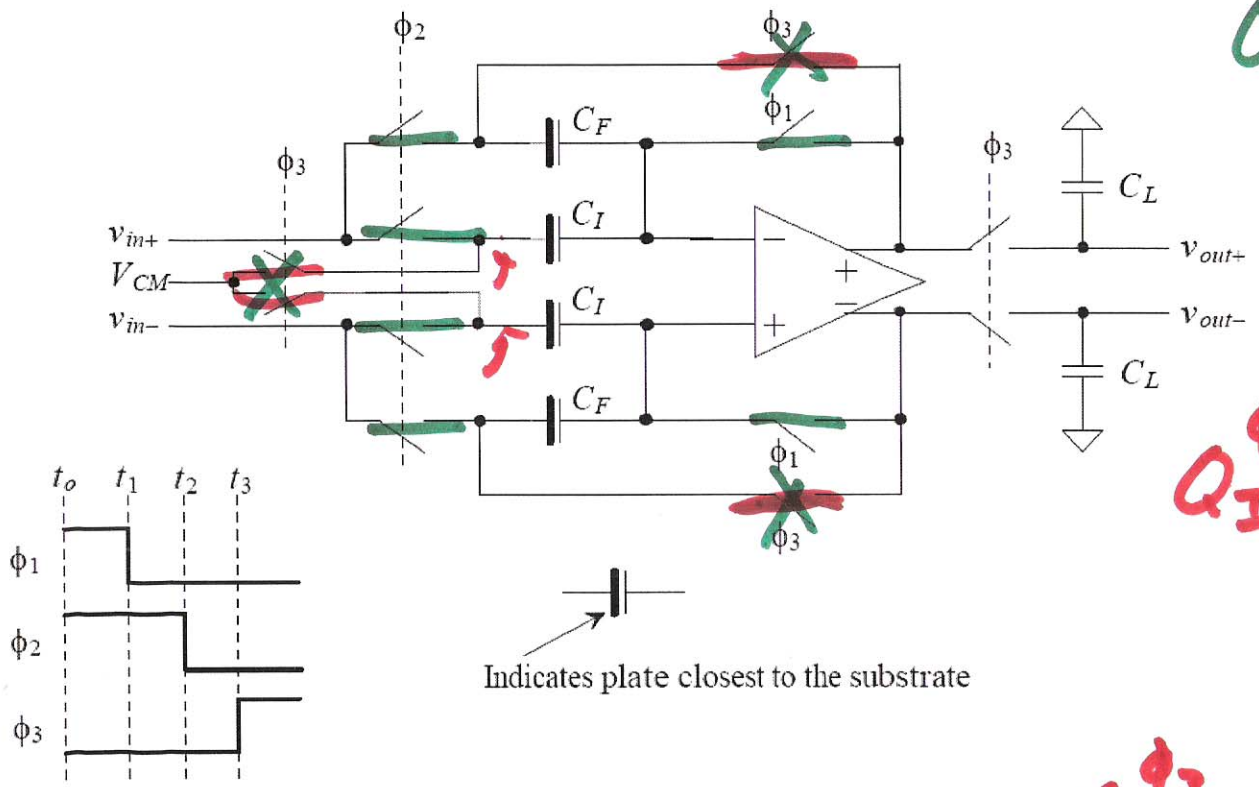


Figure 30.30 Data converter S/H building block.

$$Q_{I,F}^{\phi_1} = C_{I,F} \cdot \left(V_{IN} - (V_{cm} \pm V_{os})\right)$$

$$Q_I^{\phi_3} = C_I \cdot \left(V_{cm} - (V_{cm} \pm V_{os})\right)$$

$$Q_F^{\phi_3} = C_F\left(V_{OUT} - (V_{cm} \pm V_{os})\right)$$

$$\underbrace{C_F(V_{out} - V_{cm} \pm V_{os})}_{Q \text{ ON } C_F|_{\phi_3}} + \underbrace{C_I(V_{out} - V_{cm} \pm V_{os})}_{Q \text{ ON } C_I|_{\phi_3}} = \text{NEXT stage}$$

4)

$$= \underbrace{C_I\left(V_{IN} - V_{cm} \pm V_{OS}\right)}_{Q \text{ ON } C_I\,|_{\phi_1}} + \underbrace{C_F\left(V_{IN} - V_{cm} \pm V_{OS}\right)}_{Q \text{ ON } C_F\,|_{\phi_1}}$$

$$C_F\left(V_{OUT} - V_{cm} \pm V_{OS} - V_{IN} + V_{cm} \mp V_{OS}\right) =$$

$$C_I\left(V_{IN} - V_{cm} \pm V_{OS} \mp V_{OS}\right)$$

$$C_F\left(V_{OUT} - V_{IN}\right) = C_I\left(V_{IN} - V_{cm}\right)$$

$$C_F V_{OUT} = V_{IN} C_I\left(1 + \frac{C_F}{C_I}\right) - C_I \cdot V_{cm}$$

$$V_{outT} = \left(1 + \frac{C_I}{C_F}\right) V_{in} - \frac{C_I}{C_F} \cdot V_{cm}$$

Notice no opAmp offset!

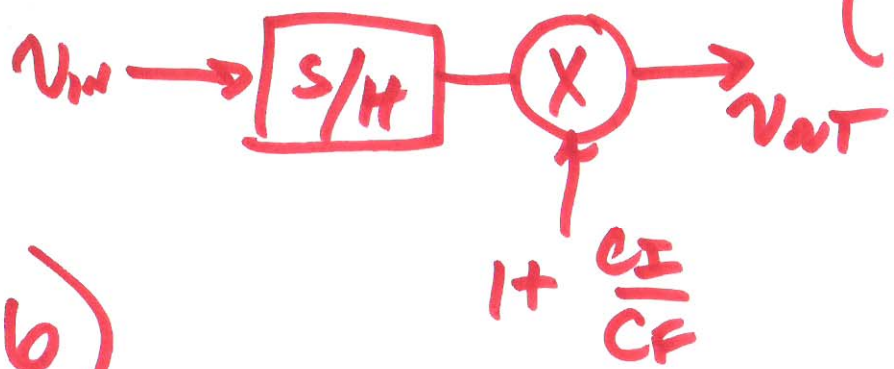
→ 1000 = A_{OL}

V_{os} = 50mV

$$\frac{V_{os}}{A_{OL}} = \underline{\underline{50nV}}$$

$V_{outT} = V_{outT+} - V_{outT-}$ =

$$\left(1 + \frac{C_I}{C_F}\right)\underbrace{(V_{in+} - V_{in-})}_{V_{in}}$$



6)

8-cyclic ADC

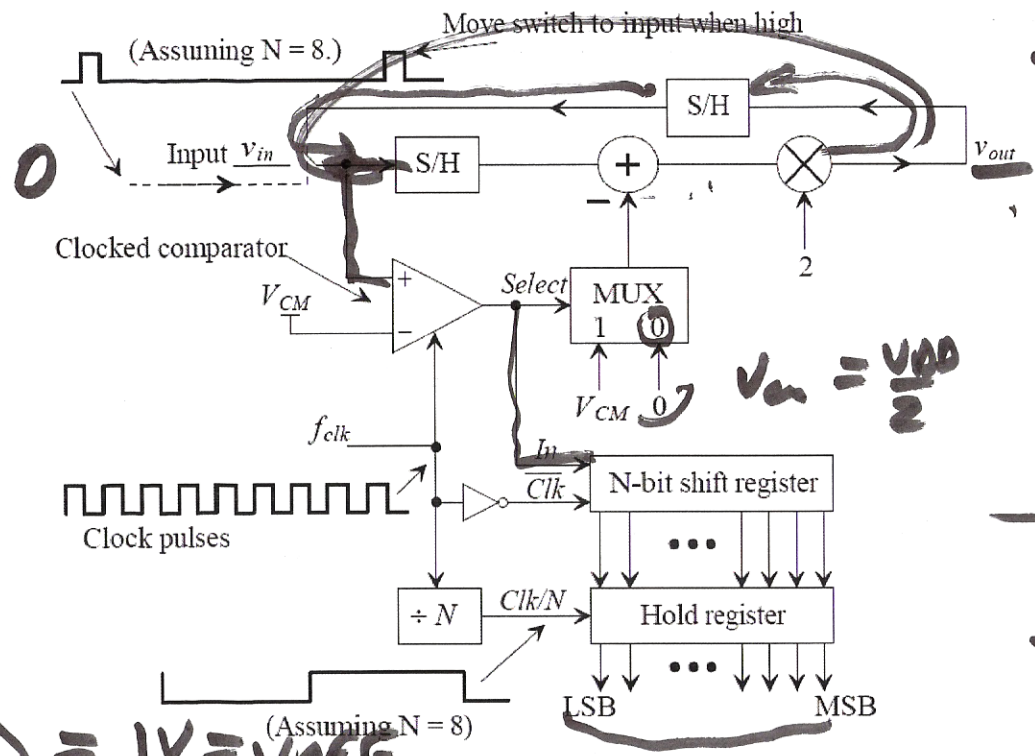


Figure 30.38 Block diagram of a cyclic ADC.

N	INPUT	Vout	bit
1	0	0	0
2	0	0	0
3	0	0	0
⋮			⋮
			0

$V_m = \frac{V_{DD}}{2}$

1	VDD	VDD	1
2	VDD	VDD	1
⋮			⋮
			1

$VDD = 1V = V_{REF}$

$1LSB = \frac{1}{256} \approx 4mV$

1	600mV	200mV	1
2	200mV	400mV	0
3	400mV	800mV	0
4	800mV	600mV	1
5	600mV	200mV	1

256 / 128 / 64 / 32 / 16 / 8 / 4 / 2 / 1

512 → 1001

$V_m = 500mV$

512 / 64 / 32 = 608

7)

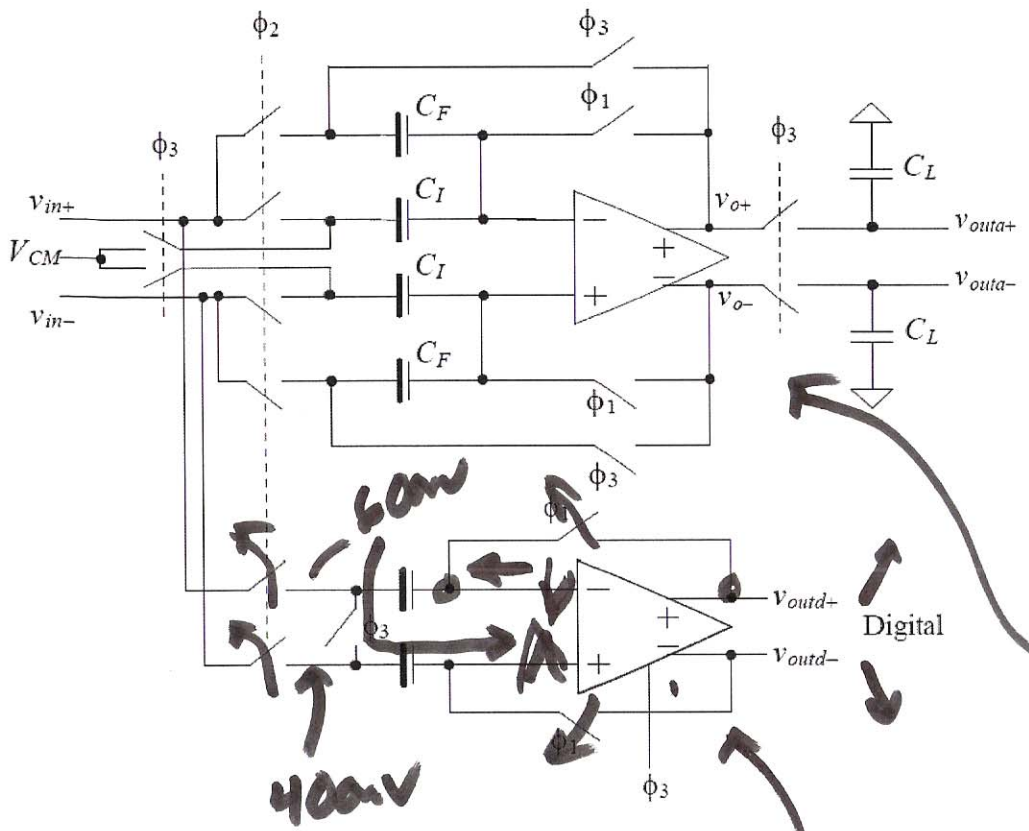
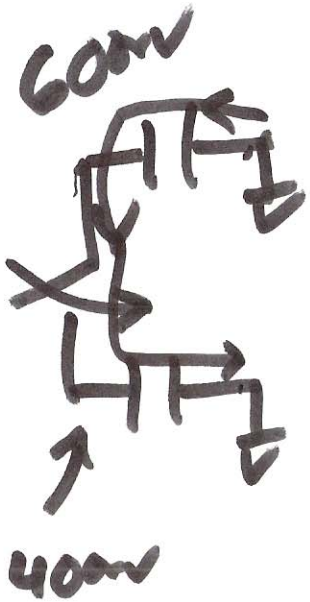


Figure 30.39 Implementation of the comparator with an S/H for use in a cyclic ADC.



Capacitor error averaging!

1.5 bits/stage RSD

8)

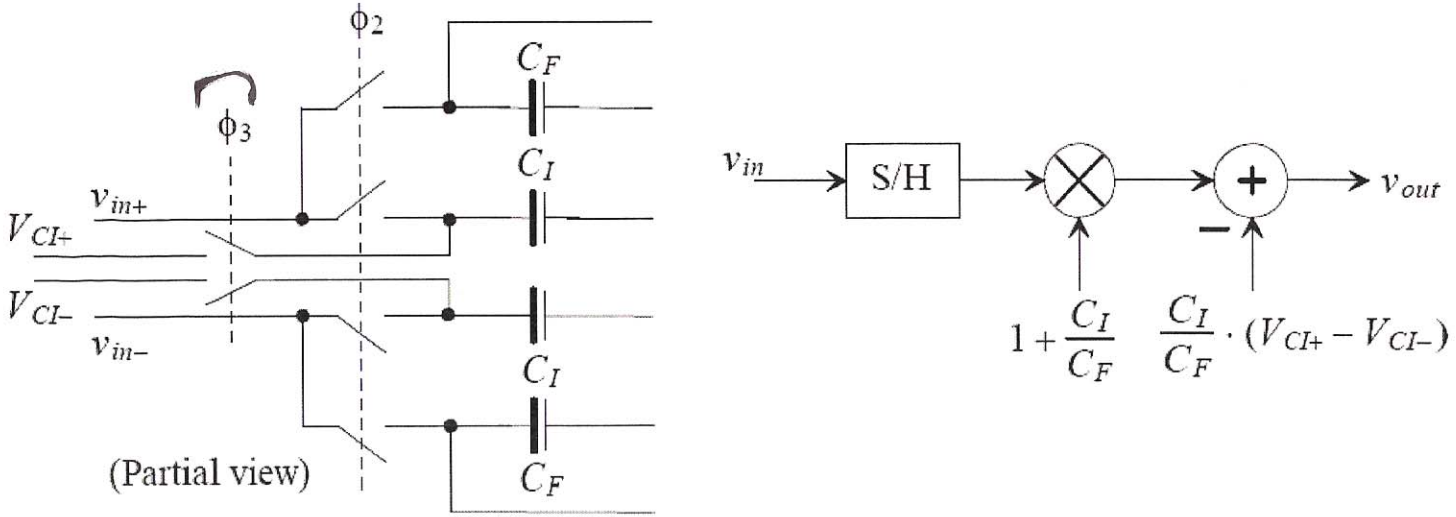


Figure 30.40 Implementing subtraction in the S/H.

$$C_F(V_{OUT} - V_{os} \pm V_{os}) + C_I(V_{CI} - V_{os} \pm V_{os}) =$$

$$C_I(V_{IN} - V_{os} \pm V_{os}) + C_F(V_{IN} - V_{os} \pm V_{os})$$

9) $$C_F V_{OUT} = C_I V_{IN} - C_I V_{CI} + C_F V_{IN}$$

$$V_{OUT+} = \left(1 + \frac{C_I}{C_F}\right) V_{in+} - \frac{C_I}{C_F} \cdot V_{CI+}$$

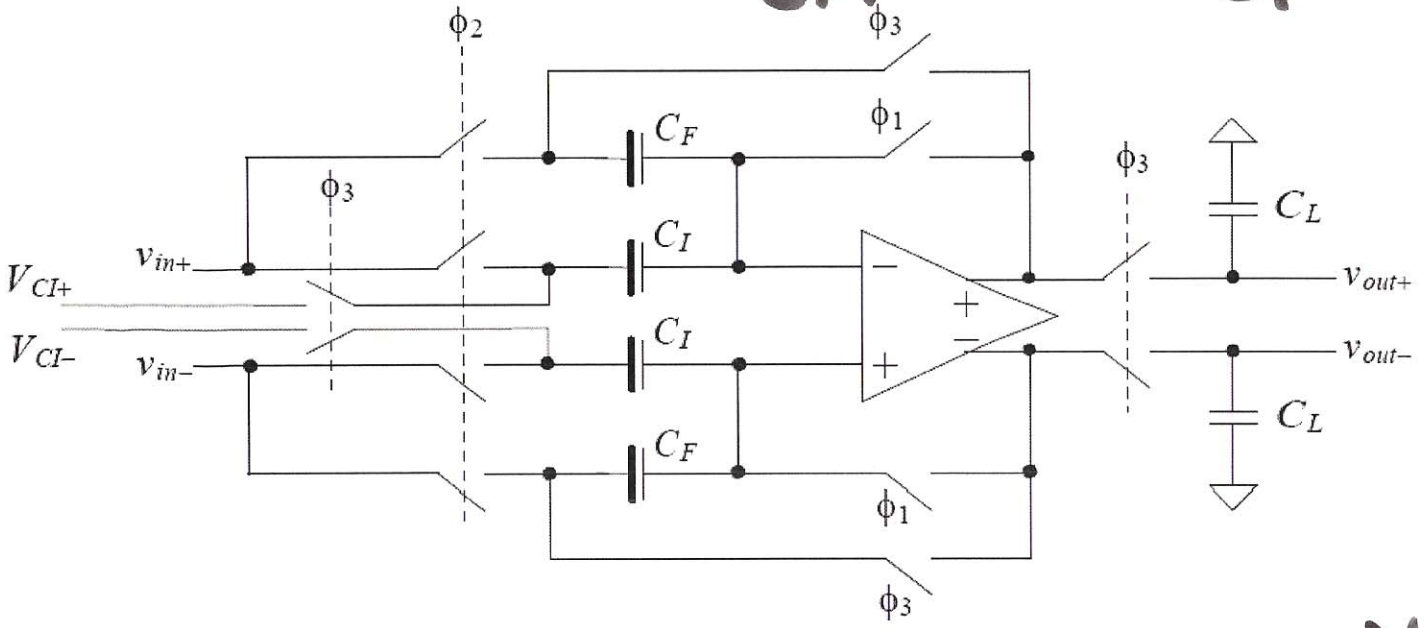


Figure 30.42 S/H used in Ex. 30.12

$$V_{CI} = V_{CI+} - V_{CI-}$$

$$V_{OUT} = \left(1 + \frac{C_I}{C_F}\right) V_{in} - \frac{C_I}{C_F} V_{CI}$$

10)

Single-ended

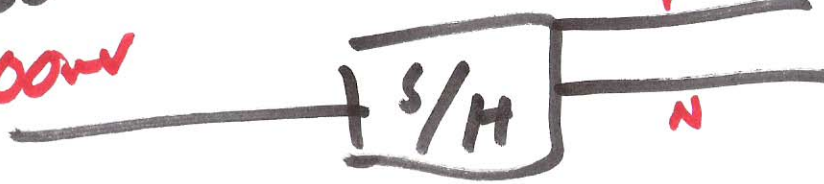
Diff.

$V_{cm} = 500mV$ $= V_{1,2}$

$V_{DIFF} = 0$

600mV

400mV



$V_{DIFF} = 100mV$ $= -100mV$

1V → 750mV

250mV

$V_{DIFF} = 500mV$

0V → 250mV

750mV

$V_{DIFF} = -500mV$

11)