ECE614 – Lecture 19

2-step flash ADC

Opamp → Residue

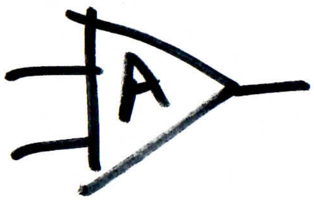
8-bit Flash

Accuracy issues with opamp

↳ Gain ($2^{N/2}$)

↳ S/H

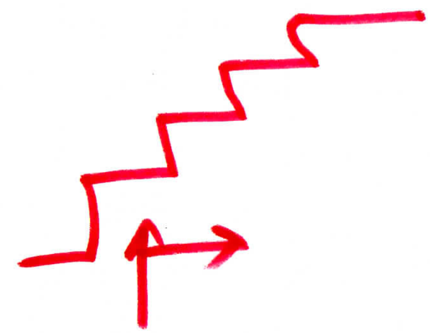
↳ subtraction



opamps

↳ offset (V_{os})

- noise
- f_{un} ✓
- A_{OL} ✓ (DC OL gain)
- SR



$\frac{1}{2}$ LSB → $\Delta V < \left(\frac{V_{REF}}{2^{N+1}}\right)$

B-993

Closed Loop gain $1/\beta = 2^{N/2}$

Linear non-idealities

- $|A_{OL}| \geq \frac{2^{N+1}}{\beta}$
- $f_{un} \geq \frac{f_{clk} \cdot \ln(2^{N+1})}{\pi \cdot \beta}$ (Assuming Linear Settling

$$A(s) = \frac{A_{OL}}{\left(1 + \frac{s}{2\pi f_{un}}\right)}$$

Pipelined ADC

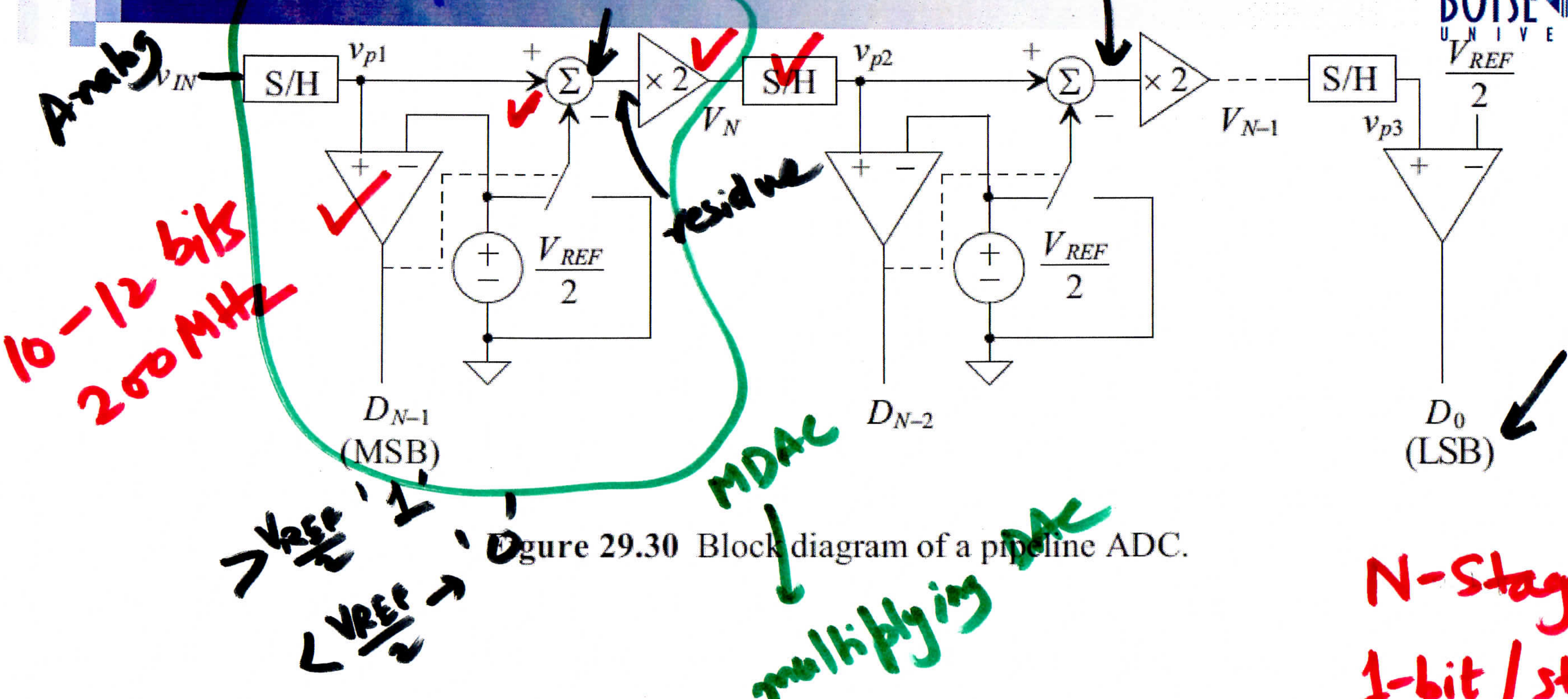
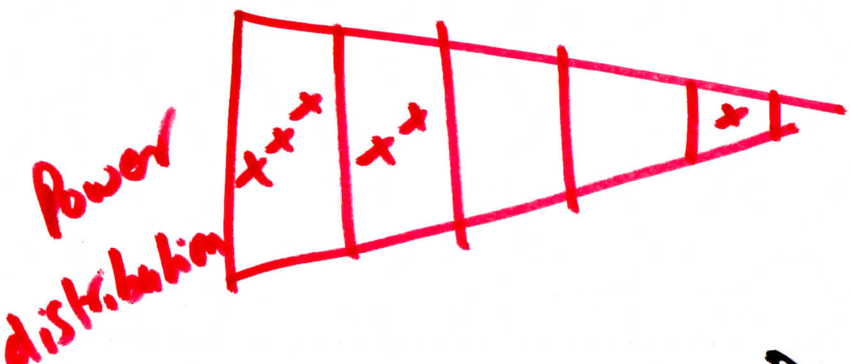


Figure 29.30 Block diagram of a pipeline ADC.

N-Stages

1-bit / stage

N-cycle latency



→ Not enough gain in nano-cmos

* Digital Assistance Technique
  * Calibration
  * Adaptive Filter

Integrating ADC (single-slope)

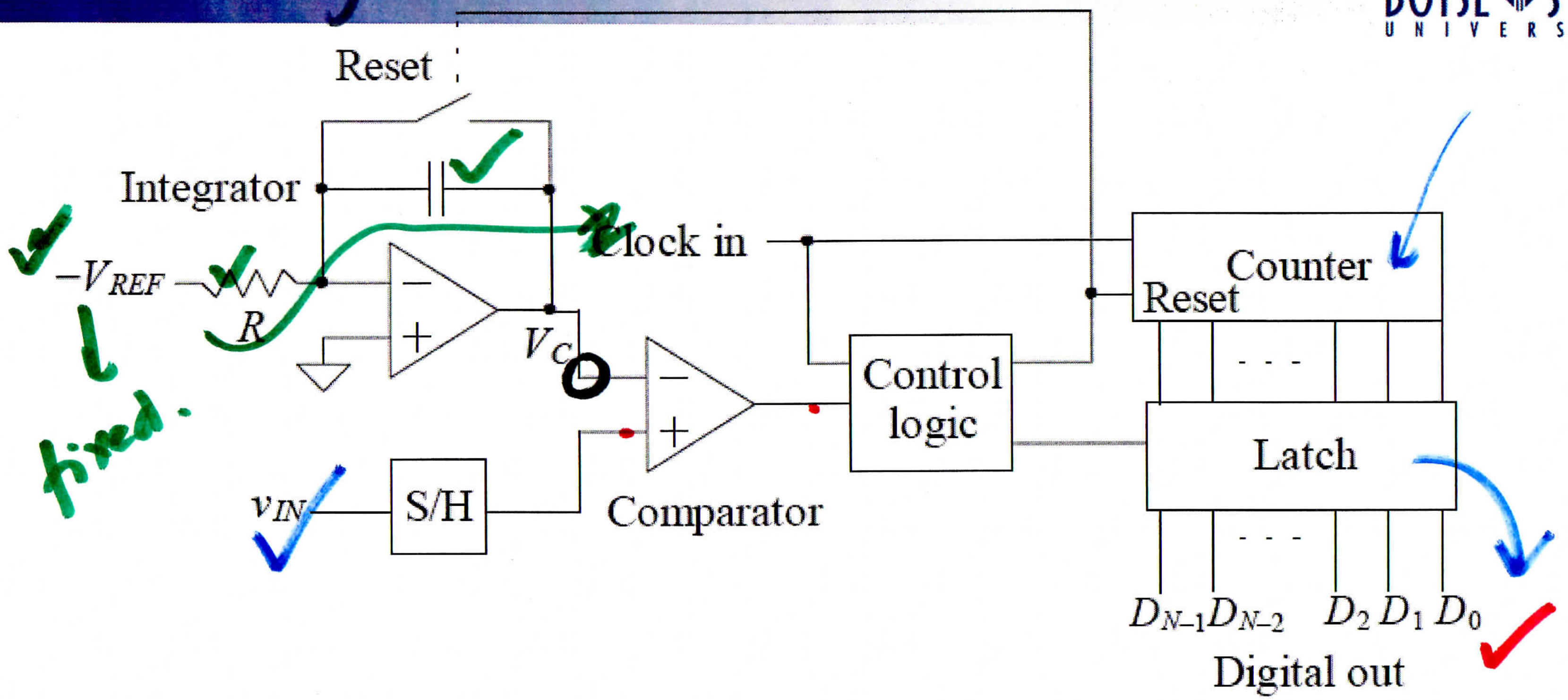
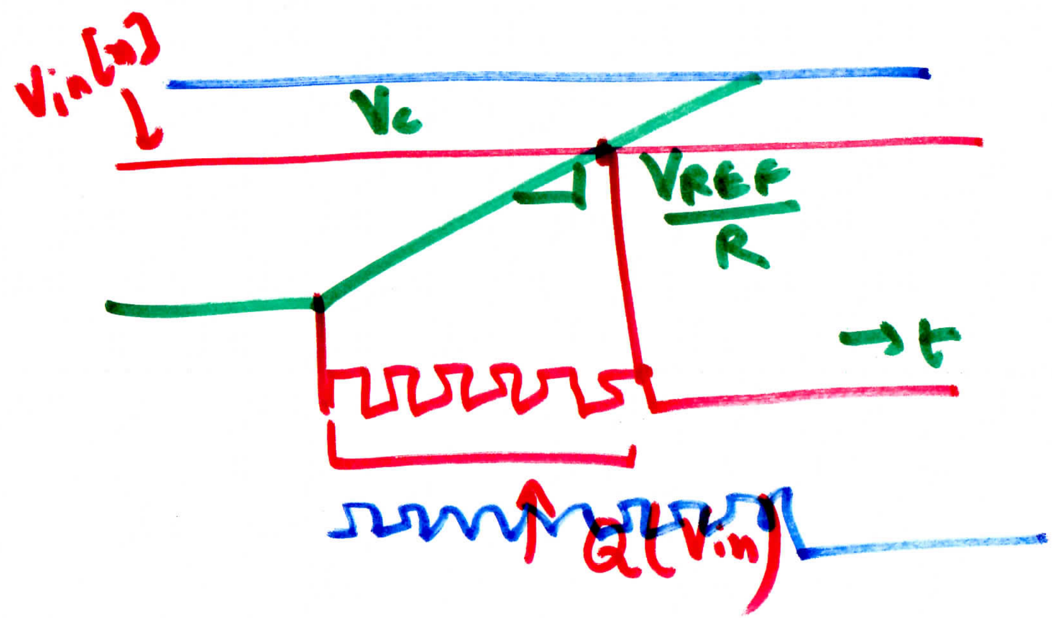


Figure 29.32 Block diagram of a single-slope ADC.

$$I = \frac{V_{REF}}{R}$$



(7)

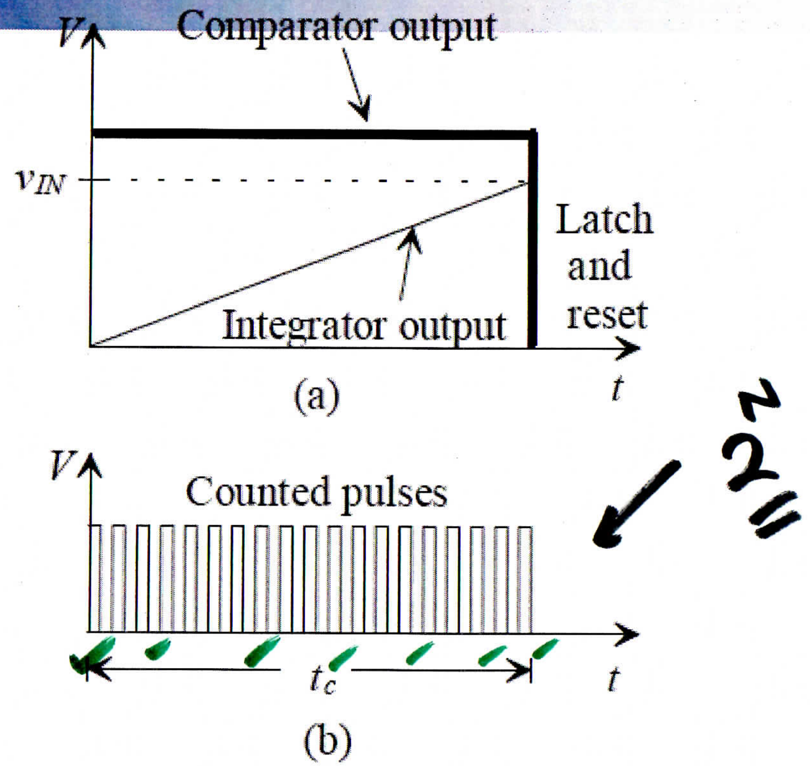


Figure 29.33 Single-slope ADC timing diagrams for (a) the comparator inputs and outputs and (b) the resulting counted pulses.

$$t_c = \frac{V_{in}}{V_{REF}} \cdot 2^N \cdot T_{CLK}$$

$$V_c = \frac{2^N \cdot V_{in}}{f_{CLK} \cdot RC}$$ → ±15%

Dual Slope ADC

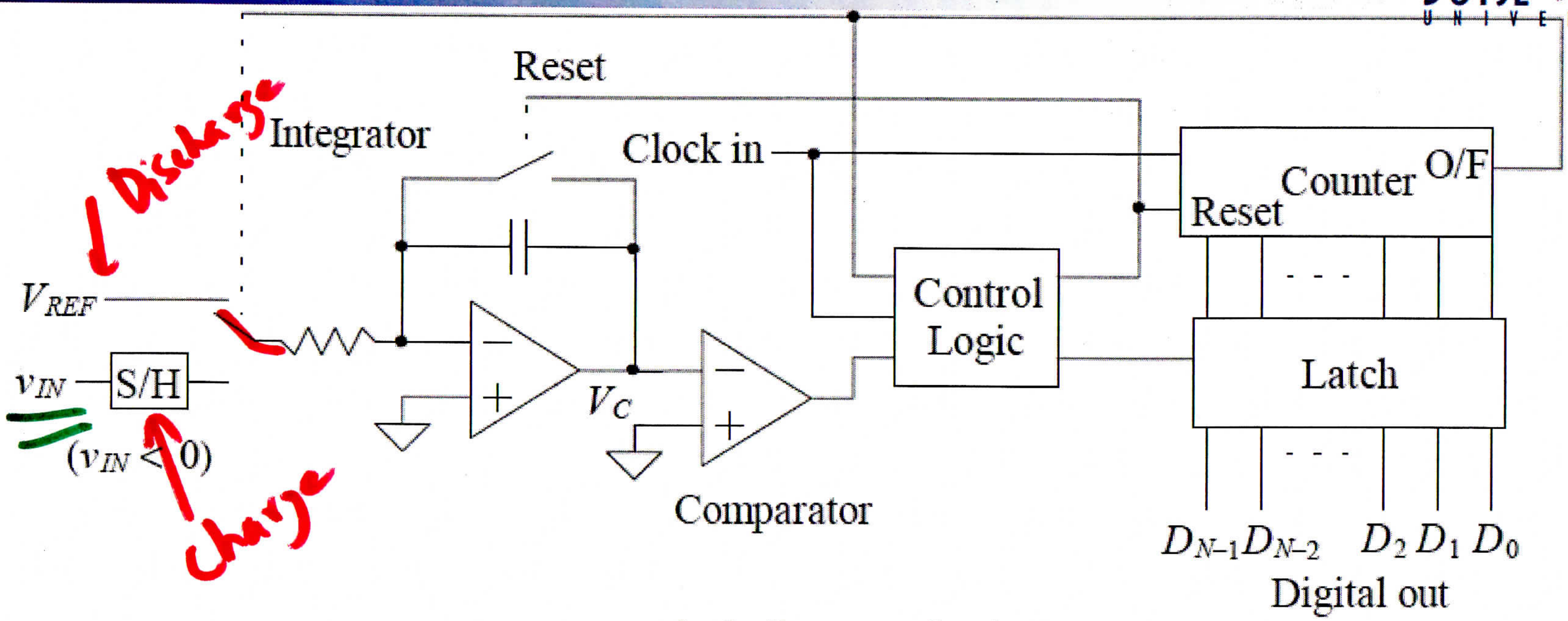


Figure 29.34 Block diagram of a dual-slope ADC.

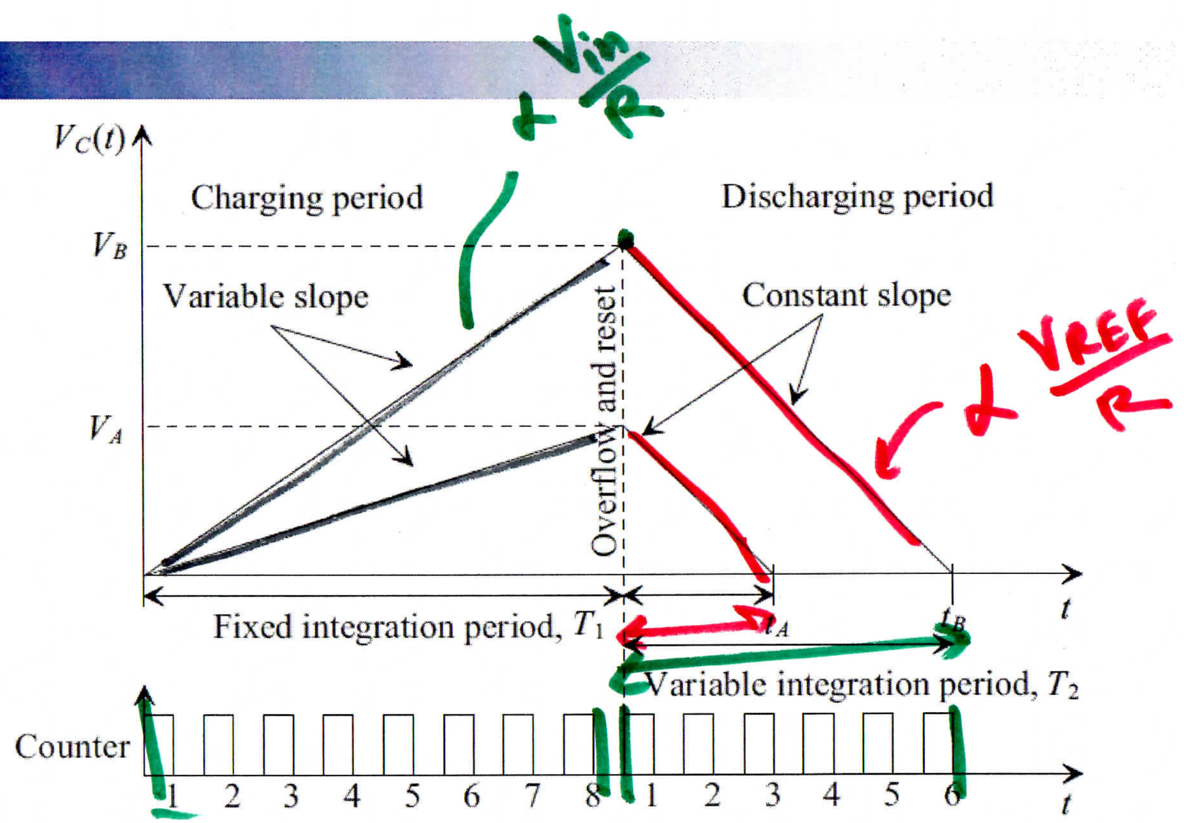


Figure 29.35 Integration periods and counter output for two separate samples of a 3-bit dual-slope ADC.

$$\frac{V_{in}}{V_{REF}} = \frac{D}{2^N}$$

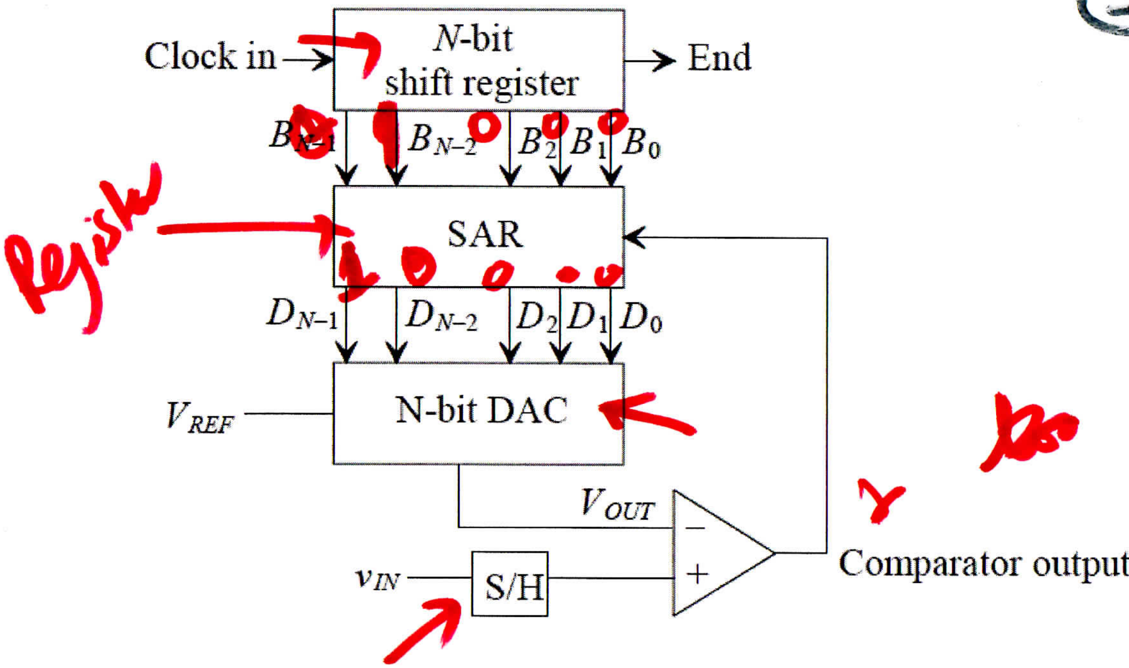
D ← counter output

2^N ↑ total number of counter cycles

Successive Approximation Register ADC

(SAR) ADC

↑ Low-Power



$\log_2 N$

Figure 29.36 Block diagram of the successive approximation ADC.

1 ③ 4 6 7 9 8 2

1 2 3 4 6 7 8 9

③

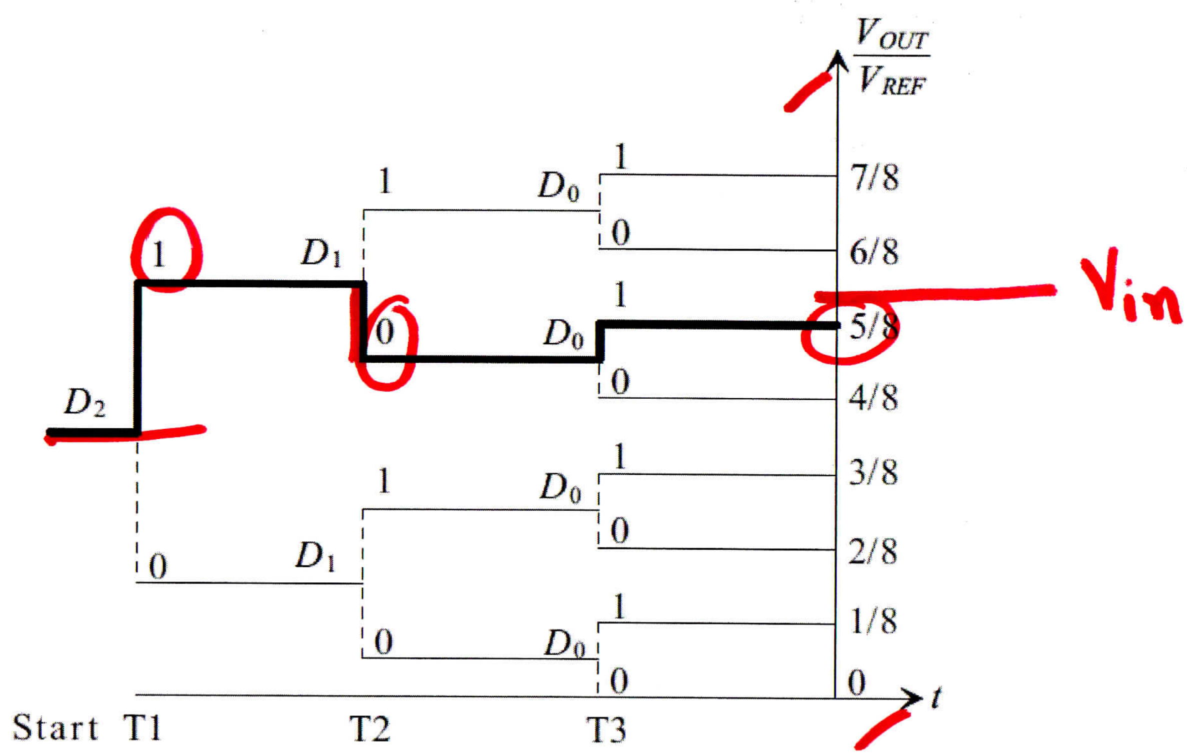


Figure 29.37 Binary search performed by a 3-bit successive approximation ADC for D=101.

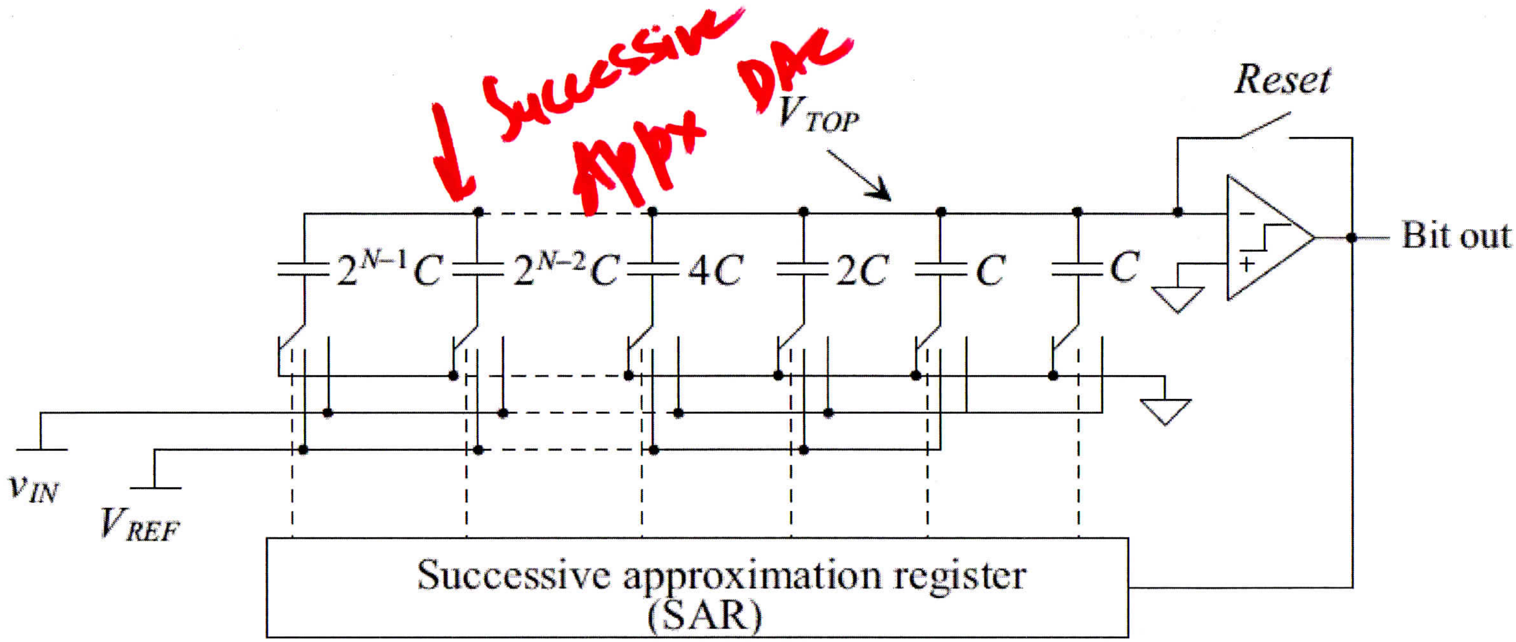


Figure 29.39 A charge redistribution ADC using a binary-weighted capacitor array DAC.

Nyquist-rate ADCs

$f_s \geq 2BW$

10 MHz

Oversampling ADC's

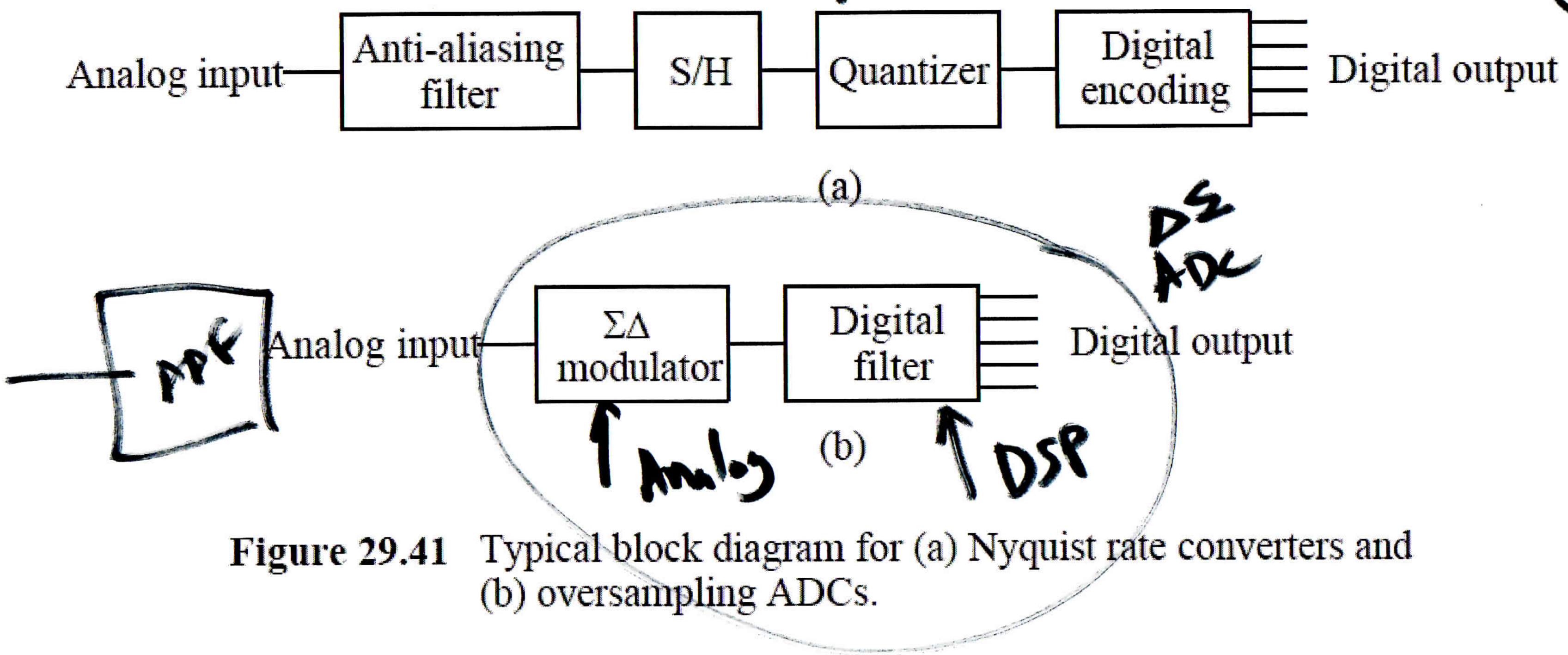
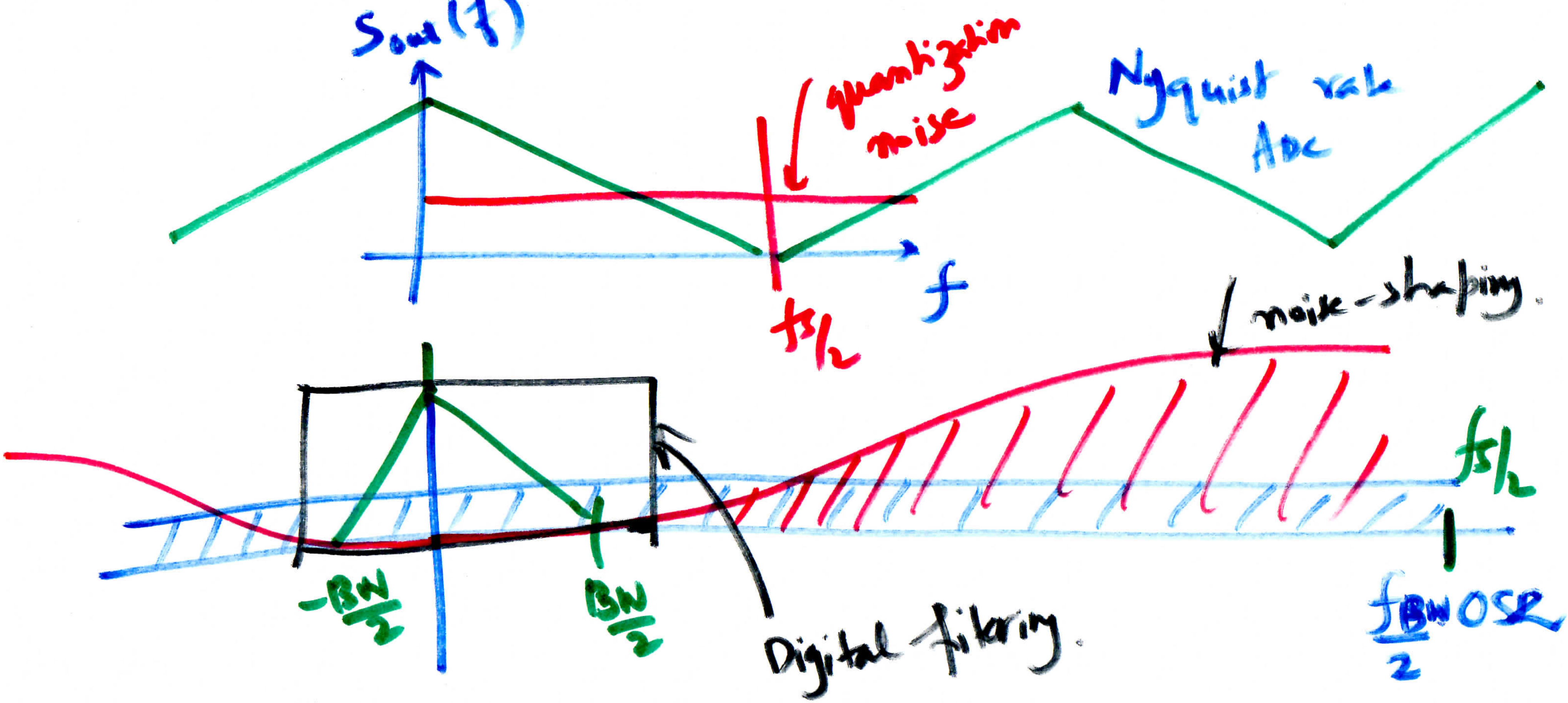


Figure 29.41 Typical block diagram for (a) Nyquist rate converters and (b) oversampling ADCs.



ΔΣ → much larger SNR

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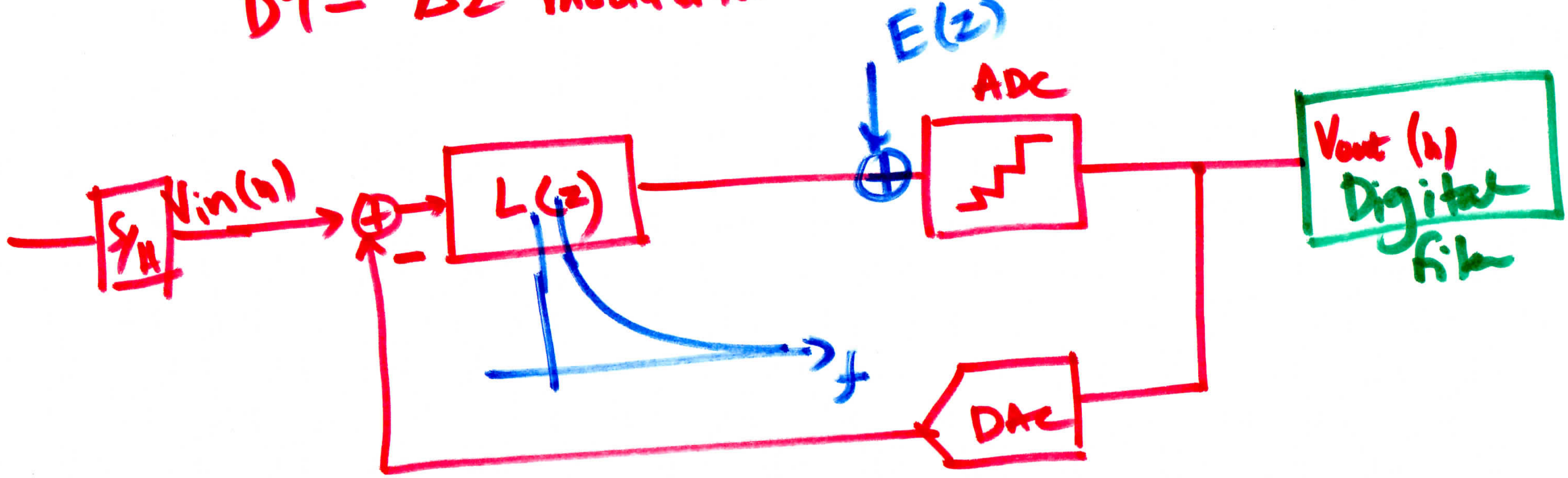
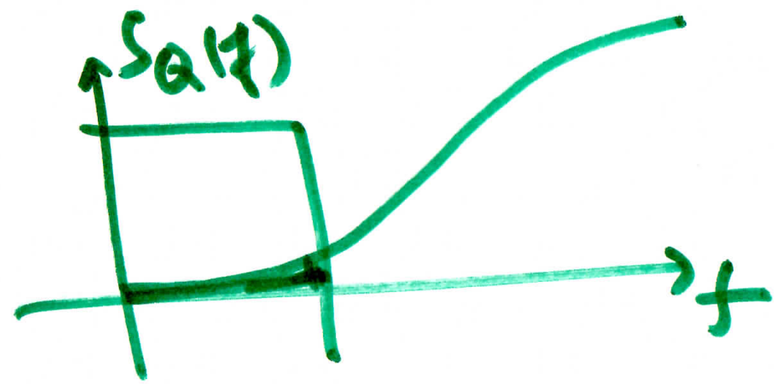
DT- ΔΣ modulator.





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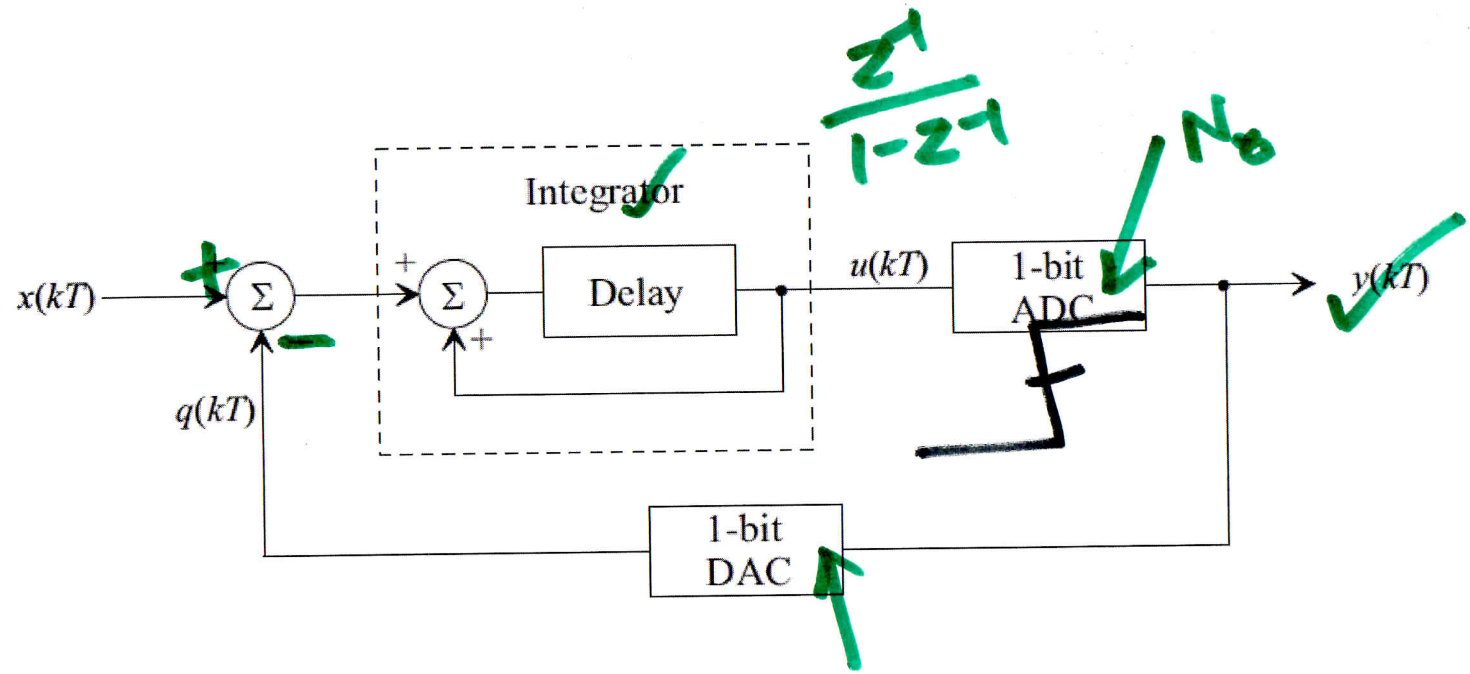

Figure 29.44 A first-order sigma-delta modulator.

$$N_{eff} = N_0 + \frac{3}{2}\cdot\log_2(OSR)$$

$N_0 = 1$, $OSR = 64$

$$= 1 + 1.5\times 6$$

$$= \underline{10 \text{ bits}}$$

16

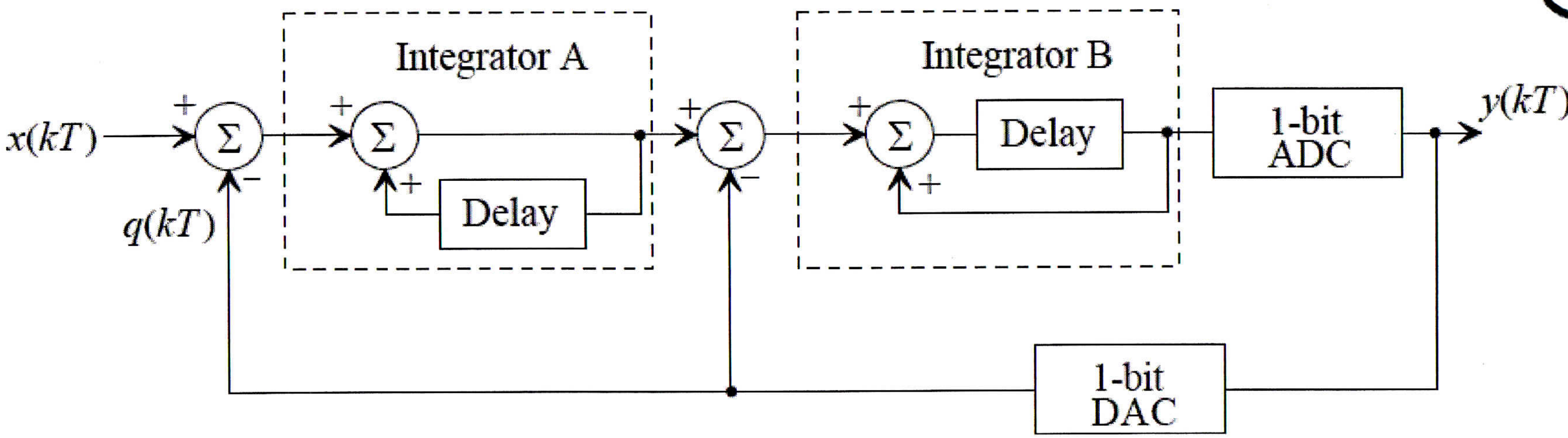

Figure 29.49 A second-order, sigma-delta modulator.

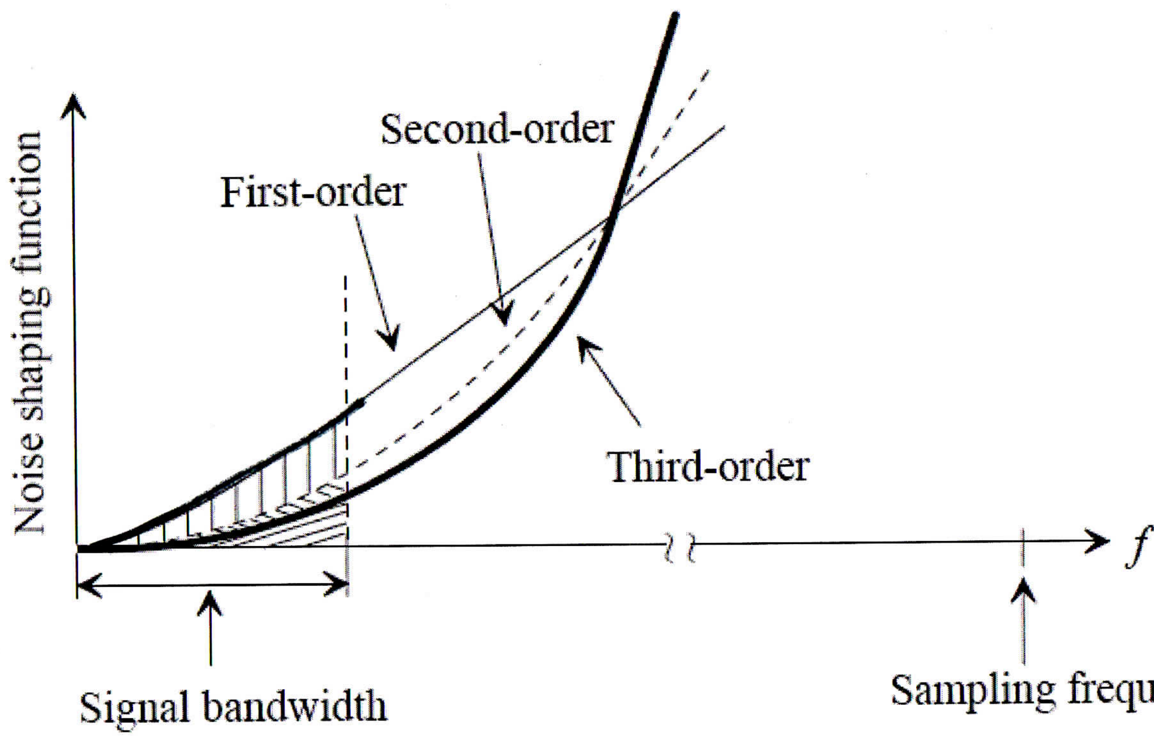

Figure 29.50 Noise shaping comparison of a first-, second- and third-order modulator.

AD9262:

BW = 10 MHz – "16 bits"

f_s = 640 MHz

OSR = 32

5th-order CT ΔΣ