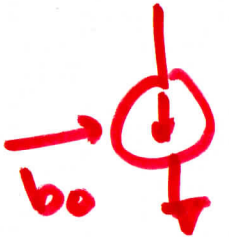
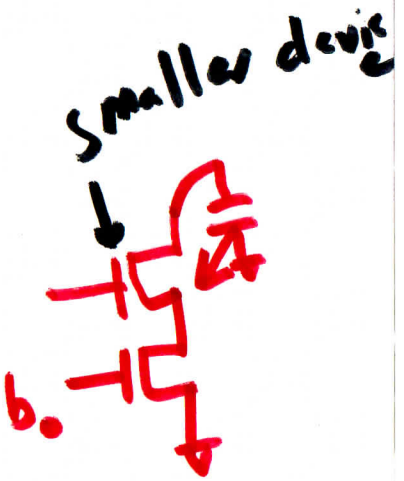
ECE 614 – Lecture 18

① Current Mismatch

$$|INL|_{max} = 2^{N-1} \cdot |\Delta I|_{max}$$

② Glitching





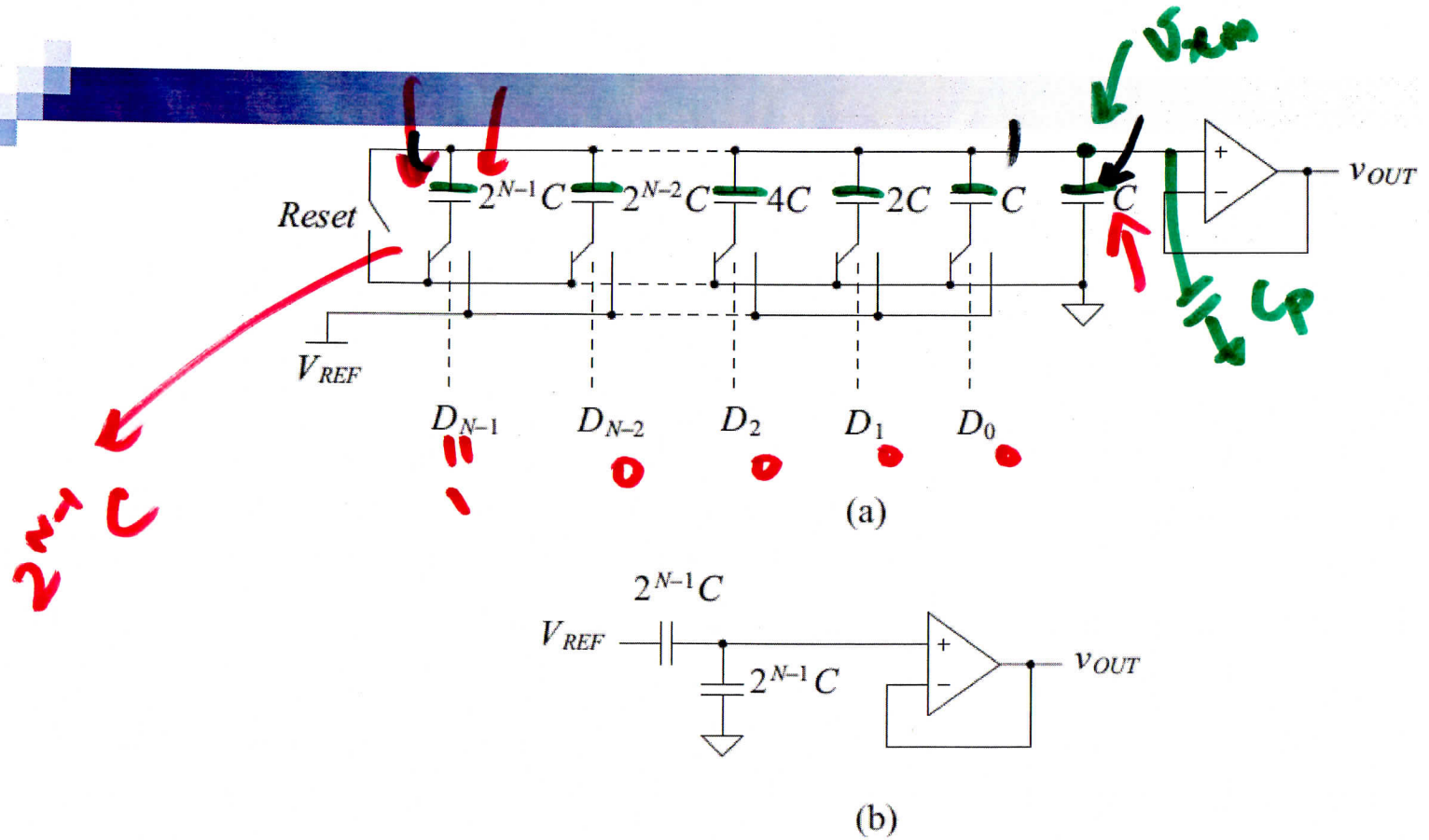


Figure 29.12 (a) A charge-scaling DAC, (b) the equivalent circuit with the MSB = 1, and all other bits set to zero.

$$V_{out} = V_{REF}\frac{2^{N-1}C}{(2^{N-1}+2^{N-2}+\cdots+2+\underbrace{1+1}_{2})C}$$

$$= \frac{2^{N-1}}{2^N}\cdot V_{REF} = \frac{V_{REF}}{2}$$

$$2(1+2+4\cdots+2^{N-2}) = 2\cdot M2^{N-1} = 2^N$$

k^{th}-bit is "1"

$$V_{out} = \frac{2^k C}{2^N C} V_{REF} = 2^{K-N} V_{REF}$$

for $k = 0$ to $N-1$

$$V_{out} = \sum_{k=0}^{N-1} D_k \, 2^{K-N} \cdot V_{REF}$$

$D_{N-1} D_{N-2} \cdots D_0$

for $k=0 \Rightarrow \frac{1}{2^N}$ ← LSB

$k = N-1 \Rightarrow \frac{1}{2}$ ← MSB

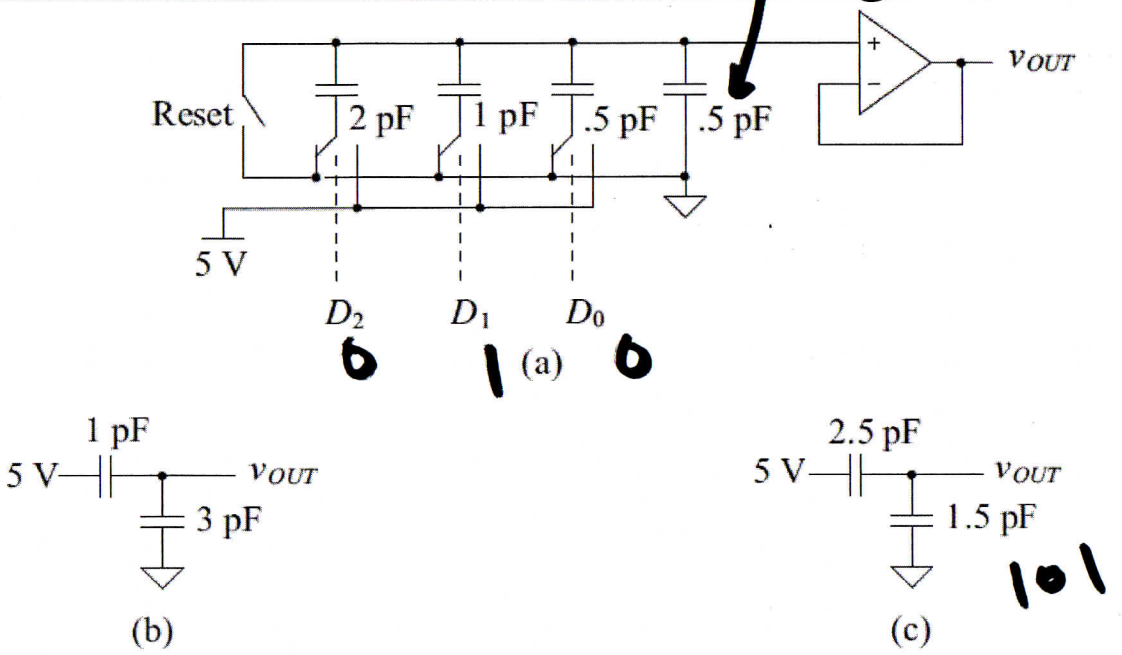


Figure 29.13 (a) A 3-bit charge-scaling DAC used in Ex. 29.6 and the equivalent circuits inputs equal to (b) 010 (c) 101.

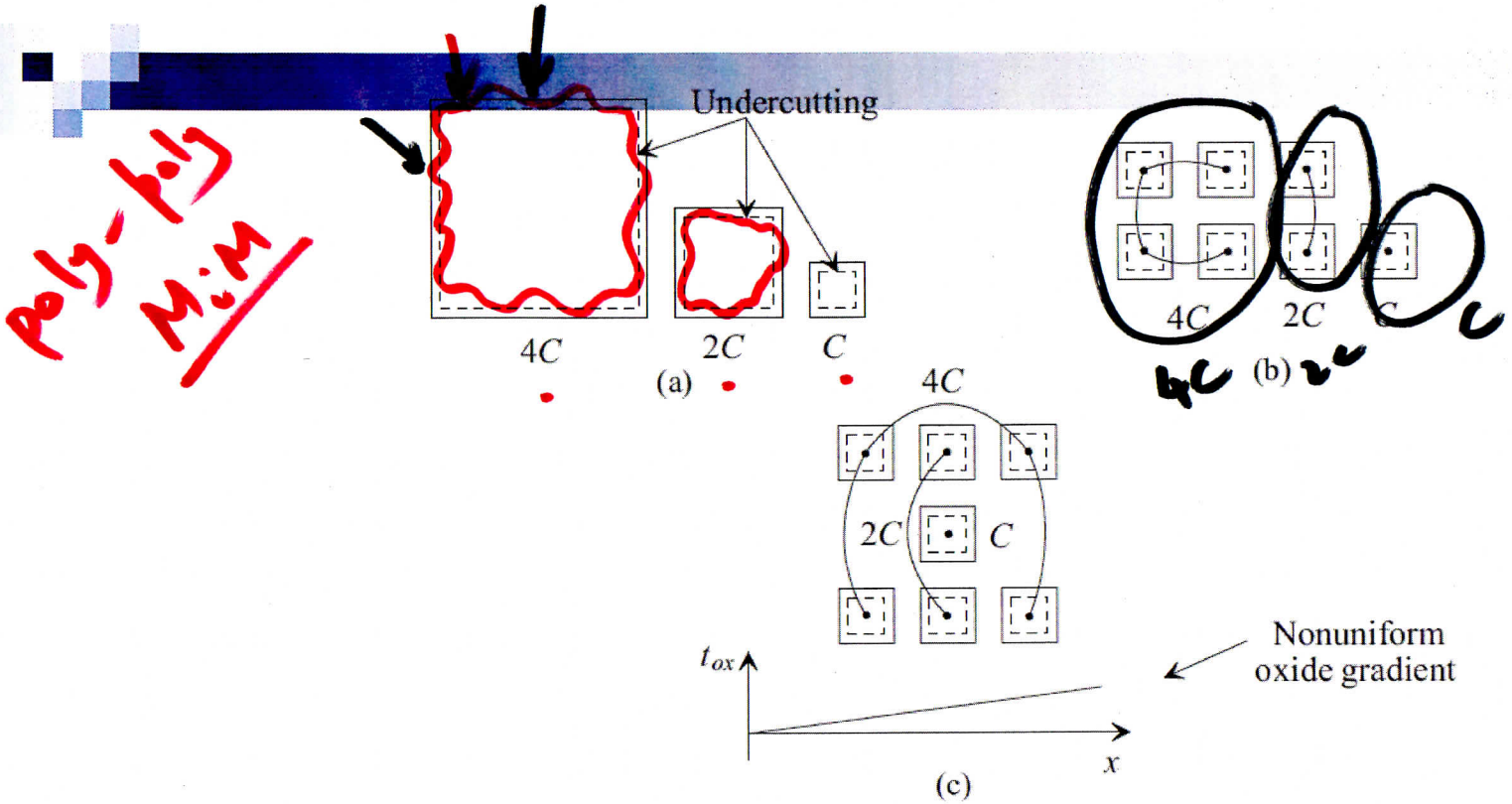


Figure 29.14 Layout of a binary-weighted capacitor array using (a) single capacitors (b) unit capacitors to minimize undercutting effect, and (c) common-centroid to minimize oxide gradients.

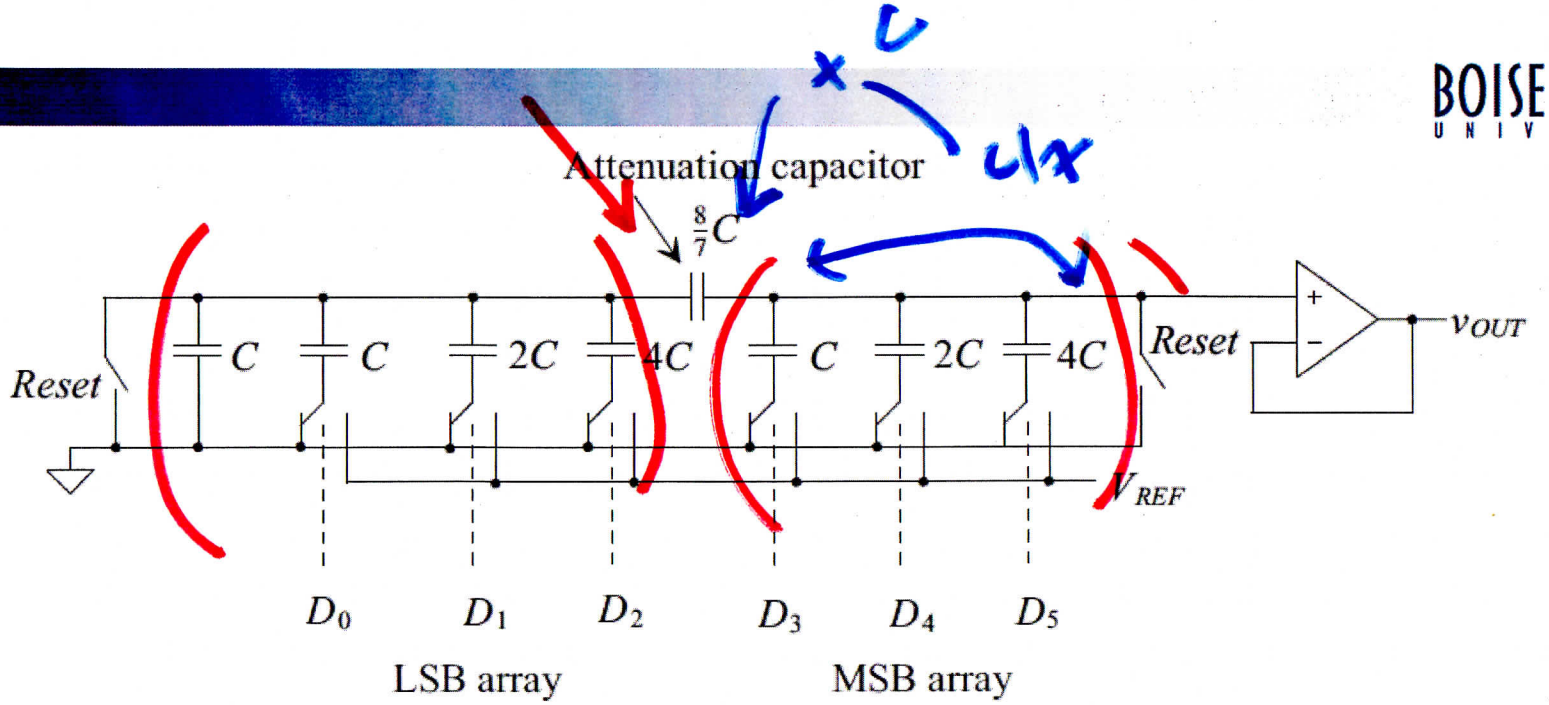


Figure 29.15 A charge-scaling DAC using a split array.

Split Array.

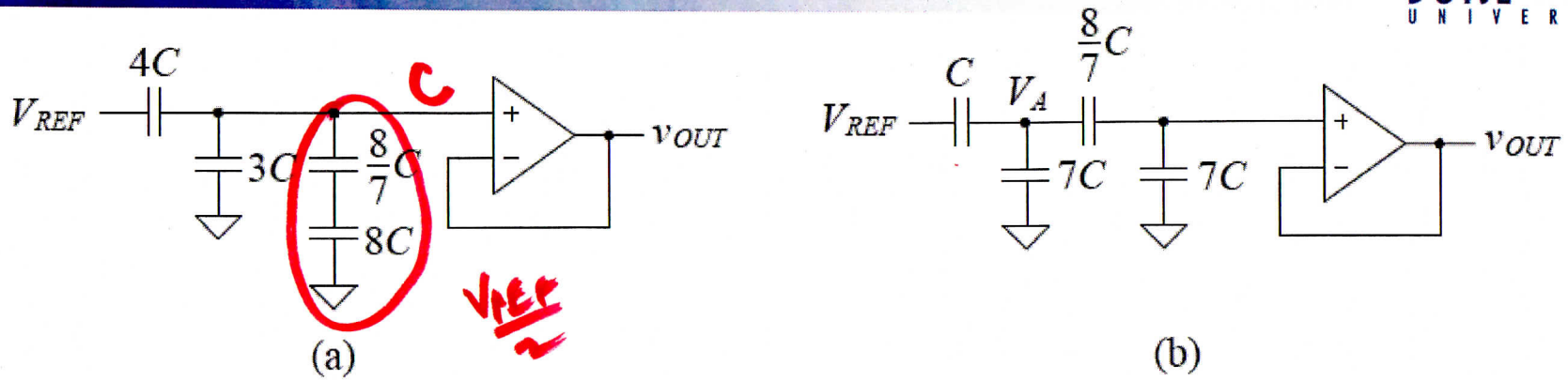


Figure 29.16 Equivalent circuits for Example 29.7.

6-bit DAC

100000

MSB

000001

$$V_A = V_{REF} \cdot \frac{1}{7 + \frac{\frac{8}{7}\cdot 7}{\frac{8}{7}+7}} = \frac{V_{REF}}{64}$$

LSB

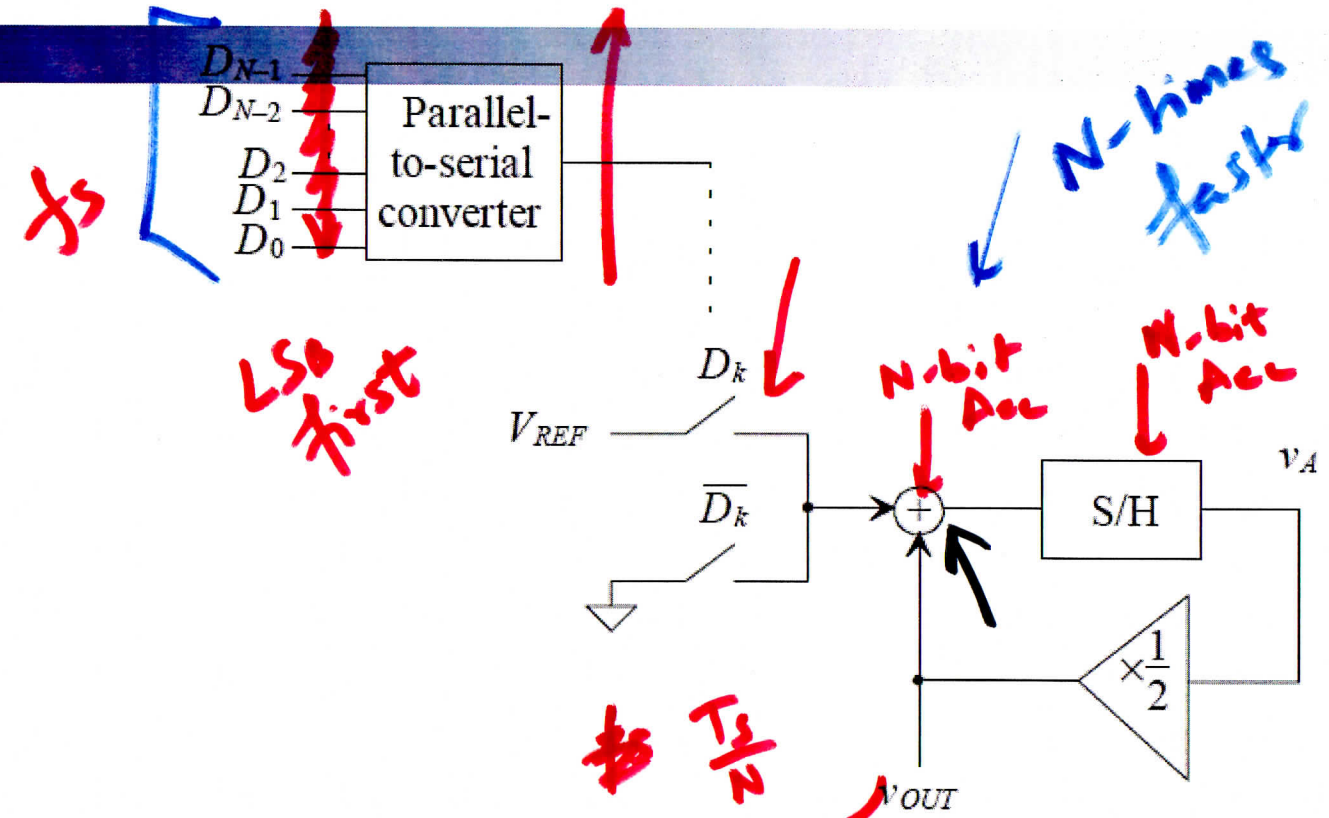


Figure 29.17 A cyclic digital-to-analog converter.

$$V_{out}(n) = \left[D_{n-1} V_{REF} + \frac{1}{2} \cdot v_A(n-1) \right] \cdot V_2$$

I.C. $\rightarrow v_A(0) = 0\,V$

Cycle Number, n	D_{n-1}	$v_A(n\text{-}1)$	$v_{OUT}(n)$
1	1	0	½ (5 + 0) = 2.5 V
2	0	5	½ (0 + 2.5) = 1.25 V
3	1	2.5	½ (5 +1.25) = 3.125 V
4	0	6.25	½ (0 + 3.125) = 1.5625 V
5	1	3.125	½ (5 + 1.5625) = 3.28125 V
6	1	6.5625	½ (5 + 3.28125) = 4.140625 V

Figure 29.18 Output from the 6-bit cyclic DAC used in Ex. 29.8.

N-cycles for conversion

110101

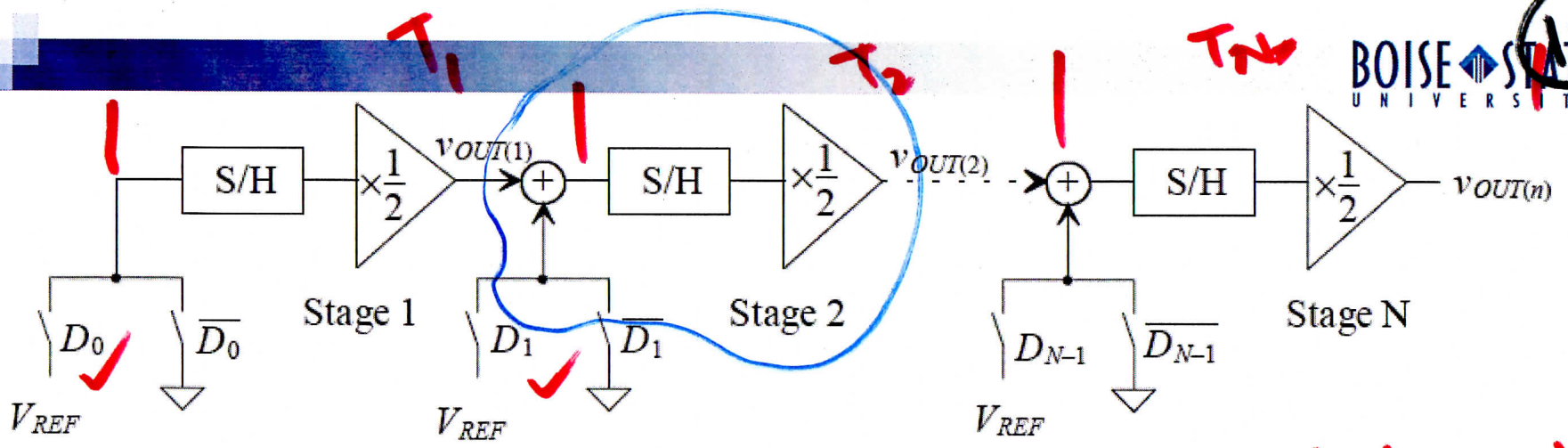


Figure 29.19 A pipeline digital-to-analog converter.

Latency of N - cycles

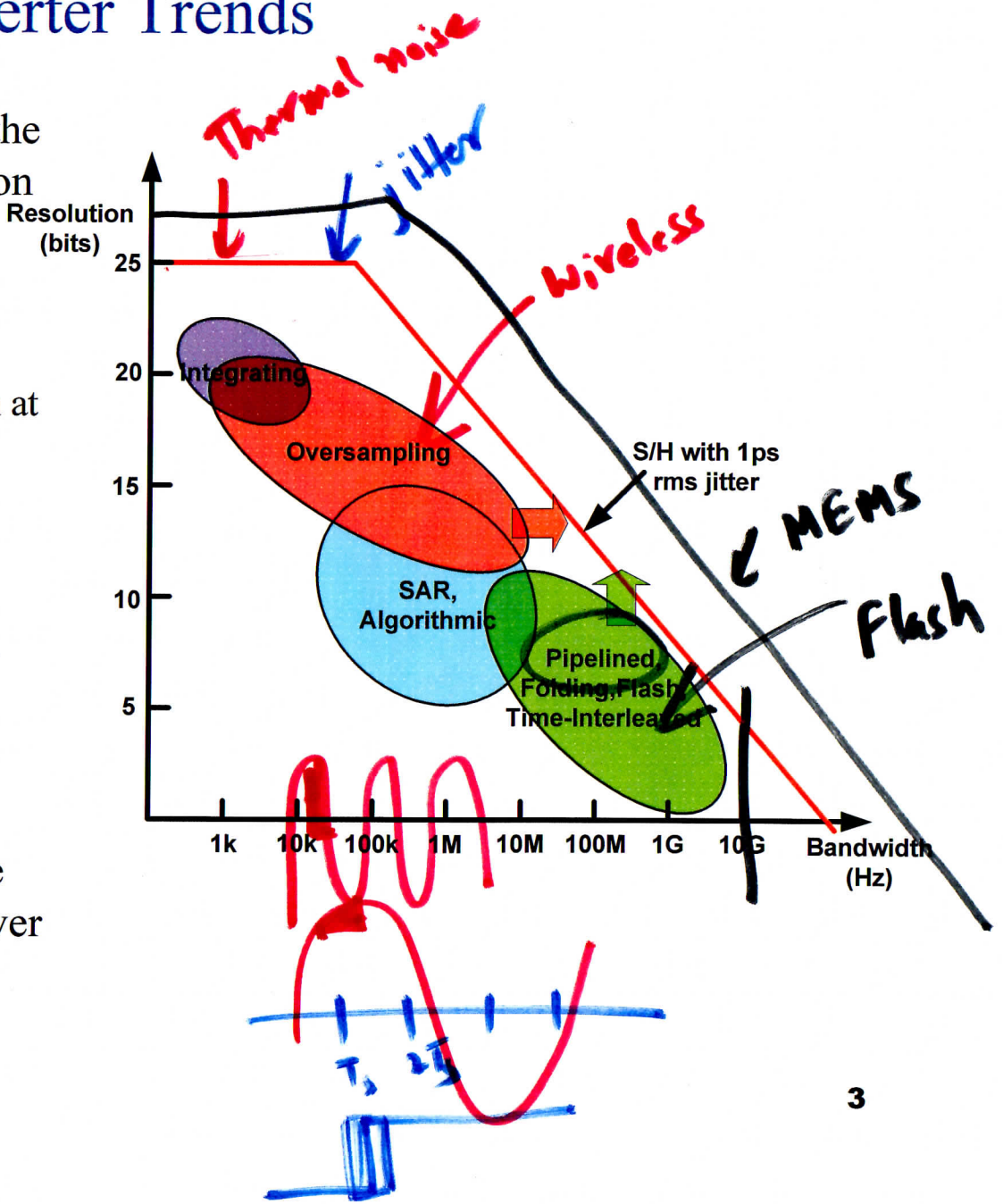
$$V_{out}[n] = [D_{n-1} \cdot V_{ref} + V_{out}[n-1]] \cdot \tfrac{1}{2}$$

Clock Cycle	$v_{OUT(1)}$	$v_{OUT(2)}$	$v_{OUT(3)}$	D_0	D_1	D_2
1	**2.5**	0	0	**1**	0	0
2	*0*	**1.25**	0	*0*	**0**	0
3	2.5	*2.5*	**0.625**	1	*1*	**0**
4		1.25	3.75		0	*1*
5			3.125			1

Figure 29.20 Output from the 3-bit pipeline DAC used in Example 29.9.

Analog to Digital Converter Trends

- Different ADC architectures for the signal bandwidth and bit resolution requirements.
- Nyquist rate ADCs for wideband conversion
  - ✓ Flash ADCs for GHz conversion at lower resolution (≤ 6 bits).
  - ✓ Pipelined ADCs for moderate resolutions and conversion bandwidth.
    - reaching 10 bits over 200 MHz.
- Oversampling ADCs for higher resolution but lower bandwidth
  - ✓ 12-24 bits resolution.
- New wireless applications require higher bandwith (25 MHz) and over 10-12 bits of resolution.



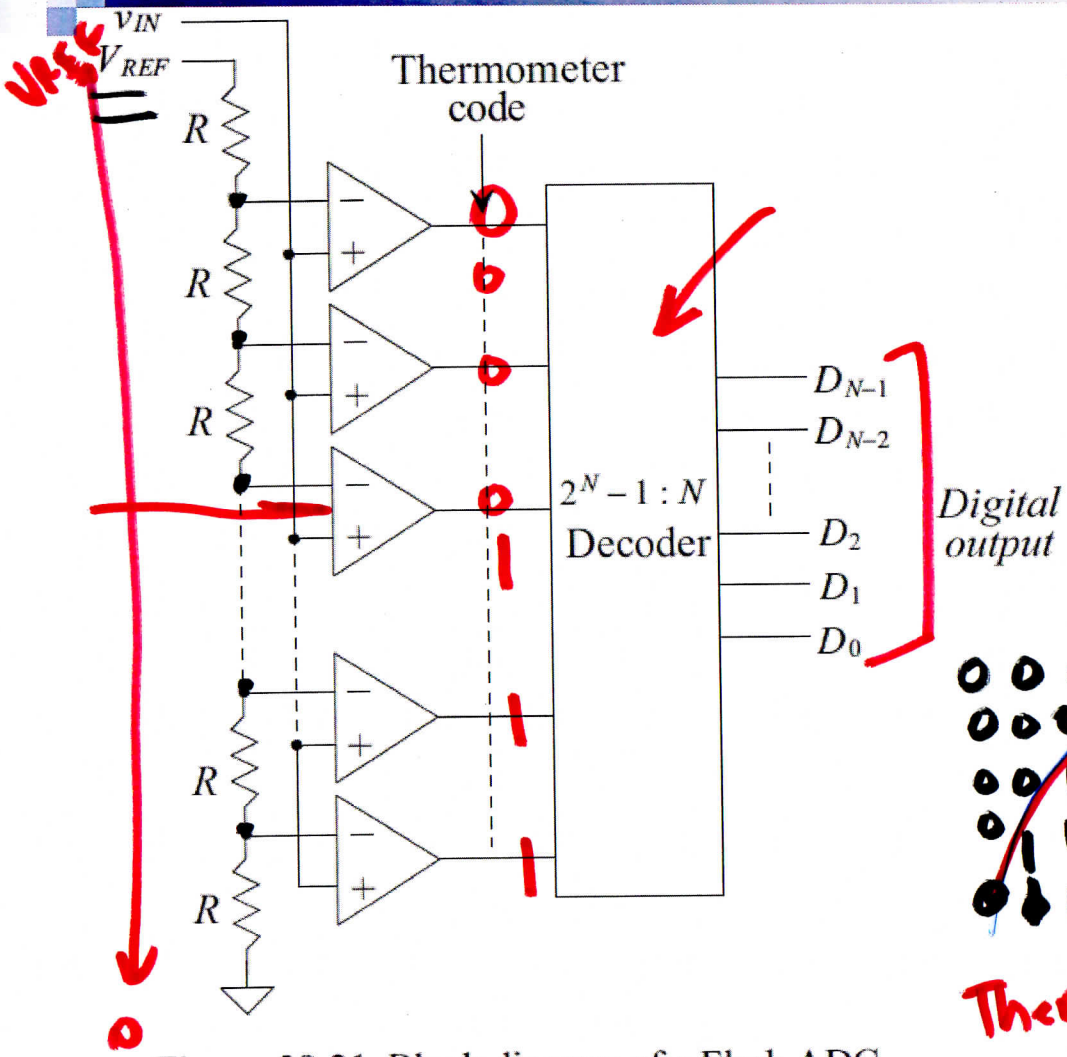
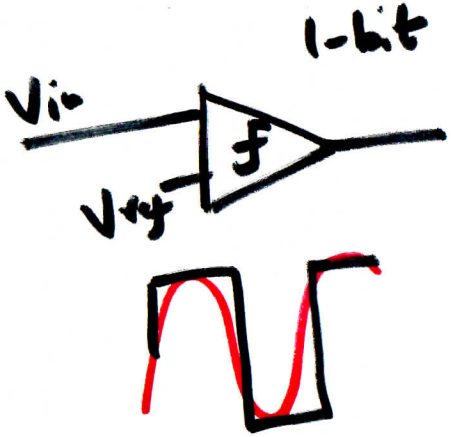
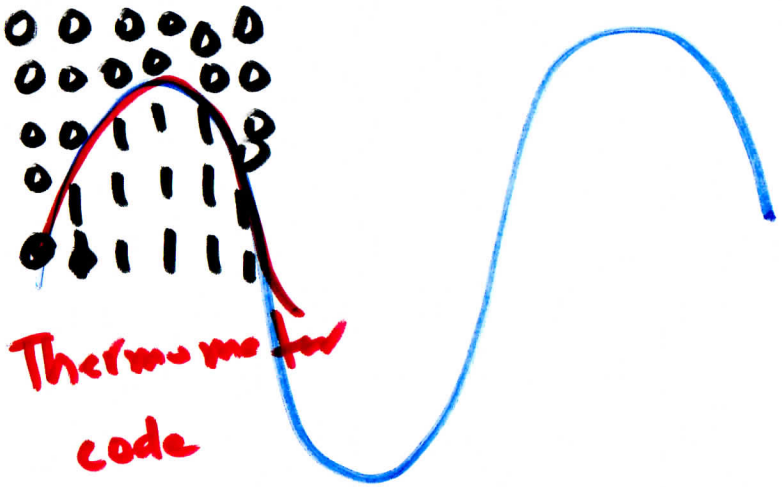


Figure 29.21 Block diagram of a Flash ADC.





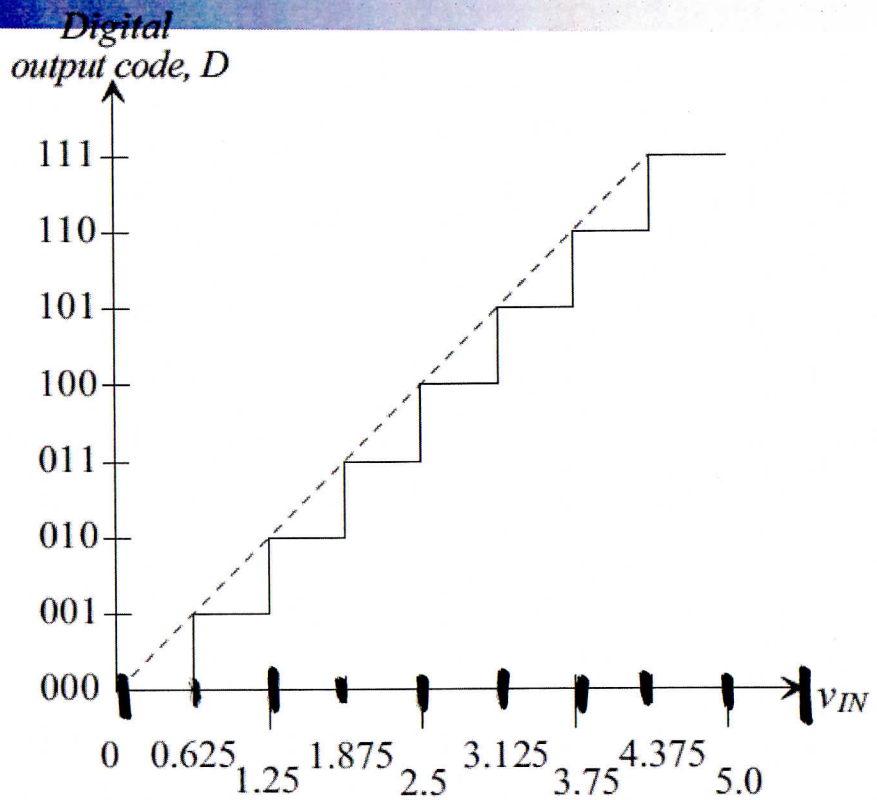
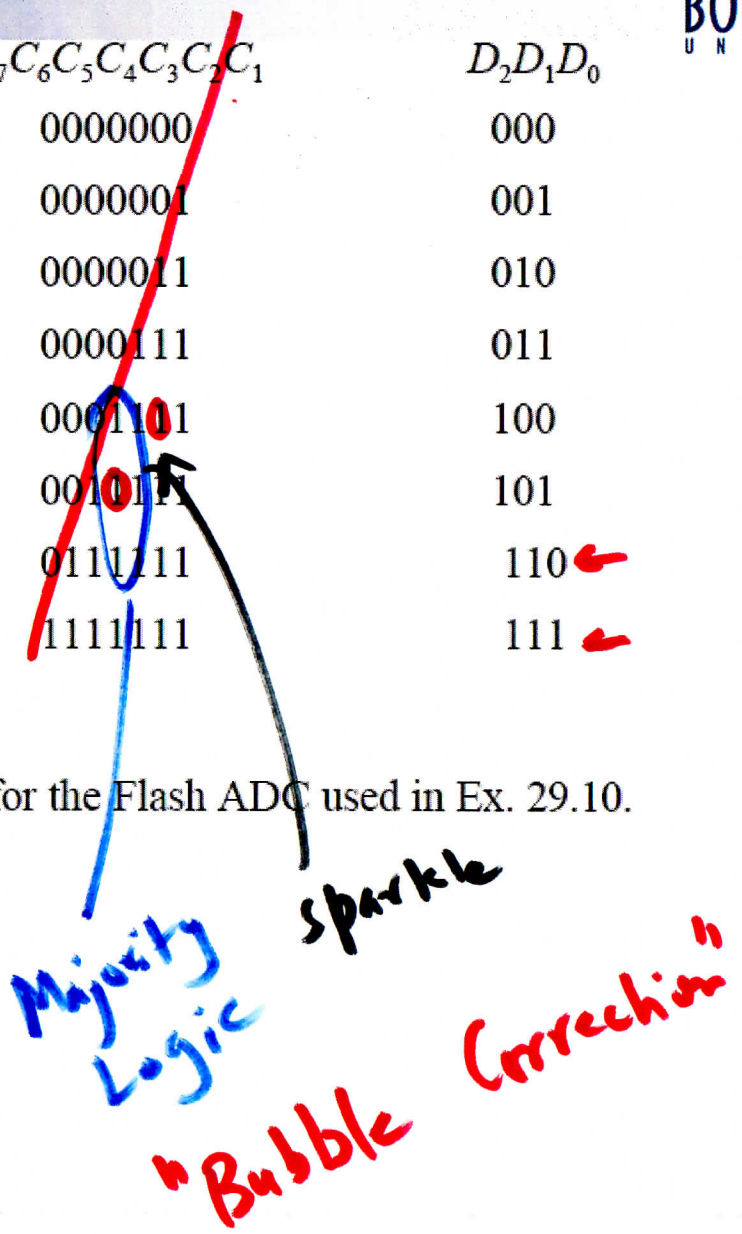
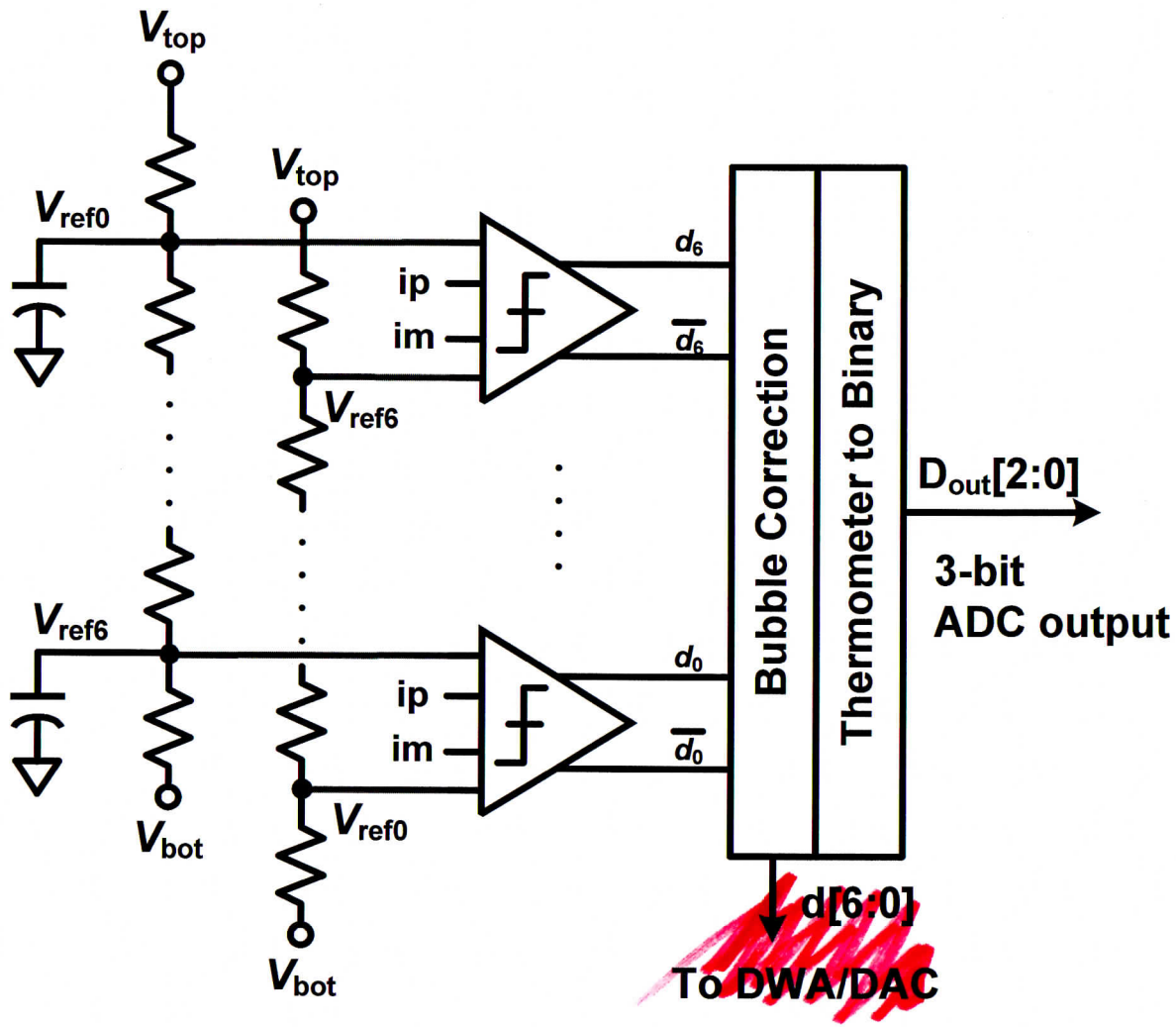


Figure 29.23 Transfer curve for the 3-bit Flash converter in Example 29.10.

v_{IN}	$C_7C_6C_5C_4C_3C_2C_1$	$D_2D_1D_0$
$0 \le v_{IN} < 0.625$ V	0000000	000
0.625 V $\le v_{IN} < 1.25$ V	0000001	001
1.25 V $\le v_{IN} < 1.875$ V	0000011	010
1.875 V $\le v_{IN} < 2.5$ V	0000111	011
2.5 V $\le v_{IN} < 3.125$ V	0001111	100
3.125 V $\le v_{IN} < 3.75$ V	0011111	101
3.75 V $\le v_{IN} < 4.375$ V	0111111	110
$4.375 \le v_{IN}$	1111111	111

Figure 29.24 Code transitions for the Flash ADC used in Ex. 29.10.




V_{top}
V_{top}
V_{ref0}
ip
im
d_6
$\overline{d_6}$
V_{ref6}
V_{ref6}
d_0
$\overline{d_0}$
ip
im
V_{bot}
V_{ref0}
V_{bot}
Bubble Correction
Thermometer to Binary
$D_{out}[2:0]$
3-bit
ADC output
d[6:0]
To DWA/DAC

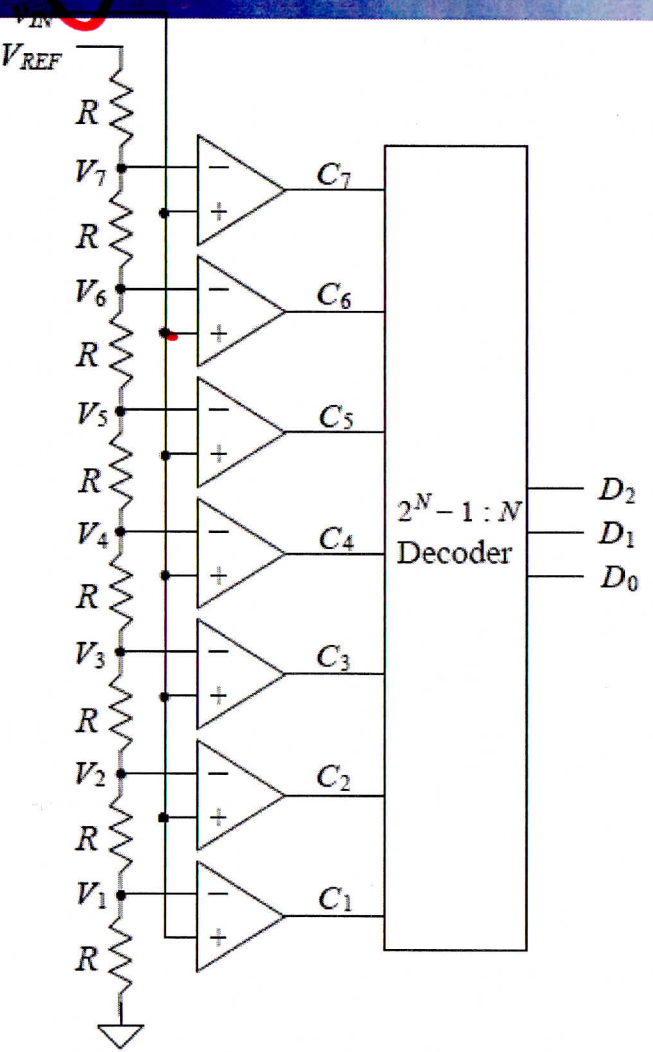


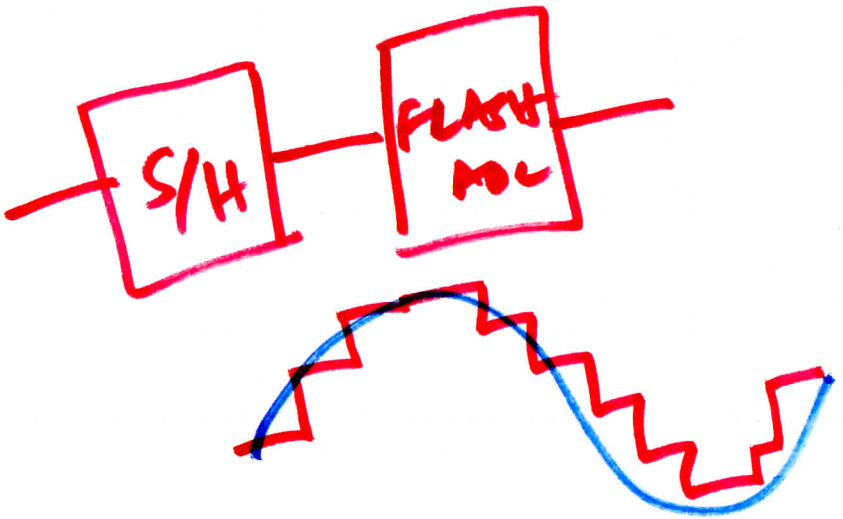
Figure 29.22 Three-bit Flash A/D converter to be used in Ex. 29.10.

N-bits

2^N R

2^{N-1} Comparators

→ 1 GHz



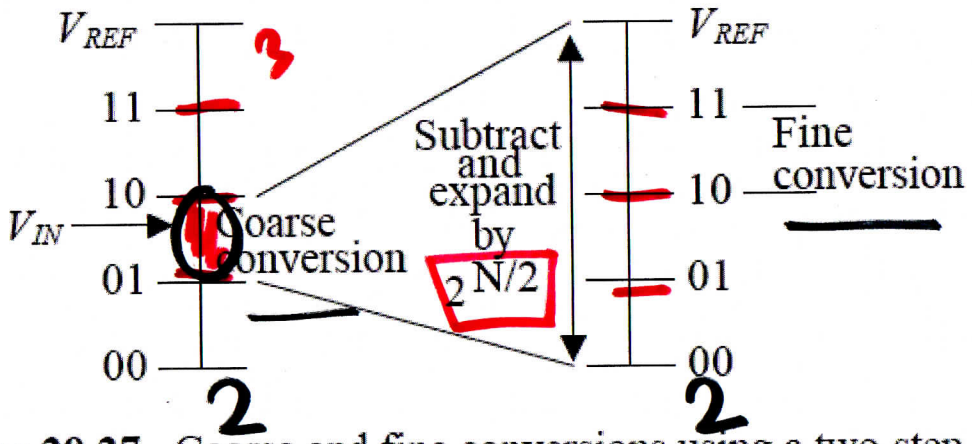


Figure 29.27 Coarse and fine conversions using a two-step ADC.

4-bit ADC

6 comparators

→ Signal processing

→ Latency

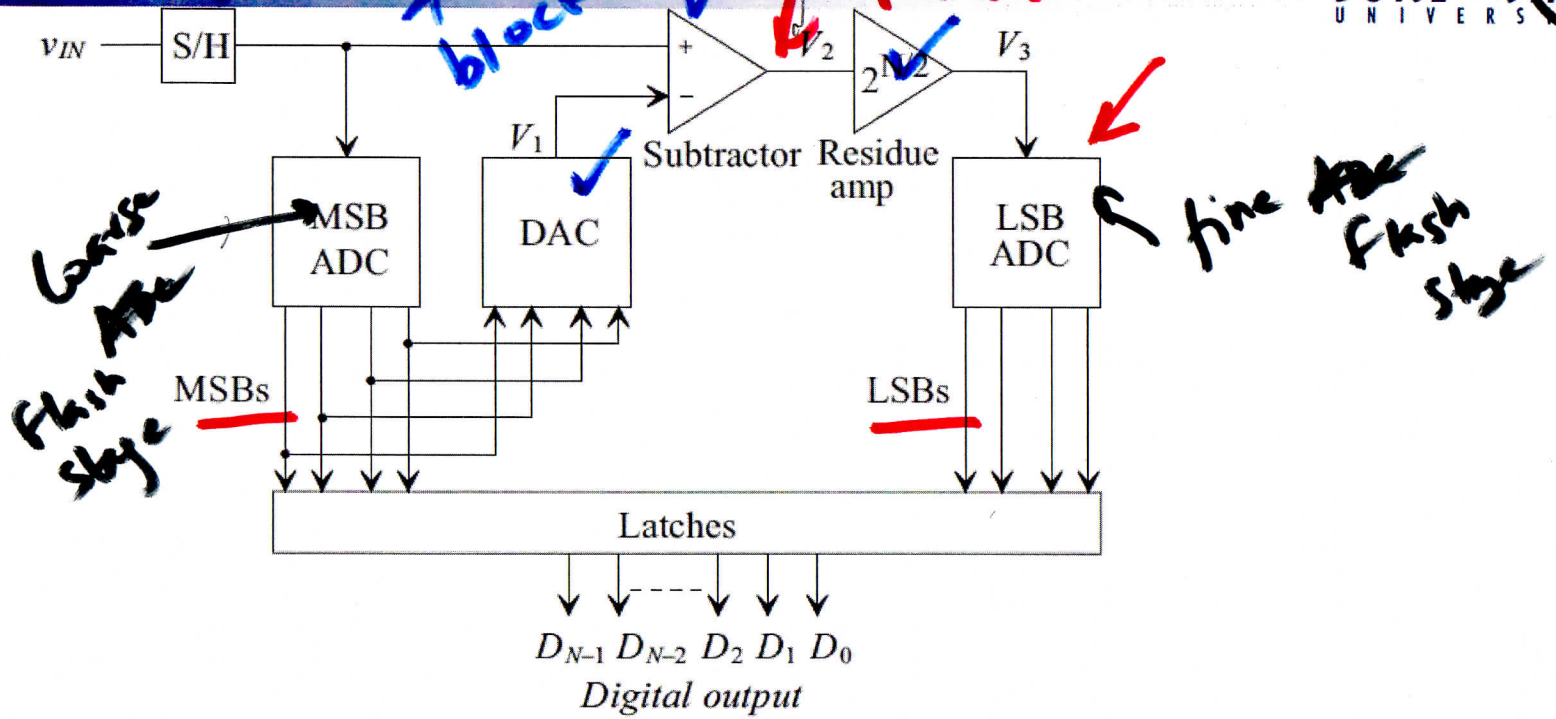
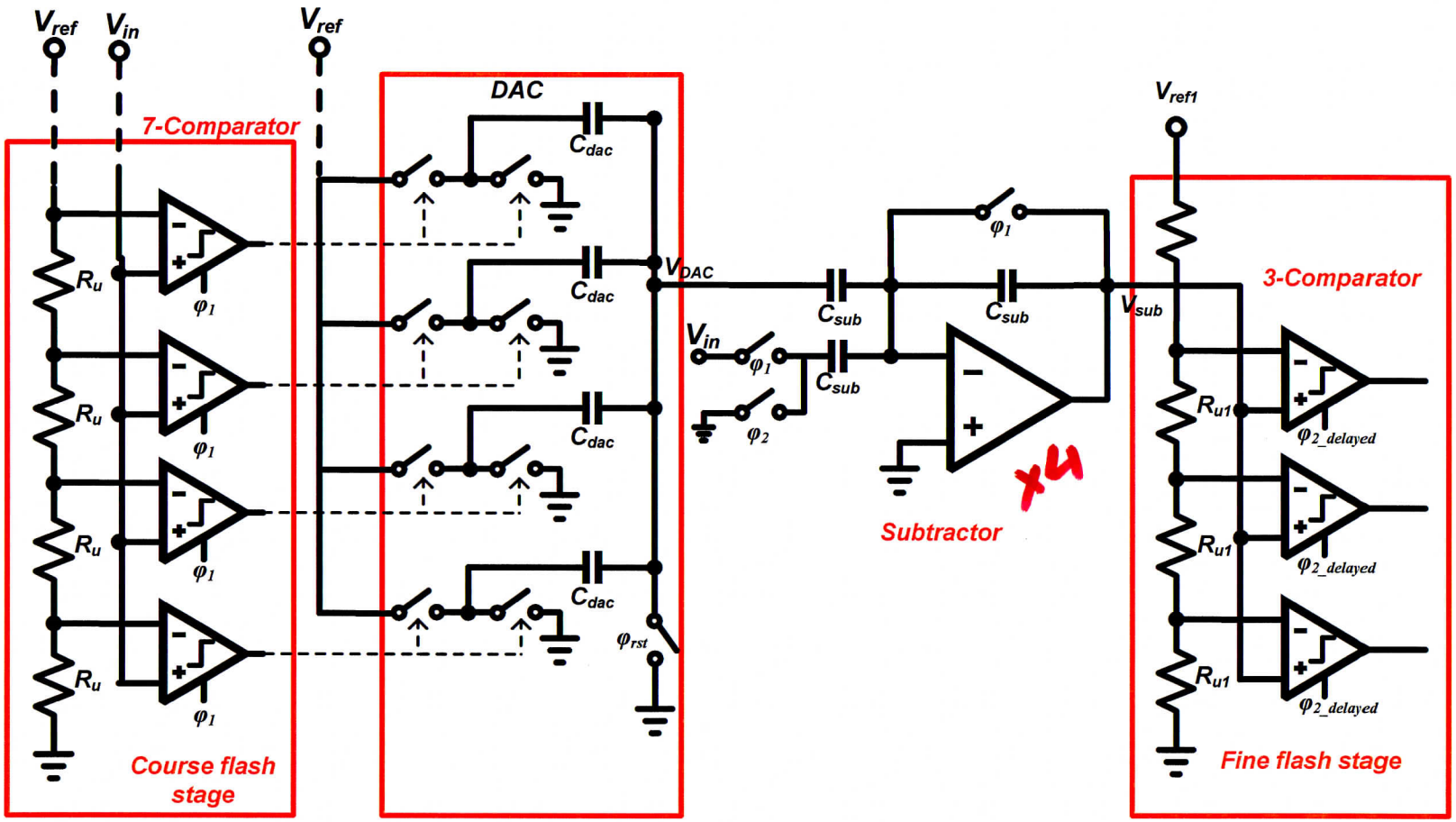


Figure 29.26 Block diagram of a two-step Flash ADC.

5-bit two-step Flash