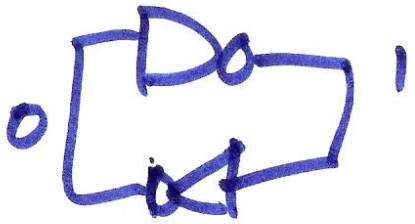
BOISE STATE UNIVERSITY

Lecture 9

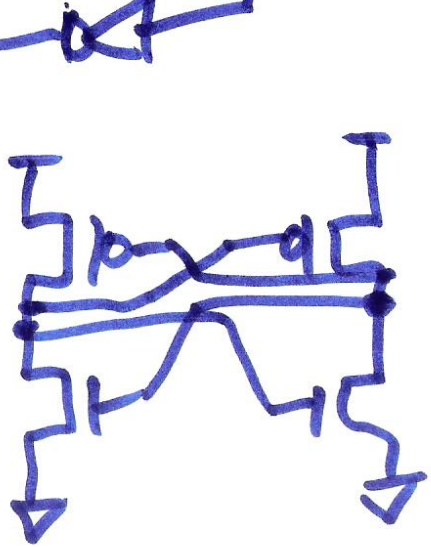
2/16/11

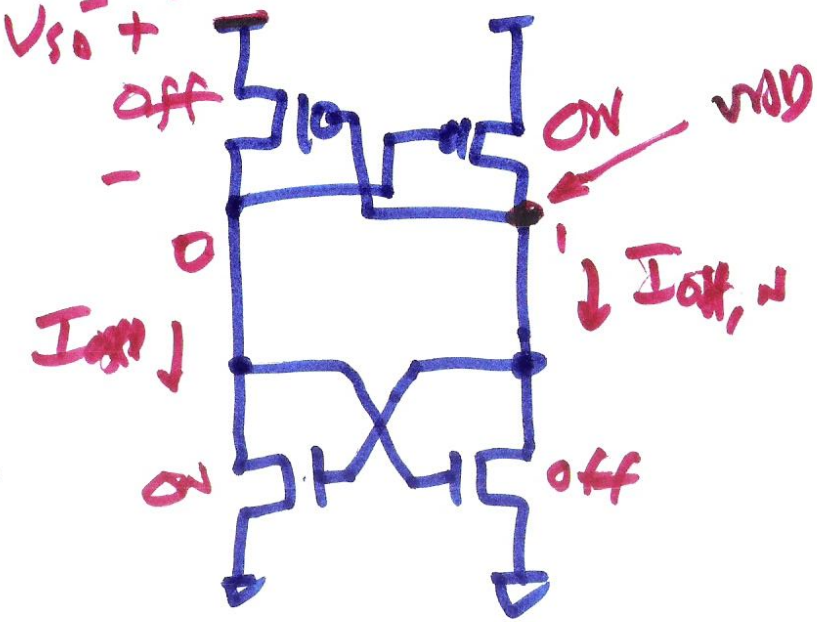
H.W. A16.6 in the additional H.W. at CMOSedu.com

No class on Monday, Feb. 21 (Pres. day)



$P_{diss} = VDD(I_{off,N} + I_{off,P})$





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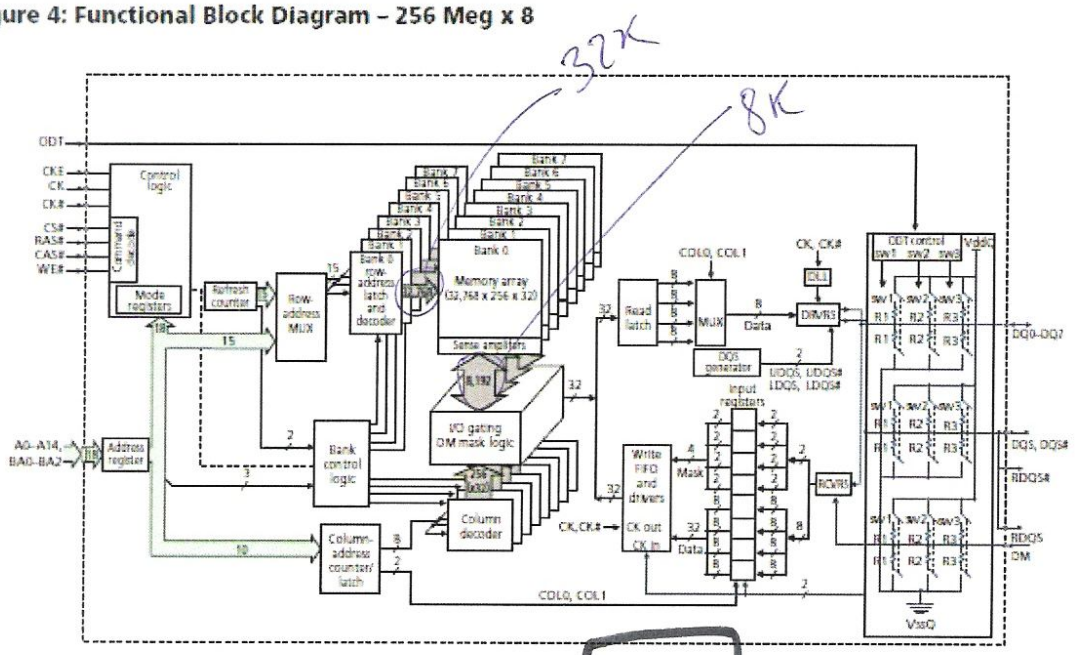
Quiz 3 Name:_____
ECE 518/418 Memory Circuit Design
Spring 2011

Micron

2Gb: x4, x8, x16 DDR2 SDRAM
Functional Block Diagrams

Figure 4: Functional Block Diagram – 256 Meg x 8



1. How many bits does this DRAM store? 2Gb

2. How many address pins are needed for the row address?

32K = 2^{15} 15 pins

3. If this is a x8 part how many bits come out of the part with the rising edge of DQS? the falling edge of DQS?

8 bits in either case

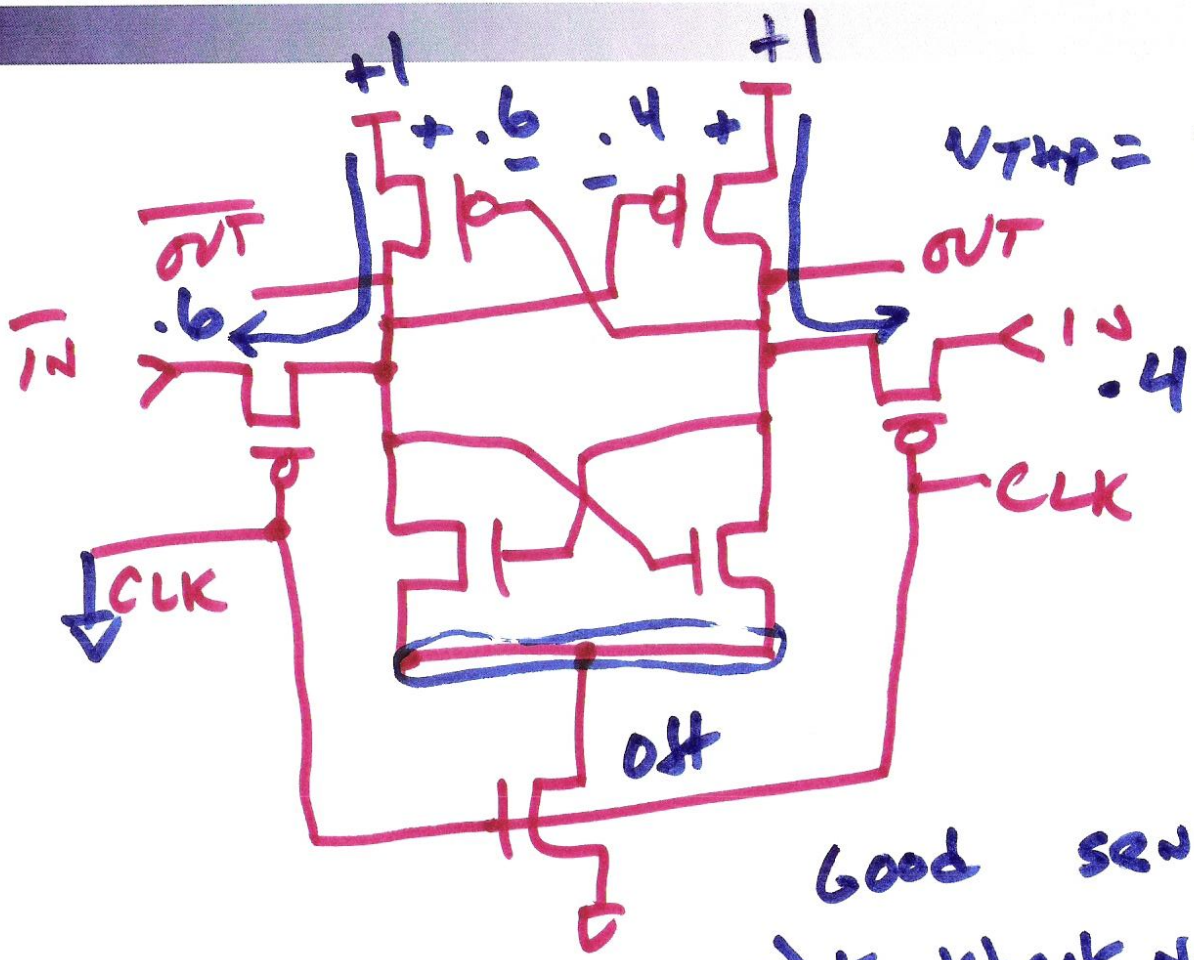
4. If there are 8k column lines what is the page size (how many 8-bit words can be addressed with column addresses for a single row address)?

page size = 1K

5. If the array size is 512 rows by 512 columns how many arrays are "opened" (a row line goes high) when a row address is applied to the part?

512 bits

16 ARRAYS



Good sense-Amp

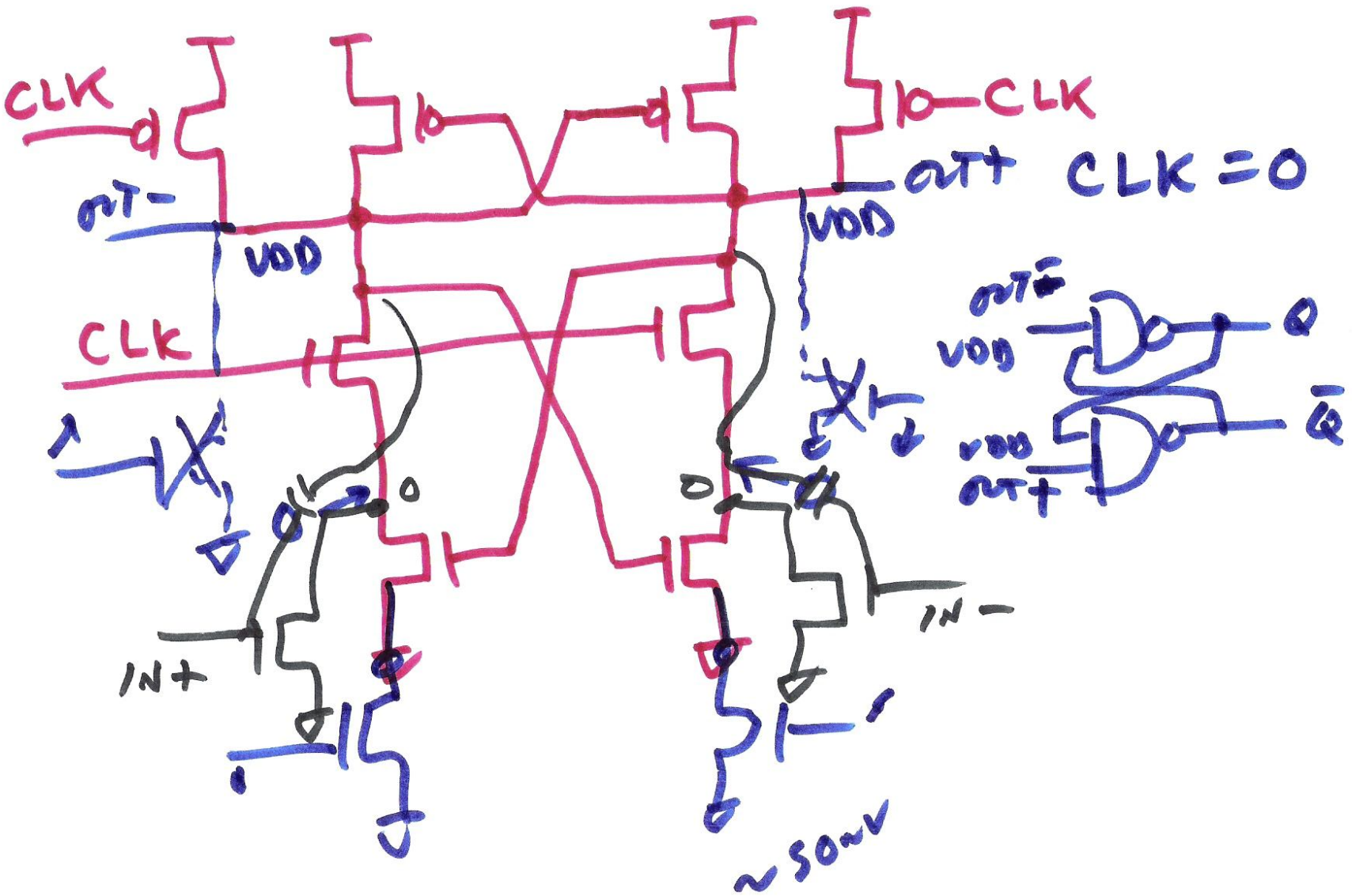
1) Kickback noise is small

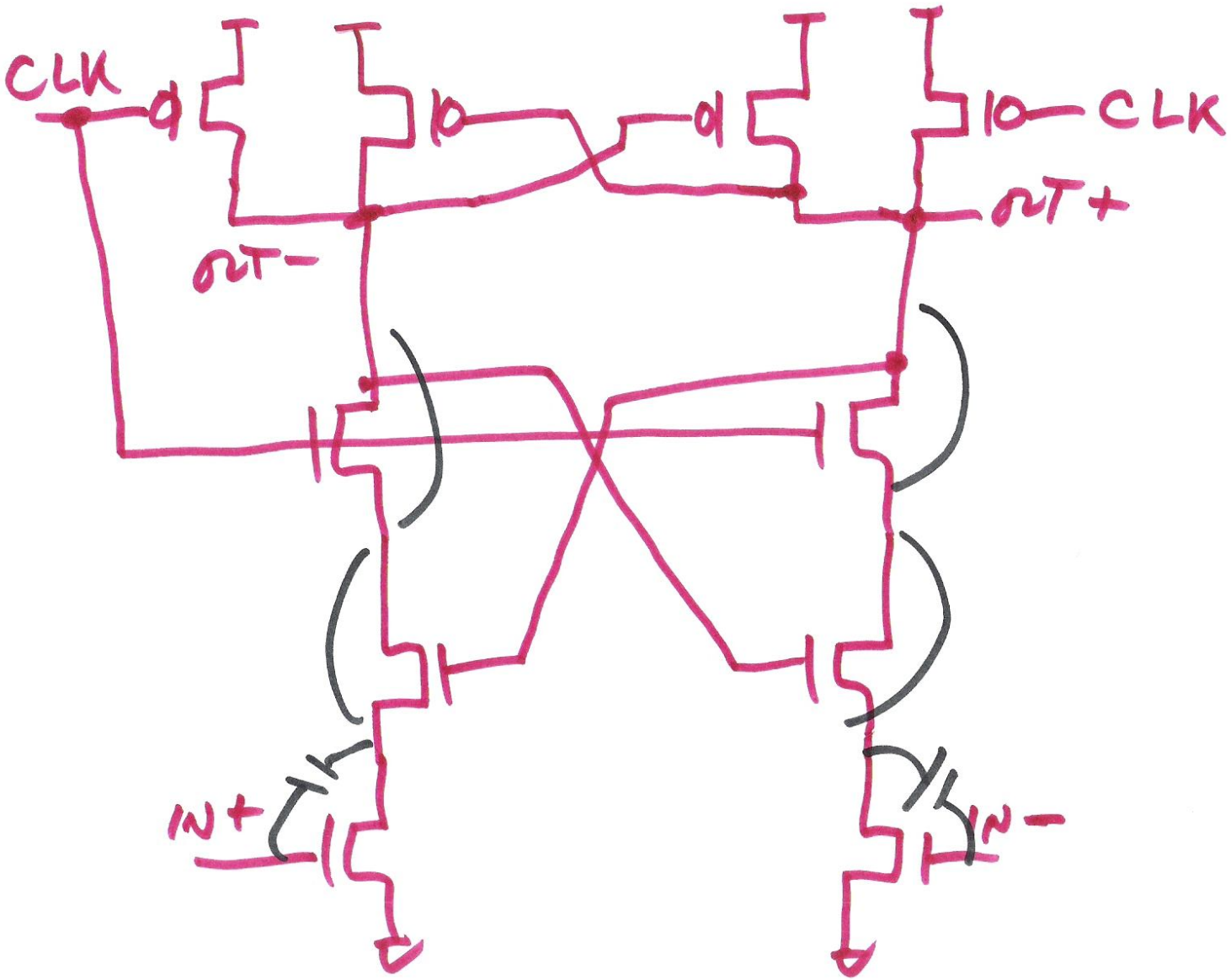
2 memory
all nodes actively driven

3) Don't want current flow from VDD → gnd.
Reduce current!

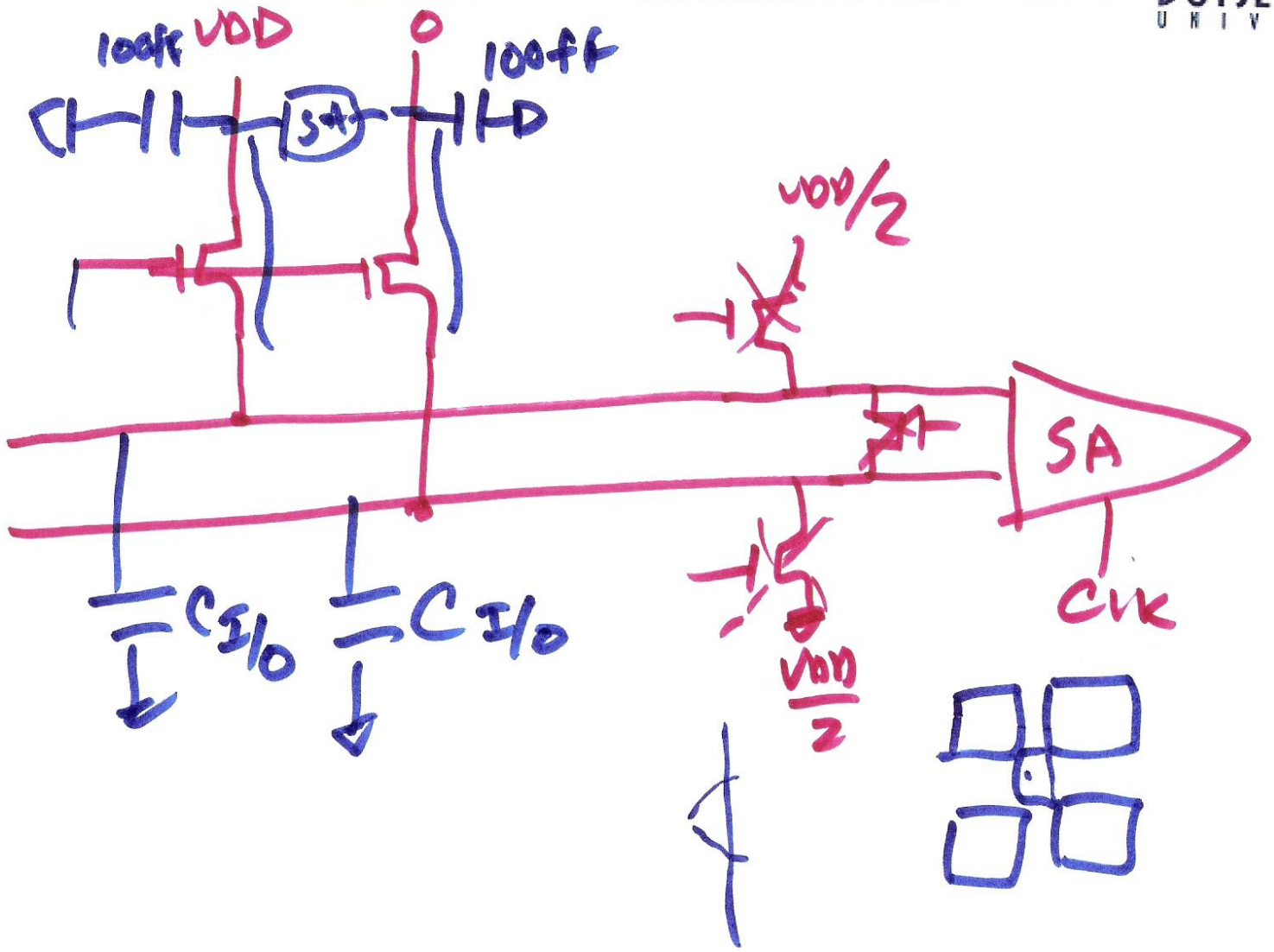
3)

Making a better Sense Amp





5)


100ff
VDD
0
100ff
SA
VDD/2
SA
Clk
$C_{I/O}$
$C_{I/O}$
VDD/2