ECE 5/418 memory circuits

BOISE STATE UNIVERSITY

2/14/11 Lecture 8

1Gb

256Mb x 4 banks

1 bank → 256 Mb

64M x 4

32m x 8

16m x 16

16K Row addresses

How many bits? 14 bits

10 → 1K

11 → 2K

12 → 4K

13 → 8K

14 → 16K

page size

1 row high

16K Row addresses / Bank

256 Mb / Bank

How Col Addresses for x1?

Col x row = 256 M

$Col = \frac{2^{28}}{2^{14}} = 2^{14} \times 1$

2 pins for Bank address

14-pins A0-A13

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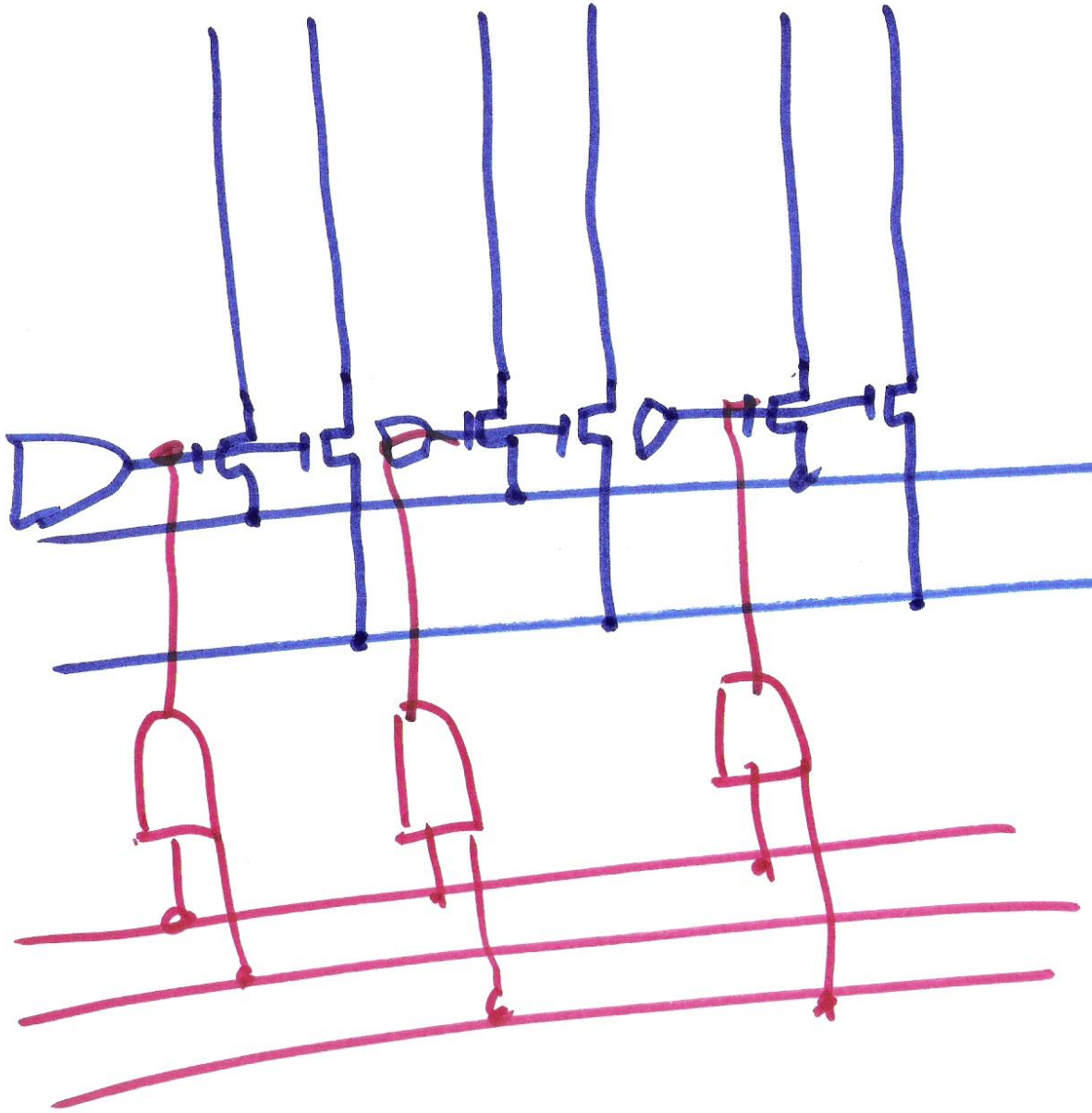
x4 → $Col = 2^{12} \times 4$

x8 → $Col = 2^{11} \times 8$

x16 → Col Addr. $= 2^{10} \times 16$



512 x 512

256kb

BANK=

256 Mb

Row lines 1,000 Array

16K

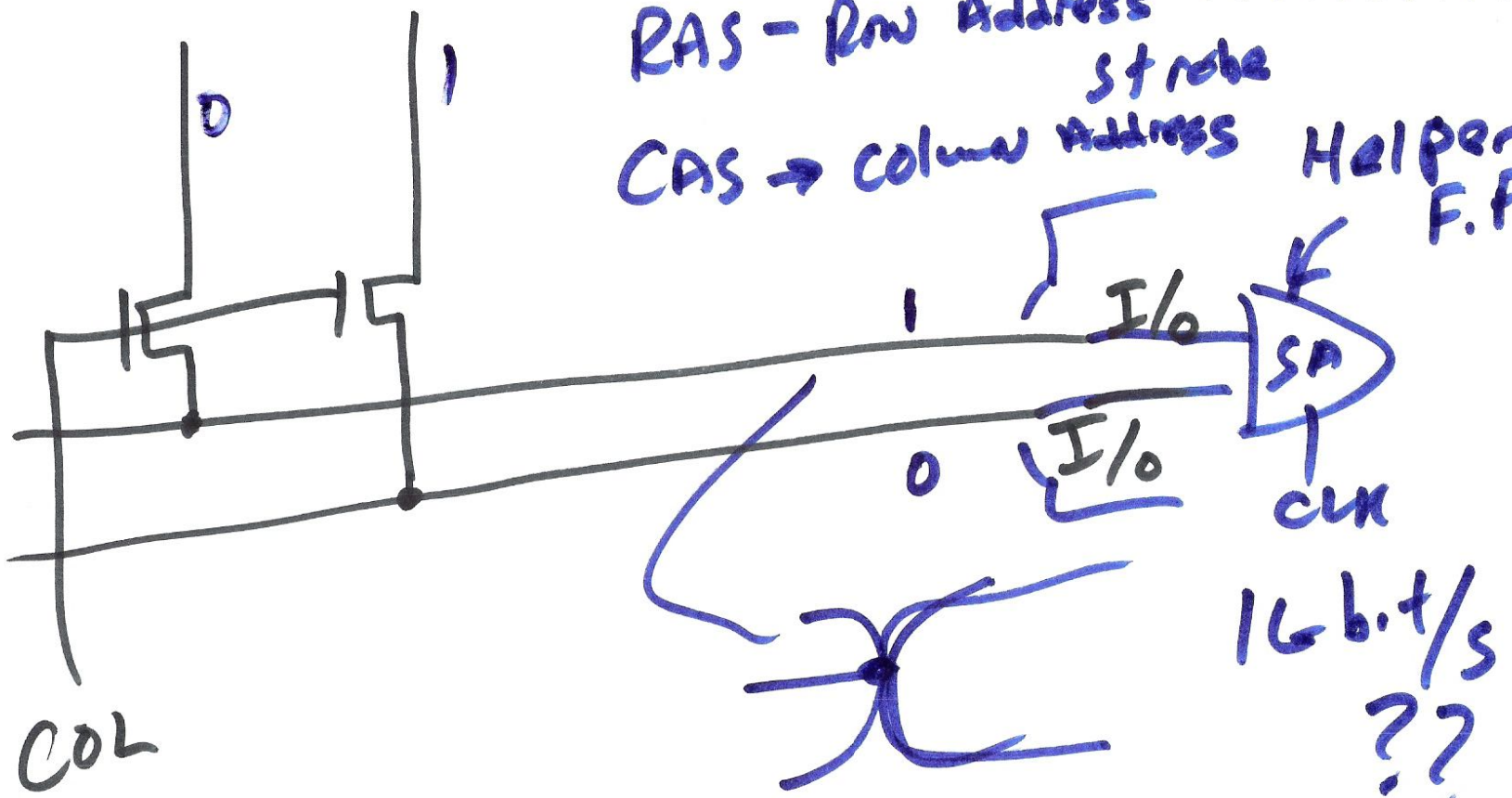
512K wordlines

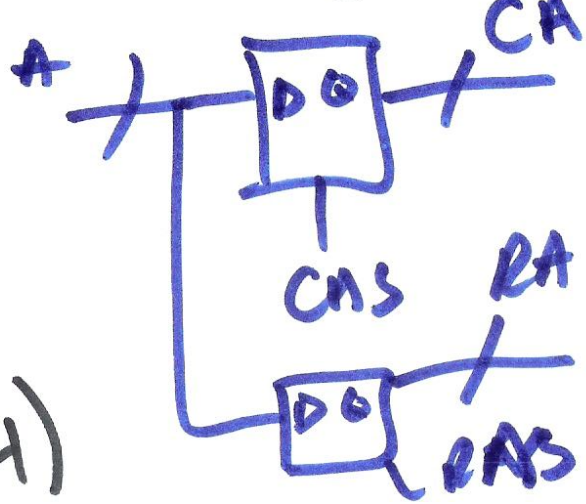
ARRAY

32 ARRAYS

Active at a time

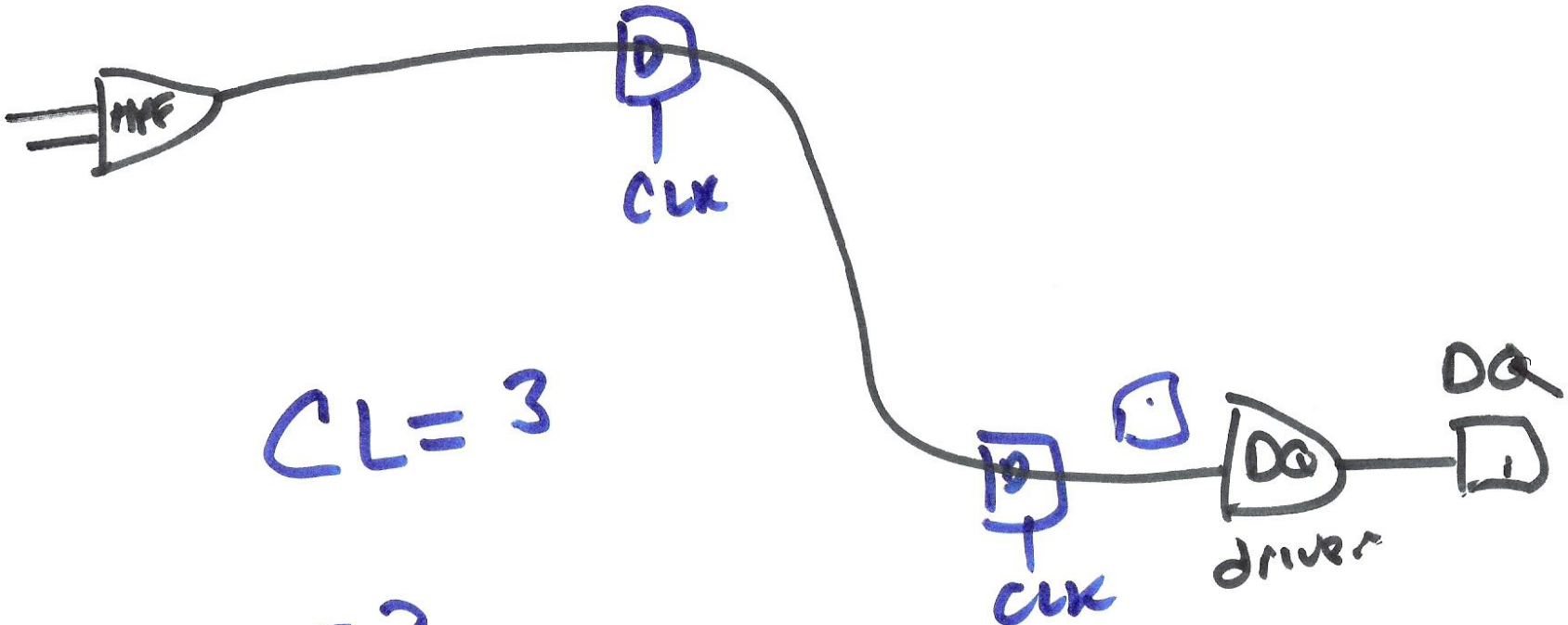
3)


RAS - Row Address Strobe
CAS → Column Address
Helper F.F.
0
1
I/O
I/O
SA
CLK
16 b.t/s
??
COL dec.
EQ first


A
CA
CAS
RA
RAS

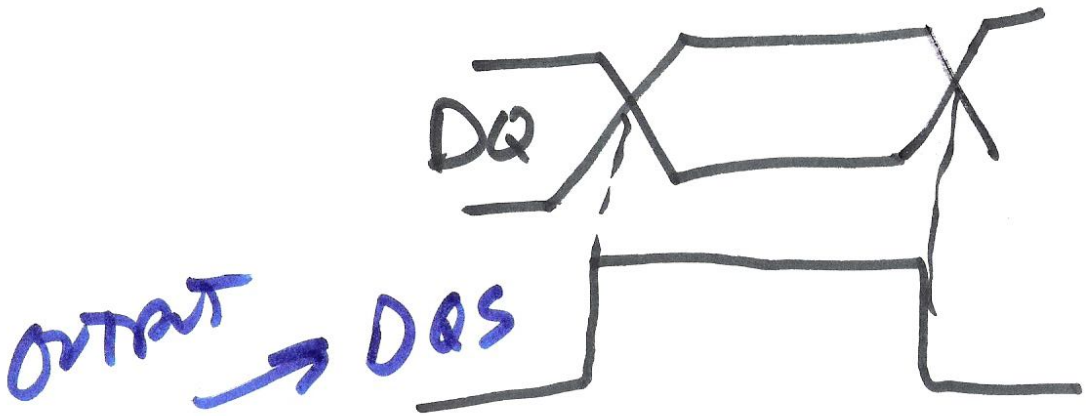
Pipelie

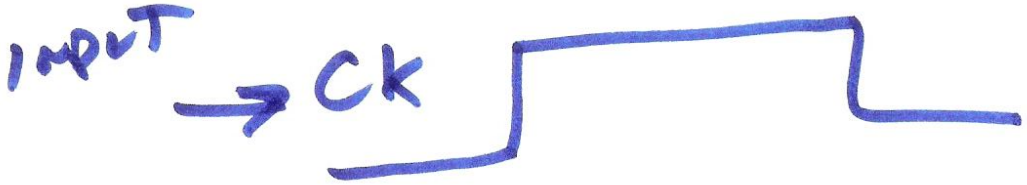
4)



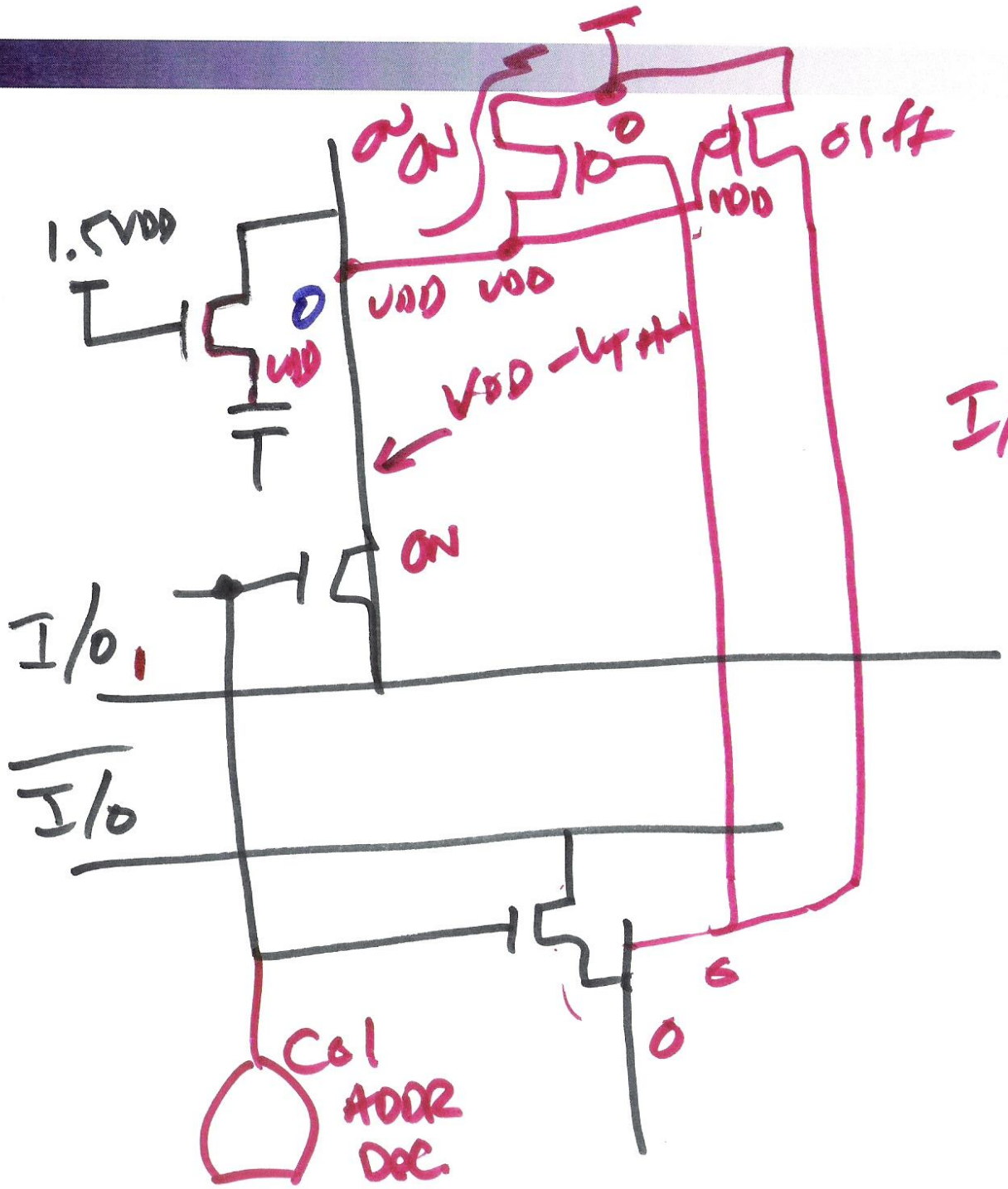
CL = 3

COST?





5)



I/O transistor has to stronger than p-sense!