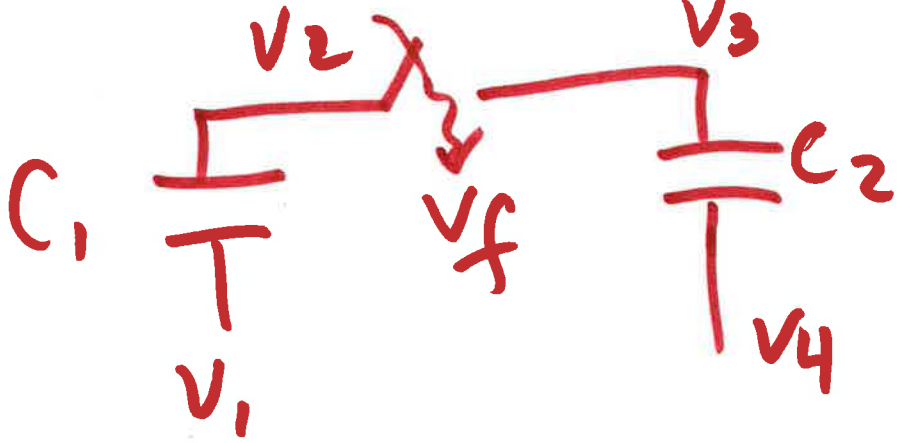
ECE 5/418 memory circuits

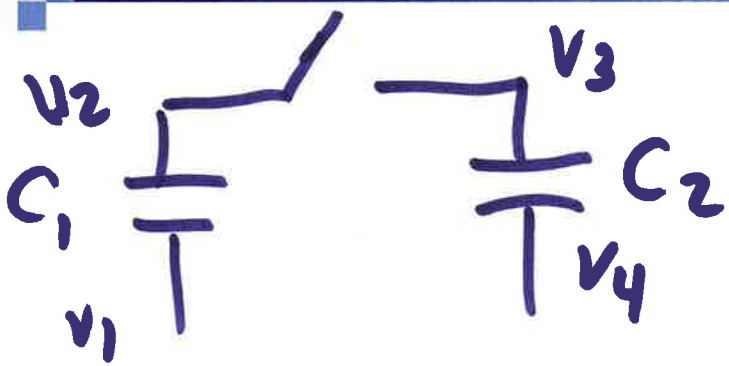
2/7/11

H.W. #6

1) use TSMC 180nm
- Simulate reading a 1 and a 0 in a DRAM (show Eq. N-sense, P-sense)

2) Show energy isn't conserved in capacitive divider. Where did it go? 2 sharing





$$Q_1 = C_1(V_2 - V_1)$$

$$Q_2 = C_2(V_3 - V_4)$$

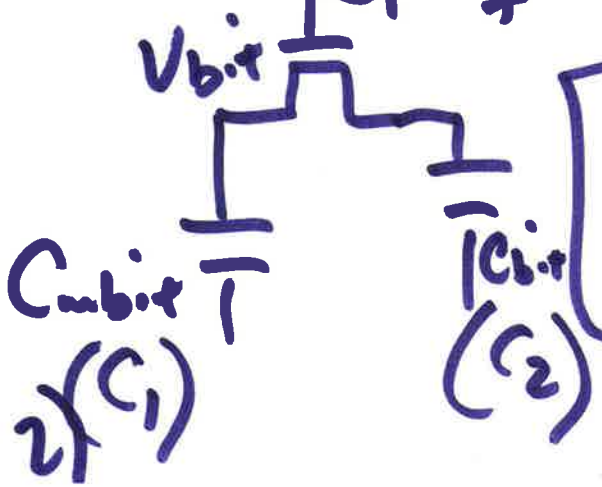
Charge must be conserved

$$Q_f = Q_1 + Q_2$$

$$Q_f = C_1(V_f - V_1) + C_2(V_f - V_4)$$

$$C_1 V_f + C_2 V_f = C_1 V_2 + C_2 V_3$$

$$V_f = \frac{C_1 V_2 + C_2 V_3}{C_1 + C_2}$$



Energy

$$\frac{1}{2}C_1(V_2-V_1)^2 + \frac{1}{2}C_2(V_3-V_4)^2$$

$$= \frac{1}{2}C_1(V_f-\cancel{V_1}^{0})^2 + \frac{1}{2}C_2(V_f-\cancel{V_4}^{0})^2$$

$$V_f = \frac{C_1V_2 + C_2V_3}{C_1 + C_2}$$

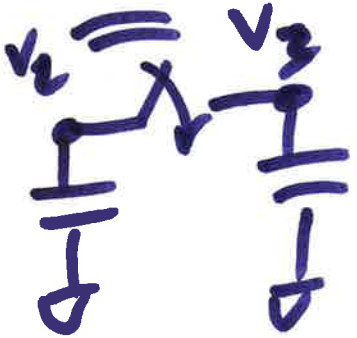
$$= \frac{1}{2}C_1\left(\frac{C_1V_2 + C_2V_3}{C_1+C_2}\right)^2 + \frac{1}{2}C_2\left(\frac{C_1V_2+C_2V_3}{C_1+C_2}\right)^2$$

3)

$$\frac{1}{2}\left(C_1 V_2^2 + C_2 V_3^3\right) =$$

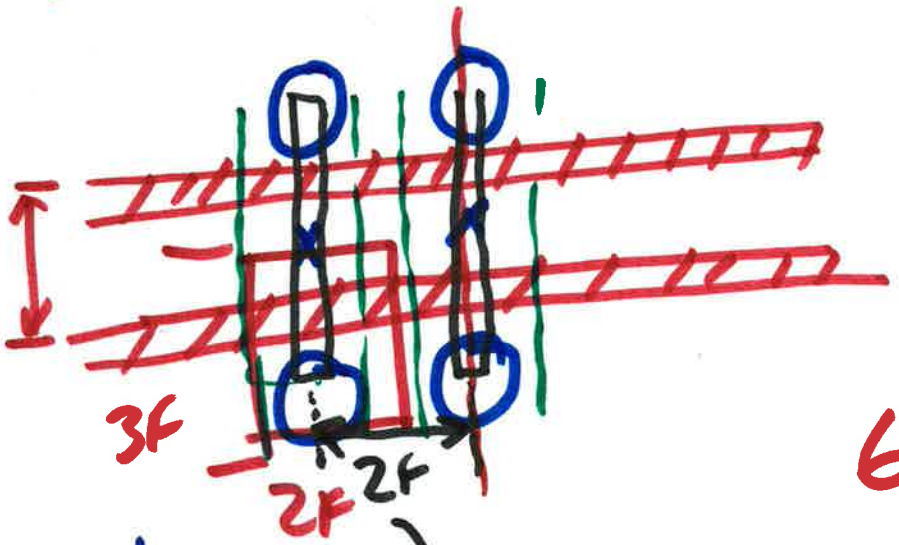
$$\frac{1}{2}(C_1 + C_2)\left(\frac{C_1 V_2 + C_2 V_3}{C_1 + C_2}\right)^2$$

$$= \frac{(C_1 V_2 + C_2 V_3)^2}{C_1 + C_2}$$



$$\stackrel{?}{=} C_1 V_2^2 + C_2 V_3^2$$

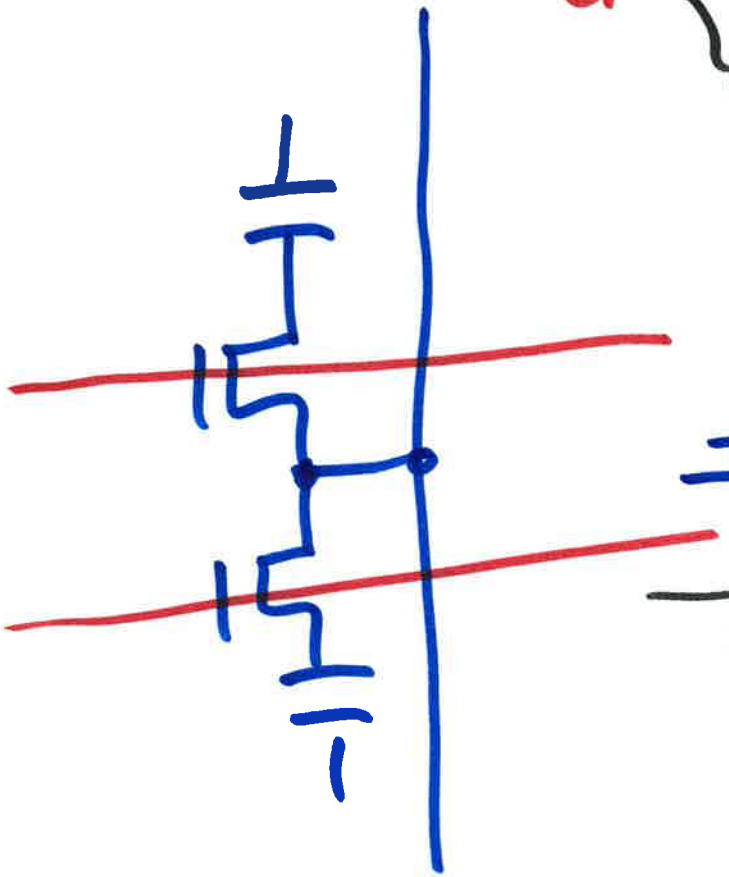
4)

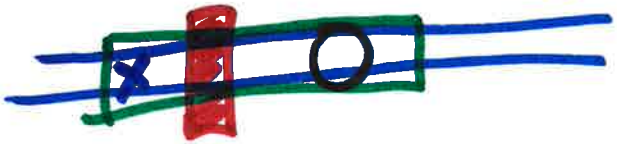


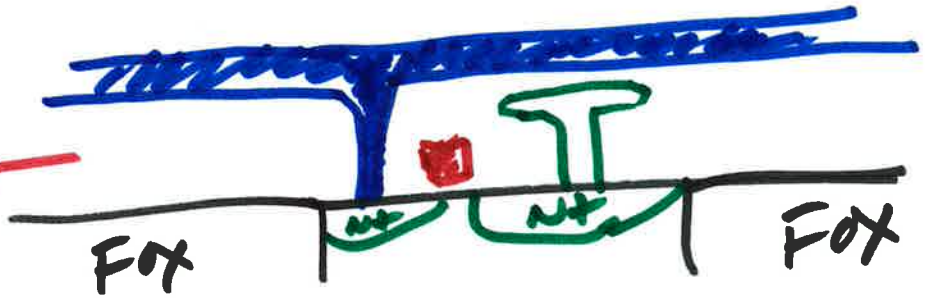
$6F^2$ Open

Bitline pitch

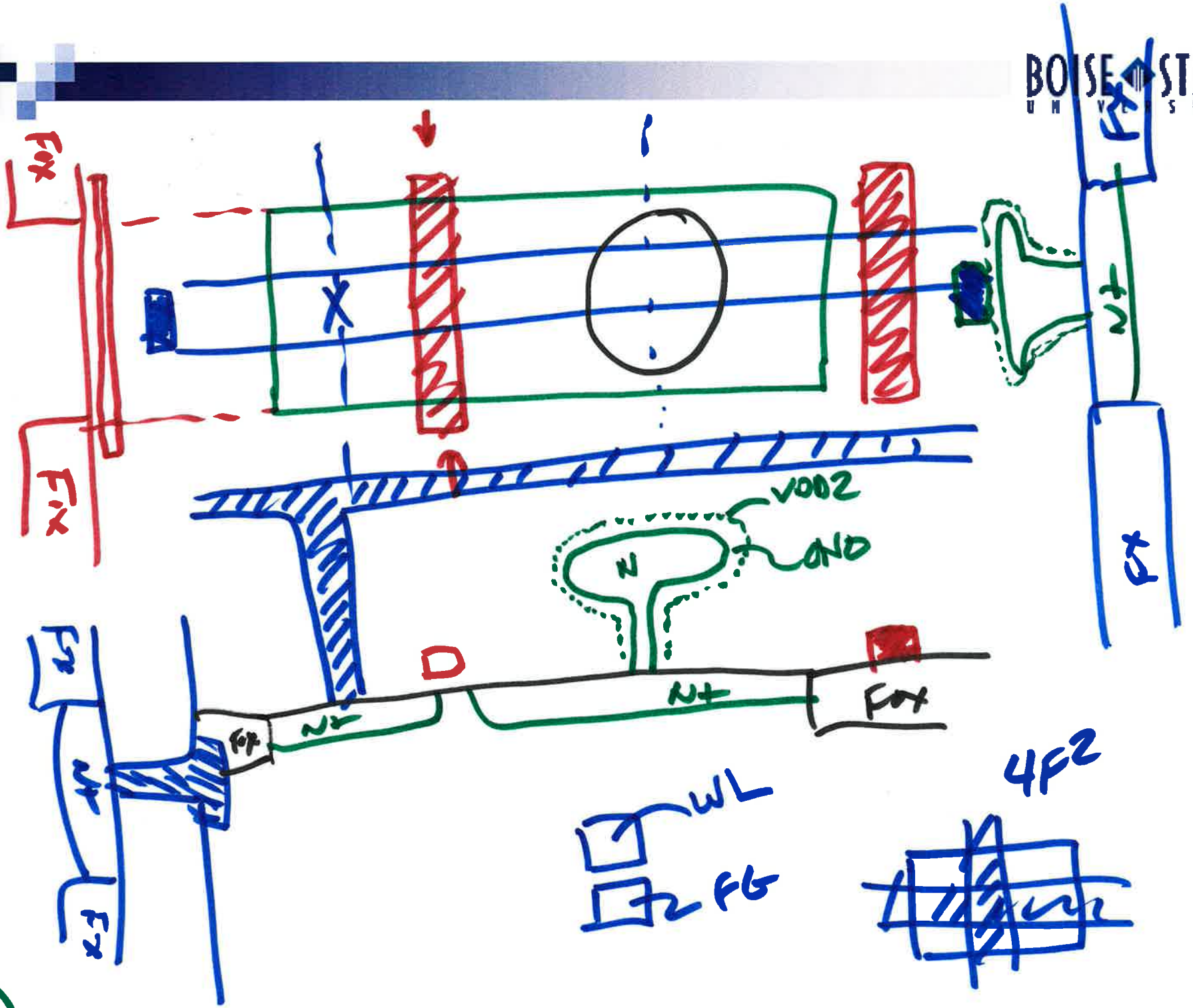
Buried capacitor







5)

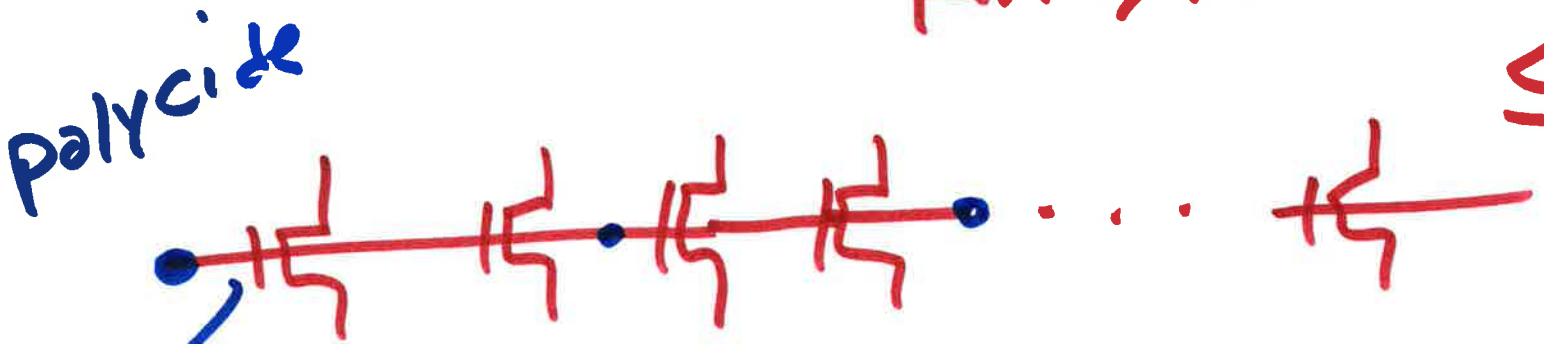


6)

Word line delay

Opening a row

FAST → reduce # of cols. ≤ 512



~ 5ns to open a row?

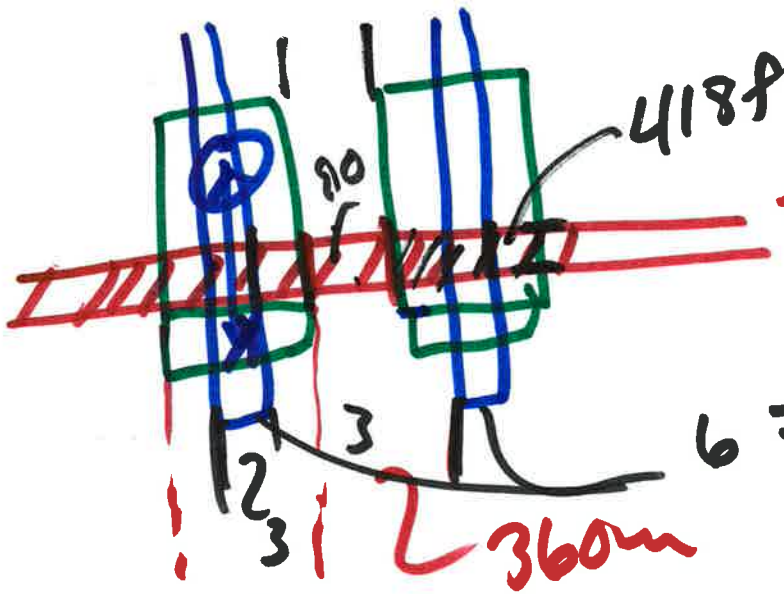
tricks

W/L

Example – have 512 columns

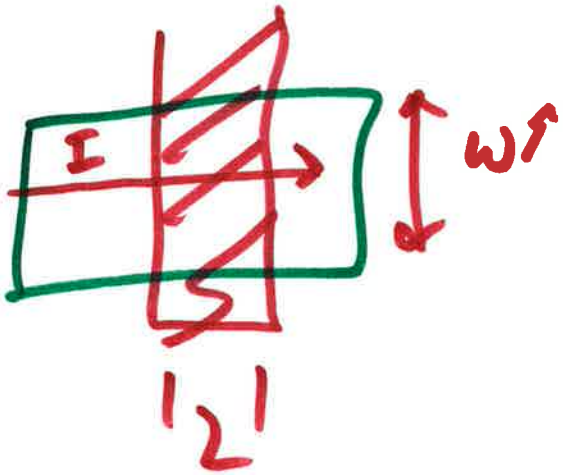
$$C_x = C_x' \cdot L \cdot W = \frac{8.6\,fF}{\mu m^2}(.18\mu)(.27\mu)$$

$$= 418\,aF \nearrow 500\,aF$$

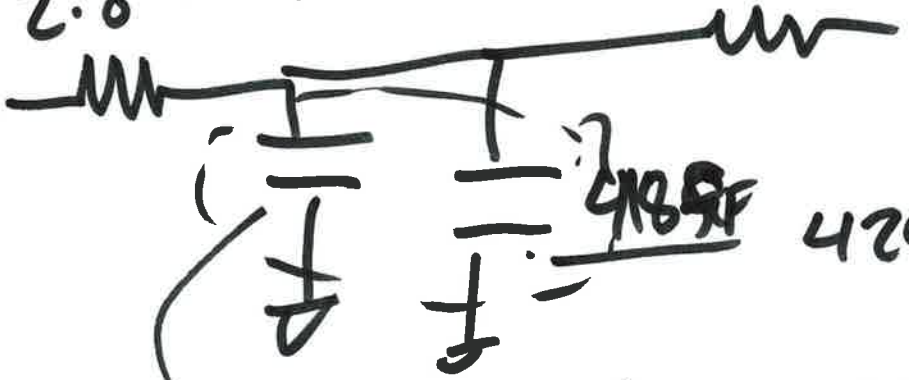


512 columns

W = 270nm



2.8 = 165Ω



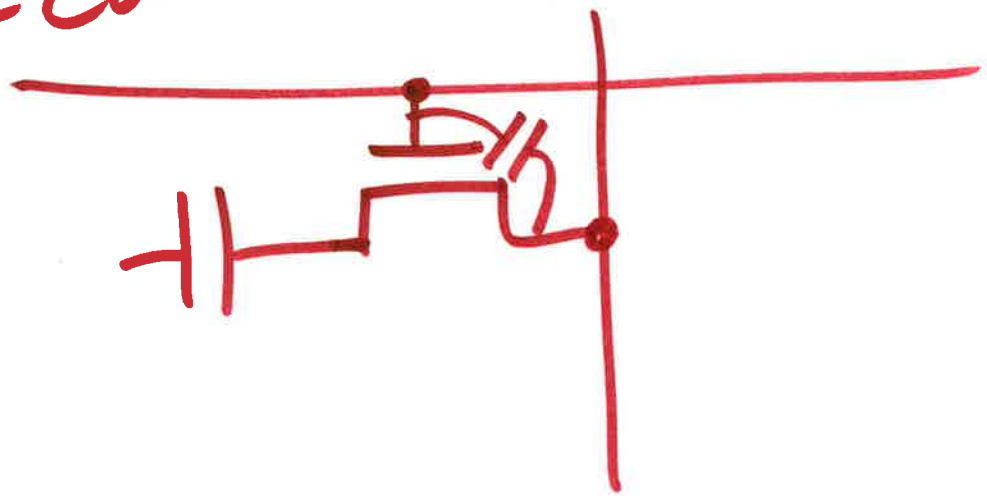
$.90 \cdot .180 \cdot 100\,aF/\mu m^2 = 1.62\,aF$

$t_d = 0.35 \cdot 16 \cdot 420\,aF \cdot 512^2$

$= 616\,ps$

8)

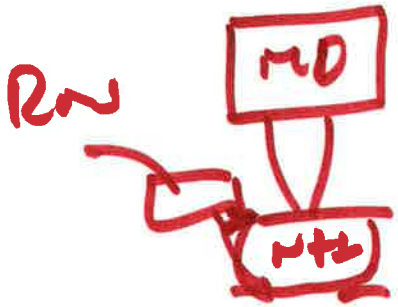
512 Colums



512 x 512

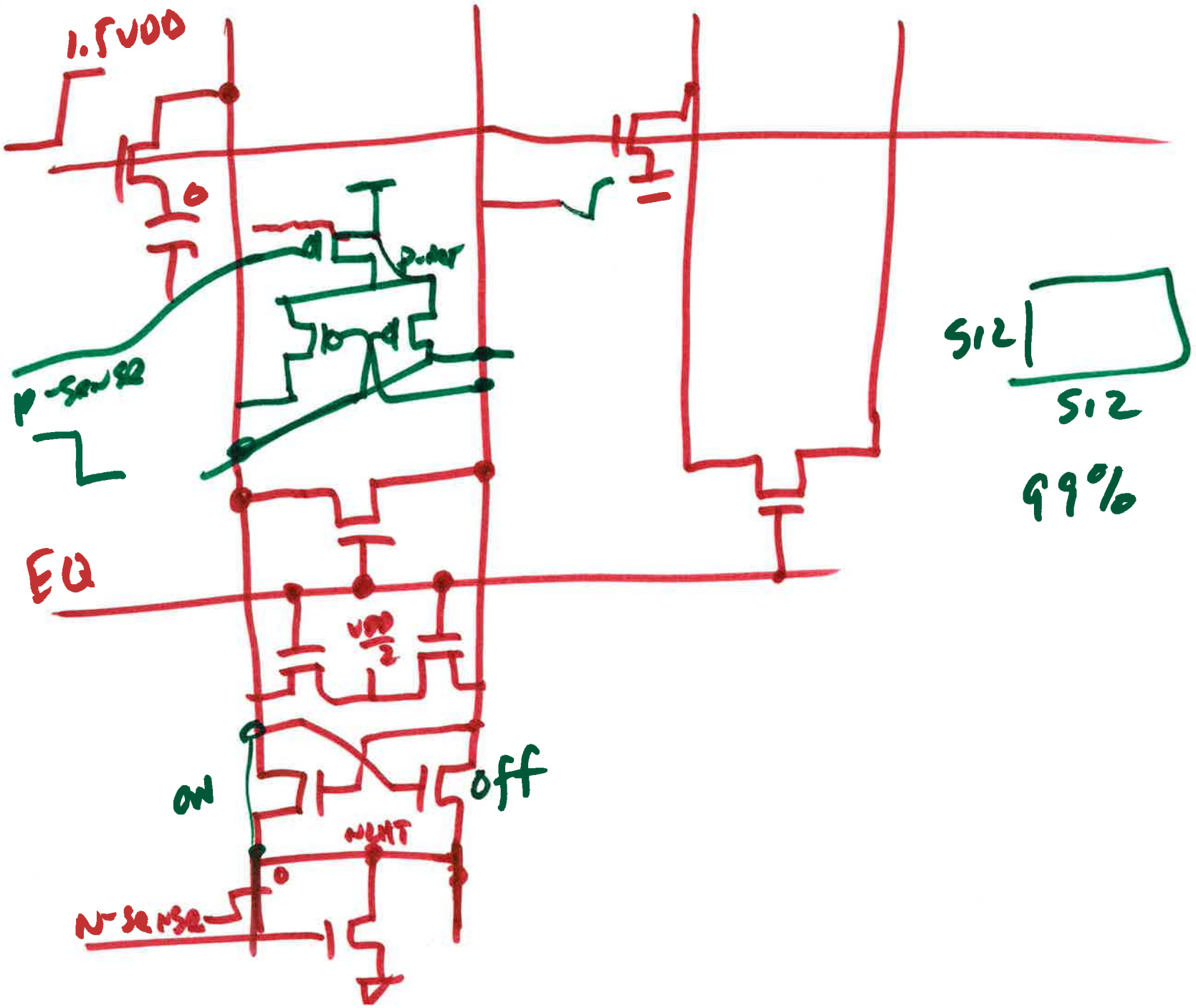
256Kb

1Gb

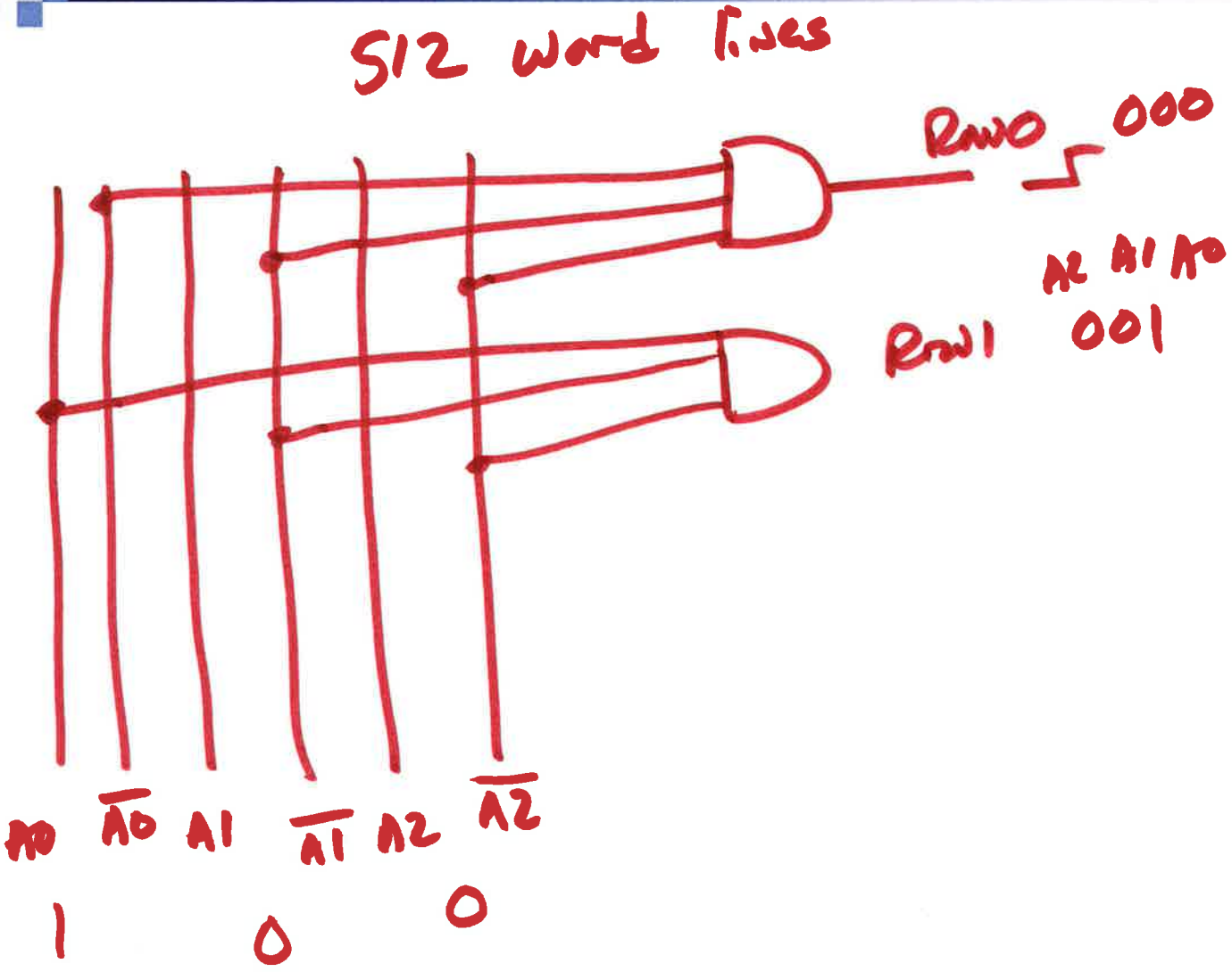


$C_{GDO} \cdot W \cdot 512 +$
$C_j \cdot 512$

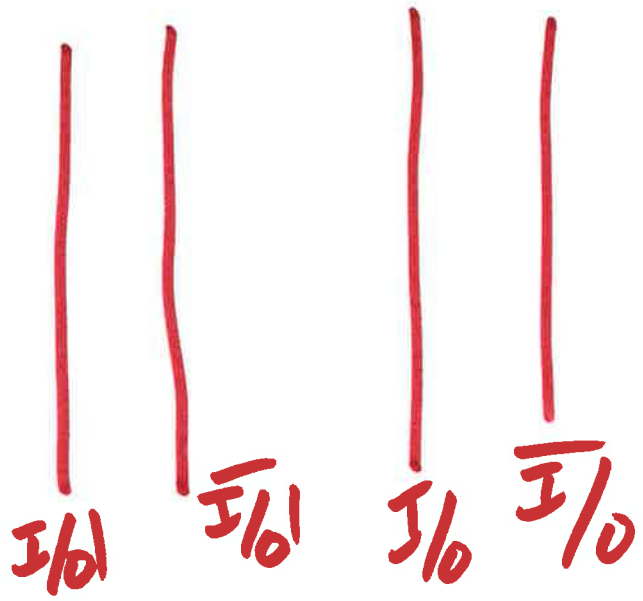
9)



10)


512 word lines
Row0
000
A2 A1 A0
Row1
001
A0
$\overline{A0}$
A1
$\overline{A1}$
A2
$\overline{A2}$
1
0
0

11)



×1
×2
×4
×8

13)