1) Layout 51-stage ring osc
& DRC/LVS

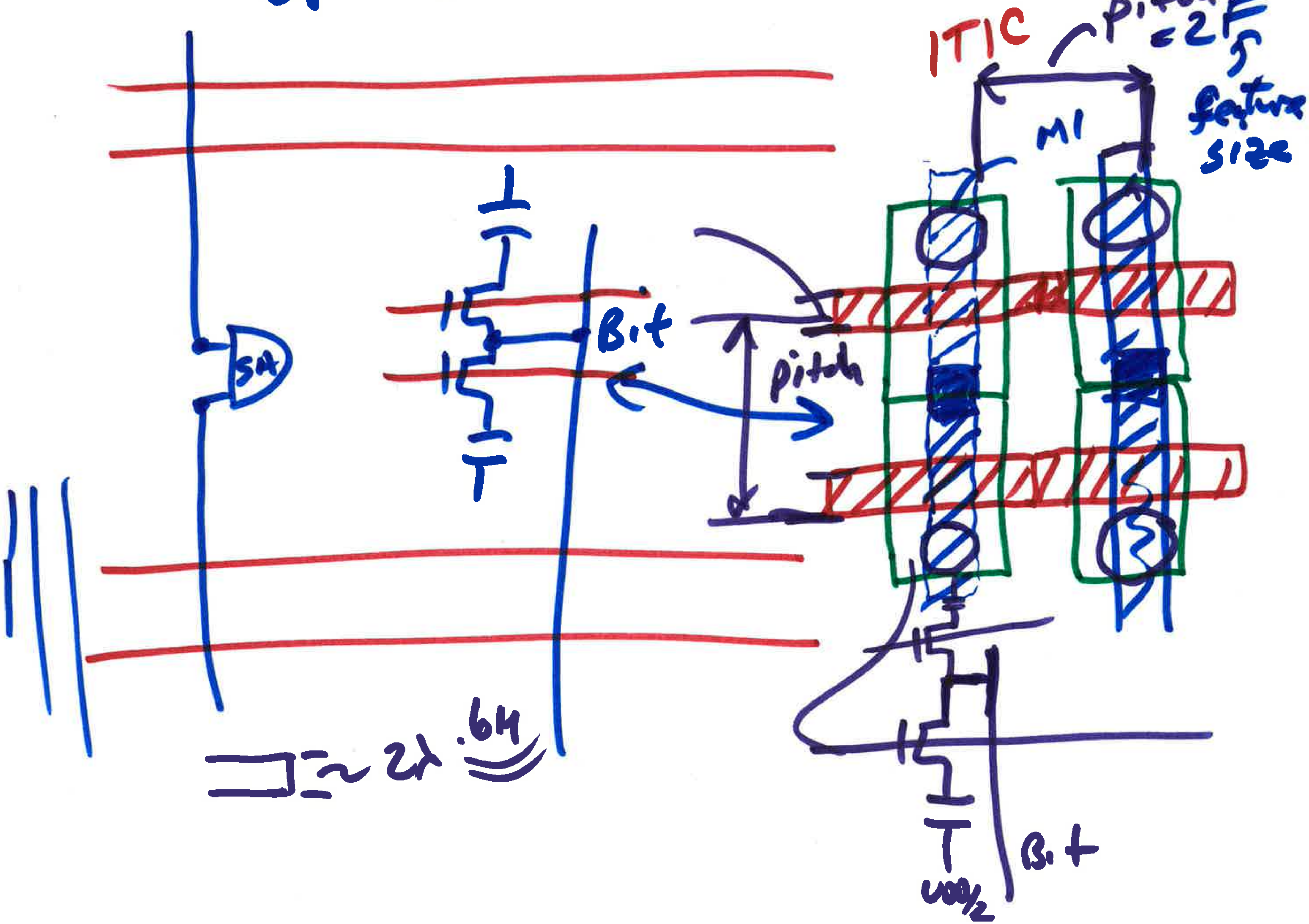
2) simulate EQ, N-sense P-sense (read operation) using TSMC 180nm process
↳ wait

VDD = 1.8
$C_{mid} = 30fF$
$C_{bit} = 200fF$

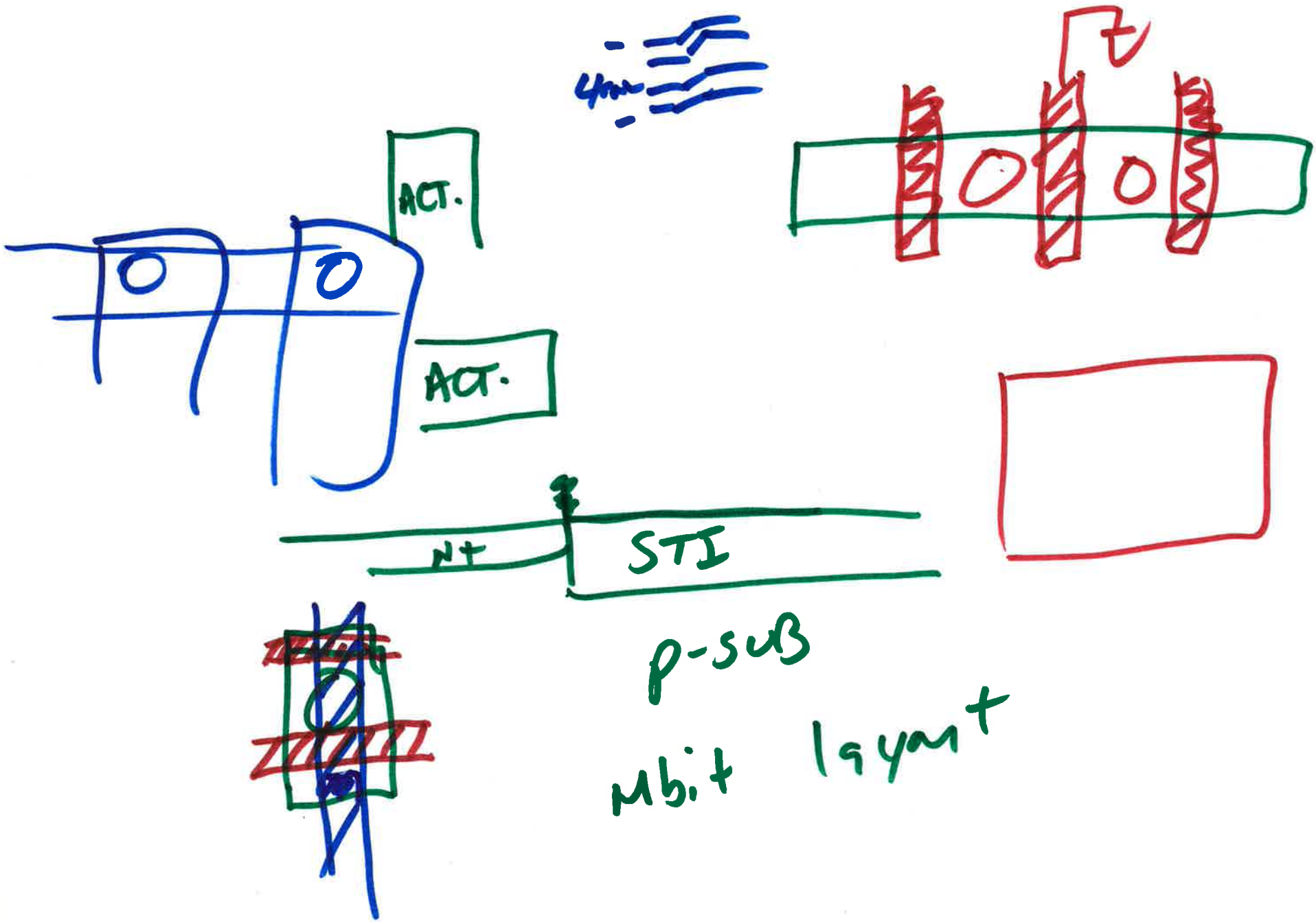
Reading a 1 & 0
READING

1)

open folded



2)


4nm
ACT.
ACT.
N+
STI
p-sub
Mbit layout