H.W. # 4

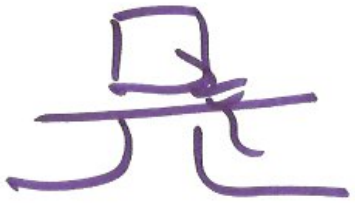
16.1 - 16.3

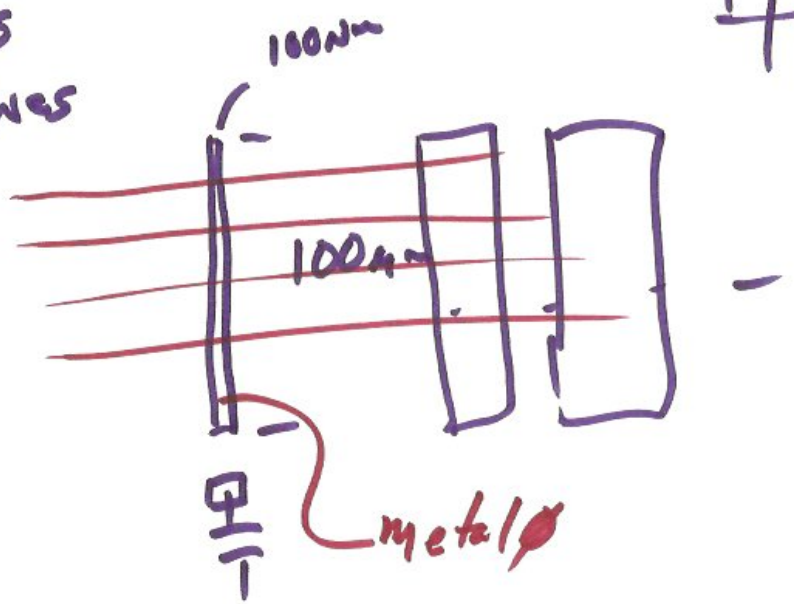
using TSMC 180nm process

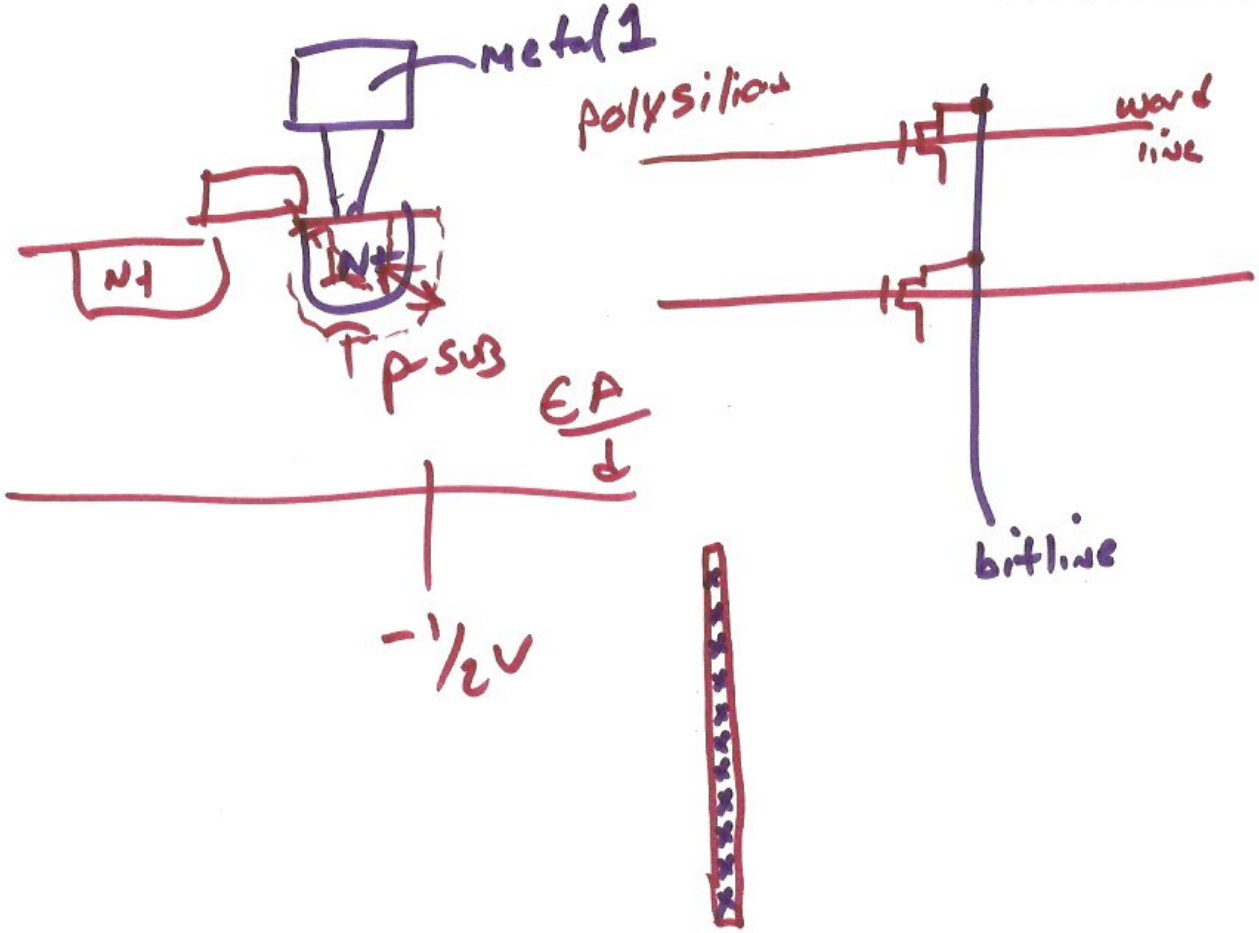
270n / 180n

overlap cap $C_{gdo}.W$ / $C_{gso}.W$

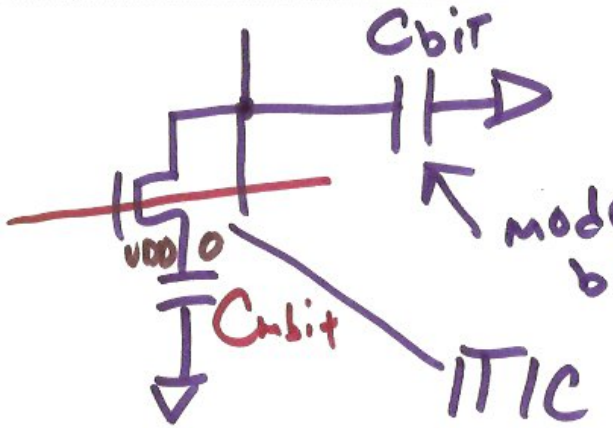
bit lines
digit lines
column lines
word lines
row lines

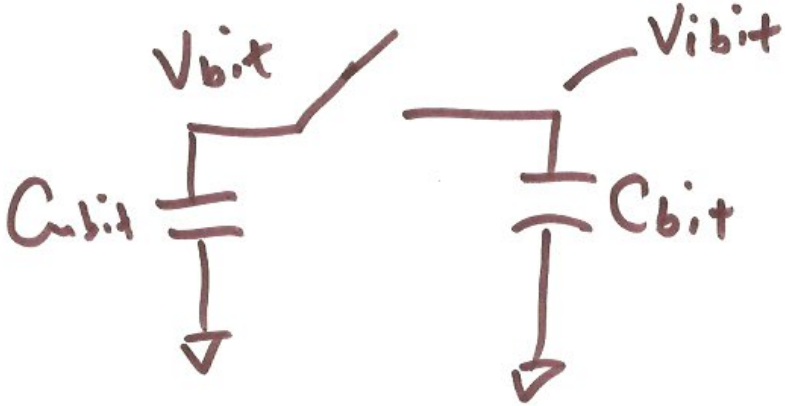





Metal 1
polysilicon
word line
N+
N+
P sub
$\frac{\epsilon A}{d}$
bitline
$-\frac{1}{2}V$

2)



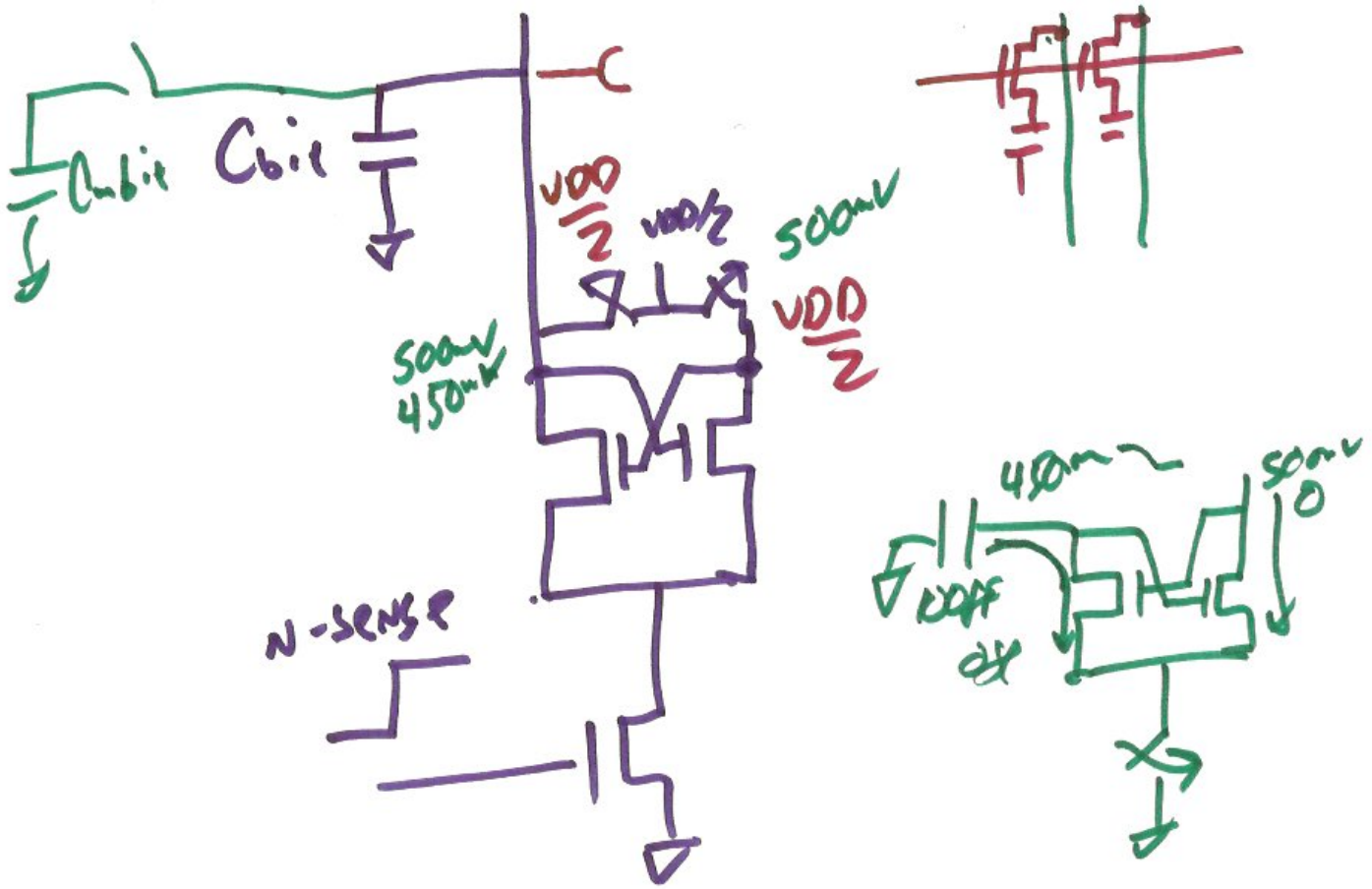


$C_{mbit} \cdot V_{bit} + V_{ibit} \cdot C_{bit}$

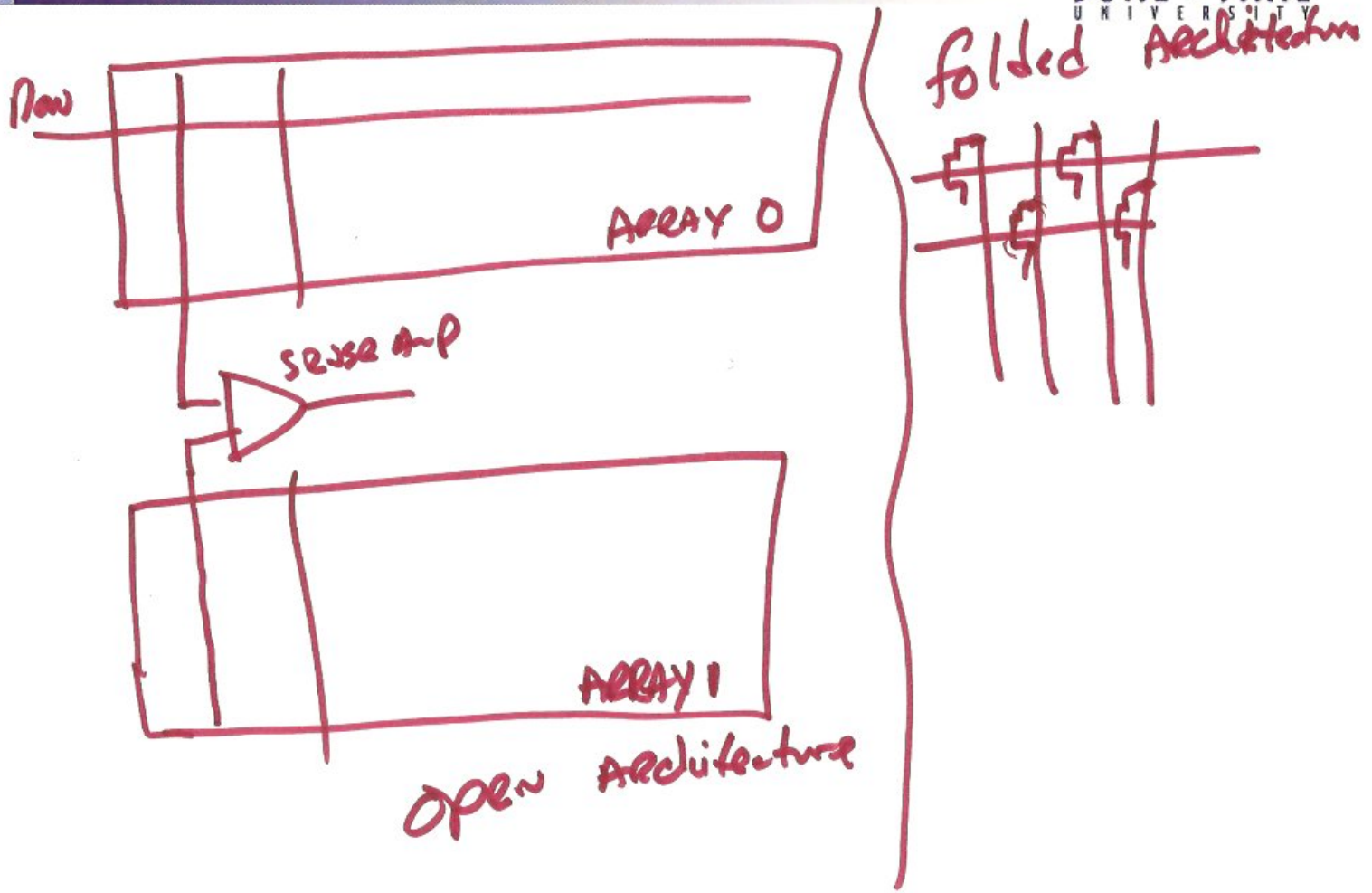
$= V_f (C_{bit} + C_{mbit})$

$$V_f = \frac{C_{mbit} \cdot V_{bit} + V_{ibit} \cdot C_{bit}}{C_{bit} + C_{mbit}}$$

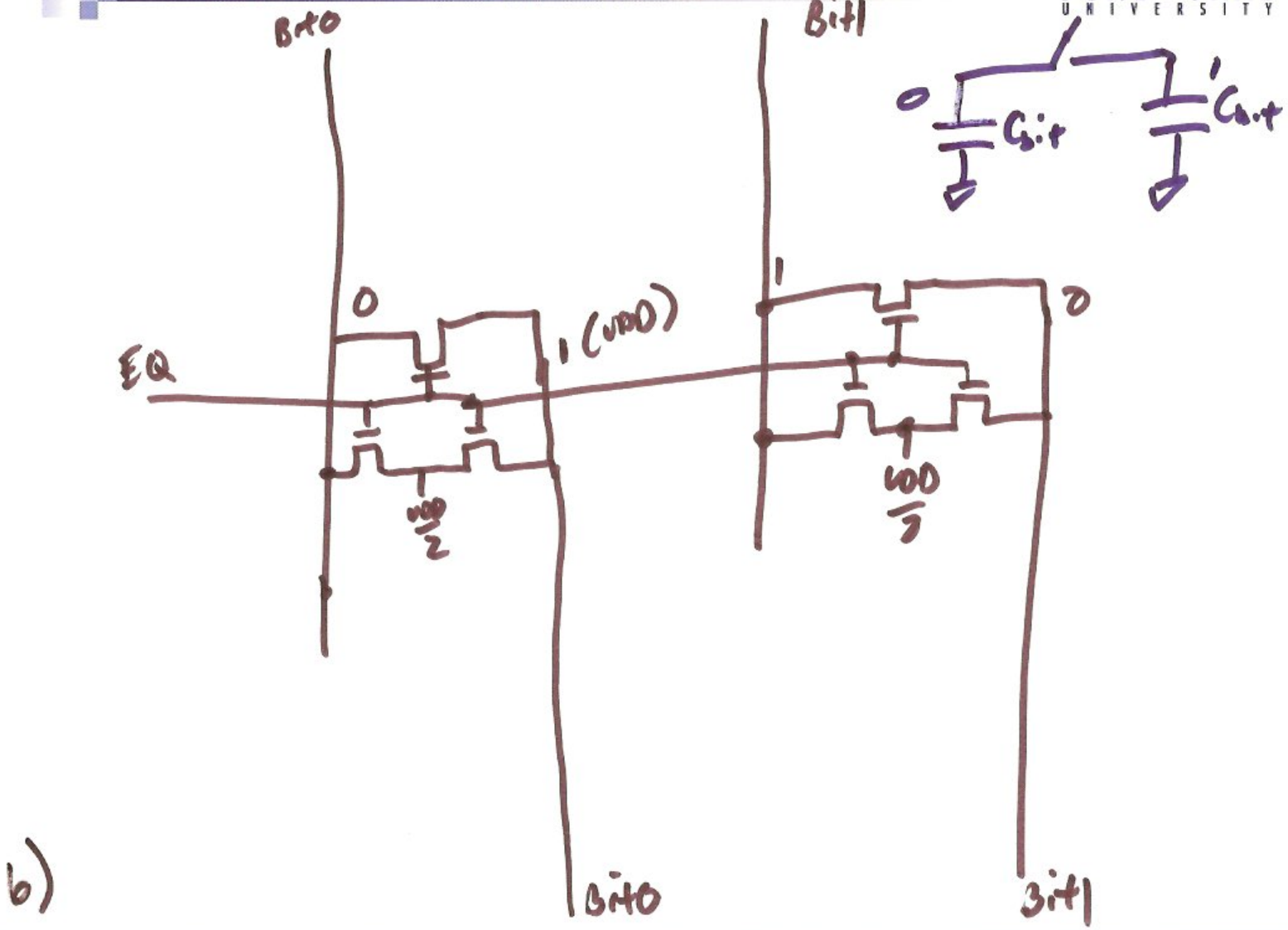
3)

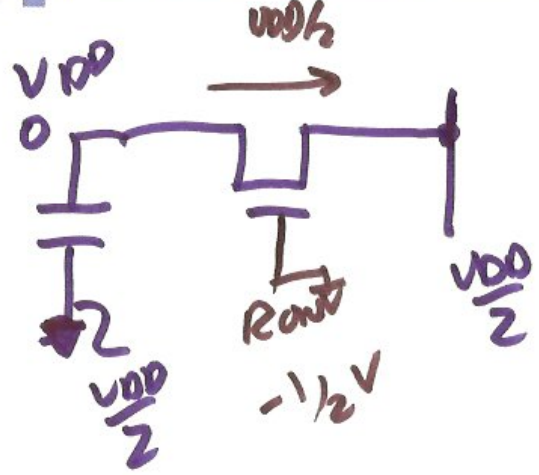


4)


folded Architecture
Row
ARRAY 0
sense amp
ARRAY 1
open Architecture

5)

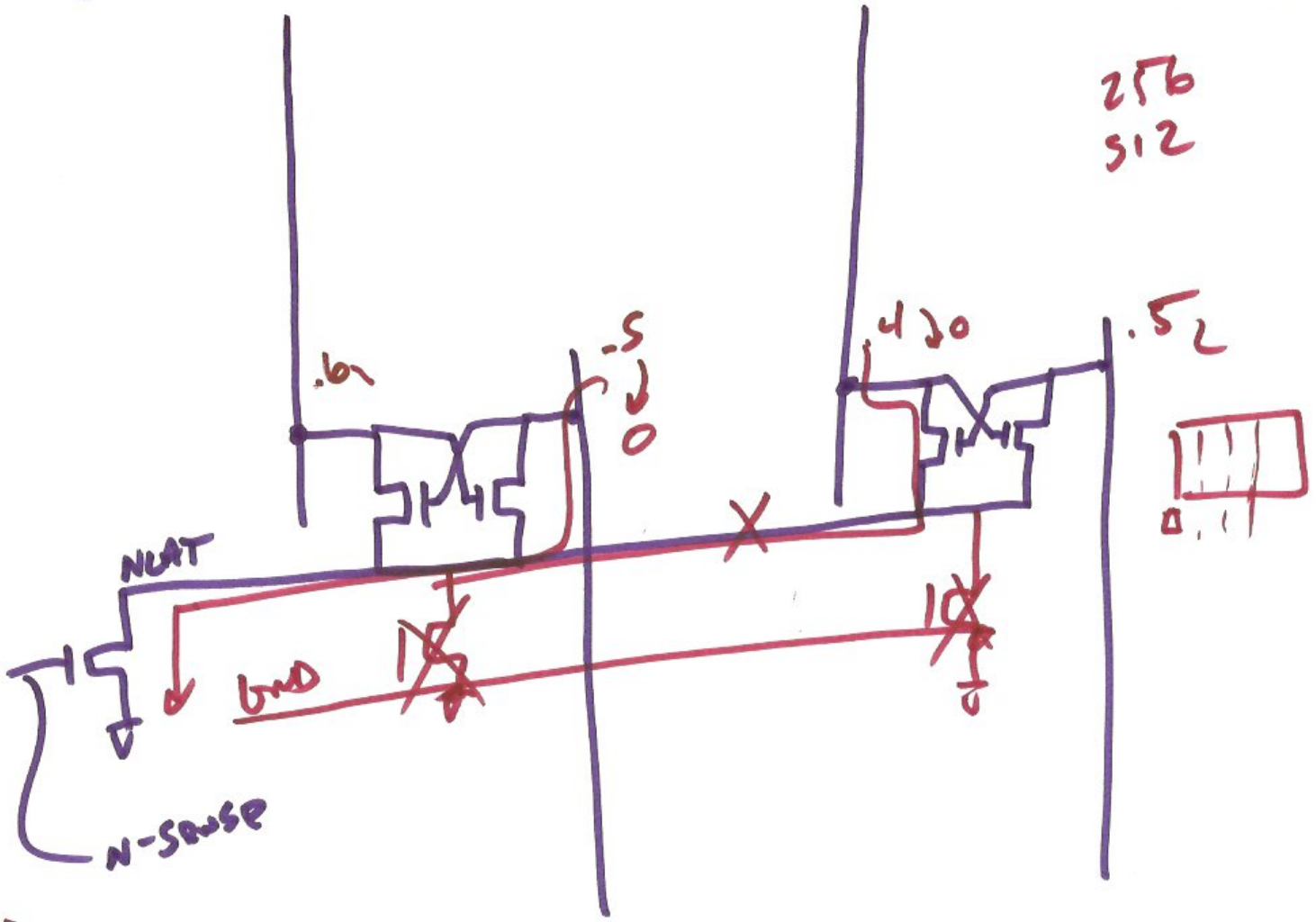

BOISE STATE UNIVERSITY
Bit0
Bit1
0
1
C_{bit}
C_{bit}
EQ
0
1 (VDD)
1
0
VDD/2
VDD/2
b)
Bit0
Bit1



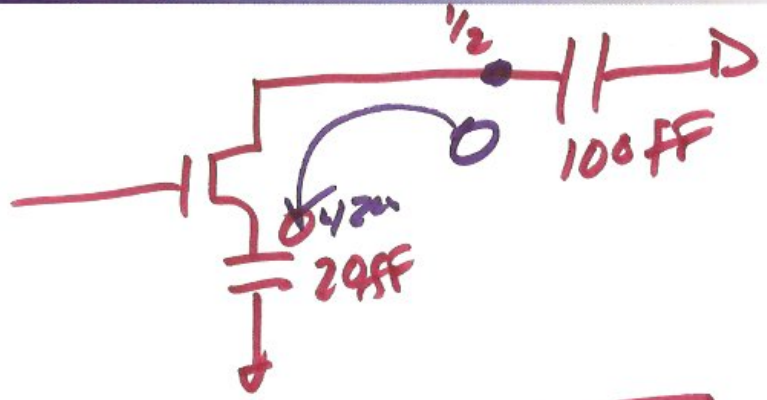
Rough dielectric

$\frac{\epsilon A}{t_{ox}}$

7)

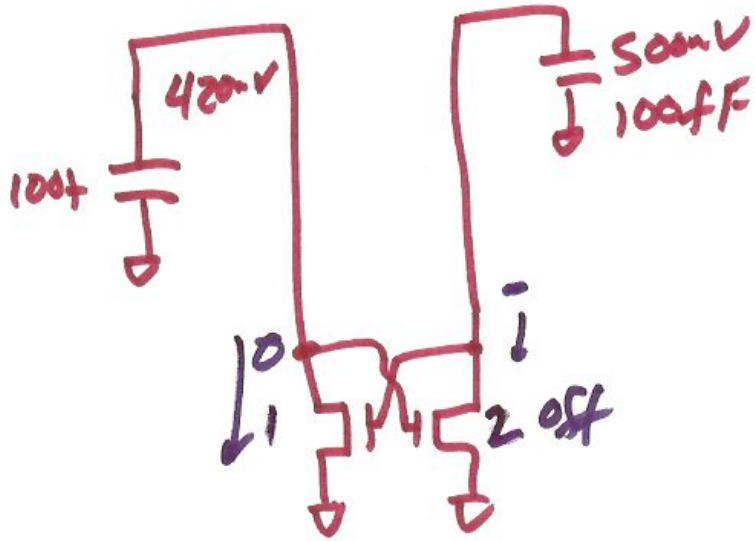


8)



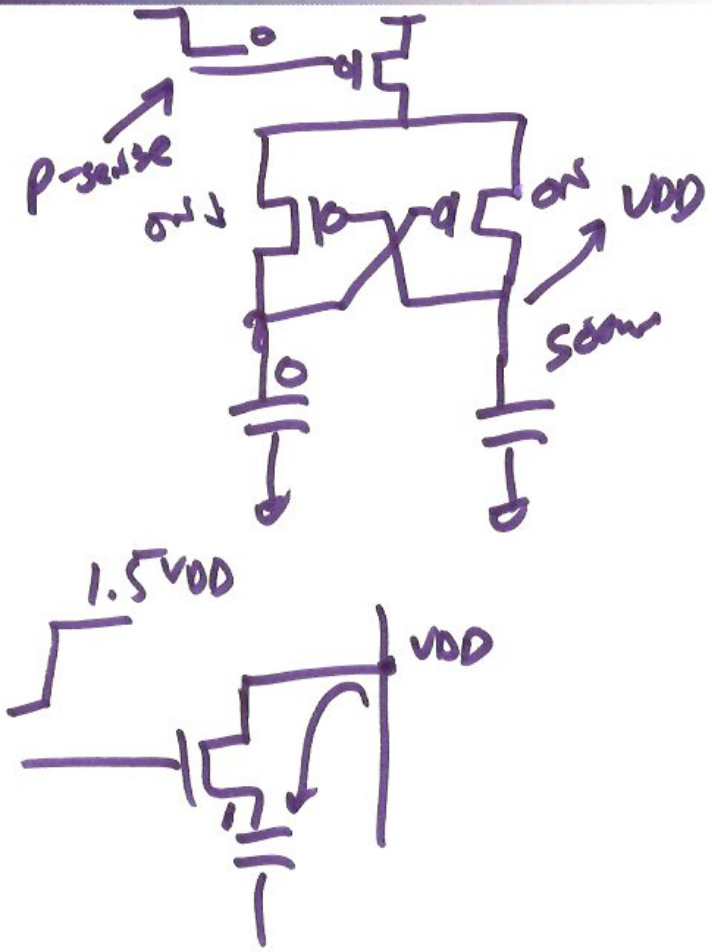
$$V_f = \frac{0.20 + \frac{1}{2}\cdot 100}{120f}$$

$$= \frac{1}{2}\cdot\frac{5}{6} = 416mV$$



9)

p-sense Amp



10)