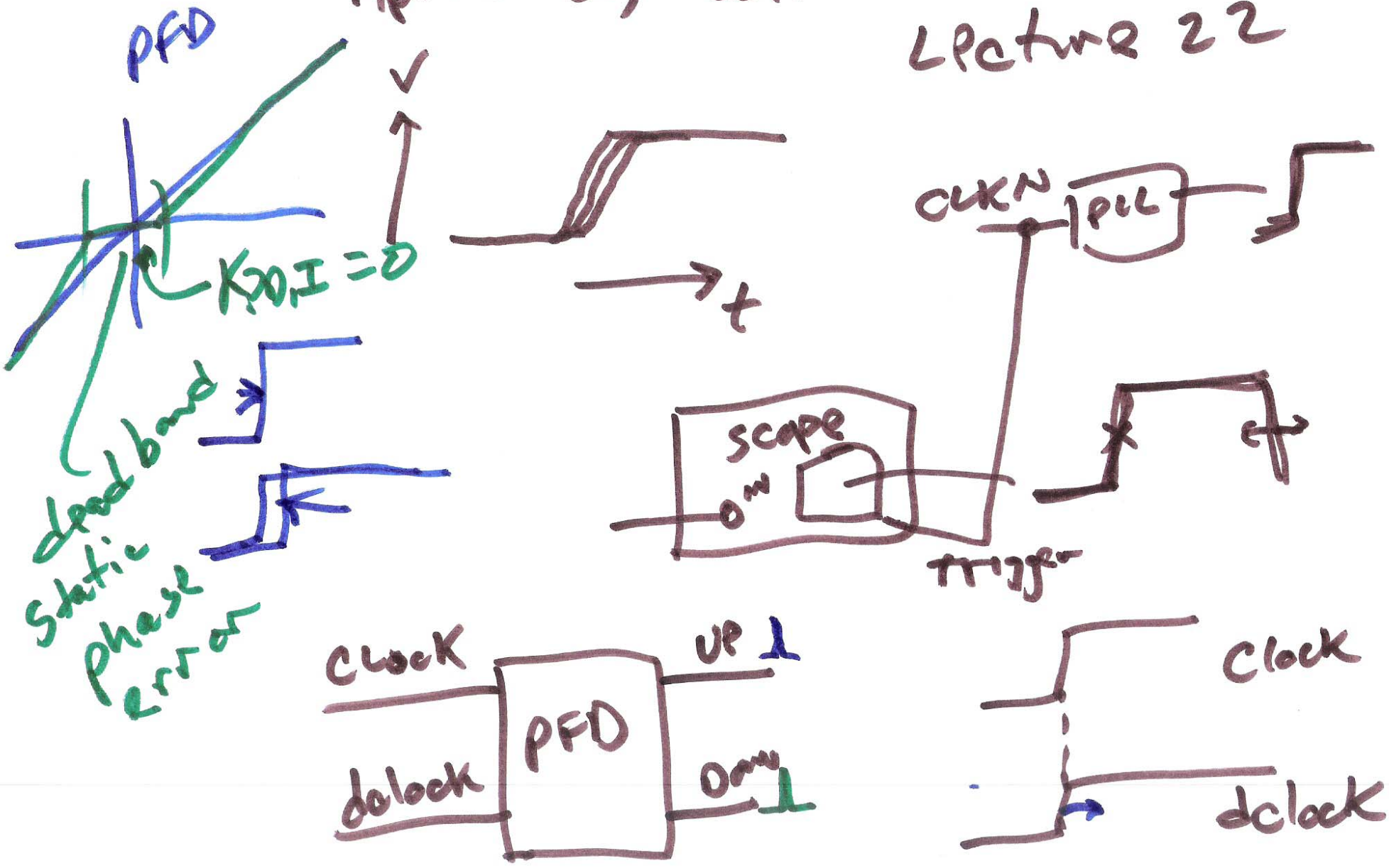
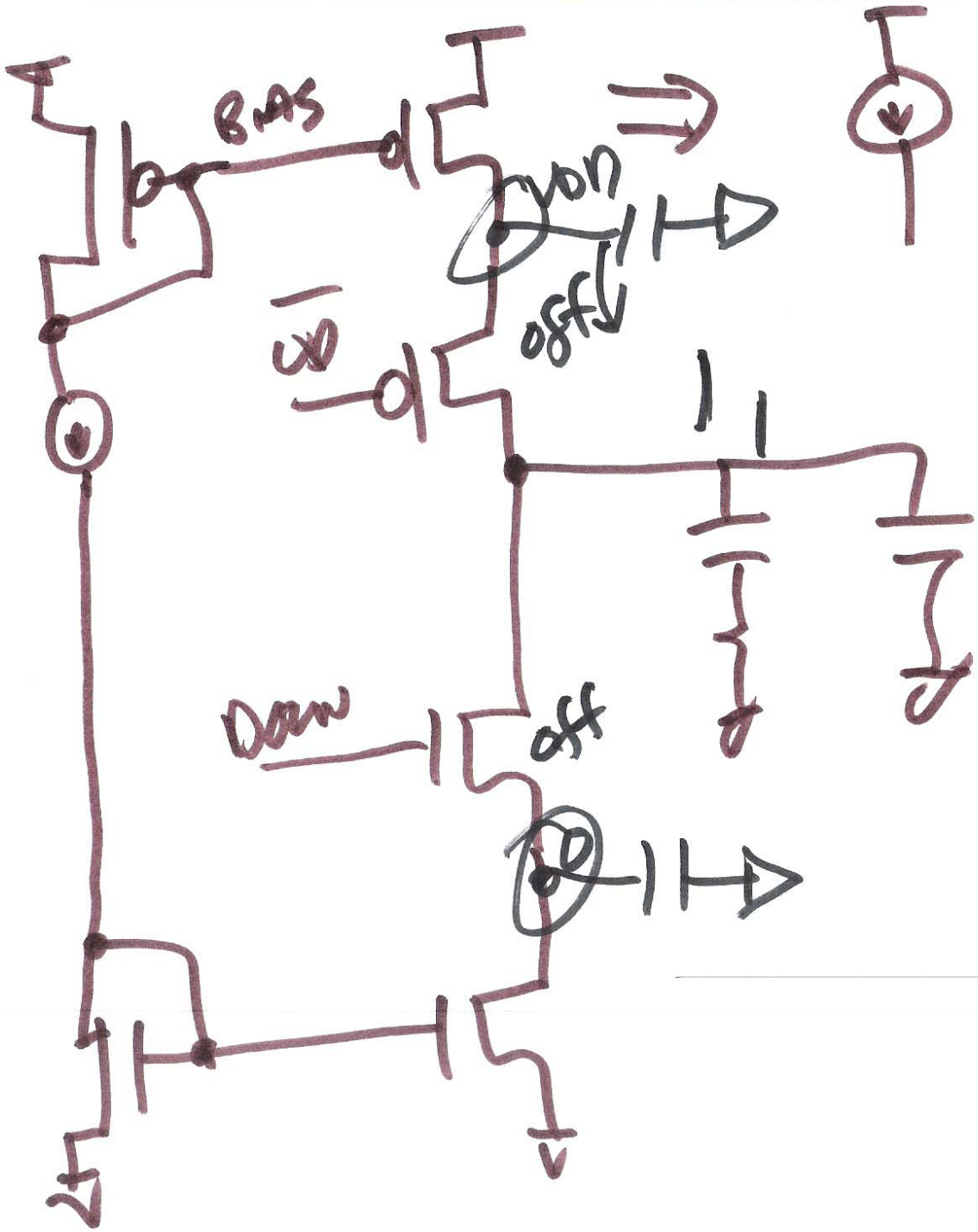
ECE 5/415 Memory Circuit Design

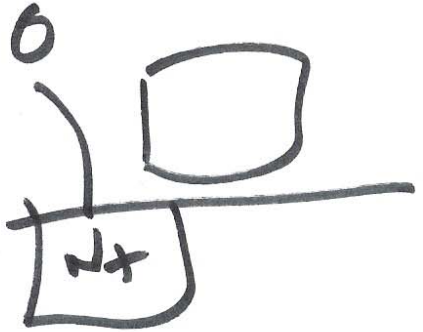
BOISE STATE UNIVERSITY

April 20, 2011

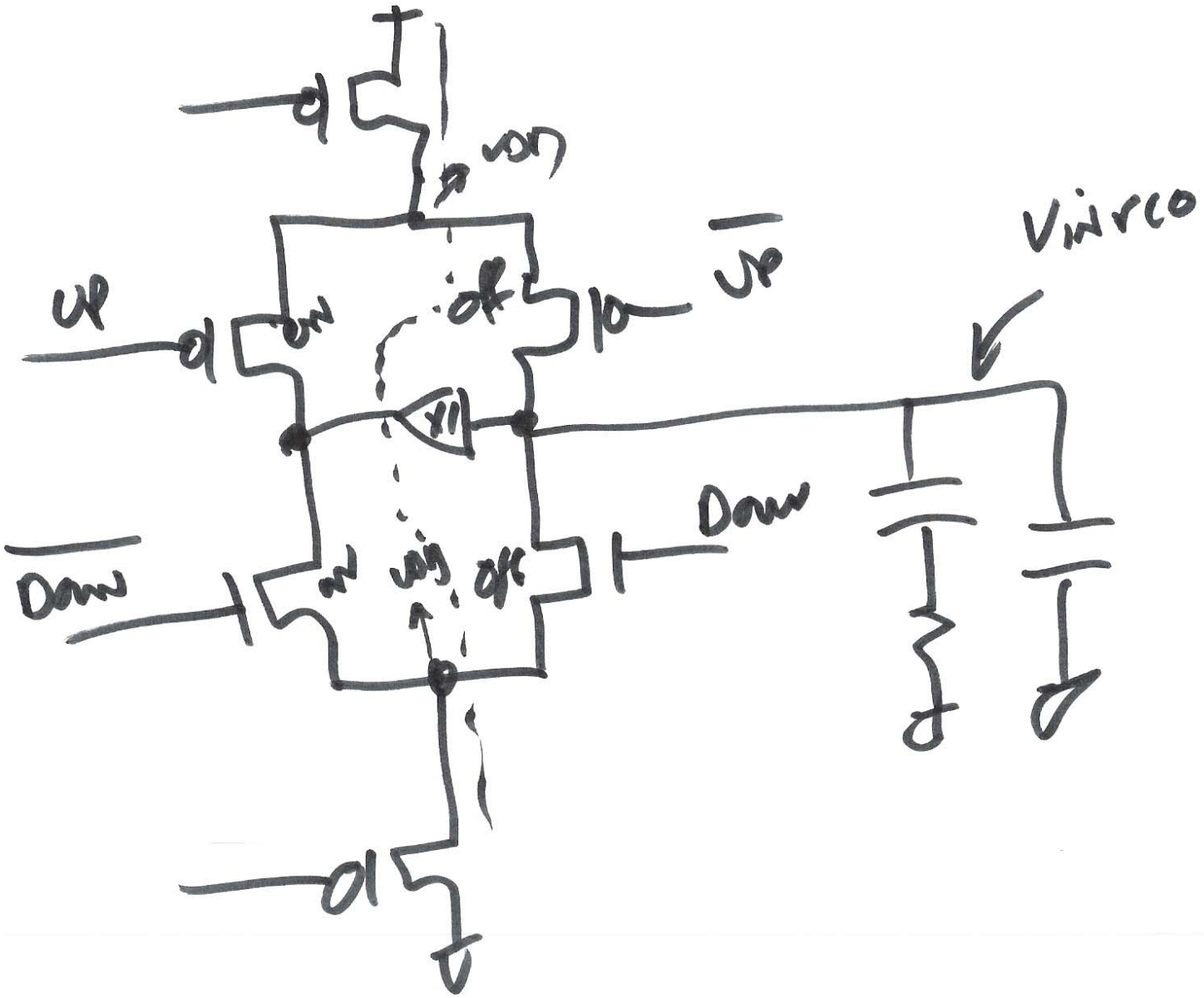
Lecture 22







2)

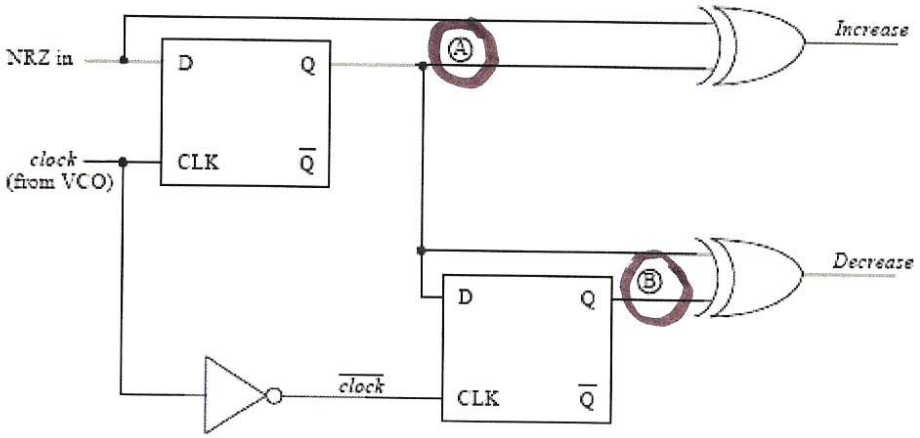


3)

PD

Locked

Hogge ALL CDR



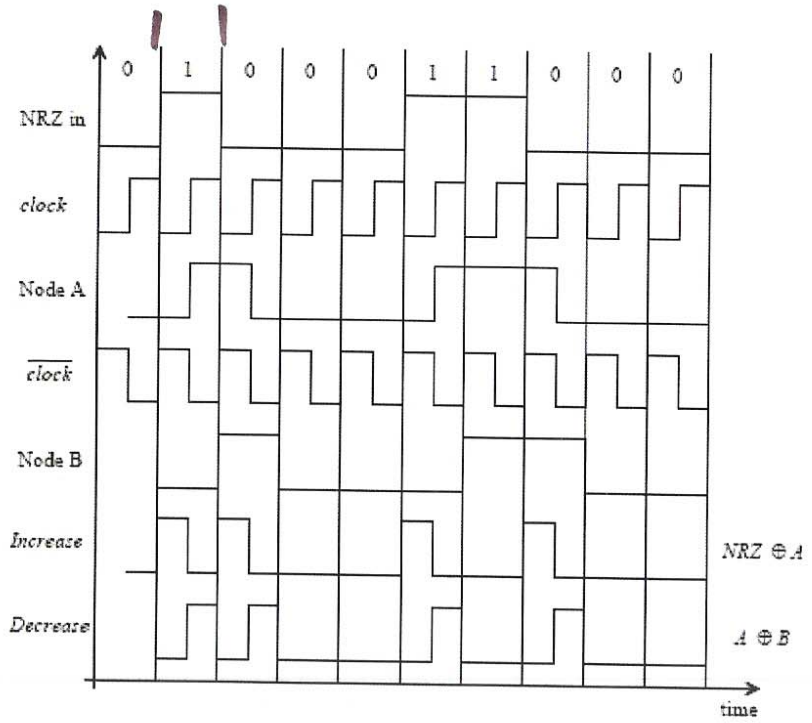
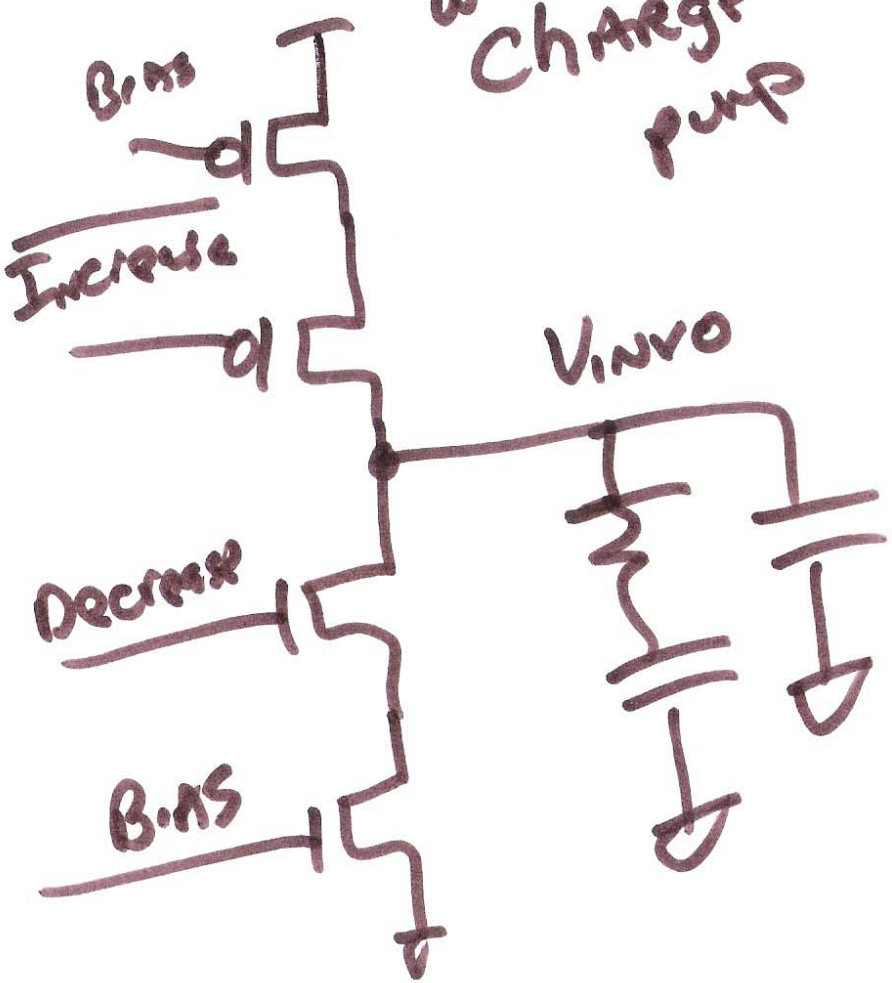
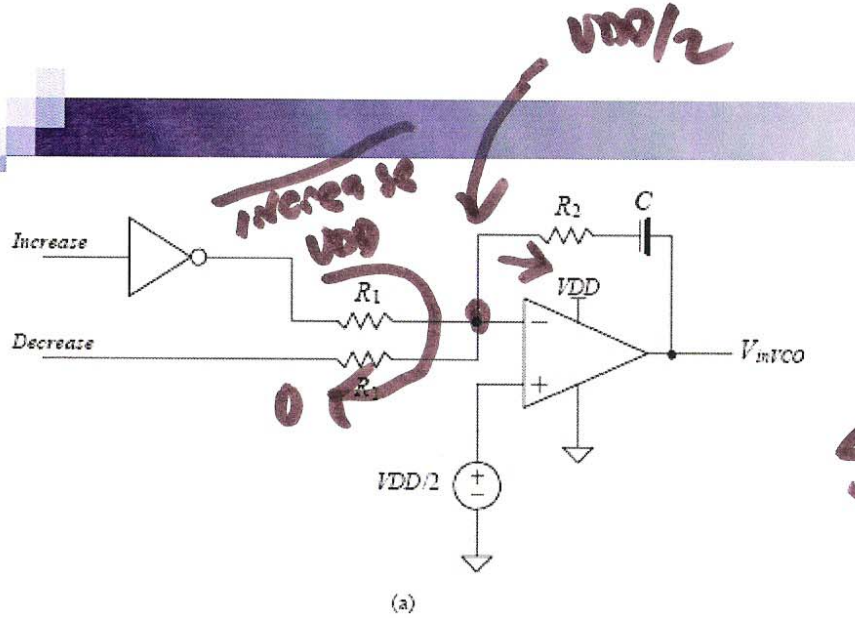


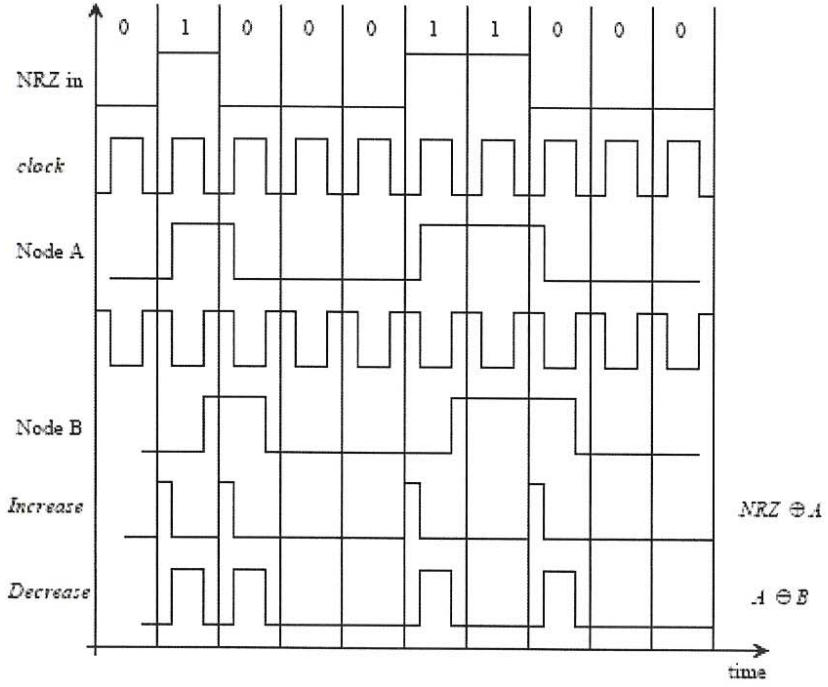
Figure 19.49 The PD (Hogge) portion of a self-correcting, clock-recovery circuit in lock.



4)



(a)



(b)

Figure 19.50 (a) Possible loop filter used in a self-correcting (Hogge) DPLL and (b) waveforms when the loop is not in lock and the clock leads the center of the data.

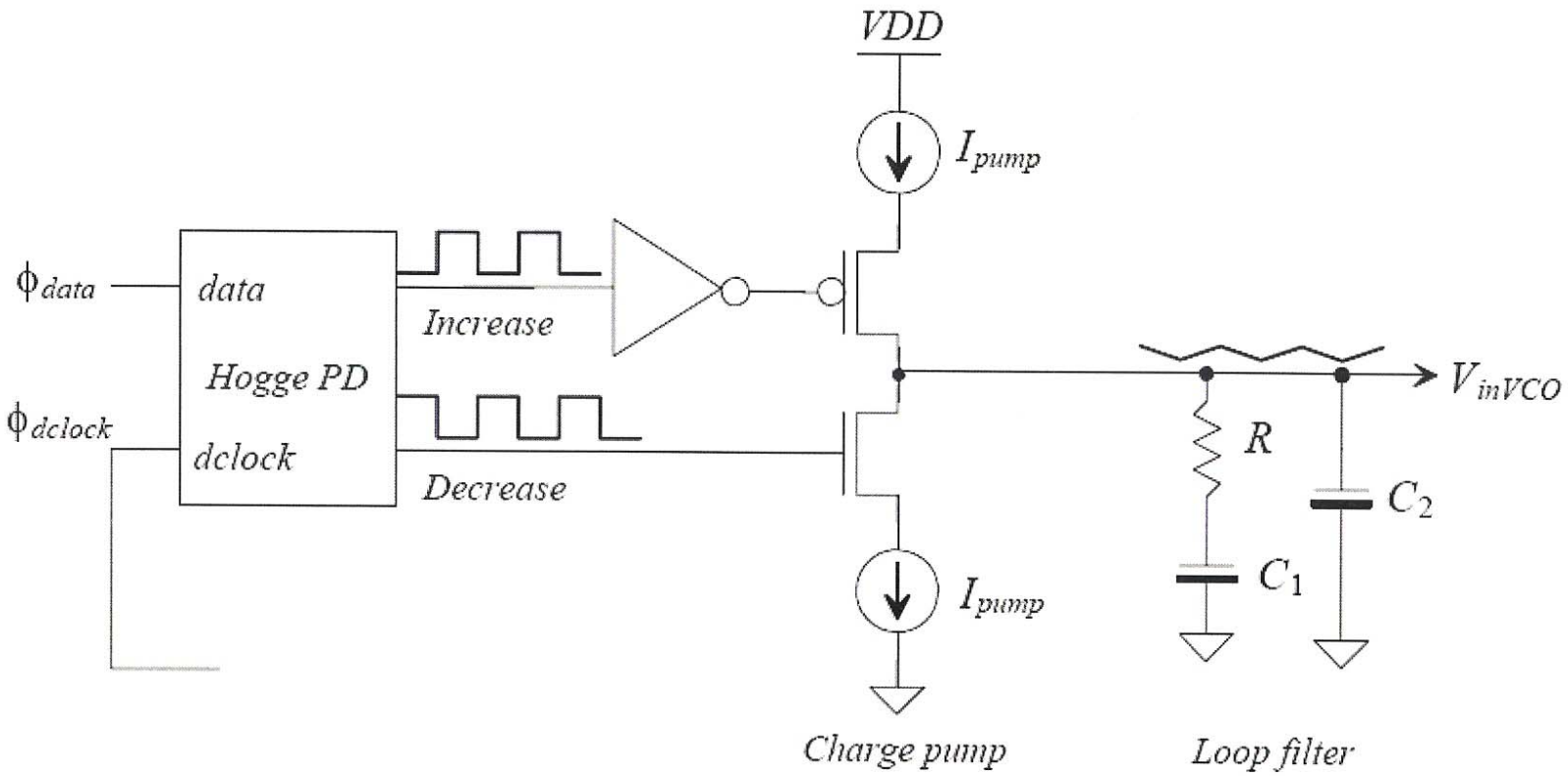


Figure 19.52 Self-correcting PD with charge pump output.

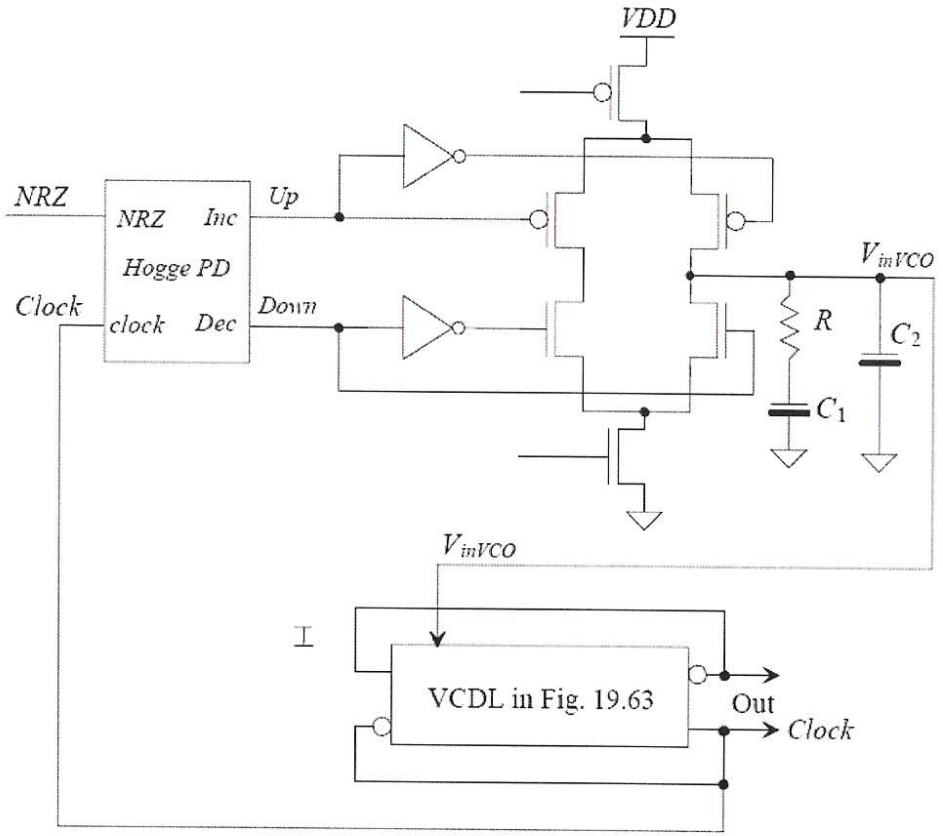
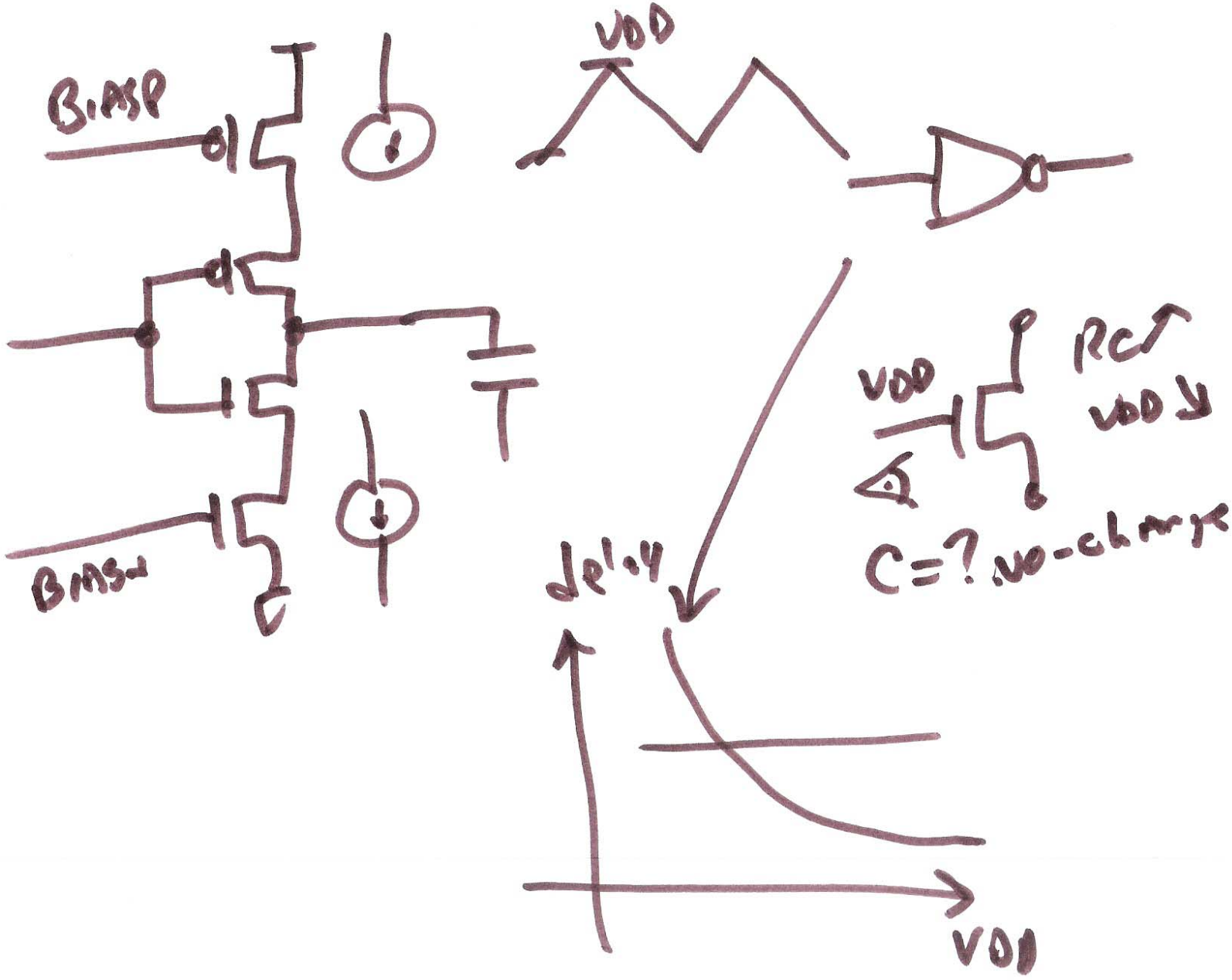


Figure 19.73 Block diagram of the DPLL used for clock-recovery discussed in this section.

H.W. due Monday

1) Redesign the PLL used in 19.5 so that ξ = 2.0 (Fig. 19.33 & eye diagram)

2) Redesign the PLL in Ex. 19.23 using an edge detector (Show Fig. 19.27 & eye diagram)



8)

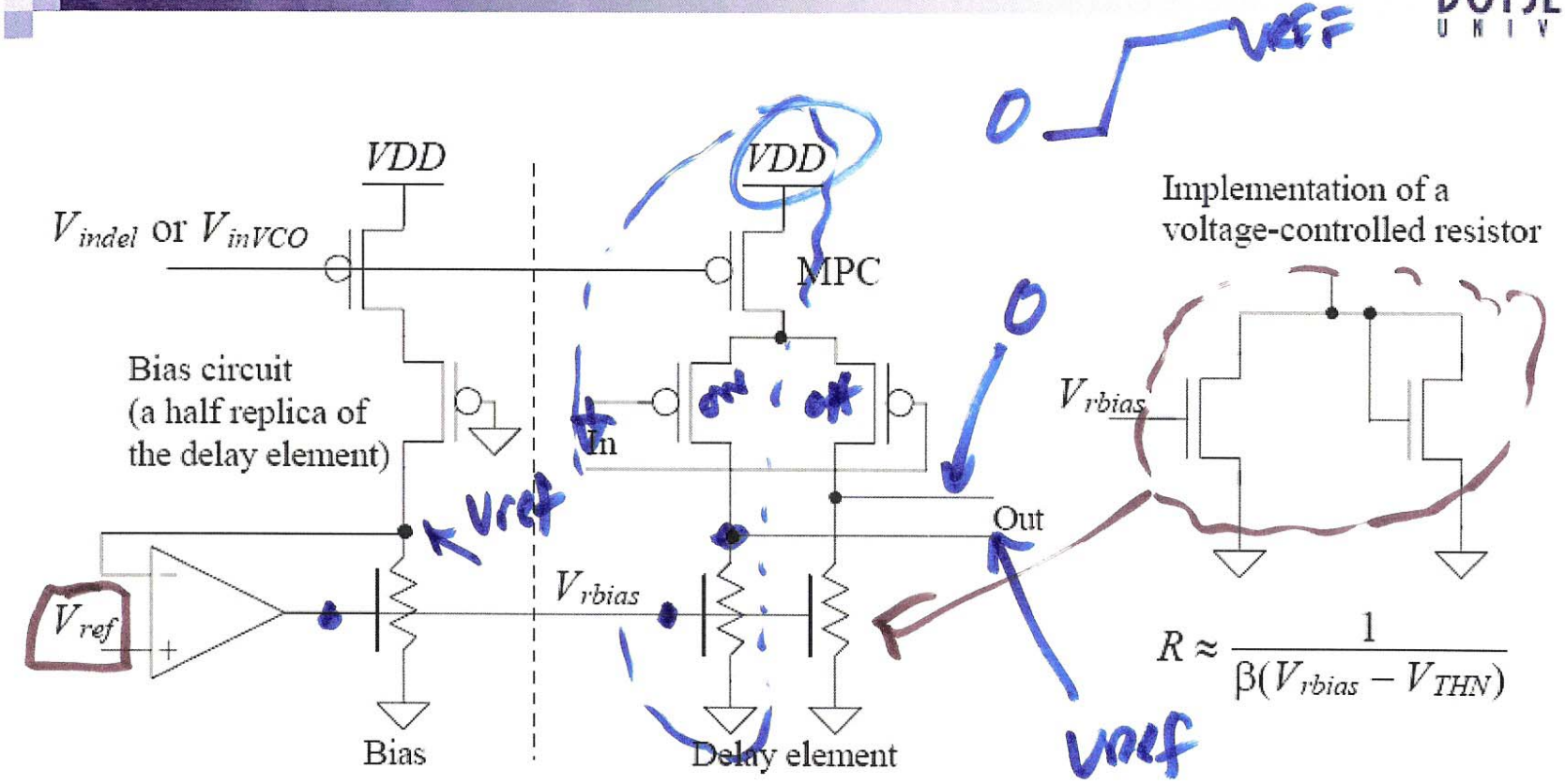


Figure 19.57 A differential delay element based on a voltage-controlled resistor. The bias circuit adjusts the value of the resistors used in the delay elements to sink the current sourced by the p-channel MOSFETs.

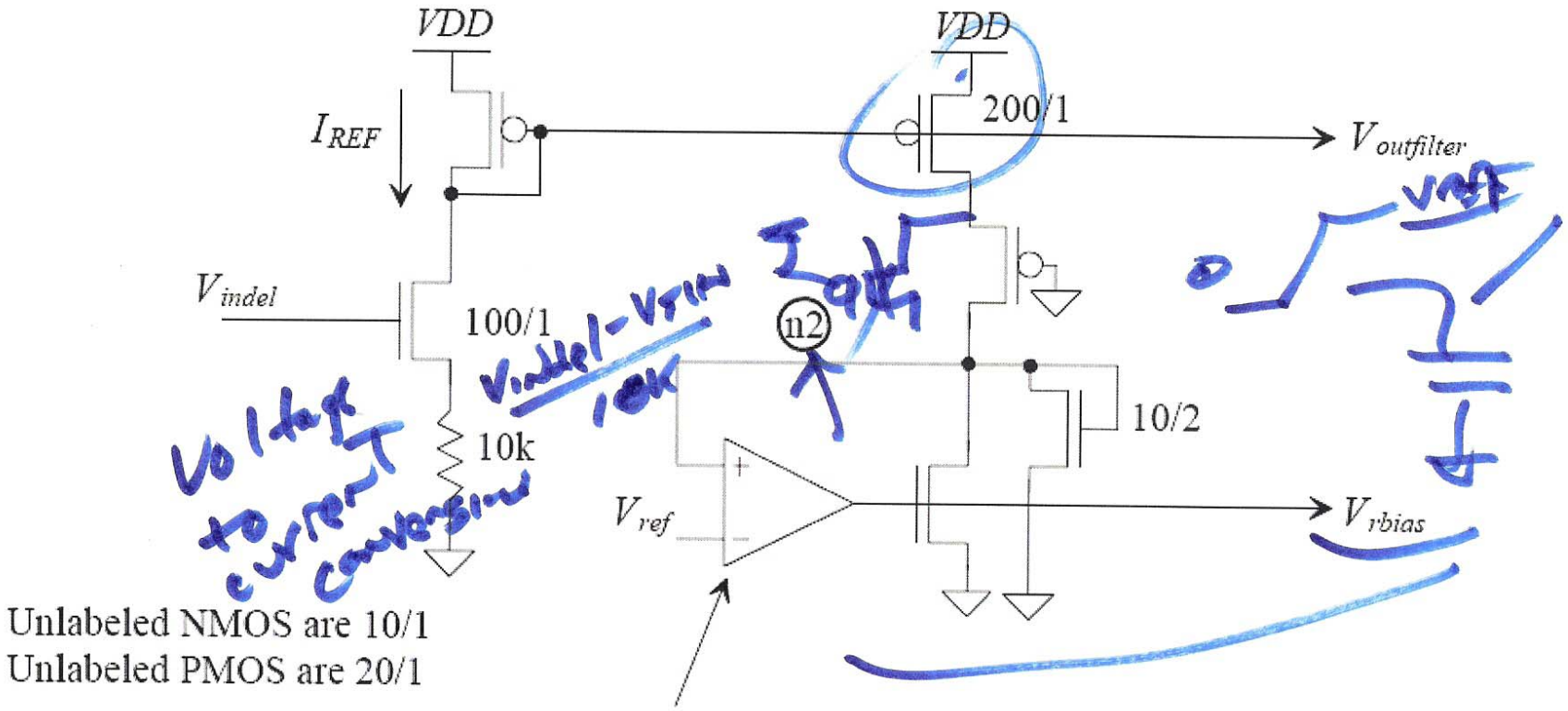


Figure 19.58 Bias circuit for a 500 ps delay line.

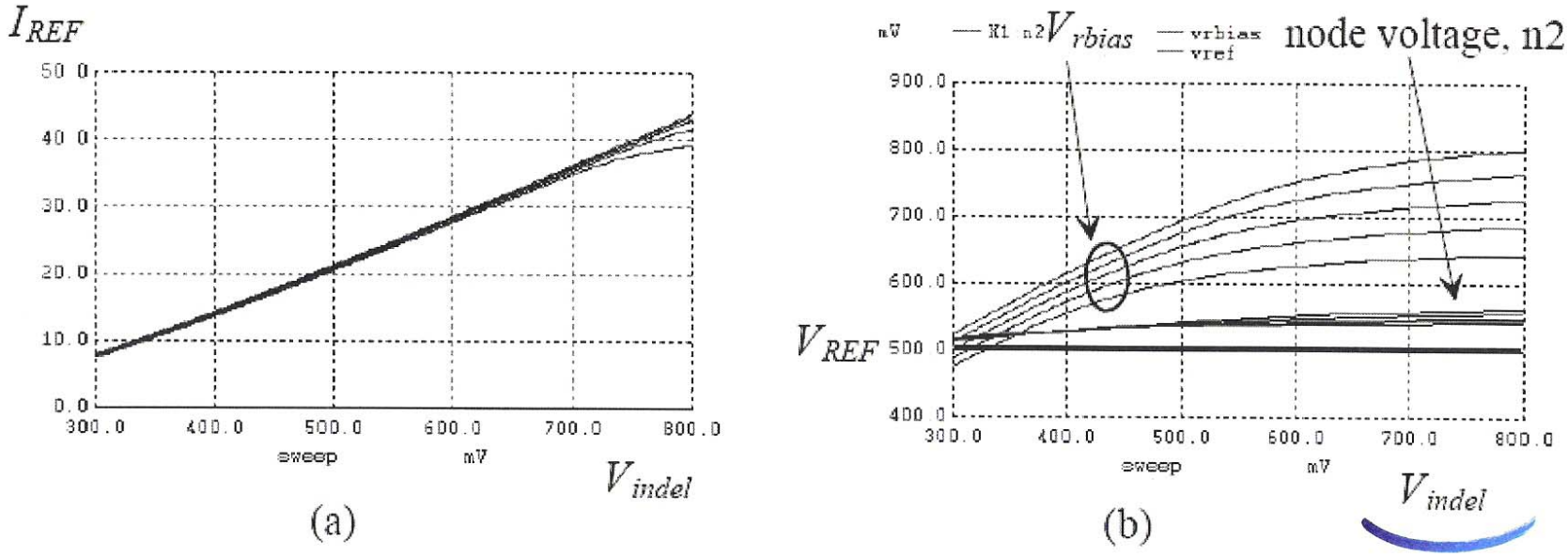


Figure 19.59 The performance of the bias circuit in Fig. 19.58.

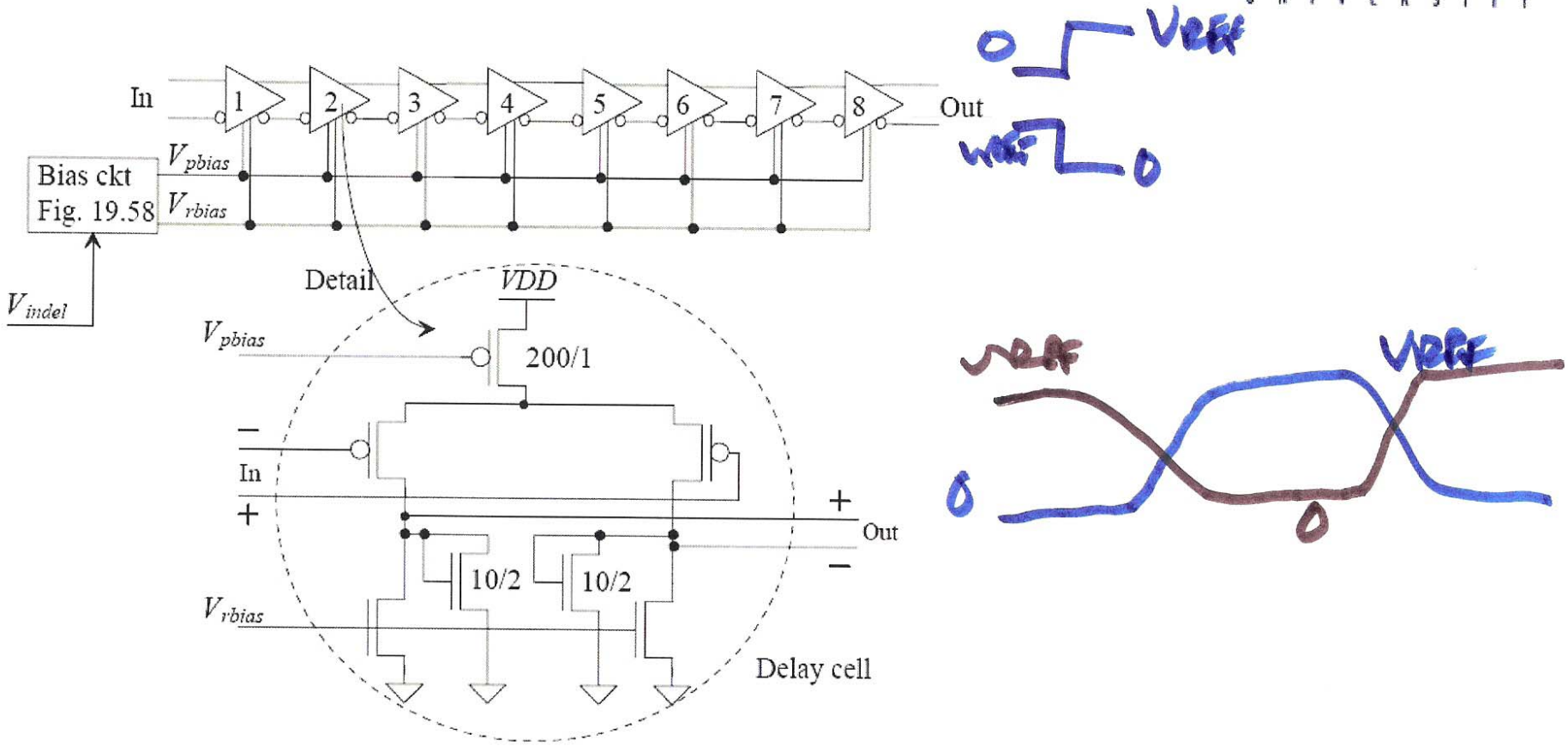
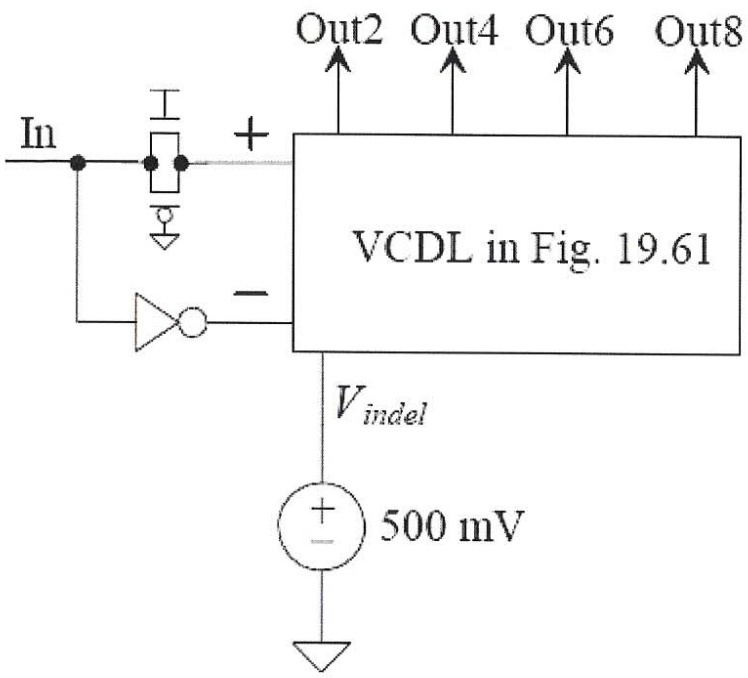


Figure 19.61 An eight-stage VCDL.

12)



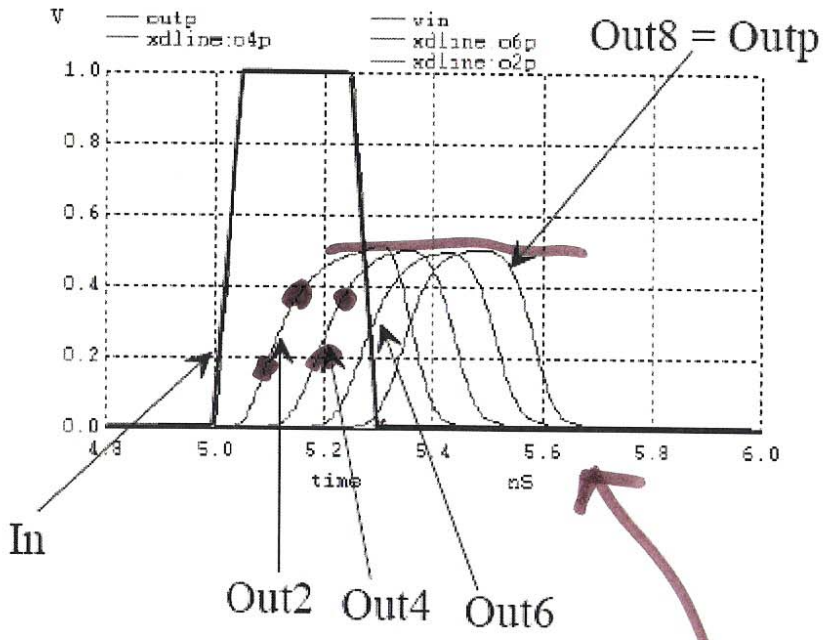


Figure 19.62 Simulating the VCDL in Fig. 19.61.

Hogge PD → gain
Level translating
Delay lines
and DLLs

13)