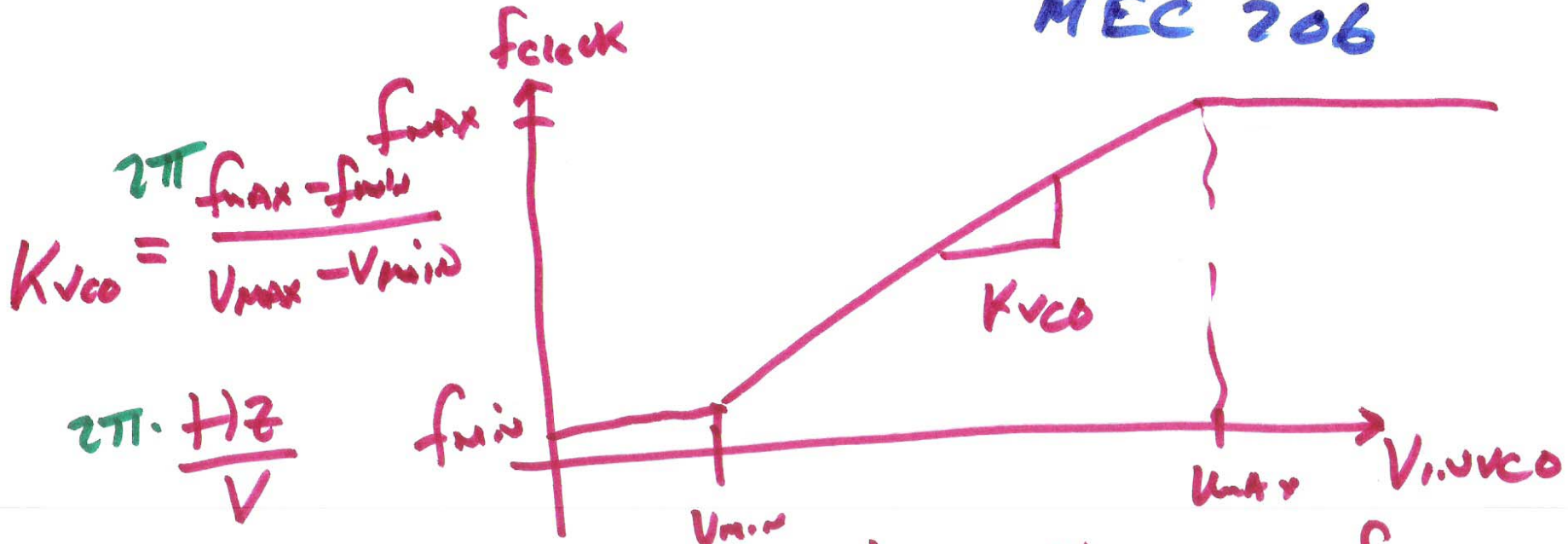
ECE 5/418 Memory circuit design

BOISE STATE UNIVERSITY

Lecture 19 April 13, 2011

Make-up lecture this friday, 5 - 6:15 pm MEC 206



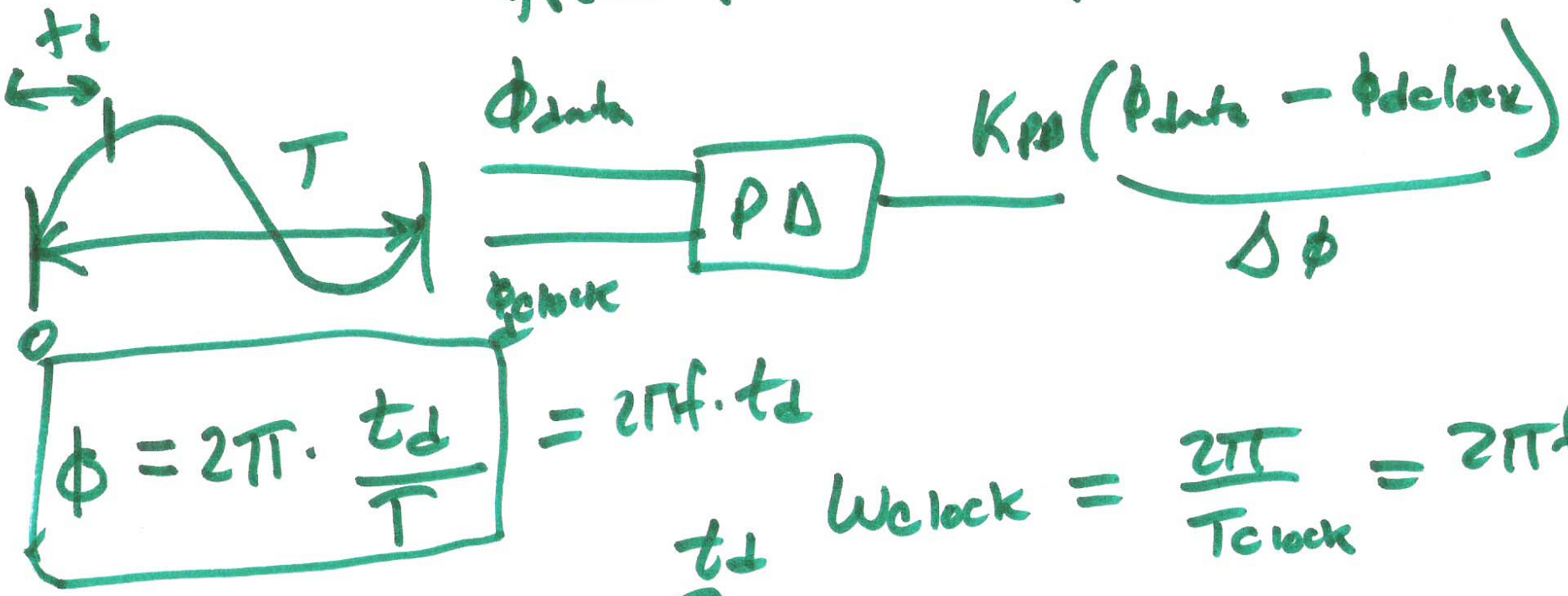
$$K_{VCO} = \frac{2\pi \, f_{MAX} - f_{MIN}}{V_{MAX} - V_{MIN}}$$

$$2\pi \cdot \frac{Hz}{V}$$

$$K_{VCO} \cdot V_{INVCO} = f_{clock}$$

1)

feeding back phase



$$\phi = 2\pi \cdot \frac{t_d}{T} = 2\pi f \cdot t_d$$

$$\omega_{clock} = \frac{2\pi}{T_{clock}} = 2\pi f_{clock}$$

$$\phi_{clock} = \int_0^{t_d} \omega_{clock} \cdot dt = \frac{2\pi}{T_{clock}} \cdot t_d$$

$\int \cdot dt \rightarrow \frac{1}{s}$

2) time domain freq.

$$= \frac{1}{s} \cdot \frac{K_{VCO} \cdot V_{in\,VCO}}{\omega_{clock}}$$

$$\int dt \rightarrow \frac{1}{s}$$

$$\int \cos \omega t \, dt = \sin \omega t$$

let $x = \omega t$

$$\frac{dx}{dt} = \omega$$

$$dt = \frac{dx}{\omega}$$

$$\int \cos x \cdot \frac{dx}{\omega} = \frac{\sin \omega t}{\omega}$$

3)

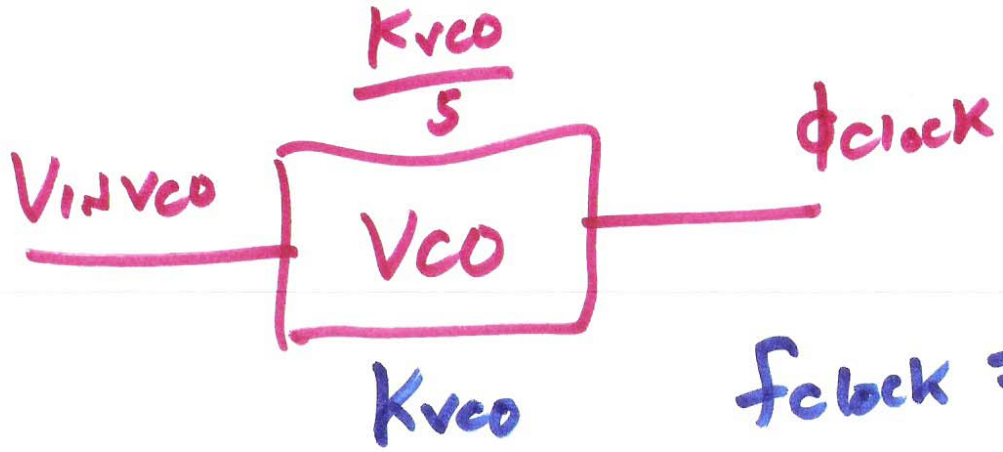
$$\int \underbrace{\cos \omega t}_{f(t)} \overset{H}{=} \frac{e^{j\omega T} + e^{-j\omega T}}{2} \cdot \frac{1}{j\omega}$$

$$= \frac{1}{s} \cdot f(\omega)$$

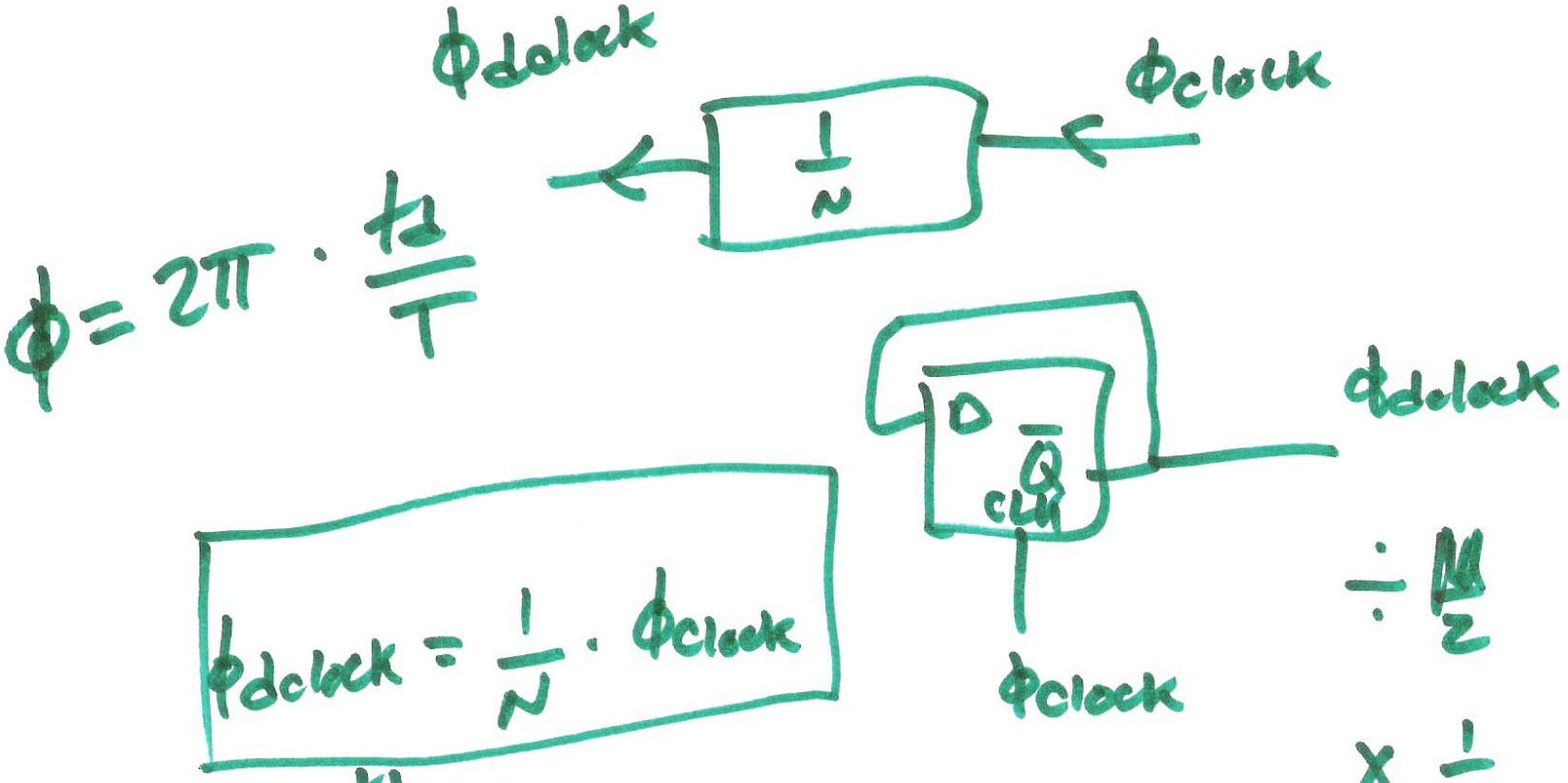
$$s = \cancel{\sigma}^{0} + j\omega$$

for Sinusoidal Analysis

$$\frac{\sin \omega T}{\omega}$$



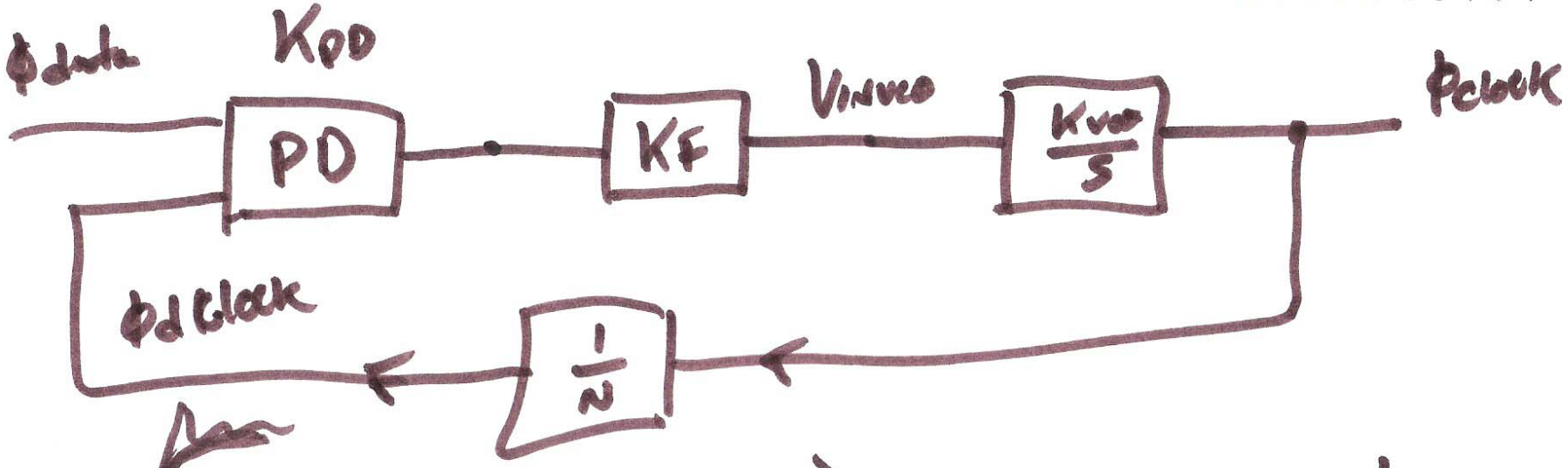
$$f_{clock} = K_{VCO} \cdot V_{inVCO}$$



$$2\pi \cdot \frac{t_d}{2T} = \frac{\phi}{2}$$

5)

PLL Block diagram



$$K_{PD}\left(\phi_{data} - \frac{\phi_{clock}}{N}\right) \cdot K_F \cdot \frac{K_{VCO}}{S} = \phi_{clock}$$

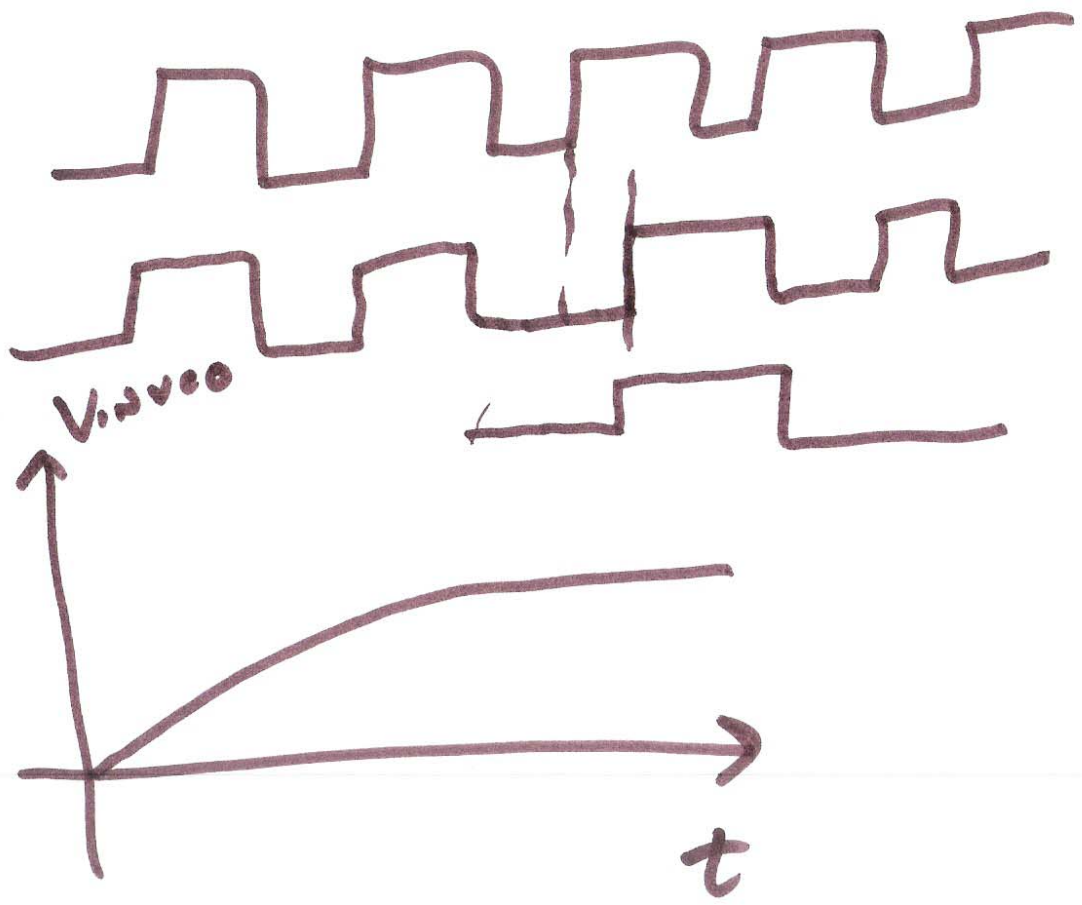
$$\frac{V_{step}}{S}\,\phi_{data} \cdot K_{PD} \cdot K_F \cdot \frac{K_{VCO}}{S} = \phi_{clock}\left(1 + \frac{K_{PD}}{N} K_F \frac{K_{VCO}}{S}\right)$$

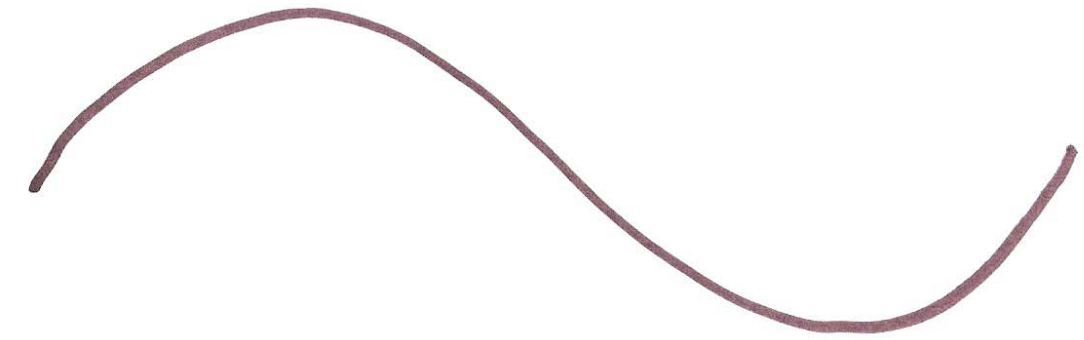
$$\phi = \frac{f}{S}$$

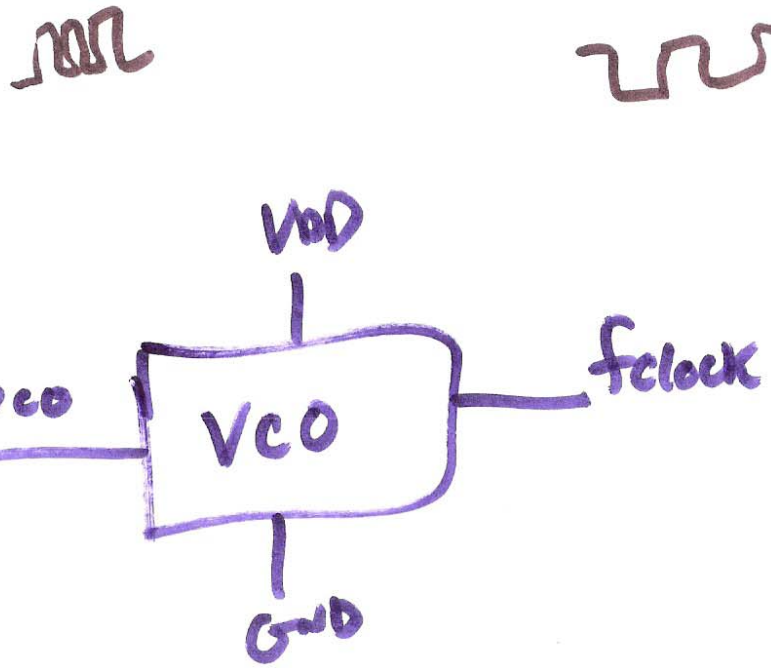
$$\left(\frac{\phi_{data}}{\phi_{clock}}\right)^{-1} = \frac{K_{PD} \cdot K_F \cdot K_{VCO}}{S + \frac{K_{PD}}{N} \cdot K_F \cdot K_{VCO}}$$

6)

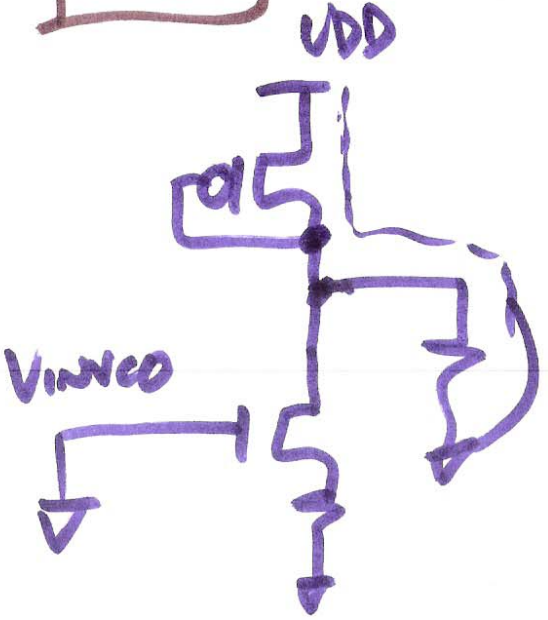
Step in frequency
step in phase
or a step in both



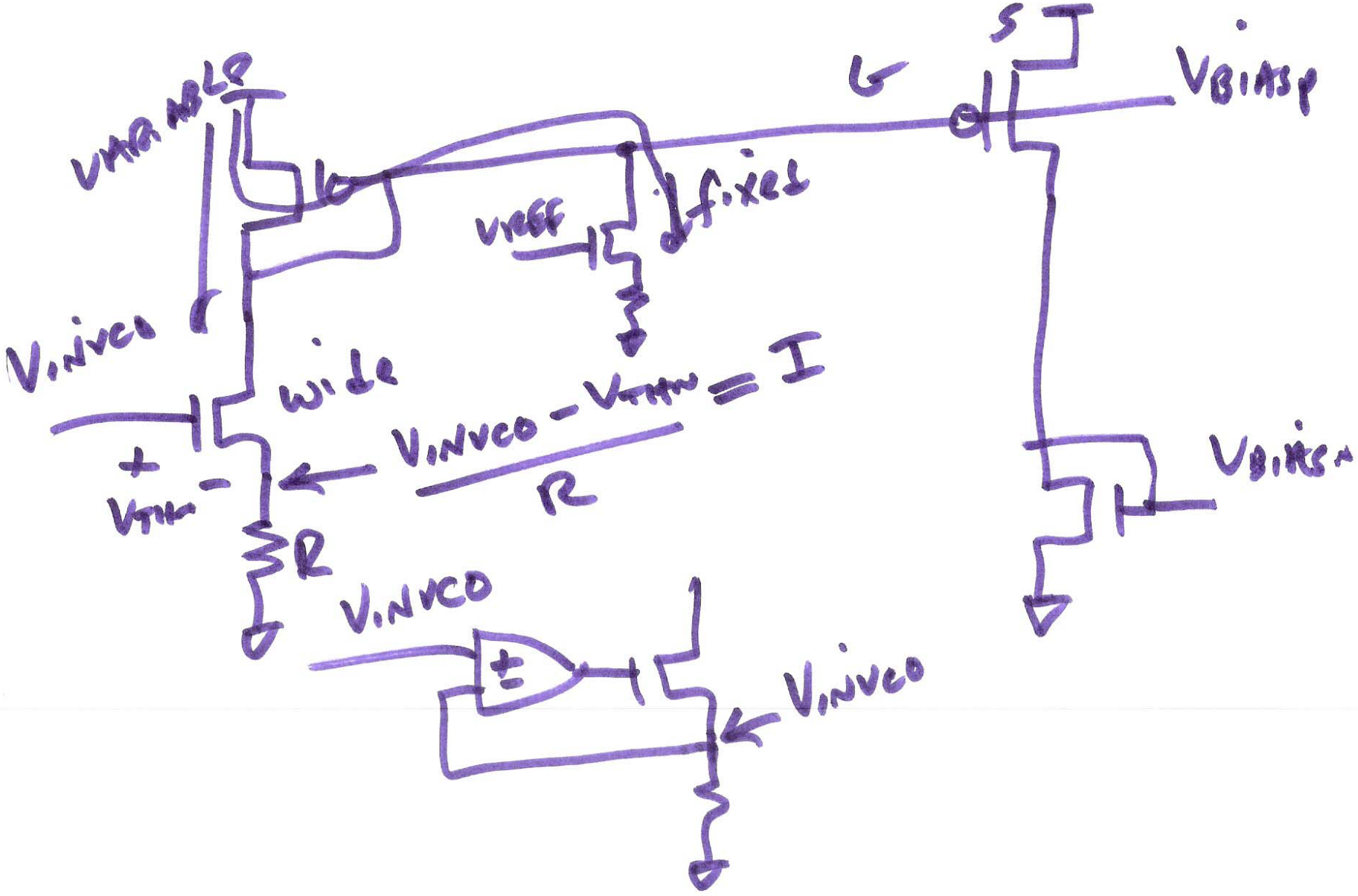


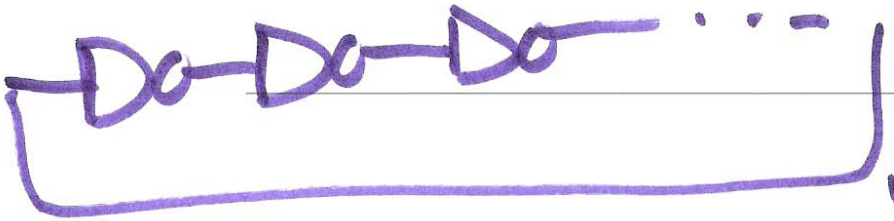

VDD
VINVCO
VCO
fclock
GND

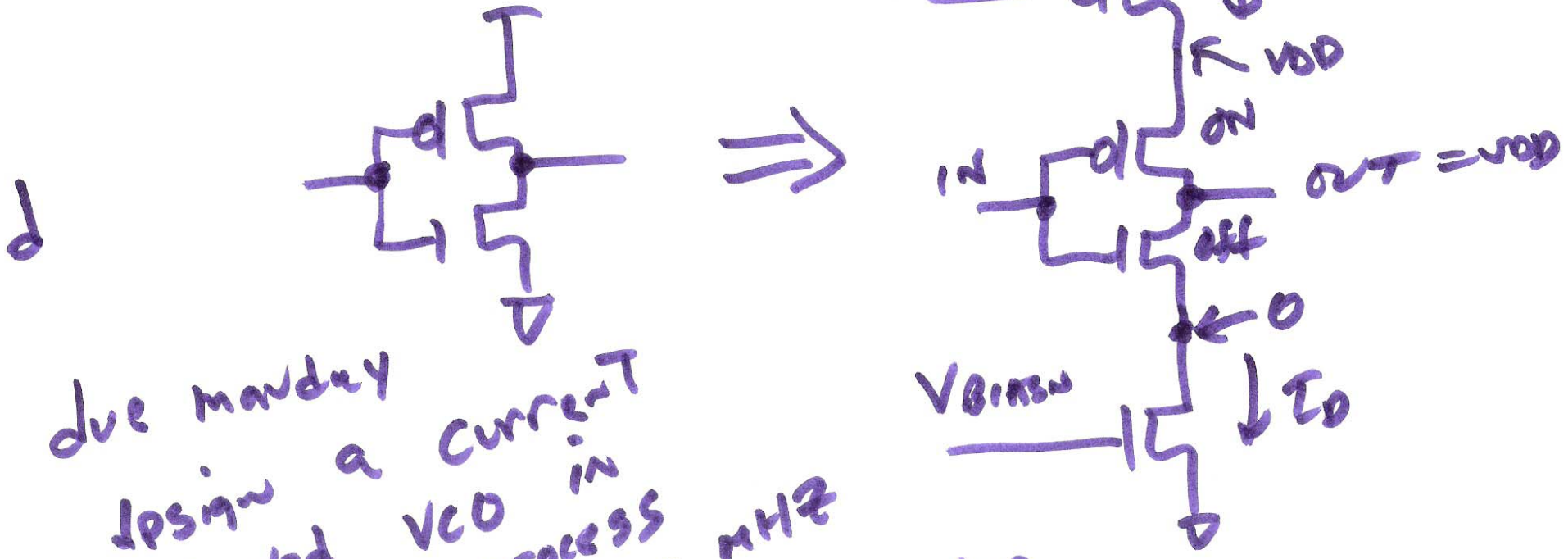

Butt
top


VDD
VINVCO

Linear voltage to current Conversion







d

due monday

Design a current Starved VCO in 180 nm process

100 → 200 MHz

VS. VDD

Temp

Show linear freq vs Vin VCO

10)