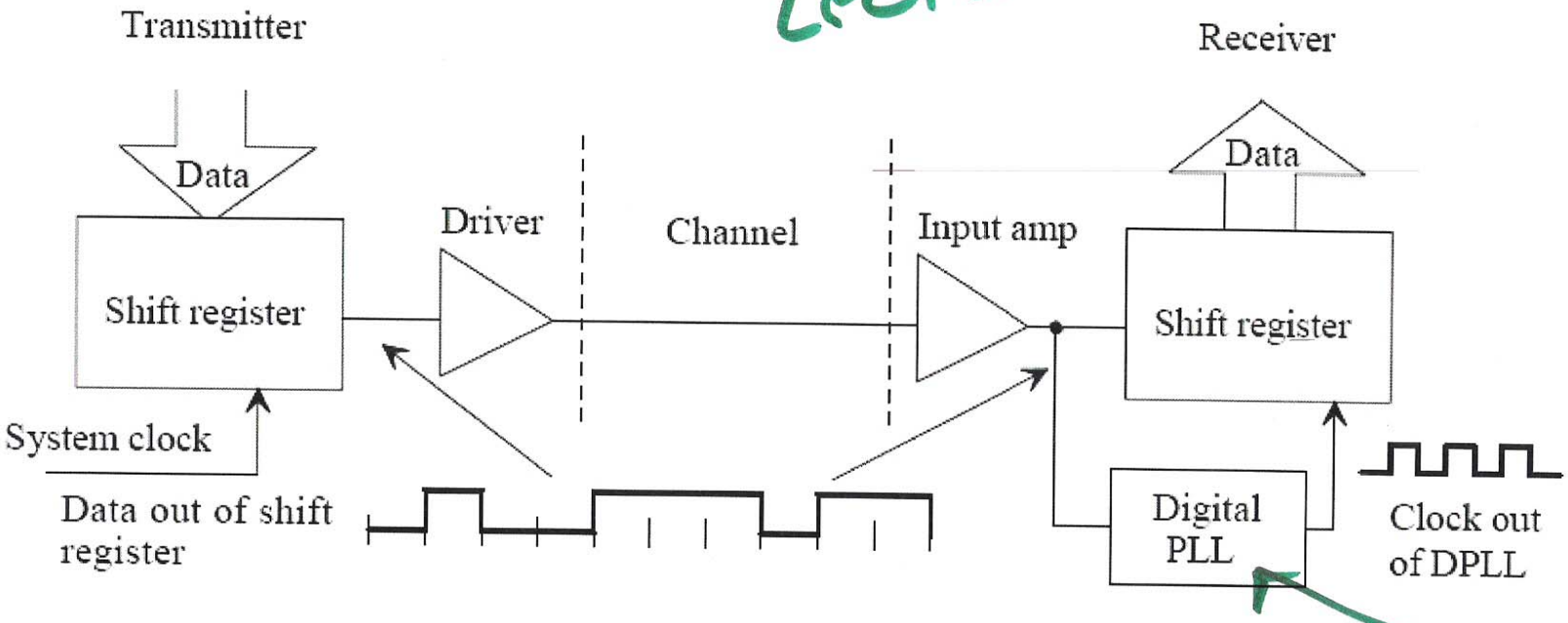


Figure 19.1 Block diagram of a communication system using a DPLL for the generation of a clock signal.

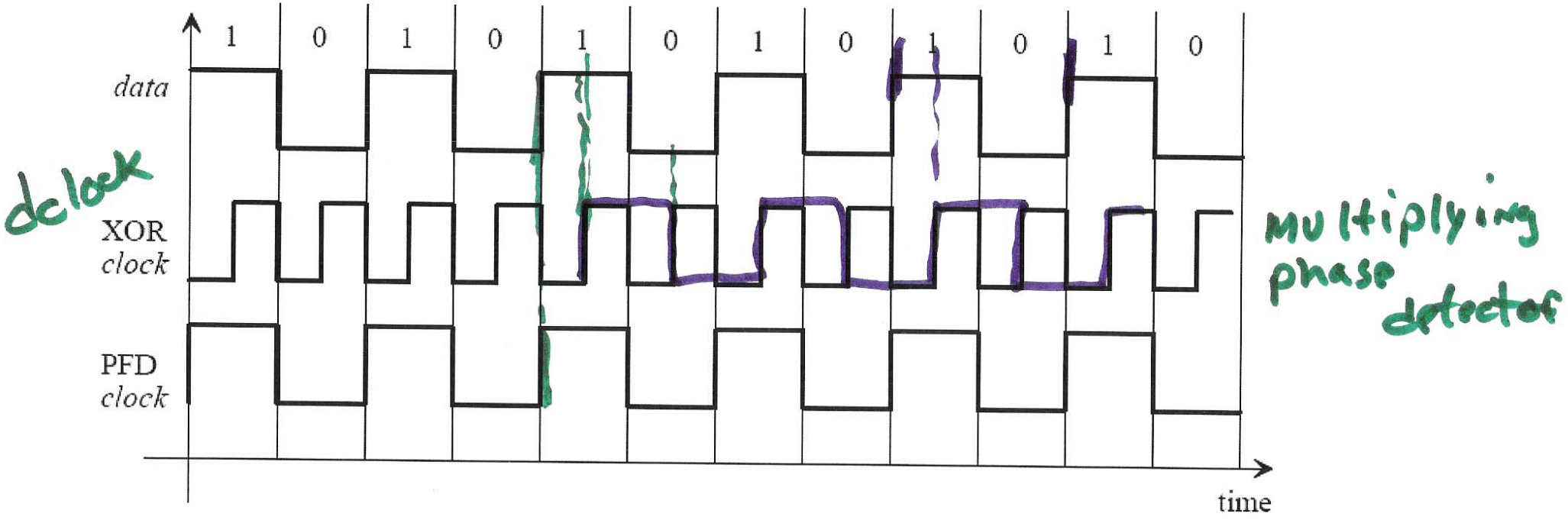
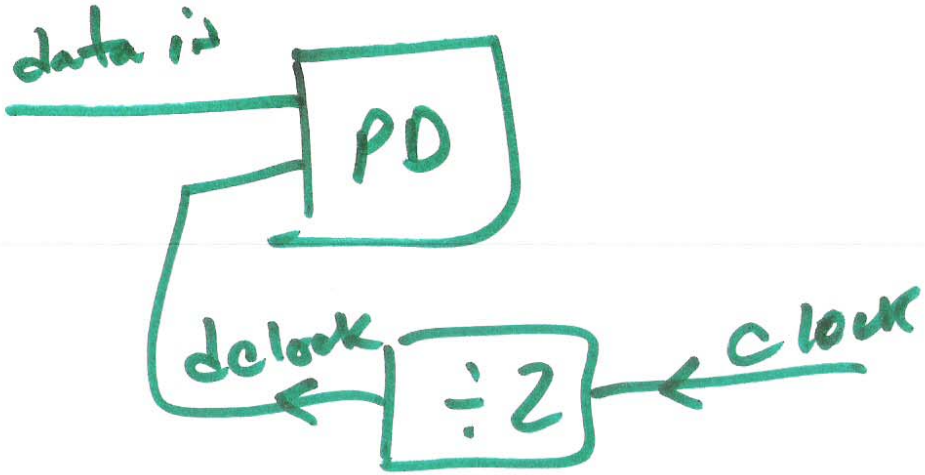


Figure 19.2 Data input to DPLL in lock and possible clock outputs using the XOR phase detector and PFD.



2)

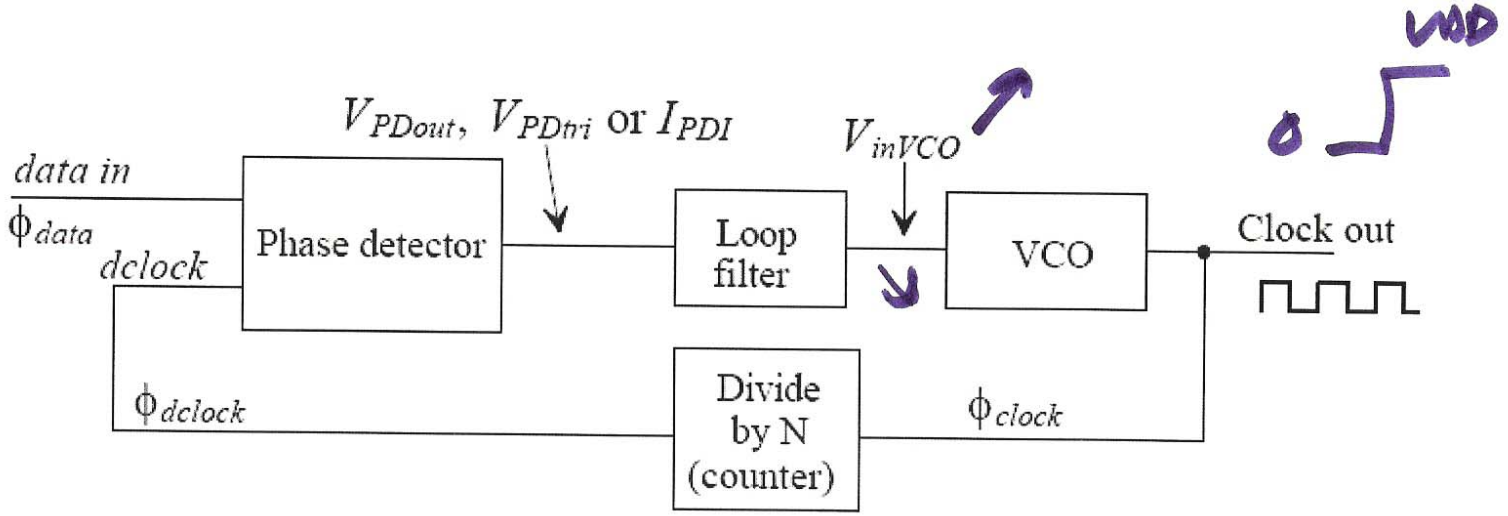
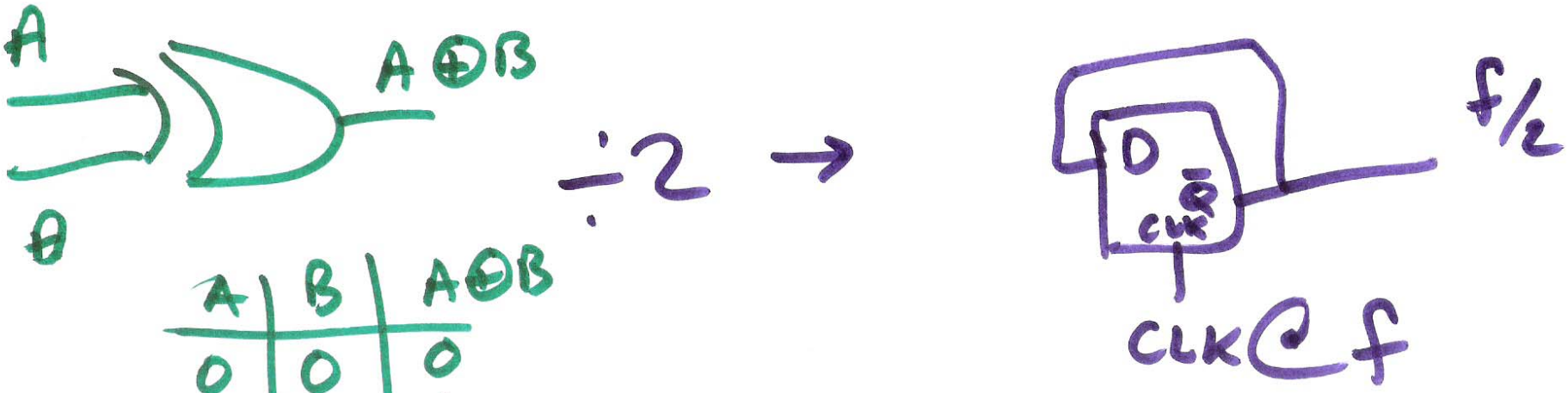
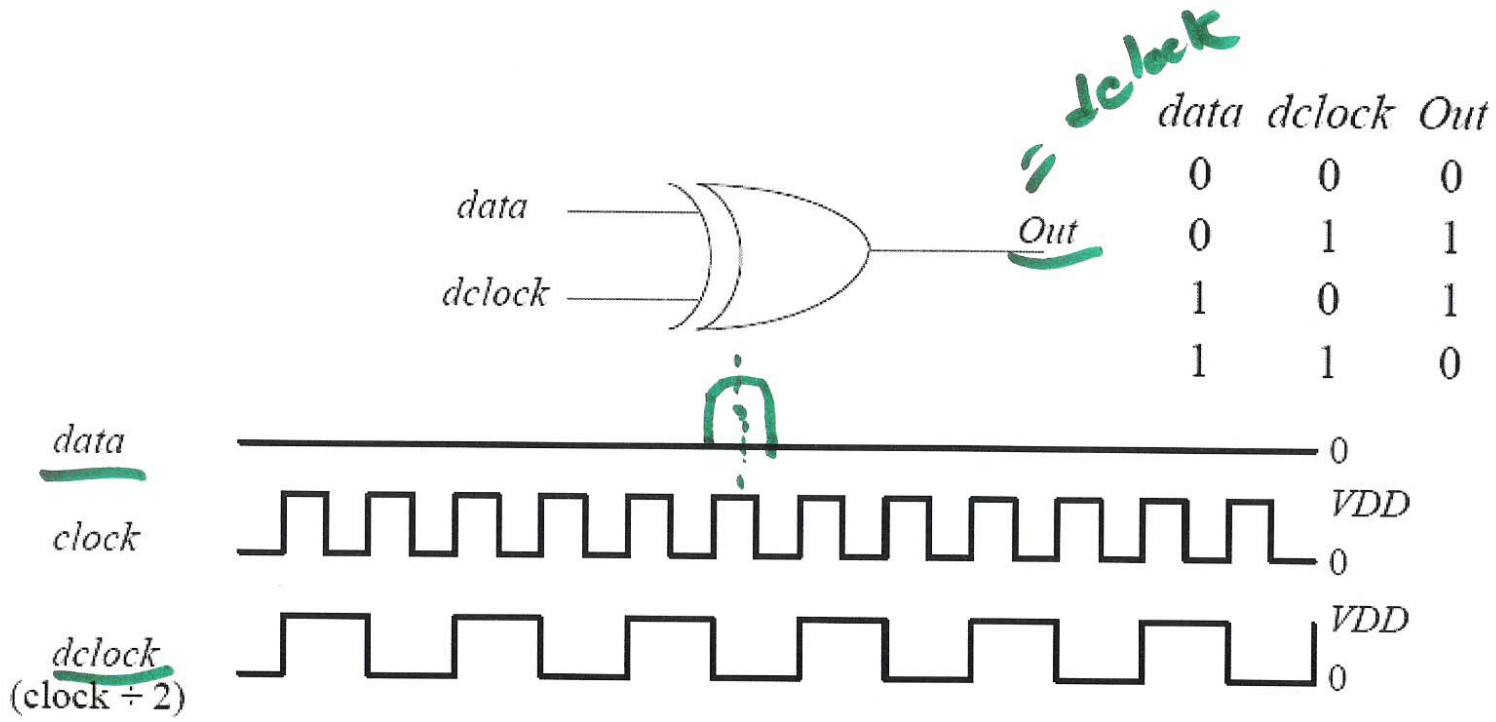


Figure 19.3 Block diagram of a digital phase-locked loop.



A	B	A⊕B
0	0	0
0	1	1
1	0	1
1	1	0

3)



data	dclock	Out
0	0	0
0	1	1
1	0	1
1	1	0

Figure 19.4 Operation of the XOR phase detector.

1) we need a minimum # of transitions for the loop to stay locked

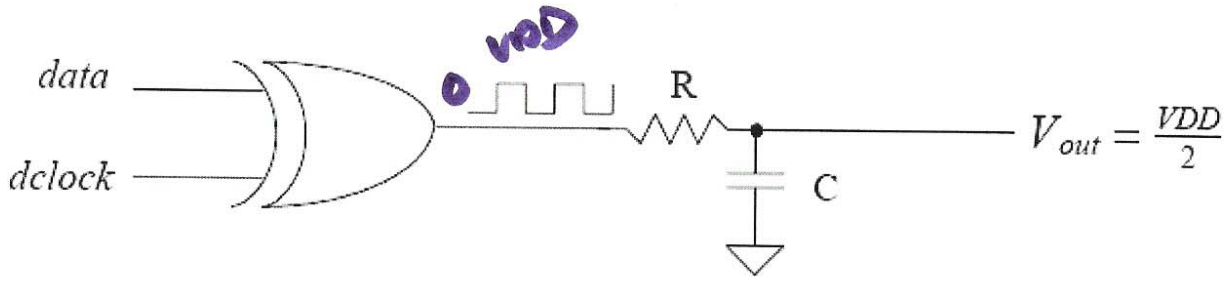
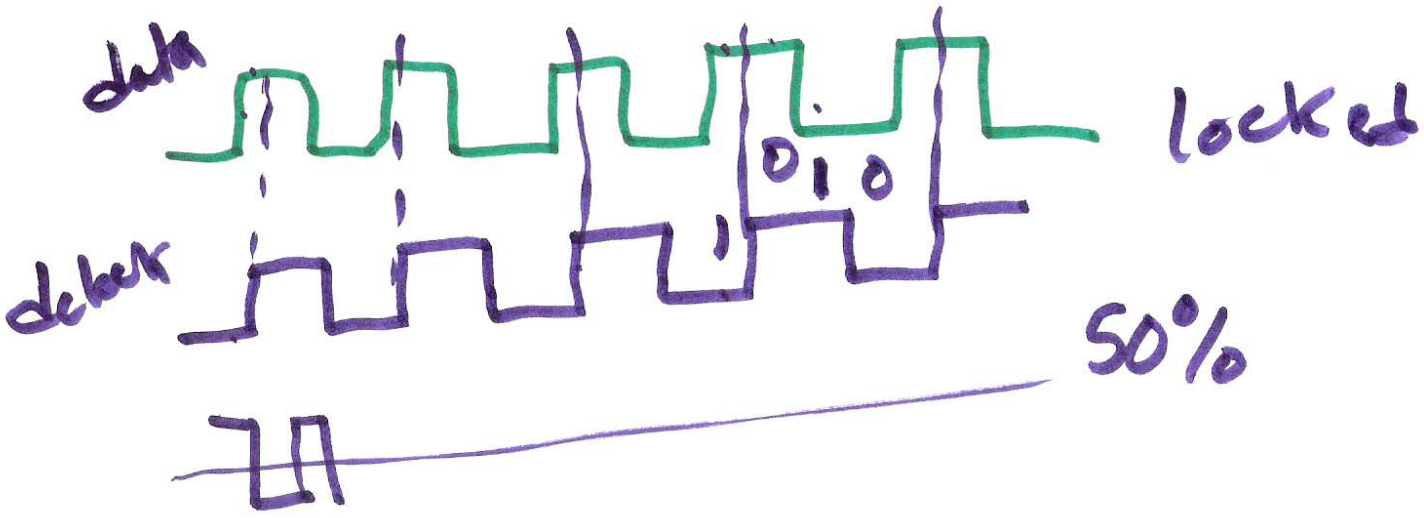
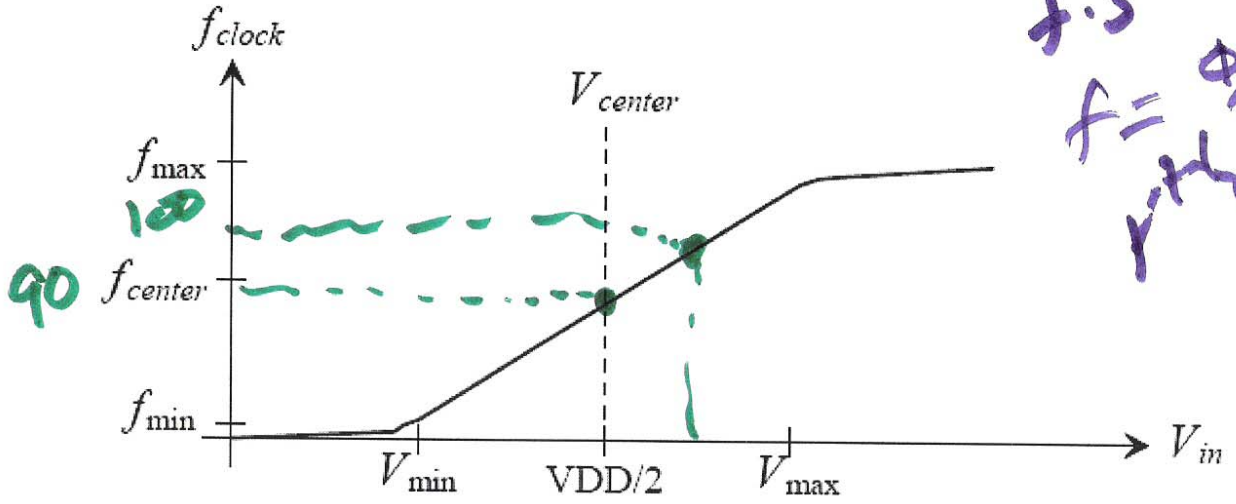


Figure 19.5 How the filtered output of the phase detector becomes VDD/2.



5)



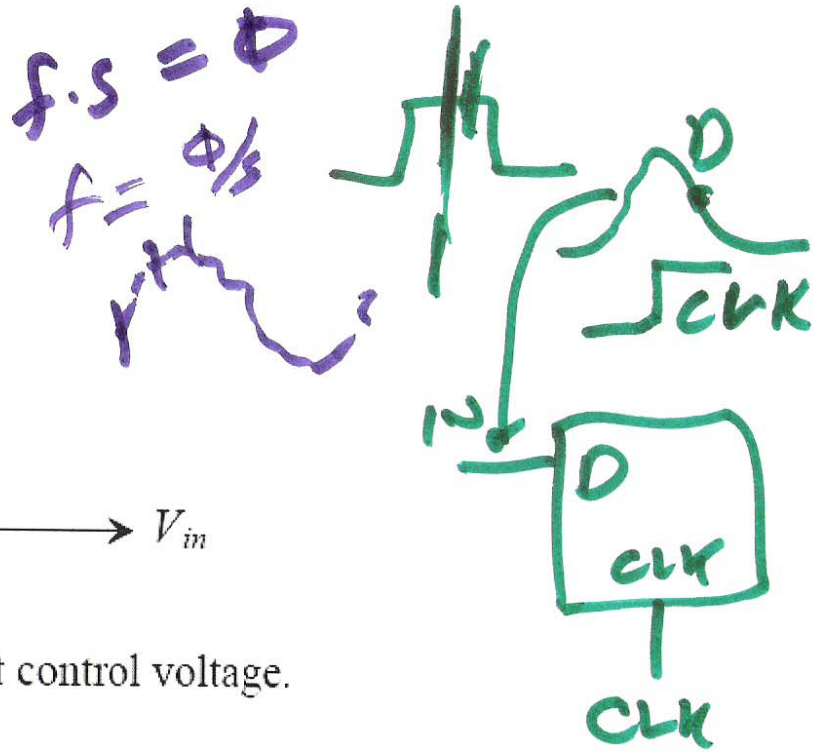
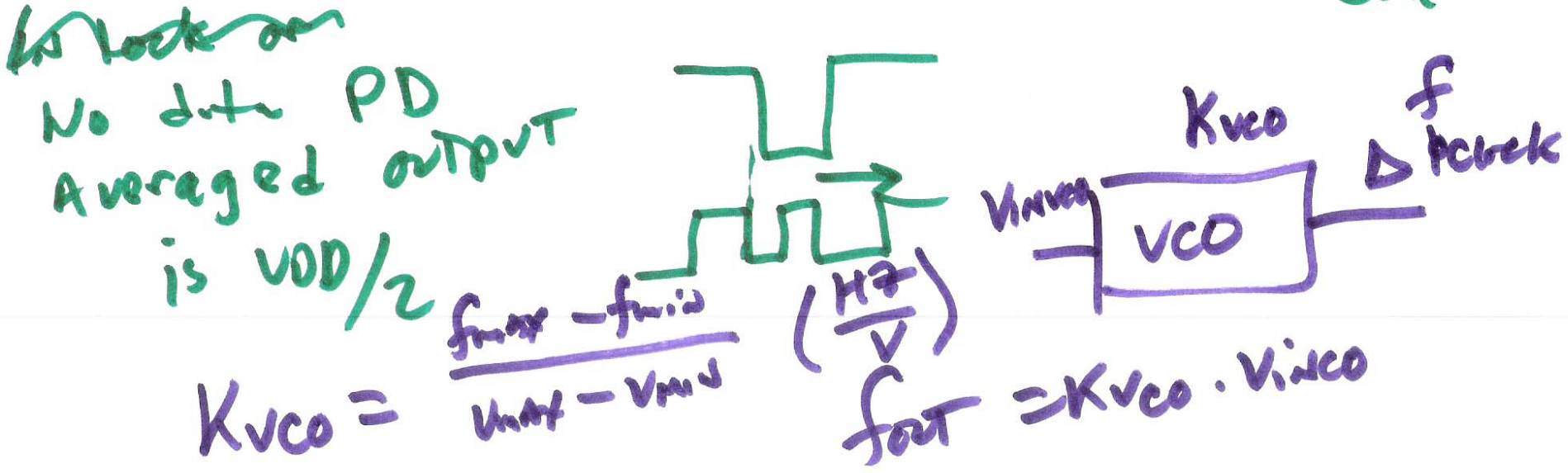


Figure 19.6 Output frequency of VCO versus input control voltage.



6)

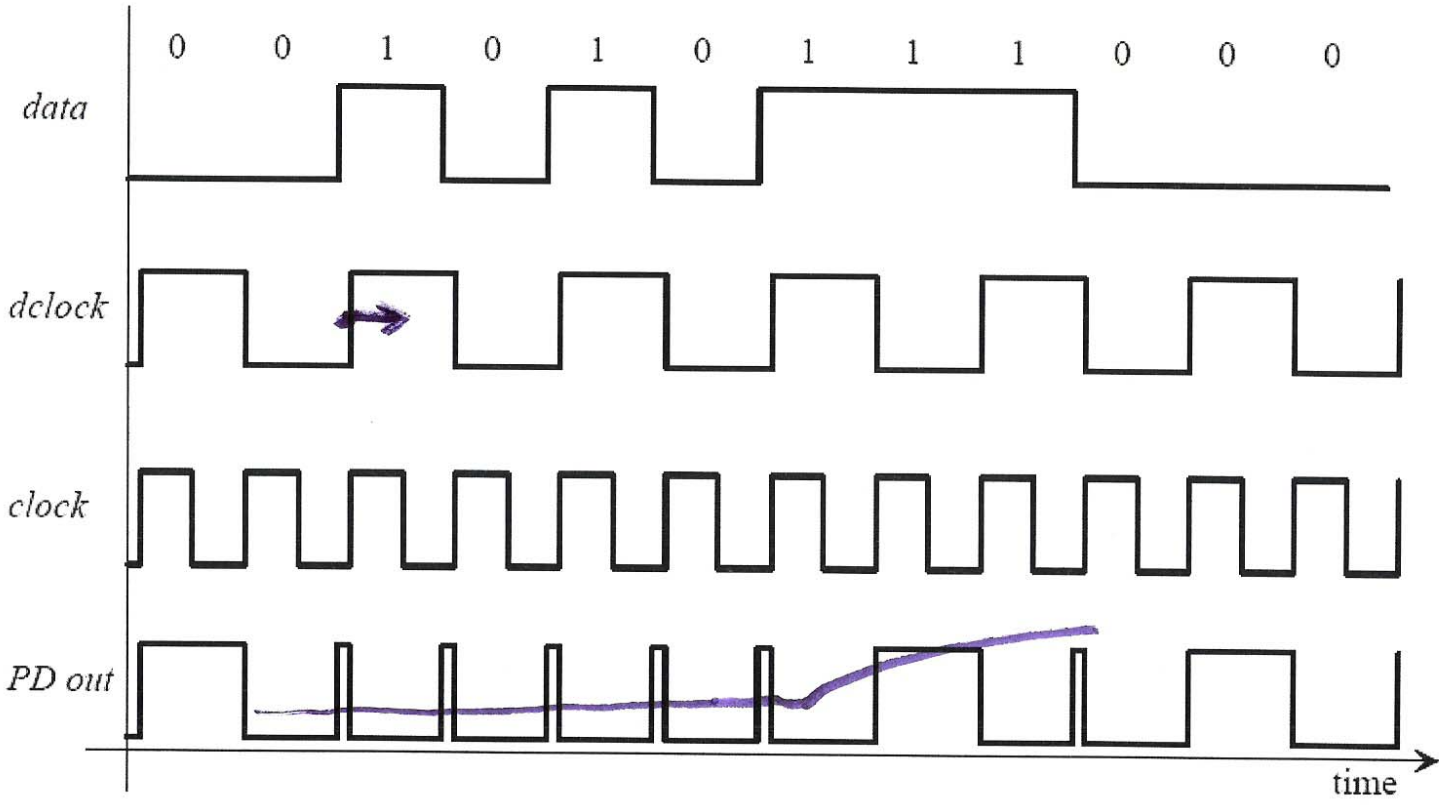


Figure 19.7 Possible XOR phase-detector inputs and the resulting output.

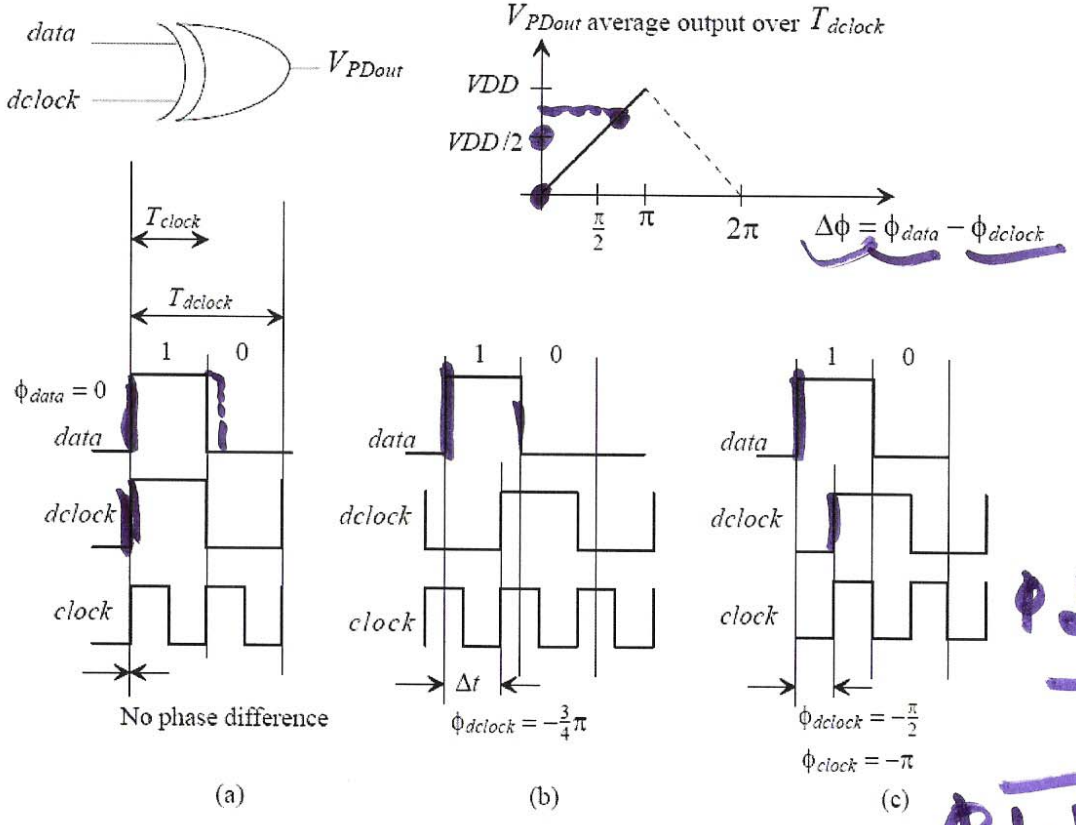
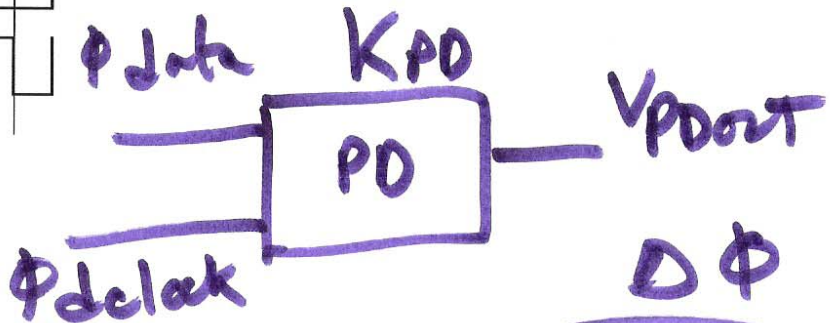


Figure 19.8 XOR PD output for various inputs (assuming input data are a string of alternating ones and zeros).

WANT 50% duty signals

XOR → PD
→ XOSC

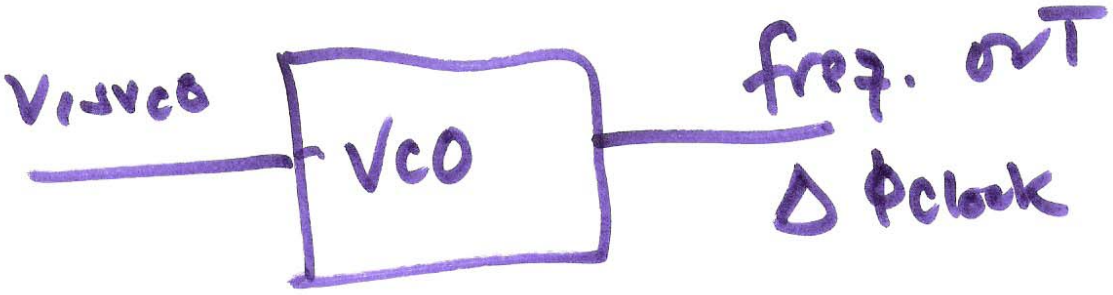


$\Delta\phi$

$$K_{PD} = \frac{V_{PDOUT}}{\phi_{data} - \phi_{dclock}} = \frac{VDD}{\pi} \frac{V}{RAD}$$

$$V_{PDOUT} = K_{PD} \cdot (\phi_{data} - \phi_{dclock}) = K_{PD} \cdot \Delta\phi$$

8)


V_tune
VCO
freq. out
Δ φclock


V_tune
Σ jitter

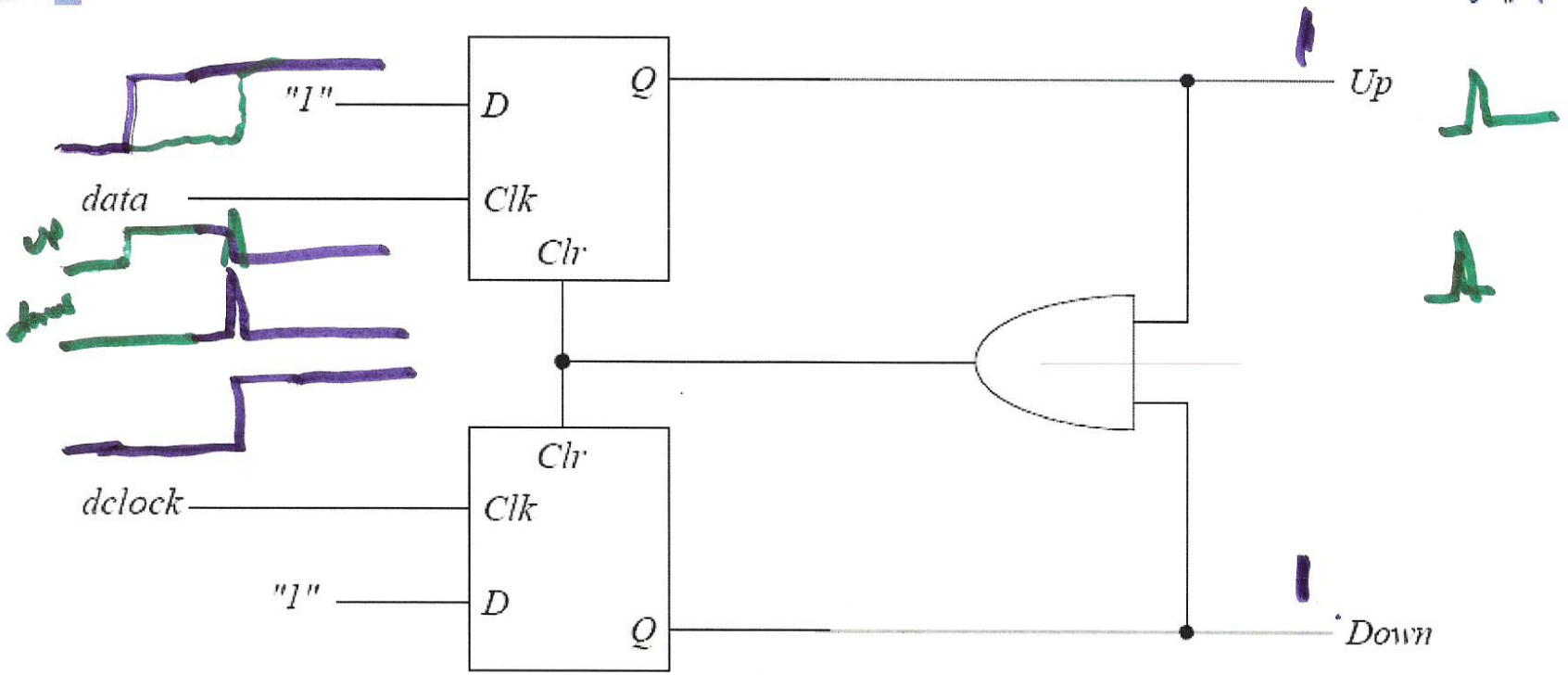
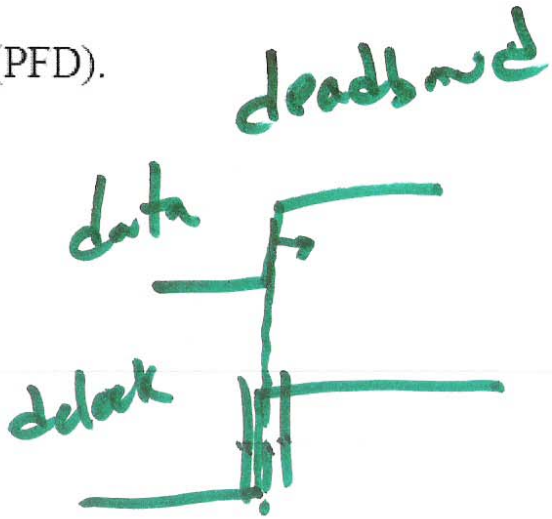


Figure 19.10 Phase frequency detector (PFD).



tri-State

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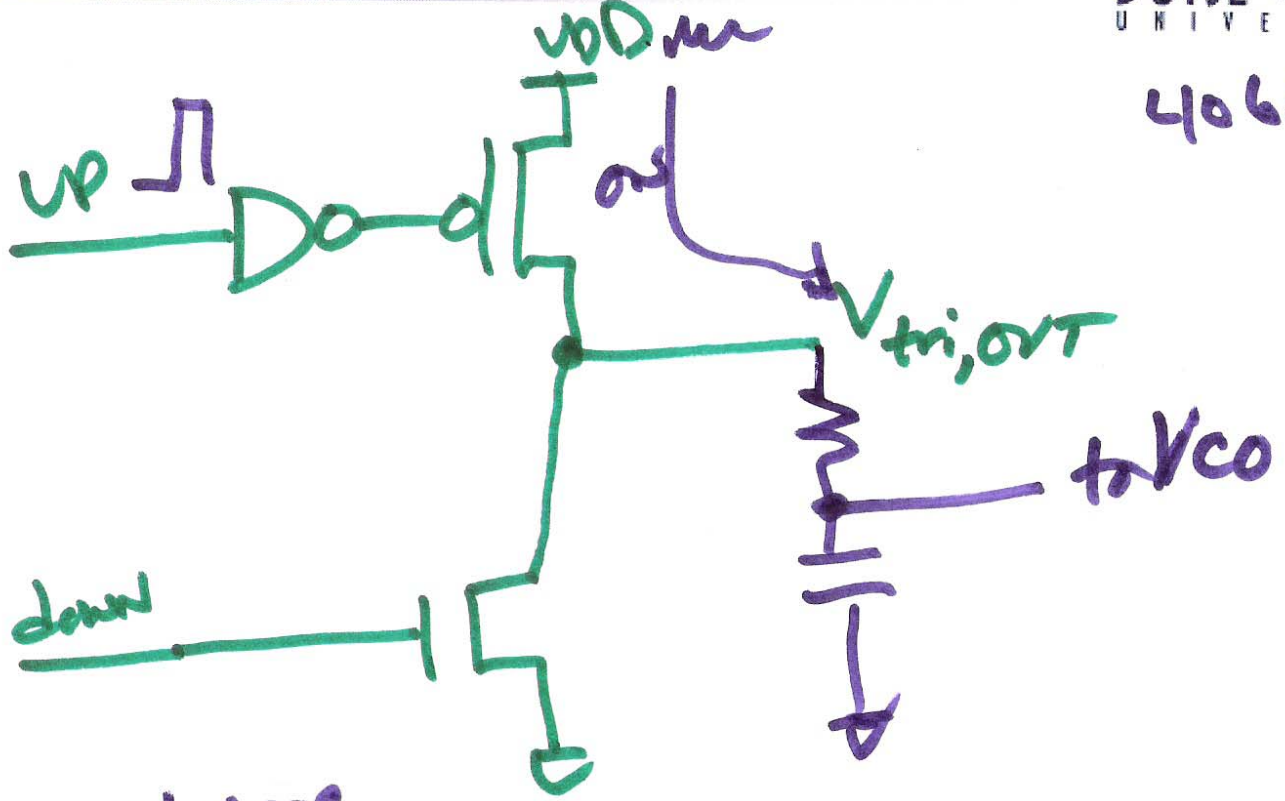
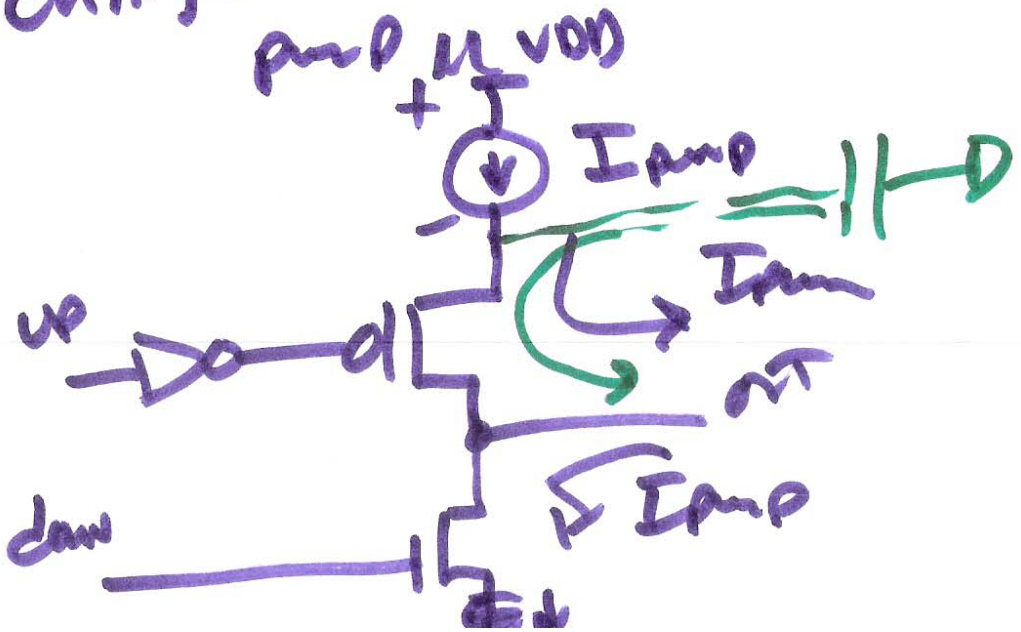


charge pump



12)

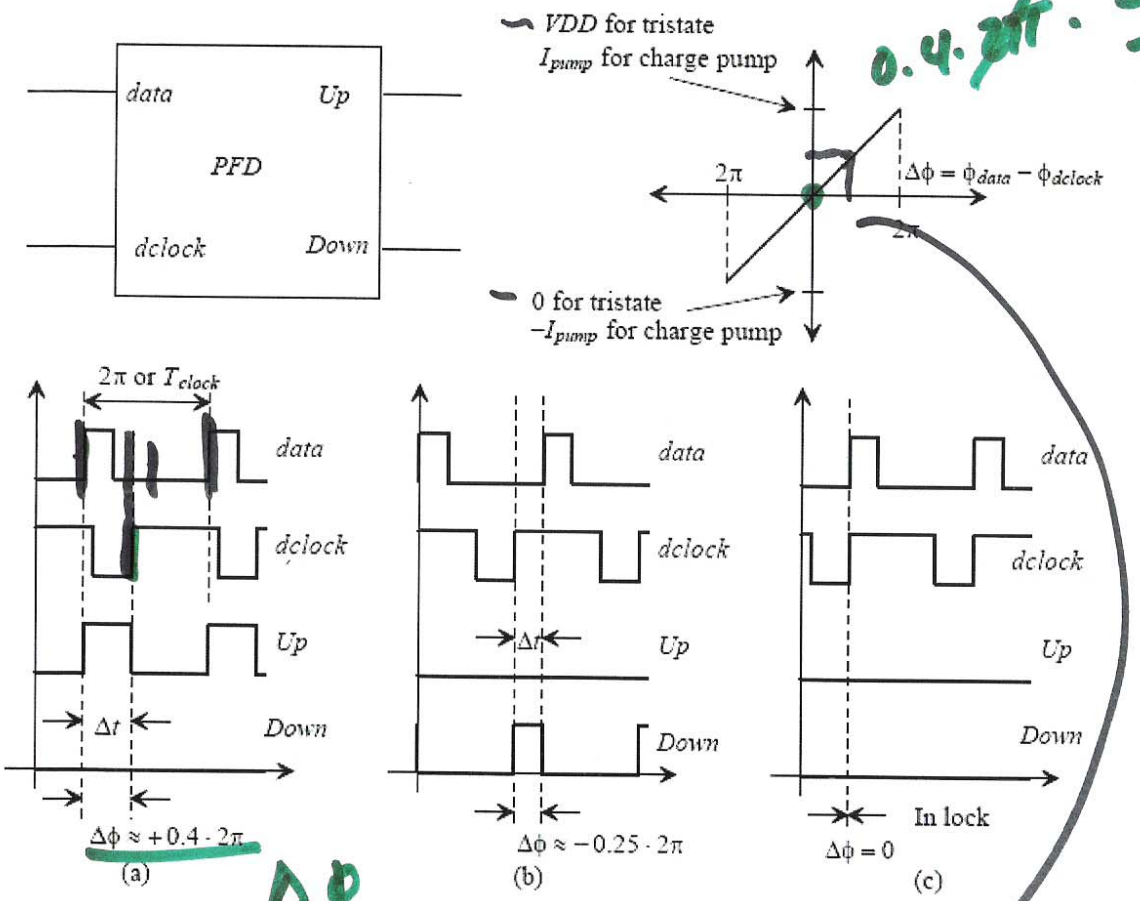
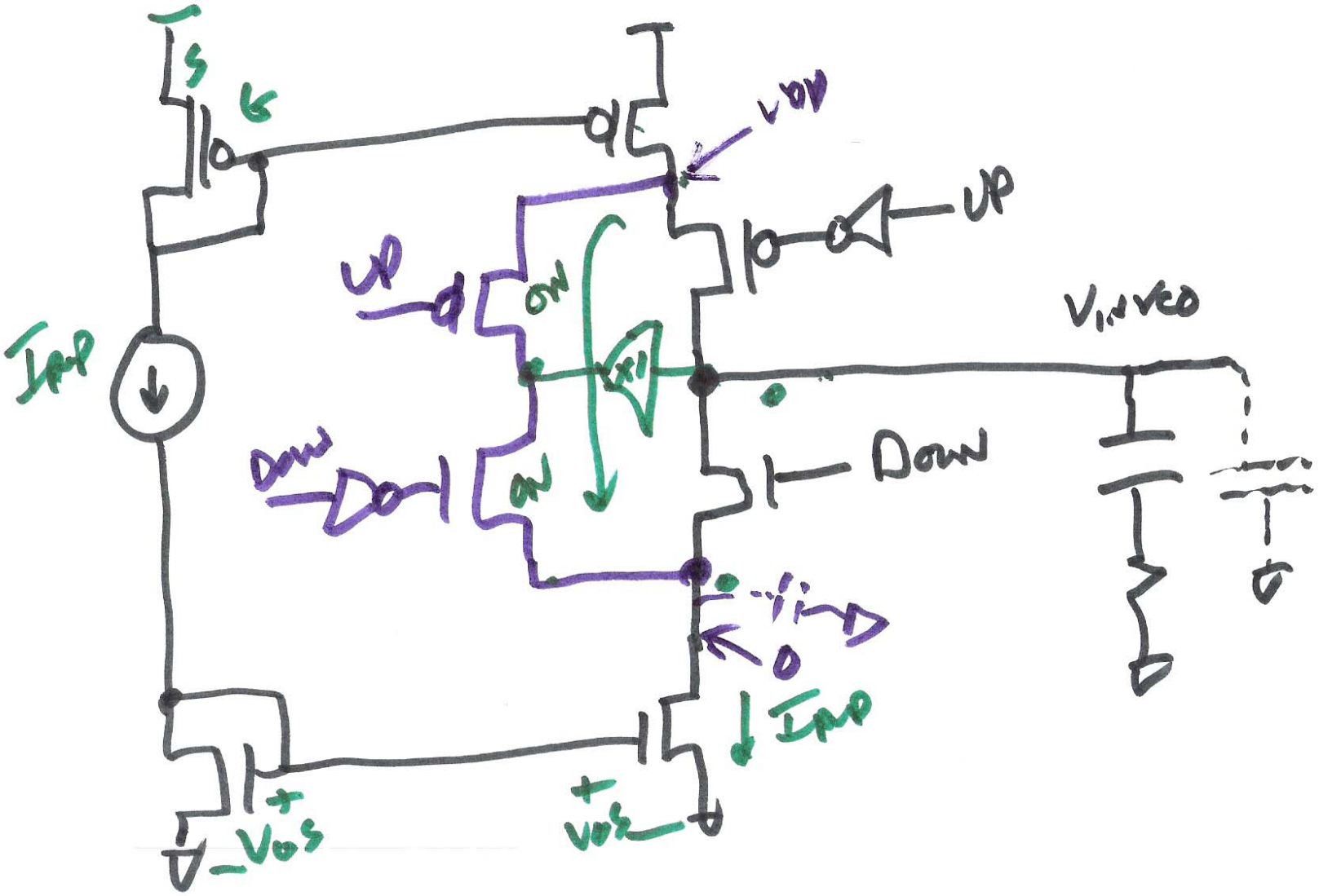


Figure 19.11 PFD phase-detector inputs and outputs.

$$K_{PD,tri} = \frac{VDD}{4\pi}, \frac{Volts}{Radian}$$

$$K_{PDI} = \frac{2\,I_{pump}}{4\pi} = \frac{I_{pump}}{2\pi} \; A/RAD$$

Charge Pump



13)