H.W. – 17.4 ECE 5/418 Memory Circuits

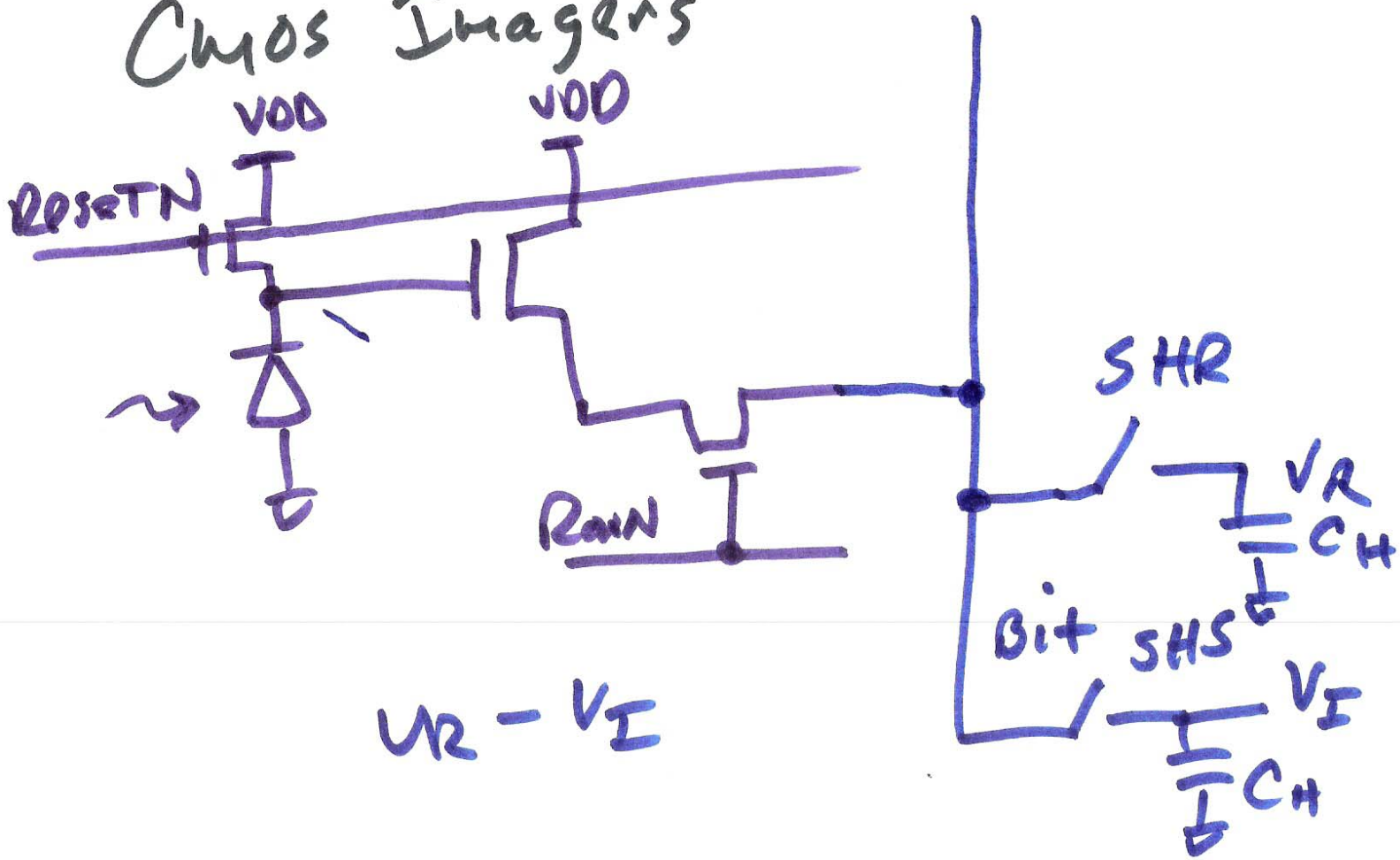
BOISE STATE UNIVERSITY

March 16, 2011

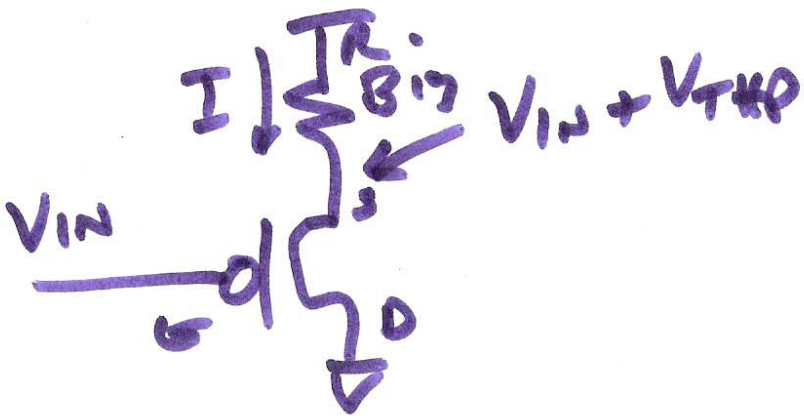
Lecture 16

A17.4 due next Monday

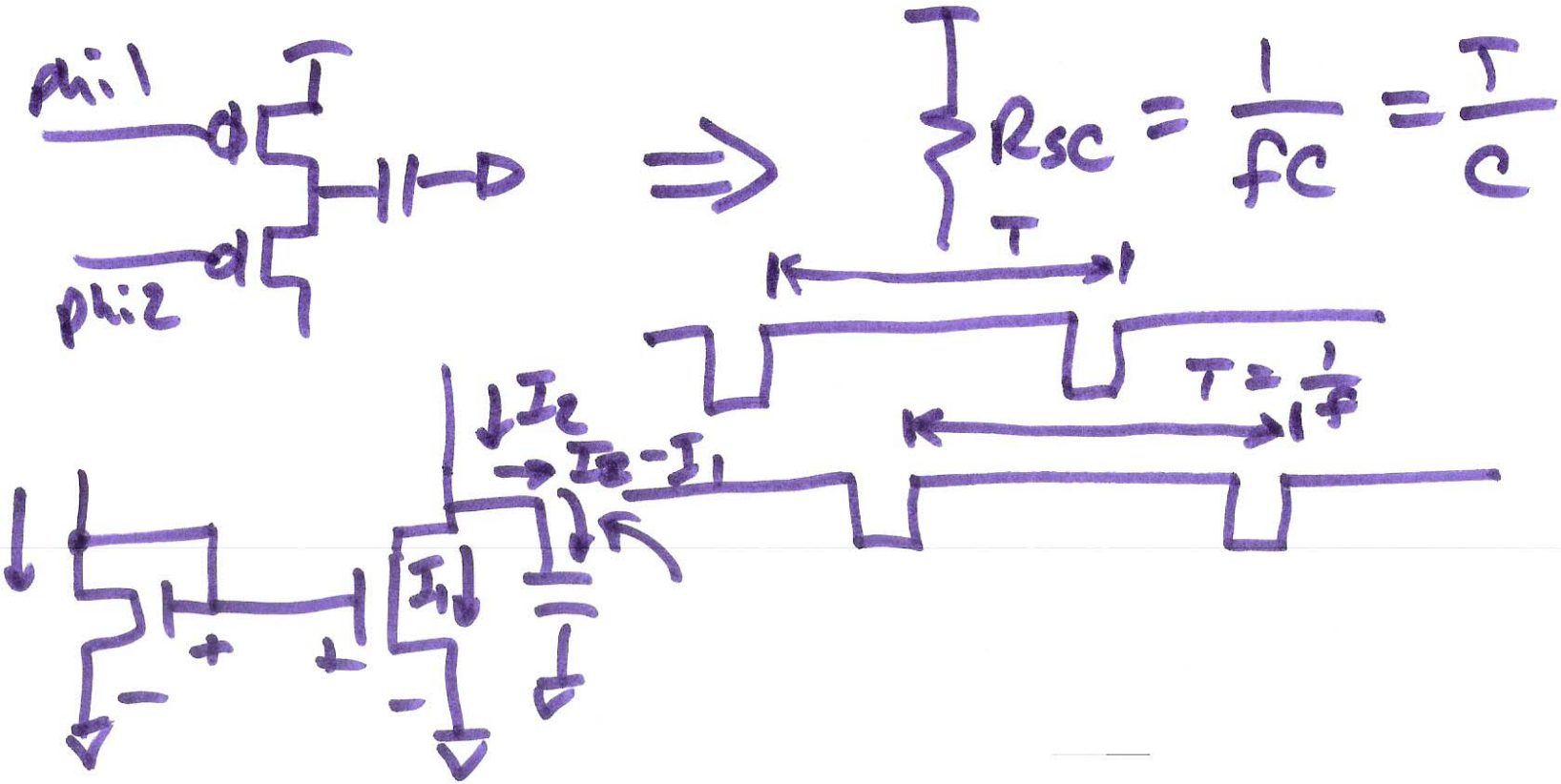
CMOS Imagers



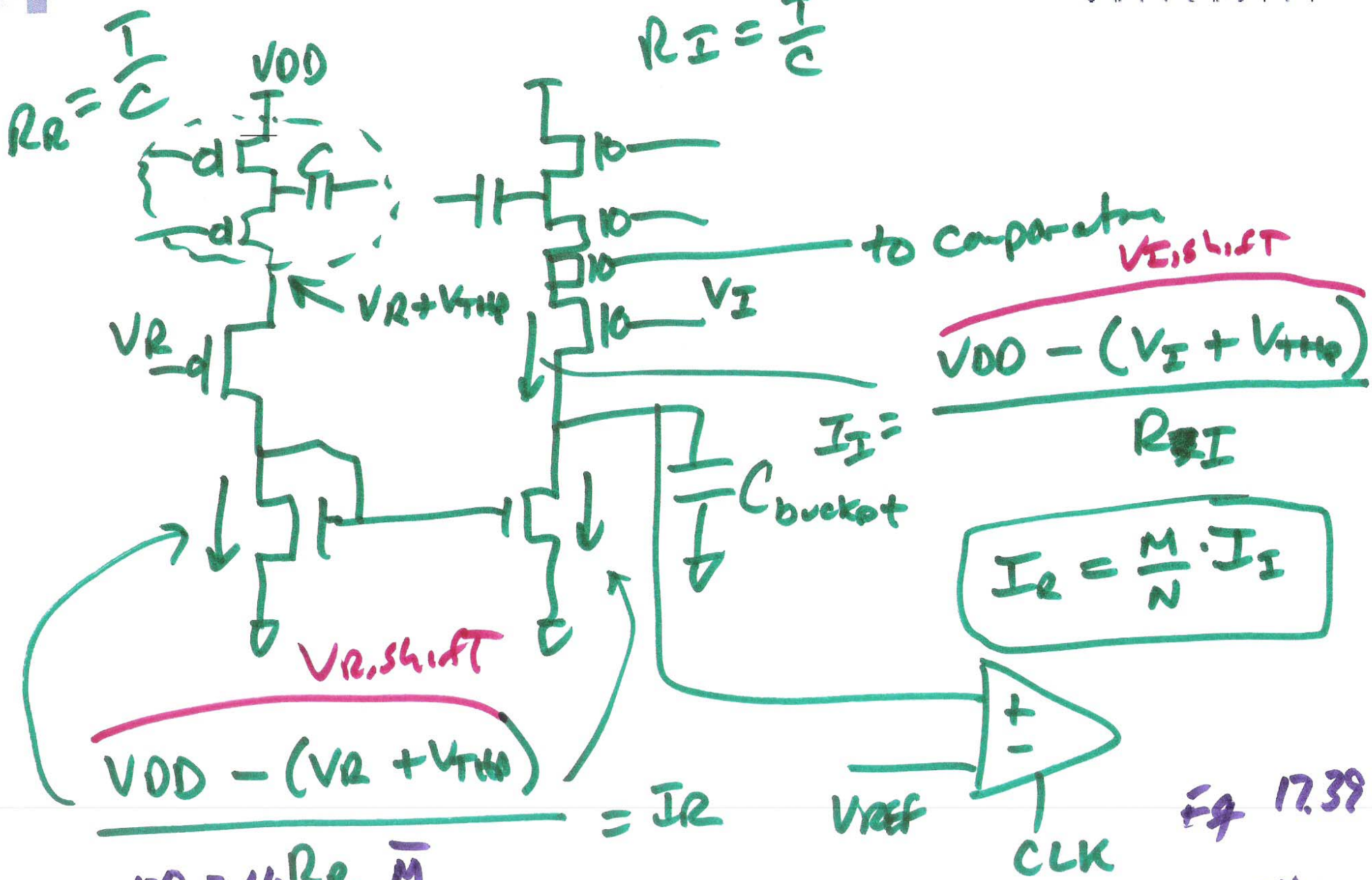
V to I



$$I = \frac{VDD - (V_{TN} + V_{THP})}{R_{Big}}$$



2)


$R_R = \frac{T}{C}$
$R_I = \frac{T}{C}$
VDD
d
d
C
10
10
10
10
to comparator
V_I
$V_R + V_{THp}$
V_R
$V_{I,shift}$
$V_{DD} - (V_I + V_{THp})$
R_{SI}
$I_I =$
C_{bucket}
$I_R = \frac{M}{N} \cdot I_I$
$V_{R,shift}$
$V_{DD} - (V_R + V_{THp})$
$100 - 40R_R \overline{M}$
$= I_R$
V_{REF}
CLK
Eq 17.39
3)
$N - M = 60$
$V_{Rshift} = \frac{M}{N} \cdot V_{I,shift} = \frac{M-N}{N} \cdot V_{I}$
SIA

N = total # of clocks

M = # of times output goes high

$\overline{M}$ = # of times output goes low

$N - M = \overline{M}$

$$V_{R,shift} = \frac{M}{N} \cdot V_{I,shift}$$

$$V_{I,shift} = \frac{N}{M} \cdot V_{R,shift}$$

$VDD - (650mV + 280mV) = 70mV$

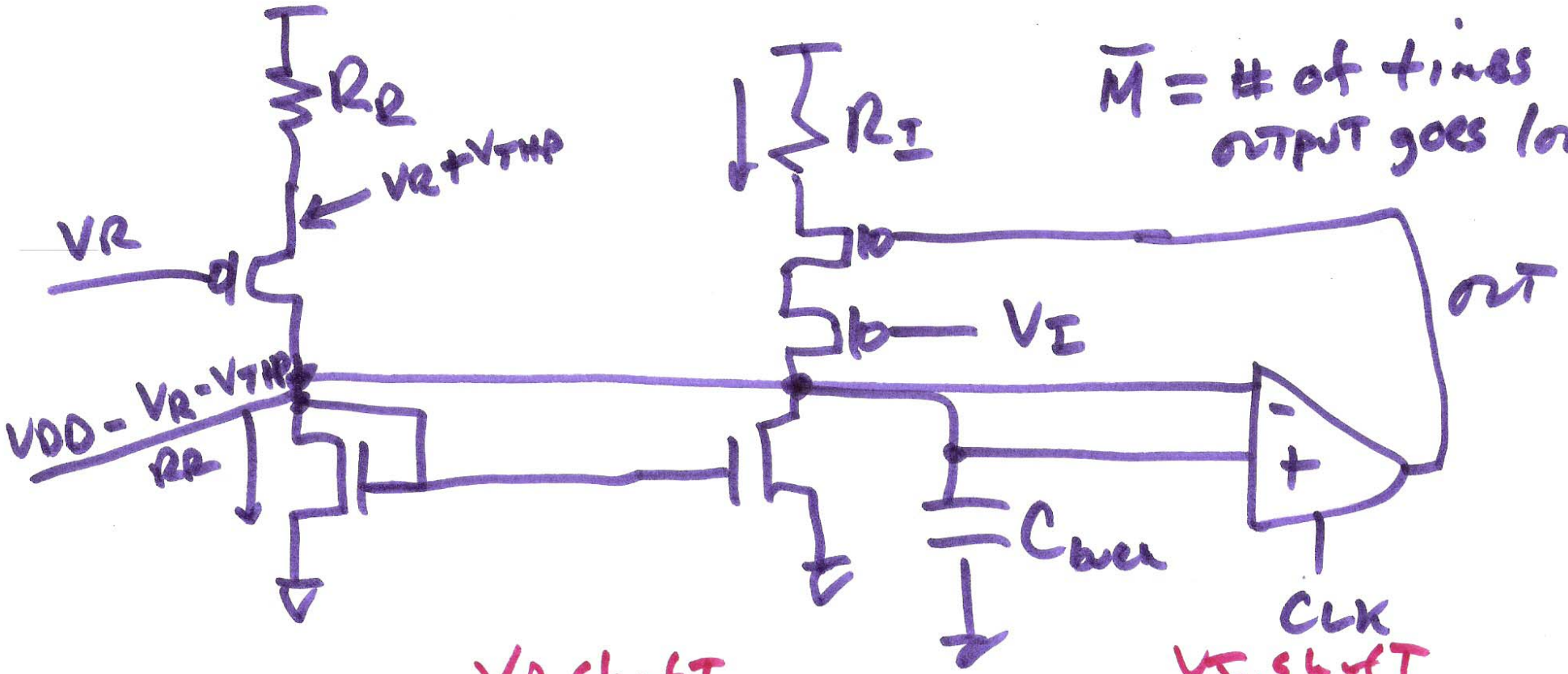
$1 - (V_I + V_{THN}) = 70mV$

$70mV$

$$V_{I,shift} = \frac{N}{M} \cdot V_{R,shift}$$

$\frac{N}{N-m}$

4)



$\bar{M}$ = # of times OUTPUT goes low

$$\frac{V_{R,shift}}{V_{DD} - V_R - V_{THP}} = \frac{V_{I,shift}}{V_{DD} - V_I - V_{THP}}$$

$$\frac{\cancel{R_R}}{\cancel{R_R}} \qquad \frac{\cancel{R_I} \cdot \frac{\bar{M}}{N}}{}$$

5) $\left(\frac{N-\bar{M}}{N}\right)^{-1} V_{R,shift} = V_{Rshift} \cdot \frac{\bar{M}}{N} = V_{I\,shift}$

$$V_{I,Shift} = V_{R,Shift} \cdot \frac{N}{N-M} \quad (17.39)$$

$V_{DD} = 1$

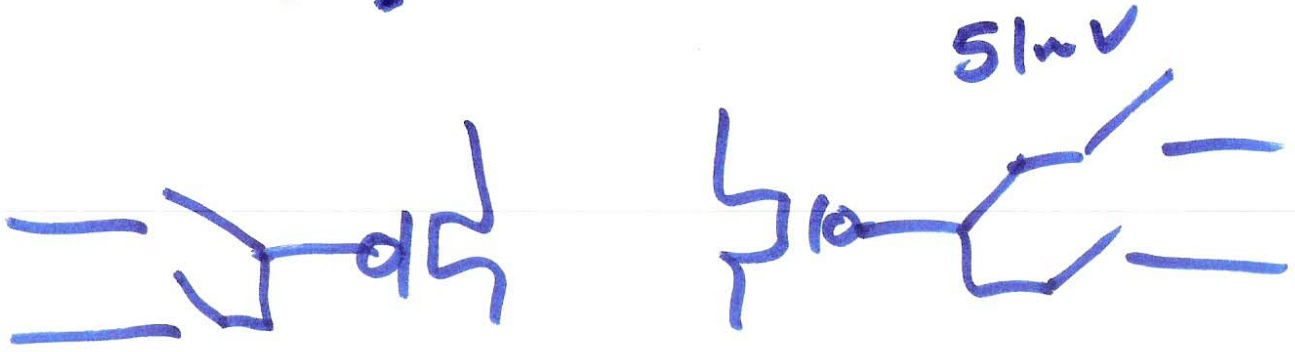
$V_{THP} = 300mV$

V_I , V_R

$V_R = 650mV$

$V_{R,Shift} = 50mV$

$$V_{I,Shift} = 55mV = 50mV \cdot \frac{100}{98}$$



6)

PLLs & DLLs

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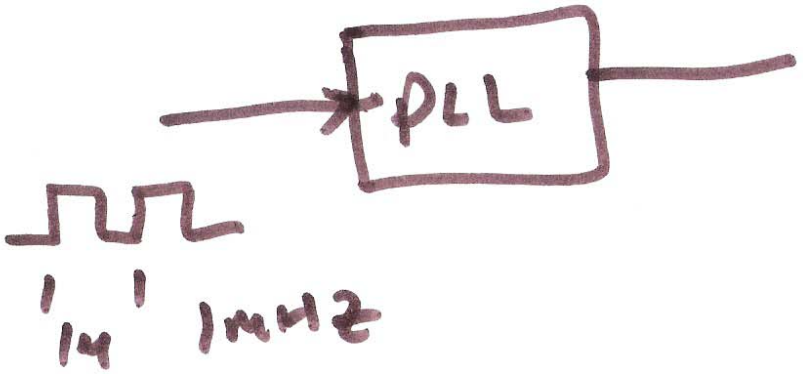
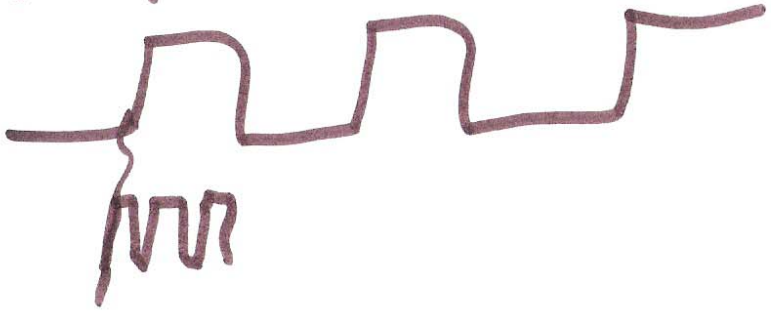
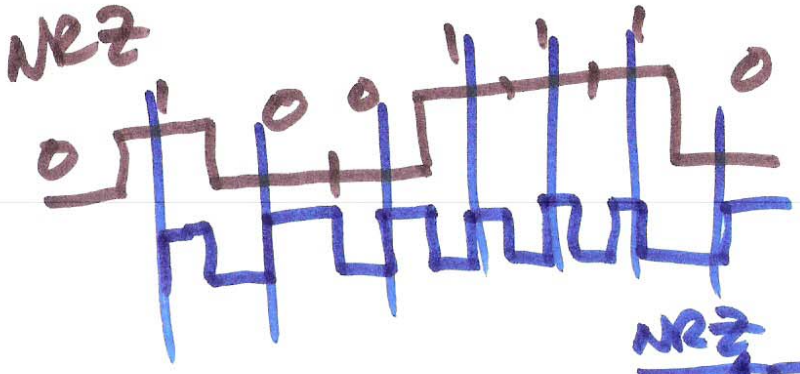
Phase-Locked Loops (PLLs) · second-order

Delay-Locked Loops (DLLs) · first-order



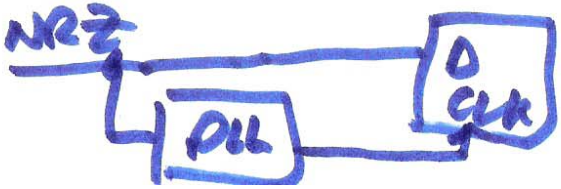
frequency synthesis



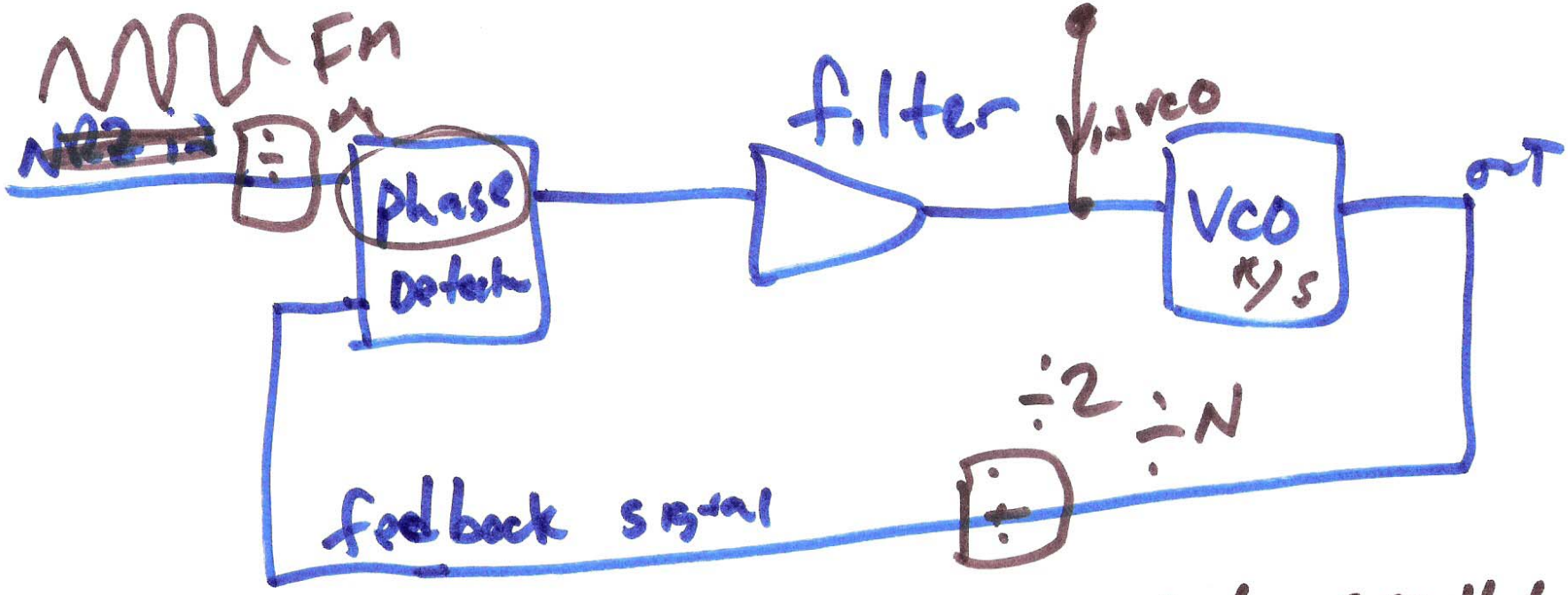


CDR

Clock & data recovery



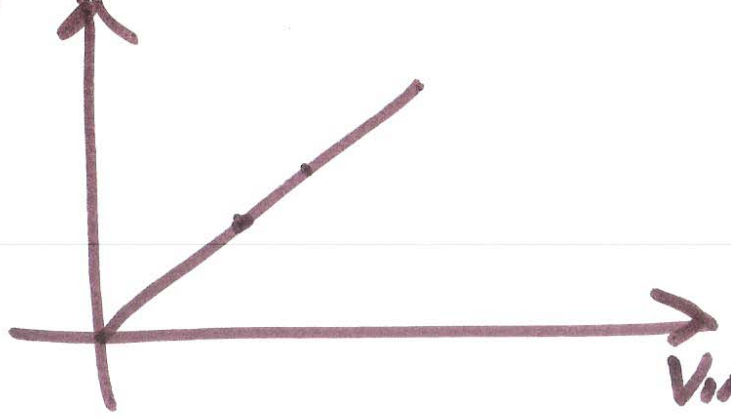
PLL



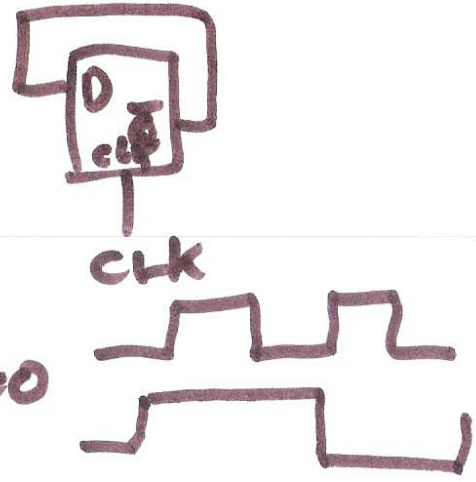
Voltage Controlled Oscillator

$f_{IN} \cdot N = f_{OUTPUT} \cdot M$

$f_{IN} = f_{OUT} \cdot \frac{M}{N}$



VCO



DLL (Delay-Locked Loop)