ECE 5/418 Memory Circuit Design

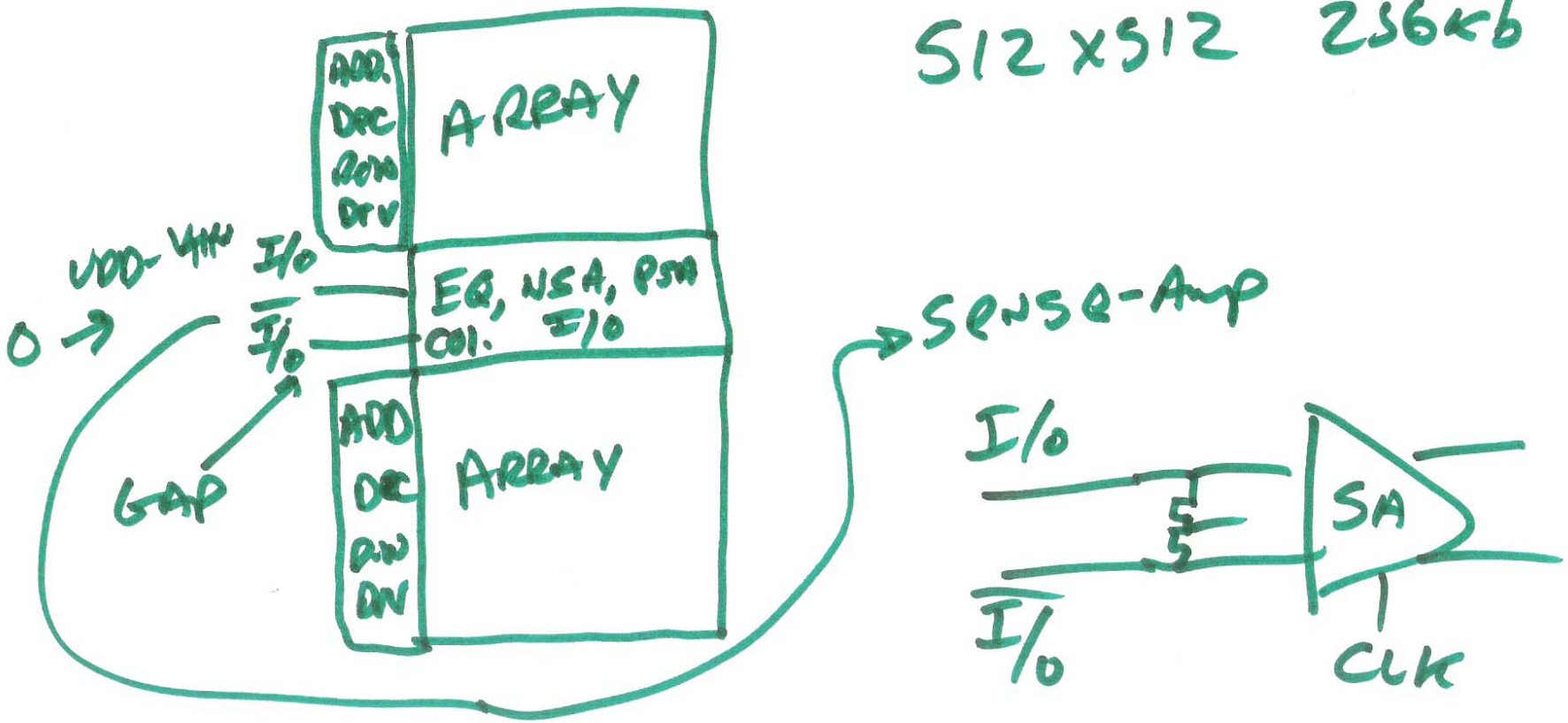
BOISE STATE UNIVERSITY

Lecture 11 2/28/11

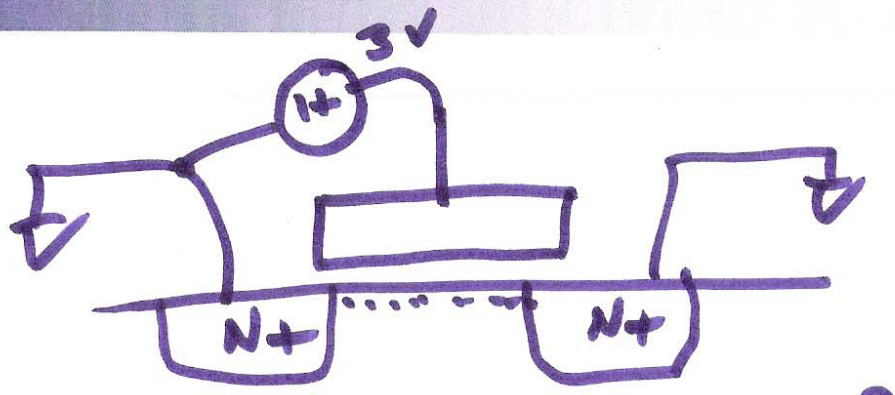
H.W. #9 A16.13, A16.14, A16.15

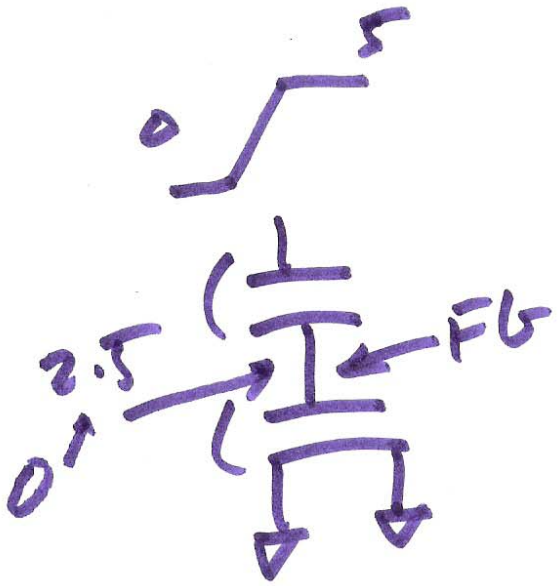
Due March 7, 2011

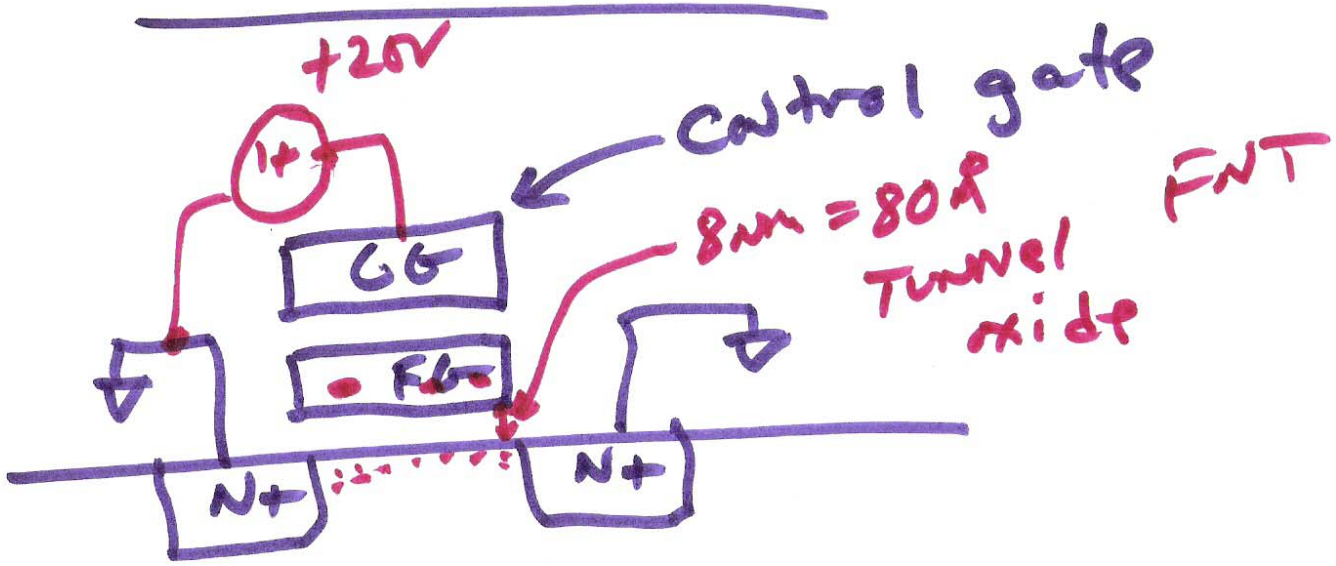
512 x 512 256Kb



Floating Gate Memory

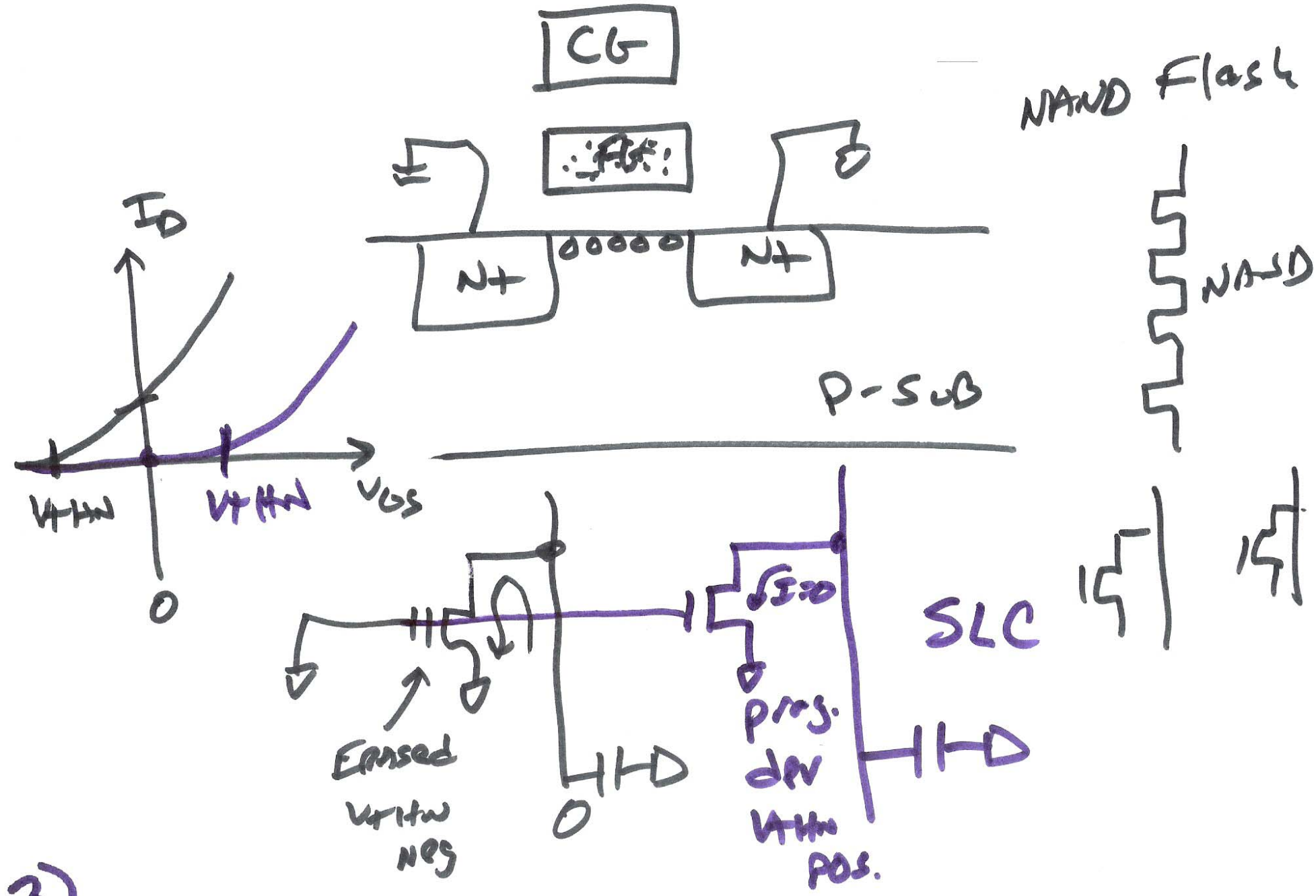






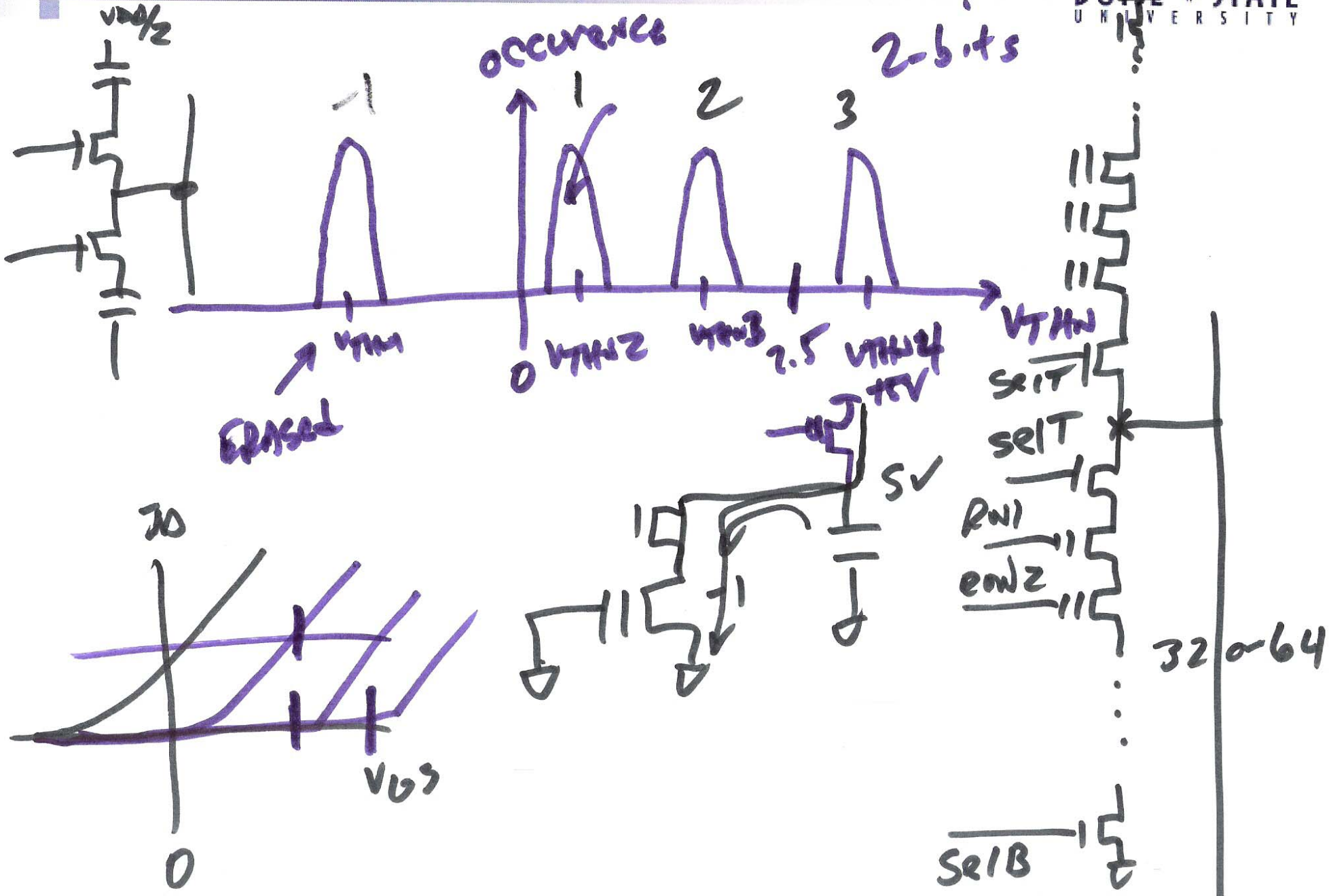
Negative V_{TH} Erased

2)


CG
FG
S
D
N+
N+
P-SUB
I_D
V_{THN}
V_{THN}
V_{GS}
0
NAND Flash
NAND
SLC
Erased
V_{THN}
NEG
0
prog.
V_{THN}
POS.

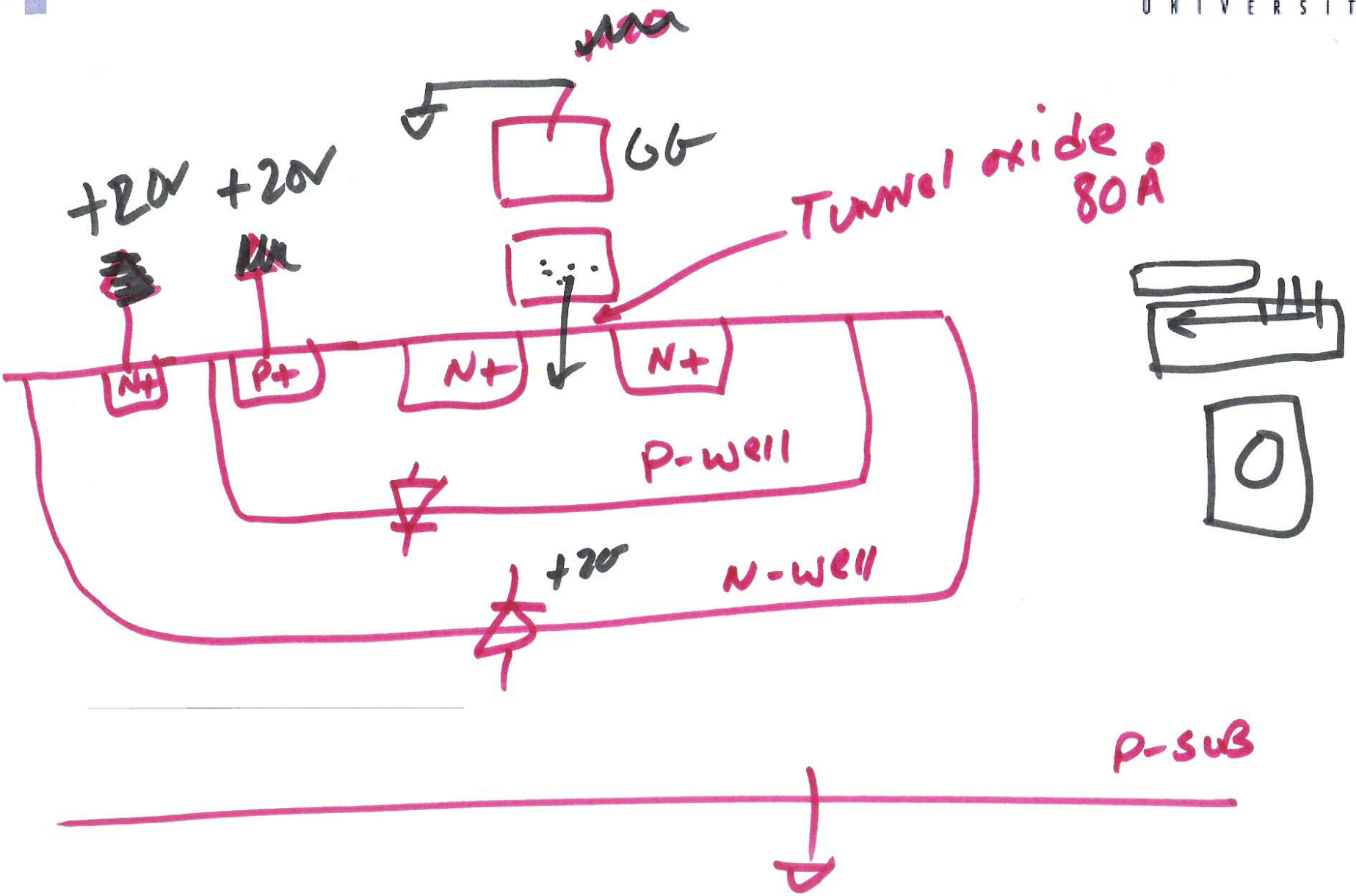
3)

Multi-level Cell (MLC)



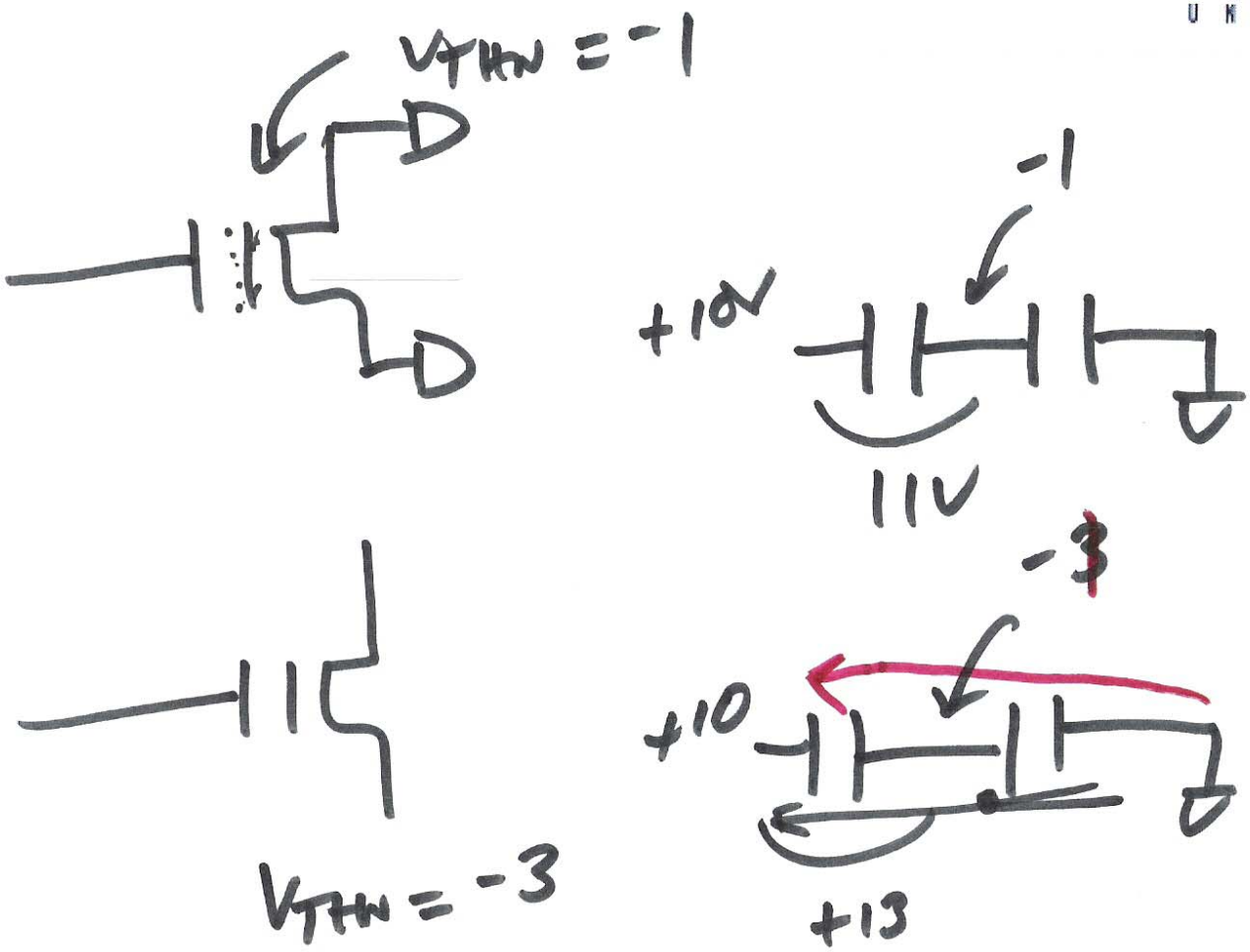
4)

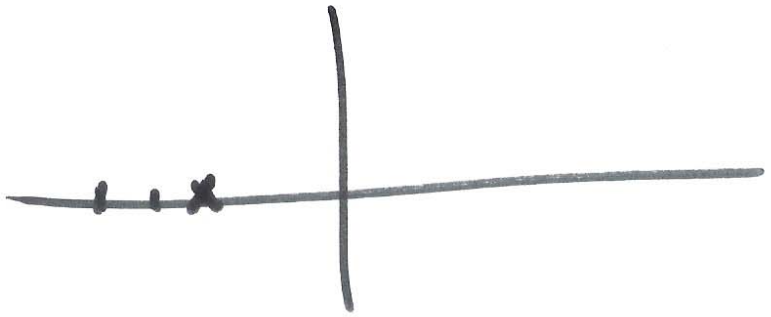
Flash ERASE



5)

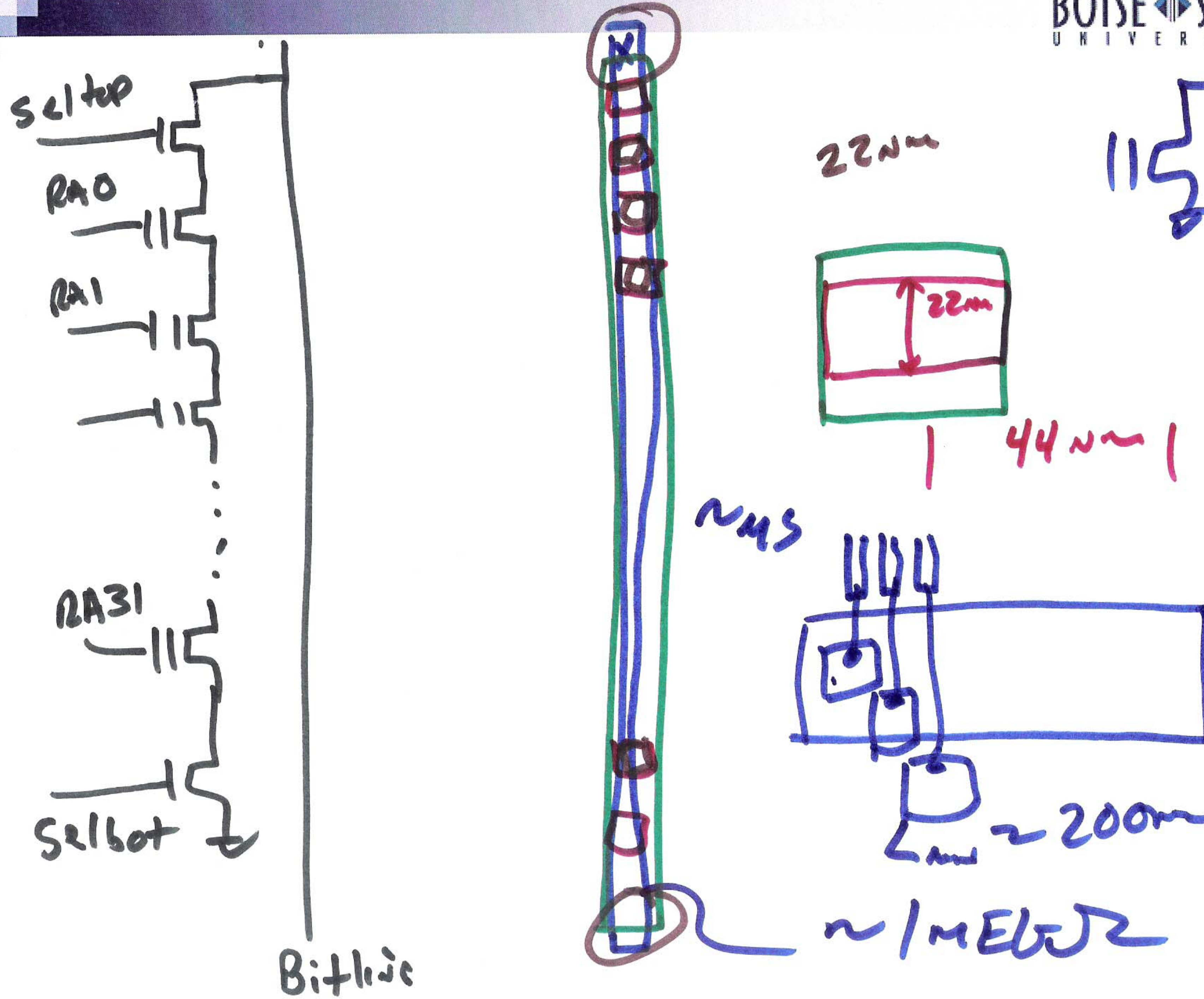
SOFT Programming





6)

Flash $4F^2$


Sel top
RA0
RA1
RA31
Sel bot
Bitline
22nm
22nm
44nm
~1MEG Ω
~nm3
L ~200nm

7)