Use and Design of Synchronous Mirror Delays (SMDs) in SDRAM

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Outline

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- Synchronization circuits
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- Synchronous Mirror Delay (SMD)
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SDRAM

- Synchronous DRAM (SDRAM) has a synchronized interface between DRAM core and memory controller.
- In a typical SDRAM access time, $t_{AC}$, is defined as time between CLK input and valid data out time.
  - This is specified as being less than a defined value, i.e. $t_{AC} < 1\text{ns}$.
- $t_{AC}$ consists of the clock skew, between the external clock and internal clock, plus data buffering time.
- Clock skew needs to be minimized or eliminated to reduce $t_{AC}$.
Synchronization Circuits

- In SDRAM internal clock needs to be generated to clock out data.
- Delay-locked loop (DLL) or phase-locked loop (PLL) is typically used to generate the internal clock.
The PLL and DLL are closed-loop (feedback) circuits in which the external and internal clocks are compared and the phase error is detected.

- The internal clock is then adjusted to correct the phase error.
Synchronous Mirror Delay

- Synchronous Mirror Delay is an open-loop fast locking system.
  - SMD first proposed by NEC group led by Saeki.

- SMD is composed of a forward delay array (FDA), mirror control circuit (MCC), and a backward delay array (BDA).
The fundamental units of the SMD: FDA, BDA, and MCC are composed of inverters and/or NAND gates.

- The delay time of the BDA unit is designed to be as equal to the delay time of the FDA unit.

- The mirror control is used for phase synchronization of the output of the clock driver to input clock.
SMD Operation

- Consider nth, (n+1)th, and (n+2)th pulse of external clock.
- Forward delay path on nth pulse is tclk-(d1+d2).
- Nth pulse is mirrored into BDA by (n+1)th pulse.
- Backward delay path of nth pulse is tclk-(d1+d2).
- BDA output of the nth pulse is advanced d2 to external unbuffered clock.
- Clock driver (d2) after BDA eliminates the clock delay.
SMD Design Considerations

- For equal delay matching, the mask pattern of the BDA unit is the mirror layout pattern of the FDA and the MCC unit.
- To adjust the load and mask pattern, the load NAND (LN{m}) whose size is equal to the NAND of MCC is arranged in the BDA.
- The symmetric pattern provides and digital nature provide better matching with PVT variations.
SMD Timing

- Typical SDRAM provides a CAS latency of 5 or more cycles.
- 2 clock cycles, can be hidden in this latency hence simplifying system design.
PLL vs. SMD Standby Current

- Lock time of the sync circuit becomes an important design issue for high speed SDRAM.
- Also the longer lock time when recovering from power down burns excess standby current.
SMD Pros and Cons

- **Pros:**
  - Fast locking time
  - Lower standby current

- **Cons:**
  - Input pulse width or duty cycle must be kept smaller than the delay value of the delay monitor (DM).
  - Large array size
  - Output phase quantization by unit delay element
  - Static phase error

- For high speed SDRAM > 500MHz, phase error between internal clock and external clock becomes overriding concern.
Nanya 256 Meg DDR DRAM SMD Layout
Nanya 256 Meg DDR DRAM SMD Schematic
Nanya 256 Meg DDR DRAM SMD Schematic
Alternative SMD Topologies

- Analog SMD (ASMD) measures and mirrors the delay of the DM block in an analog manner
  - Which has no output phase quantization problem by nature.
  - ASMD also uses toggled clocks to eliminate the duty-cycle dependency of the input clock.
For \( \{c,d\} = \{H,L\} \): eq-period. Initialize the voltage of the left node to \( V_{\text{ref}} \).

For \( \{c,d\} = \{H,H\} \): up-period. Pump up the voltage of the left node from \( V_{\text{ref}} \) toward \( V_{\text{DD}} \) using a current source whose interval is \( (T_{\text{clk}}-T_{\text{dm}}) \).

For \( c = L \): down period. Pump down the voltage of the left node from the final up-period value toward ground using the current source and measure the time when the “left” crossed the \( V_{\text{ref}} \) and generates an output pulse, then go back to the eq-period.
In the basic scheme, the input clock is fed to a toggle flip flop (TFF) to make signals c and c’.

Also the input clock is fed to the DM block followed by another T-FF to make signals d and d’.

Measurement of the delay of and mirroring can be carried out by using current sources and capacitors.
ASMD Design Concerns

- The performance of ASMD is determined mainly by two subblocks: a linear current source and a high-speed comparator.
- Conversion delay of comparator if not accounted for may cause static phase error of AMD output.
- Comparator can be replicated in delay monitor block for compensation.
- Total delay of delay monitor block and conversion delay of the comparator must be less than clock period.
References


Questions?