Using an over-damped PLL in place of DLL in SDRAM

Presentation by Lael Matthews
SDRAM Requirements

- Synchronization is important to minimize skew and latency
- High sustainable bandwidth (Bits/s)
- Low latency
- Low power
- Upgradeability
- Support large hierarchical memory configurations
Why do we need a PLL/DLL in SDRAM?

- Strobe signals and data inputs are generated with clocks which are likely out of phase
  - Synchronizing these clocks ensures the correct data is read/written
- Peak bandwidth = B (bus width) \* fclk
  - Larger bus width = more wires and higher cost
  - Higher frequency would be better, but then the window to clock in data is smaller, so again we need reliable synchronization
- Allows for faster clocks and therefore smaller latency
Why do we need a PLL/DLL in SDRAM?

- To correctly latch data and avoid setup/hold time violations PLL/DLL synchronize data, reduce skew and improve system timing.
Why is a DLL the Norm?

- Simplicity – the data signal is passed through a delay line to lock it into phase with the clock
- Better jitter performance
  - Jitter is easy to control since there is no jitter circulation
  - The VCDL does not generate a signal which would add additional noise
- A DLL is 1st order
  - Less susceptible to power supply, process and temperature variations
  - Good stability
Why is a DLL the Norm?

Figure 19.53 Block diagram of a delay-locked loop.
Why not use a PLL for SDRAM?

- Increased complexity
  - Requires transitions to prevent frequency wander
  - Data scramble or a preamble must be added to prevent this side effect which is complex and costly
  - Selecting proper gain and bandwidth while maintaining stability and limiting noise
  - Once a chip is produced hand tuning (with fuses or other digital adjustments) are required to fix the center frequency and gain
- Stability issues (second order system)
- Need for frequency locking
- Extra injected phase noise (jitter)
  - Sensitive to supply and substrate noise (for current starved VCO)
  - Gain not constant with variations of process and temperature
  - PLL is a high pass filter for VCO noise
- Longer acquisition times
  - With power saving modes present in DRAMs, circuits lose lock when powered down and must relock when restarted
Trade Offs for PLL Design

- **Gain**
  - high gain results in wider bandwidth
  - suppresses the static phase error
  - increases acquisition range and decreases acquisition time

- **Bandwidth**
  - narrow bandwidth has better external jitter performance
  - worse tracking

- **Pull In Range**

- **Acquisition Time**
Bandwidth

- Modulation frequency at which the PLL loses lock with a changing reference
- PLL is a low pass filter for reference noise
- High pass filter for VCO noise
Why is a PLL 2\textsuperscript{nd} Order?

- From the diagram

\[ \phi_{\text{clock}} = K_{PD} K_F \frac{K_{\text{VCO}}}{s} \left( \phi_{\text{data}} - \frac{\phi_{\text{clock}}}{N} \right) \]

- Changing $K_F$ to $F(s)$ and substituting $K$ for $K_{\text{VCO}} K_{PD}$

\[ H(s) = \frac{\phi_{\text{clock}}}{\phi_{\text{data}}} = \frac{K \cdot F(s)}{s + \frac{K \cdot F(s)}{N}} \]

- This appears to be a first order system, however the loop filter also contains a pole resulting in the 2\textsuperscript{nd} order system
PLL

Figure 19.32 Block diagram of a DPLL using a sequential phase detector (PFD).
Characteristics of a 2nd Order System

- Two key components of the system are
  - Natural frequency ($\omega_n$) – determines band width
  - Damping factor ($\zeta$) – determines dynamic loop response
- Both have a direct effect on the gain and stability of the system
- Adding a zero (by using a different filter) allows the gain to be held constant while adjusting the stability
- A static phase error may exist depending on the loop filter
  - Active PI has a 0 static phase error
  - RC and passive lag filter have errors of $\Delta\omega/K$ where $K$ is $N*K_{PD}*K_{VCO}$
Characteristics of a 2\textsuperscript{nd} Order System

- **General form**

  \[ H(s) = \frac{\omega_n^2}{s^2 + 2\xi \omega_n s + \omega_n^2} \]

- **Passive lag filter**

  \[ H(s) = \frac{\omega_n^2 + 2\xi \omega_n s}{s^2 + 2\xi \omega_n s + \omega_n^2} \]

- **Active PI filter**

  \[ H_e(s) = \frac{s^2}{s^2 + 2\xi \omega_n s + \omega_n^2} \]

- **Charge pump**

  \[ H(s) = \frac{K(1+sRC_1)}{s^2 + s(KR) + \frac{K}{C_1}} \]
## Characteristics of a 2\textsuperscript{nd} Order System

<table>
<thead>
<tr>
<th>TYPE</th>
<th>NATURAL FREQUENCY</th>
<th>DAMPING FACTOR</th>
<th>STATIC PHASE ERROR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Basic RC network</td>
<td>$A$</td>
<td>$\sqrt{\frac{K}{RC}}$</td>
<td>$\frac{1}{2} \cdot \sqrt{\frac{1}{K \cdot RC}}$</td>
</tr>
<tr>
<td>Passive lag filter</td>
<td>$B$</td>
<td>$\sqrt{\frac{K}{\tau_1 + \tau_2}}$</td>
<td>$\frac{1}{2} \cdot \sqrt{\frac{K}{\tau_1 + \tau_2}} \cdot (\tau_2 + \frac{1}{K})$</td>
</tr>
<tr>
<td>Active PI filter</td>
<td>$C$</td>
<td>$\frac{\sqrt{K}}{\sqrt{\tau_1}}$</td>
<td>$\frac{\tau_2}{2} \cdot \sqrt{\frac{K}{\tau_1}}$</td>
</tr>
</tbody>
</table>

Table 2.3. Different loop parameters for the second-order system based on the various loop filters (Referring to Figure 2.10, $\tau_1 = R_1C$, $\tau_2 = R_2C$; $\Delta \omega$ refers to the input frequency step)
Stability Issues

- System Transfer function vs. frequency
  - For $\zeta>0.707$ response is flat
  - For $\zeta<0.707$ response overshoots allowing amplified error to re-circulate

- Error Transfer function acts as a high pass filter

Figure 2.15. Magnitude Plots of the PLL Phase Transfer Function (left) and Error Transfer Function (right)
Stability Issues

- This is why an over-damped (\(\zeta > 1\)) system is used, and must be maintained despite source noise and changes to process and temperature.

![Phase step response graph](image-url)
Acquisition and Tracking

- **Tracking parameters**
  - Hold Range ($\Delta\omega_H$): Frequency range that the PLL can track without losing lock
  - Change Rate ($d\Delta\omega/dt$): limits how fast the frequency can change without losing lock

- **Acquisition parameters**
  - Pull in range ($\Delta\omega_P$): Range in which the loop can acquire a lock
  - Lock range ($\Delta\omega_L$): loop can quickly recapture a lock in one cycle
Acquisition and Tracking

- **Pull in Range**
  - When $\Delta \omega > \Delta \omega_L$ the PLL will gradually pull the frequency towards the lock range.
  - A PI filter ideally provides infinite DC gain so $\Delta \omega_P \rightarrow \infty$.
  - For a passive LF $\Delta \omega_P = F_{PD} \sqrt{2\xi\omega_n K}$ where $F_{PD}$ is a gain factor based on the type of loop filter.

- **Pull in Time**
  - If $\Delta \omega$ is less than 80% of $\Delta \omega_P$ the pull in time can be approximated for Phase detectors:
    \[ T_P \approx \frac{1}{F_{PD}^2} \frac{\Delta \omega^2}{\xi \omega_n^3} \]
  - As $\Delta \omega$ approaches $\Delta \omega_P$, $T_P \rightarrow \infty$.
  - For a PFD $T_P$ is the time it takes to charge the loop capacitor to the proper value. Initial conditions will also affect the pull in time.
Jitter (Phase Noise)

- Problem: Clock may not be centered on data (critical for high speed)
External Jitter

- Noise on incoming signals from off chip
  - NRZ signals can be noisy
  - Noise can be filtered by the PLL if BW is narrow
- Jitter peaking is a characteristic of under damped 2nd order systems where noise will be amplified at a certain frequency
  - Use a passive lag loop filter or active PI loop filter to keep damping factor and loop gain independent
  - Creates a zero which can lead to jitter peaking
- If the zero occurs at a lower frequency than the first pole we get a gain > 1
- Therefore we place the zero and first pole as close together as possible resulting in an over damped system
- Over damping the system results in slower acquisition
External Jitter Peaking

- Example for an active PI filter

\[ H(s) = \frac{\frac{K}{\tau_1} \left(1 + \frac{\tau_2}{\tau_1} \cdot s\right)}{s^2 + \frac{K}{\tau_1} \frac{\tau_2}{\tau_1} \cdot s + \frac{K}{\tau_1}} \]

\[ P_{\text{low}} = \frac{K \tau_2}{\tau_1} \left( -1 + \sqrt{1 - 4 \frac{\tau_1}{K \tau_2^2}} \right) \quad P_{\text{high}} = \frac{K \tau_2}{\tau_1} \left( -1 - \sqrt{1 - 4 \frac{\tau_1}{K \tau_2^2}} \right) \quad Z = \frac{1}{\tau_2} \]
Internal Jitter

- The VCO is an oscillator and therefore resonates at a particular frequency based on the voltage.
- Shifts in the phase (jitter) can occur from power and ground noise or process and temperature variations.
- Since the VCO is a closed loop, any jitter created is fed back through the PLL and is called jitter accumulation.
- Each stage of the ring oscillator injects noise with a $\Delta t_r$ and $\Delta t_f$ error and different transition slopes resulting in jitter.
Improve Internal Jitter

- Gate overdrive should be as large as possible ($V_{BP}$ and $V_{BN}$ also shown at $V_C$ in the equation)
- Phase noise degrades with scaling but a longer channel length can improve performance with the disadvantage of a slower response
- Increasing power dissipation by increasing the bias current
- Choosing the number of stages influences jitter
  - In general sensitivity is proportional to $1/N^{1.5}$
  - More stages reduce noise from unequal rise/fall times
- Add an inductor with a capacitor since higher $f_{osc}$ degrade jitter performance
- Higher temperature introduces more jitter carefully designing the tail current may reduce these effects
Improve Internal Jitter

- $V_c$ is the gate overdrive voltage ($V_{GS} - V_T$)
- $P$ is the total power dissipation
- $\alpha$ is a constant factor
- $\sigma_{N,\Delta t}$ is the overall timing error
- $T_0$ is the period

$$\frac{\sigma_{N,\Delta t}}{T_0} = \alpha \cdot \sqrt{\frac{kT}{P} \cdot \frac{VDD}{V_c}}$$
Other Tricks to Reduce Jitter

- Use a fully differential delay buffer which takes the place of a stage in the VCO to reject common mode noise

- Self-bias technique to track variation caused by process and temperature (negative effect is power supply sensitivity)
Other Tricks to Reduce Jitter

- Can achieve noise suppression and wide lock range with a two loop architecture
  - Frequency tracking occurs first providing the dominate control voltage to the VCO and a large gain
  - Once frequency is locked, the phase loop is dominate acquiring final phase lock with a small bandwidth

- Interpolation (ability to control delay of a stage through control signals that add capacitance or route signals through faster inverters)

![Two-loop architecture for the aided acquisition](image)
Can you use an over-damped PLL instead of a DLL?
- Yes although it is not very practical

Advantage:
- Input noise is filtered
- Can generate frequencies
- Lower pin counts

Drawbacks:
- More complicated design
- Must worry about stability
- Slow acquisition times
- Added noise source in the VCO
- Must track frequency input
References

- D. Fischette, “First Time, Every Time Practical Tips for Phase Locked Loop Design”. Presentation. 2007