Digital Delay Lock Loop Design

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May 2010
Digital Delay Locked Loop

- Synchronization of clock to a reference clock using a variable delay line and feedback

- Why is it important?
  - The DLL is responsible for S-DRAM output data alignment with the system clock
Synchronization Alternatives

- Use of system clock to fire output drivers
  - IO driver is too slow to respond to the system clock and fire the outputs
  - Too many devices in the path

- Static Delay
  - PVT variation is too large and if it could be done there would be independent delays for each system clock frequency

- Make it the memory controllers problem
  - Cost and complexity of controller would increase
  - Possibility of bandwidth reduction
Digital DLL Advantages

- Discrete delay steps
- Better manufacturability
- Easy to design for wide range of operating conditions
- Does not require a continuous clock to maintain lock
- Transfer function is simpler than PLL
Basic DLL Operation

- D1 – Input buffer delay
- D2 – clock tree, data latch and output driver delay
- Feedback delay models D1 and D2 across PVT
- Coarse Alignment only

\[ D1 + N \cdot tCK \]  
\[ \quad \text{-(}D1 + D2\text{)} + D2 \quad \text{N} \cdot tCK \]
Conventional DLL

ENTRY Point to the FIRST to High Transitions

DELAY ELEMENTS

SHIFT REGISTERS

Clkin

Shift Right (Remove Delay)

Initial Entry Point

Shift Left (Add Delay) from Initial Entry Point

Assume total number of delay line=8
Modified DLL Schematic

- DLL1 is a digital DLL with coarse and fine delay lines
  - Total fine delay = 1 coarse delay
  - Options exist to disable the fine delay line
Digital DLL Major Components

- Input Buffer
- Delay Line
  - Coarse and Fine Delay Elements
  - Serial Delay and Ring Delay Lines
- Phase Detector
- Clock Insertion Point Selection
- Data Path Models
Input Buffer Designs

Self Biased Differential Amplifier

Differential Amplifier with VREF

Differential Amplifier using Complimentary Clocks
Delay Line

- Measured delay elements used to delay the clock signal for proper alignment
- Quantizes the clock delay into discrete units of delay
- Better resolution can be achieved by using Coarse and Fine delay combinations
- Typically regulated to ensure stability
- Constant unit delay across all PVT
Coarse and Fine Delay Elements

Coarse delay line

Fine delay line
Delay Designs

- Linear Delay line
  - All delay elements are lined up in series.
  - Clock delay is determined by discrete time delay of each element
  - Requires excellent matching of each delay element

- Ring Delay Line
  - Delay line is only as long as one clock period
  - Counter is used to determine how any circuits around the delay loop are allowed
Linear Delay Line

Each Delay element feeds the next element in the delay line
Shift register selects Clock insertion point into the delay line

Forward Path delay: \( D1 + [N*_{tCK} - (D1' + D2')] + D2 = N*_{tCK} \)
Ring Counter Delay Line

Coarse Delay line is Linear
Fine delay line is a circular loop of fine delay elements and a counter

Concept of Ring Delay Line
Phase Detector

Clock Out is the Clock output from the DLL that has been passed through the Delay Model. Clock In is the incoming clock from the Input Buffer. Shift Left and Shift Right control the direction that the shift register will shift and the Shift Clock signal triggers the shift register.
Phase Detector
Clock Insertion Point Selection

- Primary function is to respond to the PD inputs and direct the delay line insertion point of the clock.
- Dynamic response to PD inputs to constantly adjust the length of the delay line.
- Locks when clock stops so constant clock is not necessary.
- Various Implementations
  - Shift Register
  - Counter
Data Path models

- The Data path models reflect the delay elements that the Clock signal has seen or will see.
- Input buffers
- Output buffers
- Intermediate boosting circuits
- Ideally these are exact copies of the routing and circuits themselves.
Additional Circuits

- Duty Cycle Correction
- Majority Filter
- Odd\Even Topology
  - Phase Mixing of Adjacent Delay elements
Duty Cycle Correction

- Ensures that Clock signal seen by DLL has a 50% duty cycle, and that Clock out of the DLL is also at a 50% duty cycle.

\[ T_{L, \text{clk-int}} = 0.5(T_{\text{clk}} - T_{L}) + 0.5T_{L} = 0.5T_{\text{clk}} \]

All-digital Fast-Locked Synchronous Duty-Cycle Corrector
Majority Filter

- Reduces the sensitivity of the DLL to CLK noise
  - Located between the phase detector and the shift register
  - Once the DLL is locked the Majority filter is engaged to filter the shift commands to the shift register. Instead of the DLL tracking every slight variation on CLK the DLL would have to see a series of shift requests before moving the insertion point.
Odd/Even Topology

EXIT Point Pairs: ExitEn=1

SHIFT REGISTERS
ExitEn

Shift Left
Initial Exit Points
Shift Right

7 (O) 6 (E) 5 (O) 4 (E) 3 (O) 2 (E) 1 (O) 0 (E)

Assume total number of delay line=8
Phase Mixer

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Design Considerations

- Jitter, Jitter, Jitter
- Solid Ground Planes
  - No other circuits that cause ground bounce and have short return paths
- Solid Power planes
  - Dedicated VDD pins?
  - Dedicated power rails or regulated potentials
- Shielding for critical signals
  - “Coax” shielding where practical
- Location
  - Quiet portion of the chip, close to supplies and ground
Questions?
References

Synchronous Mirror Delay, SMD

Forward delay path and a Backwards delay path

Forward-Path Delay:
\[ D1 + (D1' + D2') + 2 \left( N^*tCK - (D1' + D2') \right) + D2 = 2 N^*tCK \]
Measure-Controlled Delay, MCD

delay path

External Clock

Delay Monitor

Measure Delay Array

Measure Circuit (Latch)

Forward Delay Array

Forward-Path Delay = \( D1 + [N^*tCK-(D1'+D2')] + D2 \)

= \( N^*tCK \)

\( N^*tCK \)

\( N^*tCK-(D1'+D2') \)

\( D2 \)

TDC

DTC

Synchronized Output