Last time

drawbacks
- Noise sensitivity
- VDD sensitivity
- Poor resolution

Clock range

Do-Do

All-digital DLL

Benefits:
- Robust
- Easy to design

Zero-order f.d.

Loop works under

Any phase shift

results in stability

The same correction

SR or SL
Analog PLL

PLL - you have to
  don't lock freq
  and can't generate
  freq. (tracks)
\[ KV \cdot K_F \cdot K_D (\phi_{inT} - \phi_{clock}) = t_1 \]

\[ \phi = \frac{t_1}{T_{clock}} \cdot 2\pi \]

\[ \phi_{out} = \phi_{in} + \frac{t_1}{T_{clock}} \cdot 2\pi \]

\[ W_{clock} = \frac{2\pi}{T_{clock}} \]
\[
\frac{\phi_{\text{out}}}{\phi_{\text{in}}} = \frac{1}{1 - K_\text{D} K_\text{v} K_\text{F} \cdot \text{Work}}
\]

\[
K_\text{D} = -\frac{I_{\text{amp}}}{\pi}
\]

\[
K_\text{F} = \frac{1}{5C_1}
\]

\[
\frac{\phi_{\text{out}}}{\phi_{\text{in}}} = \frac{S}{S + K_\text{v} \cdot \frac{2I_{\text{amp}}}{C_1 \cdot \text{Touc}}}
\]

(Equation 19.69)
Current-starved inverter
Linearize the current

\[ V_{DD} \]

P-MOS

N-MOS

\[ V_{DD} \]

In

Out
half-replica

VREF

Vbias

Vdel

Vbias

Vbias

Vbias