4/21/10  Lecture 21

![Diagram showing a circuit with DLL and delay components.](image-url)
$$t_{	ext{rise}} + t_d + t_{	ext{tr}} = T_{	ext{clk in}}$$

Adjust so that above relation is valid.
\[ T_{OUT} \cdot N = t_d + t_{UP} + t_{OUT} \]
Drawback is high resolution.