

Additional comments on the use of K -paths (aka N -paths) seen on pages 52 – 53. Figure 2.37 is shown below for convenience.

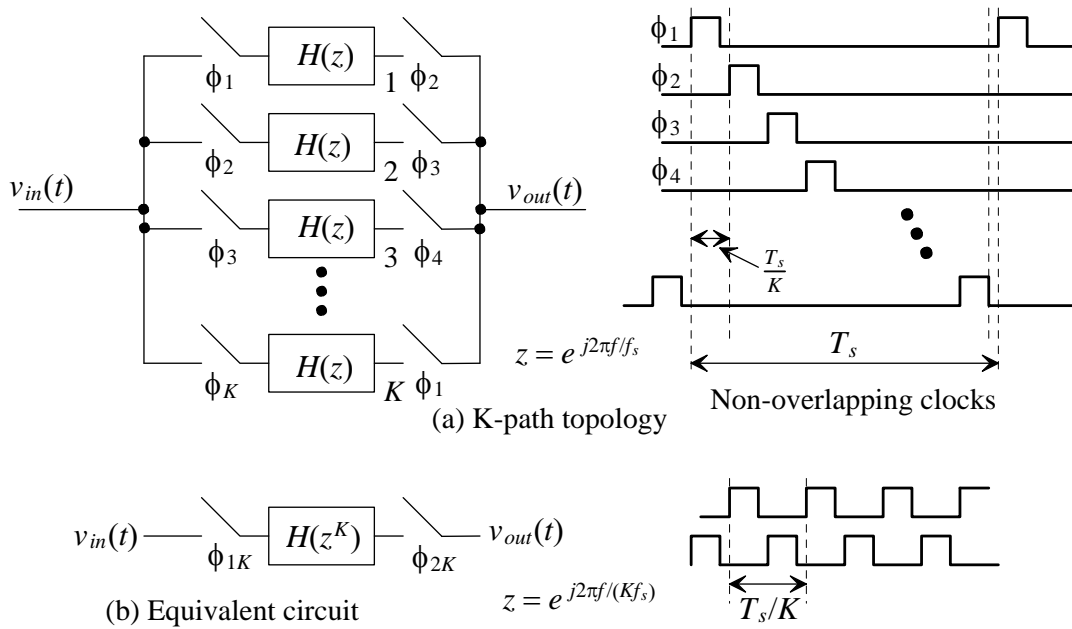


Figure 2.37 A K -path topology and its equivalent circuit.

To begin let's write the input of the top path (path 1) at times $0, \frac{T_s}{K}, 2\frac{T_s}{K}, 3\frac{T_s}{K}, \dots, T_s, T_s + \frac{T_s}{K}, T_s + 2\frac{T_s}{K}, \dots$,

$$v_{in,1} = v_{in}[0], \overbrace{0, 0, \dots, 0}^{K-1 \text{ zeroes}}, v_{in}[T_s], \overbrace{0, 0, \dots, 0}^{K-1 \text{ zeroes}}, v_{in}[2T_s], 0, 0, \dots, \text{etc.}$$

The key point is that only when the ϕ_1 input switch is closed (at times $0, T_s, 2T_s, 3T_s, \dots$) is the input to the top path nonzero. Also note that we didn't specify a rising or a falling edge. As long as we are consistent with the time the input is sampled, or valid, the following analysis is valid. For the second path, path 2 or the second from the top path, we can write

$$v_{in,2} = 0, v_{in}[\frac{T_s}{K}], \overbrace{0, 0, \dots, 0}^{K-1 \text{ zeroes}}, v_{in}[T_s + \frac{T_s}{K}], \overbrace{0, 0, \dots, 0}^{K-1 \text{ zeroes}}, v_{in}[2T_s + \frac{T_s}{K}], 0, 0, \dots, \text{etc.}$$

noting the ϕ_2 input switch is closed at times $\frac{T_s}{K}, T_s + \frac{T_s}{K}, 2T_s + \frac{T_s}{K}, 3T_s + \frac{T_s}{K}, \dots$) For the third path

$$v_{in,3} = 0, 0, v_{in}[\frac{2T_s}{K}], 0, 0, \dots, 0, v_{in}[T_s + \frac{2T_s}{K}], 0, 0, \dots, 0, v_{in}[2T_s + \frac{2T_s}{K}], 0, 0, \dots, \text{etc.}$$

and so forth.

Note that we haven't specified, or used, the phasing of the switches on the outputs of the paths. As long as the output changes between the paths every $\frac{T_s}{K}$ this analysis is valid. This means that instead of using the clock signals seen above we could use 50% duty cycle clock signals simply shifted in time by $\frac{T_s}{K}$, Fig. 9.4. Also, using (or not using) non-overlapping clocks isn't important as long as the edges are spaced apart by $\frac{T_s}{K}$.

Returning to our K -paths we can write, for any integer n ,

$$v_{in}[n \cdot \frac{T_s}{K}] = \sum_{p=1}^K v_{in,p} \left[n \cdot \frac{T_s}{K} \right]$$

noting that for any one value of n the summation on the right side of this equation has only one nonzero value, the other $K - 1$ values are 0. Knowing that $z = e^{j2\pi f T_s}$ and thus $z^{1/K} = e^{j2\pi f T_s/K}$ we can write

$$V_{in}(z^{1/K}) = \sum_{n=0}^{\infty} v_{in}[n \cdot \frac{T_s}{K}] \cdot z^{-n/K} = \sum_{p=1}^K V_{in,p}(z^{1/K})$$

Next, we know that the transfer function for any of the identical paths is

$$H(z) = \frac{V_{out,1}(z)}{V_{in,1}(z)} = \frac{V_{out,2}(z)}{V_{in,2}(z)} = \frac{V_{out,3}(z)}{V_{in,3}(z)} = \dots$$

The overall transfer function of the K -paths is

$$\frac{V_{out}(z^{1/K})}{V_{in}(z^{1/K})} = \frac{V_{out,1}(z^{1/K}) + V_{out,2}(z^{1/K}) + V_{out,3}(z^{1/K}) + \dots + V_{out,K}(z^{1/K})}{V_{in,1}(z^{1/K}) + V_{in,2}(z^{1/K}) + V_{in,3}(z^{1/K}) + \dots + V_{in,K}(z^{1/K})}$$

or

$$\frac{V_{out}(z^{1/K})}{V_{in}(z^{1/K})} = \frac{H(z) \cdot V_{in,1}(z^{1/K}) + H(z) \cdot V_{in,2}(z^{1/K}) + H(z) \cdot V_{in,3}(z^{1/K}) + \dots + H(z) \cdot V_{in,K}(z^{1/K})}{V_{in,1}(z^{1/K}) + V_{in,2}(z^{1/K}) + V_{in,3}(z^{1/K}) + \dots + V_{in,K}(z^{1/K})}$$

or finally

$$\frac{V_{out}(z^{1/K})}{V_{in}(z^{1/K})} = H(z)$$

the response of a single path where one delay, T_s , is K delays at the faster sampling rate of K/T_s . In other words, if we redefine z at the faster clock rate, $f_{s,new} = K \cdot f_s = K/T_s$ then a delay of z^{-1} at the slower clock rate is a delay of z^{-K} at the faster clock rate or

$$z \rightarrow z^K$$

For a K -path system we replace z in the single path with z^K to get the system's overall response.

Note that the output phasing of the clocks wasn't important in this result. Also note, again, that we can use clock signals like those seen in Fig. 2.37 (not a 50% duty cycle) or as seen in Fig. 9.4 (near 50% duty cycle). The only important issue is that the clock edges are spaced apart by T_s/K .