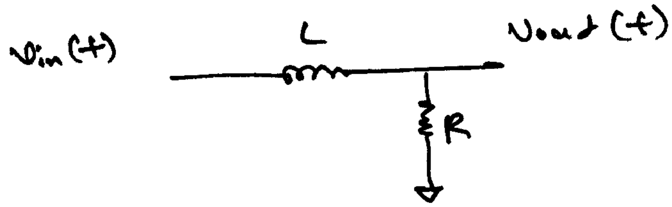
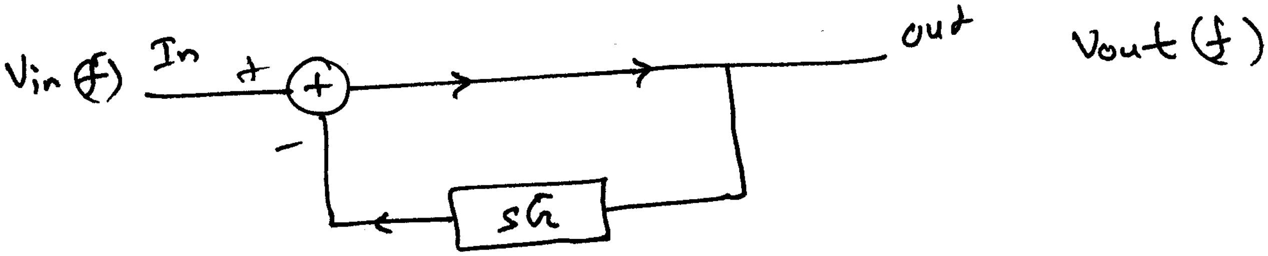
ALOK JAIN

Solution : 35.1



its block diagram would be



where $G = L/R$

35.2

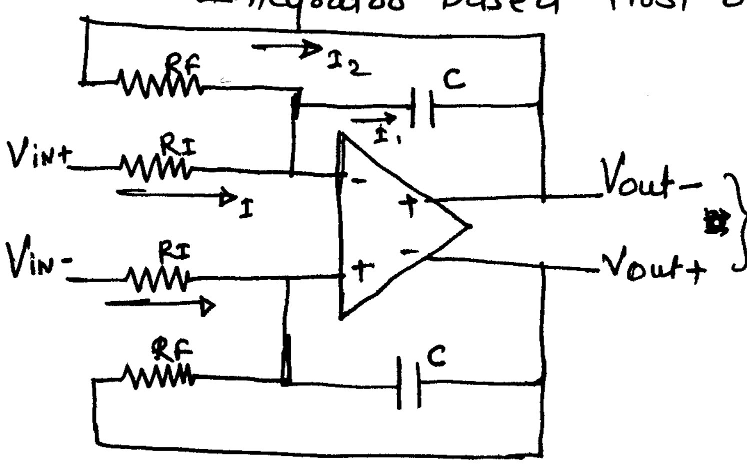
prob: 02

show that Eq. (35.6) is still valid if the circuits inputs and outputs are referenced to the common mode voltage V_{CM}. (The OPAMP inputs also be at V_{CM})

Ans:

Referring fig 35.6

Integrator-based first order filter



→ We don't have to inversion the output.

We can write

$$I = I_1 + I_2$$

$$\frac{V_{IN+}}{R_I} = \frac{V_{out}}{R_F} + \frac{V_{out}}{1/sC}$$

$$\frac{V_{IN+}}{R_I} - \frac{V_{out}}{R_F} = \frac{V_{out}}{1/sC} \quad \text{———} \quad \boxed{35.6}$$

$$V_{out}\left(\frac{1}{1/sC} + \frac{1}{R_F}\right) = \frac{V_{IN+}}{R_I}$$

$$\frac{V_{out}}{V_{IN+}} = \frac{1}{R_I}\left(\frac{1}{1/sC} + \frac{1}{R_F}\right)^{-1}$$

$$= \frac{1}{R_I}\left(\frac{R_F + 1/sC}{R_F/sC}\right)^{-1}$$

$$= \frac{1}{R_I}\left(\frac{\frac{s.R_F.C+1}{sC}}{R_F/sC}\right)^{-1}$$

$$\frac{V_{out}}{V_{IN^+}} = \frac{1}{R_I}\left(\frac{R_F}{1+S\cdot R_F\cdot C}\right)$$

$$\frac{V_{out}}{V_{IN^+}} = \frac{R_F/R_I}{1+S\cdot R_F\cdot C.} \quad \text{———} \quad \boxed{35\cdot 7}$$

If Input and output is referenced to V_{CM}; then the input and output are referenced to V_{CM} rather than 0 (GND). Also the Special hint is given in bracket that the OPAMP inputs also be at V_{CM};

With this we can write the equation 35·6 is as follows:

$$\left\{\begin{array}{l} V_{IN} \rightarrow V_{in}-V_{CM} \\ V_{out} \rightarrow V_{out}-V_{CM} \\ \quad \text{and Input of OPAMP at } V_{CM}. \end{array}\right.$$

$$\cancel{\frac{(V_{IN}-V_{CM})}{R_I}} \quad I - I_2 = I_1$$

$$\frac{(V_{IN}-V_{CM})-V_{CM}}{R_I} - \frac{(V_{out}-V_{CM})-V_{CM}}{R_F} = \frac{(V_{out}-V_{CM})-V_{CM}}{1/sc}$$

By solving this equation we can get the original 35·6 equation.

So Conclusion is if we referrenced the input and output to V_{CM}; then still equation 35·6 remains unchanged or valid.

$$\frac{V_{out}-2V_{CM}}{V_{in}-2V_{CM}} = \frac{1}{R_I}\left(\frac{R_F}{1+S\cdot R_F\cdot C}\right).$$

Hence the RHS. remains the same as 35·7. So the eqn 35·6. is still valid.

$\underline{\text{II}^{nd}\text{ Approach}}$: If we consider the OPAMP gain-BW ~~and~~ product and single ended OPAMP (i.e. $V_+ \rightarrow$ tied to V_{cm}) then

The same equation can be written

$$\frac{V_{in} - V_-}{R_I} - \frac{V_{out} - V_-}{R_F} = SC\left(V_{out} - V_-\right)$$

Also with $V_- = -\frac{V_{out}}{A_{OL}(f)}$, We get

$$\frac{V_{out}}{V_{IN}} = \frac{\frac{R_F}{R_I}}{\underbrace{1 + S.C.R_F}_{\text{Desired response}} + \underbrace{\frac{S.C.R_F}{A_{OL}(f)} + \frac{1}{A_{OL}(f)}\left(1 - \frac{R_F}{R_I}\right)}}$$

So the desired Response is

$$\boxed{\frac{V_{out}}{V_{IN}} = \frac{\frac{R_F}{R_I}}{1 + S.C.R_F}} \quad \text{— Eq}^n.\ \underline{35.7}$$

This equation was derived ~~for~~ previously from $\text{eq}^n\ \boxed{35.6}$

So still the eqn 35.6 is valid.

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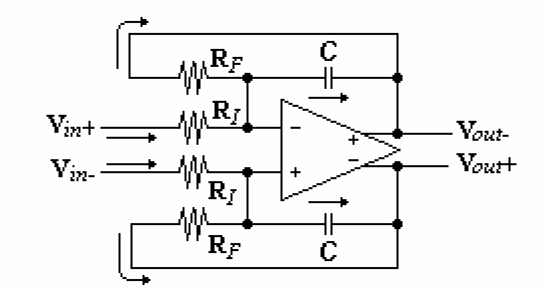
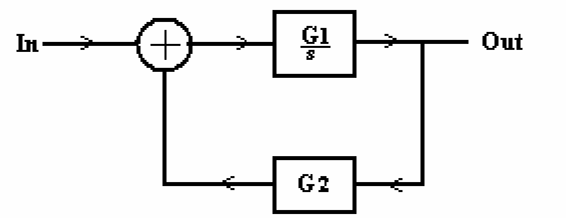
35.3) *Sketch the implementation of a first-order lowpass filter using a CAI with a 3dB frequency of 10Mhz and a DC gain of 6dB. Simulate your design to verify if it works as expected.*

Soln:





Using nodal analysis at the inputs of the op-amp we get the following:

$$\frac{V_{in}}{R_I} - \frac{V_{out}}{R_F} = \frac{V_{out}}{1/sC}$$

Solving for Vout/Vin we get the following:

$$\frac{V_{out}}{V_{in}} = \frac{\frac{R_f}{R_I}}{(1+sR_fC)}$$

Solving for Out/In we get the following:

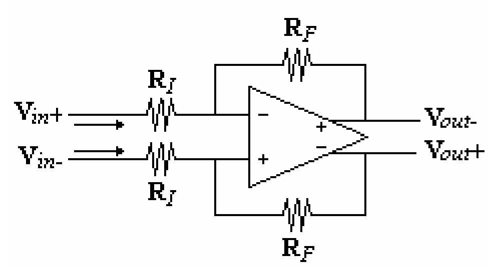
$$\frac{Out}{In} = \frac{\frac{1}{G_2}}{(1+\frac{s}{G_1G_2})}$$

From the above equations we can equate G1 and G2:

$G1=1/R_IC$ and $G2=R_I/R_F$

$f_{3dB}=G_1G_2/2\pi$

At DC the op-amp can be modeled as such, the gain would simply be R_F/R_I.



$6_{dB}=20*\log(x)$
$x=2$

set **R_I=1k and R_F=2k**

We find C by plugging the 3_{dB} frequency (10MHz) into the following equation and solving for C:

$f_{3dB}=1/R_FC2\pi$ **$C=7.95e^{-12} \approx$ 8pF**

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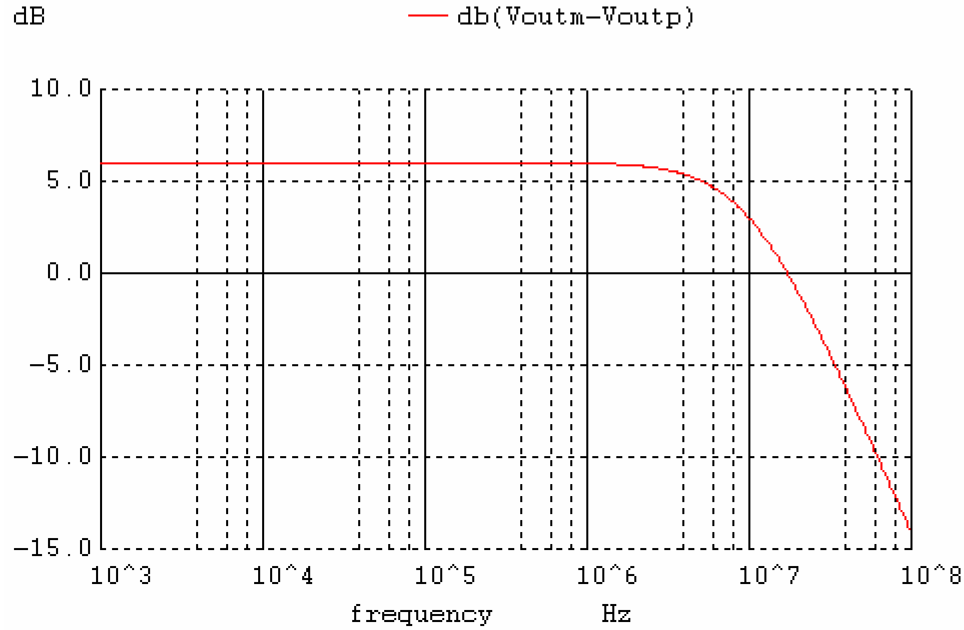
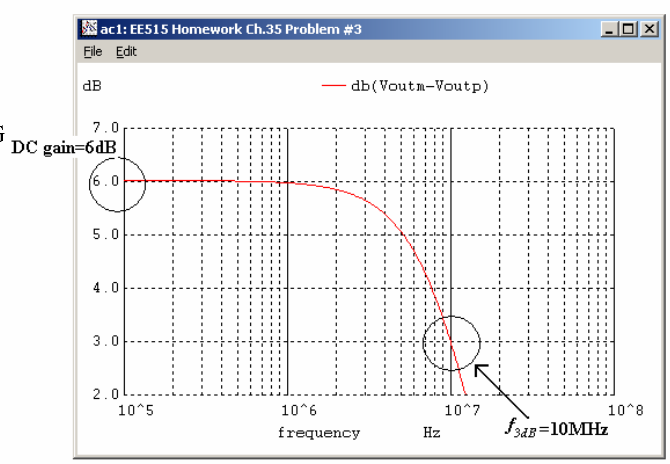
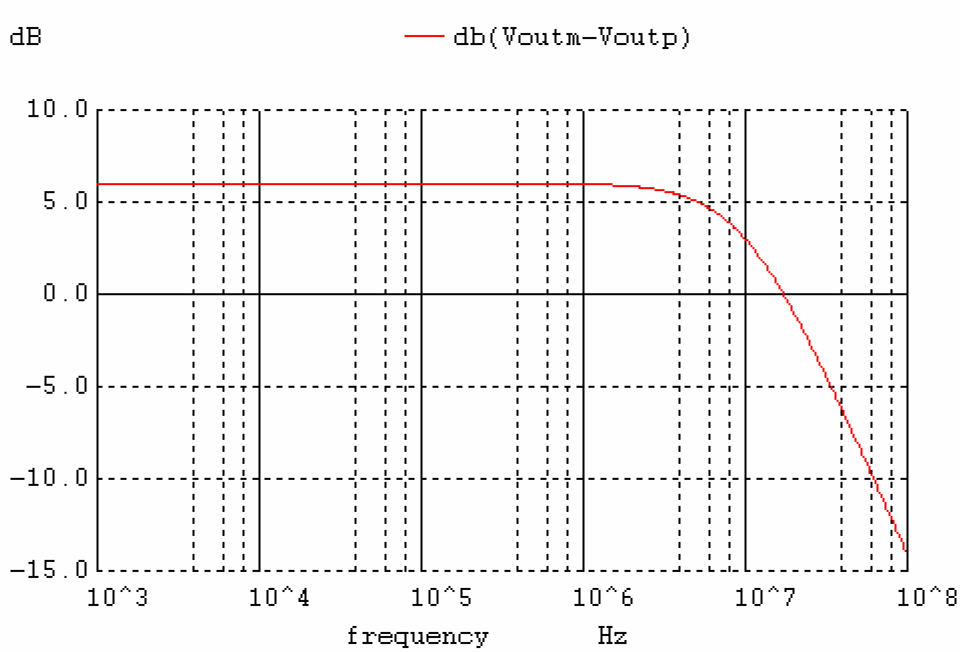
Simulations are shown below for verification along with the netlist, also shown is the phase response of the system.

E515 Homework Ch.35 Problem #3

```
.control
destroy all
run
let Vout=Voutm - Voutp
plot db(Voutm-Voutp)
plot ph(Voutm-Voutp)
.endc

*ac sweep from 1kHz to 100MHz*
.ac dec 100 1k 100MEG

VCM VCM 0 DC 0.75

Vin Vinps VCM DC 0 AC 0.5
Vina Vinms VCM DC 0 AC -0.5

Rftop Voutp Vinm 2k
Ritop Vinps Vinm 1k
Rfbot Voutm Vinp 2k
Ribot Vinms Vinp 1k

Cfp Voutp Vinm 8pF
Cfm Voutm Vinp 8pF

E1 Voutp VCM Vinp Vinm 100MEG
E2 VCM Voutm Vinp Vinm 100MEG

.end
```







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35.4) *Plot, in the complex plane, the ideal pole location and the actual pole locations due to finite op-amp unity-gain frequency for the filter described in Ex. 35.4*

Soln:

For the filter in Ex. 35.4 f_u=10MHz with C=259n and R_f=1k. We can use Eq.(35.17) from the book to find the 2 poles due to the finite op-amp unity gain.

$$s_{p1}, s_{p2} = \frac{-CR_F \pm \sqrt{(CR_F)^2 - 4\dfrac{CR_F}{\omega_u}}}{2 \cdot \omega_u}$$

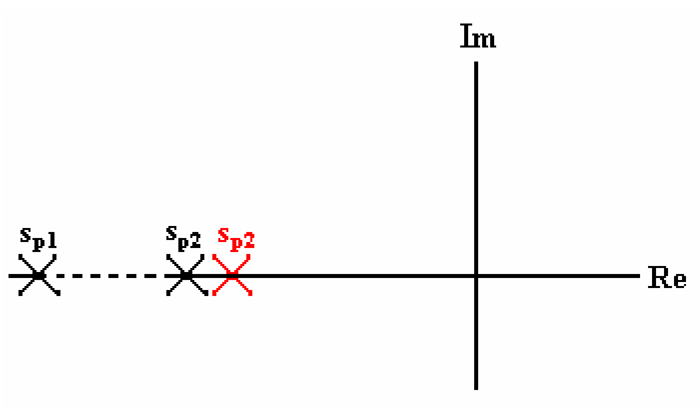
where $\omega_u=2\pi f_u$

s_{p1}=--9.99e6 and s_{p2}=--6293.27

with $\omega_u=\infty$

$s_{p1}=\infty$ and s_{p2}=-6289.31

A sketch of the effect of the unity-gain frequency on the position of the poles is shown below:



Note: the other pole is at ∞

Problem 35.5 solution

Jake Anderson
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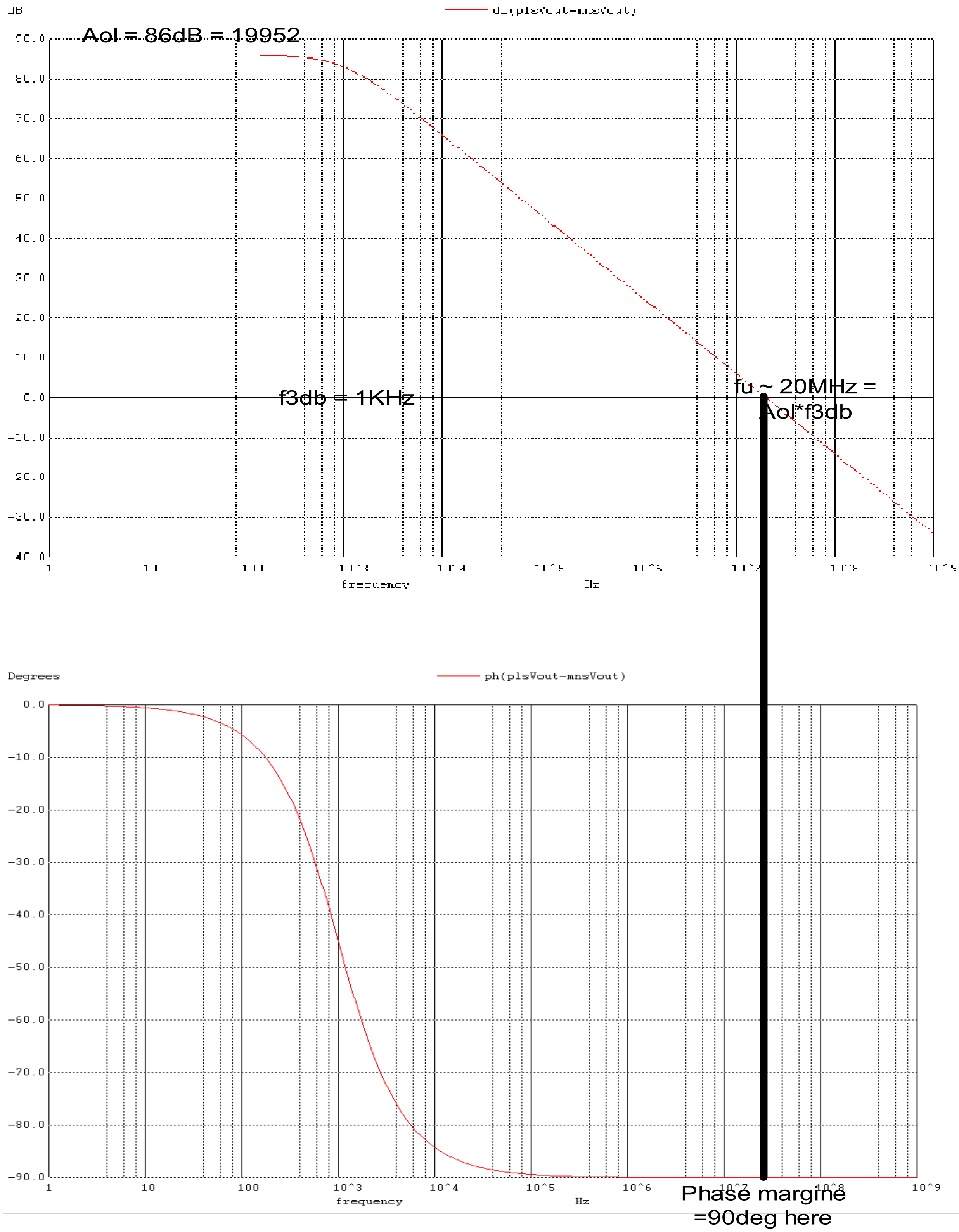
Regenerate Figure 34.21 of the last chapter using SPICE and the op-amp model shown in Figure 35.8

The netlist for Figure 35.8 is shown below:
Note that the Circuit still works with out the feedback resistors, but is to more realistic to have them in.

```
*Netlist for Problem 35.5
* Netlist for Figure 35.8 pg 401 which is a SPICE model
* for a differential input/output op-amp with finite bandwidth
* that is set by the RC filter

*following are commands for the AC analysis and plots
* Note: Fig. 35.9.cir was a good example for learning
*      the correct commands for the AC analysis. It
*      also has in it a more compact netlist of the
*      same circuit.
.control
destroy all
run
set units=degrees
* -Here Vout = Vout+ - Vout- = plsVout - mnsVout
plot ph(mnsVout-plsVout)
plot db(mnsVout-plsVout)
.endc

.ac dec 100 1 100Meg

*Set Vin to 1V (Vin+ - Vin- = 1V)
Vin ViPls VCM DC 0 AC 0.5
Vina ViMns VCM DC 0 AC -0.5

*Feedback Resistors
Rftop plsVout ViMns 1e9
Rfbtm mnsVout ViPls 1e9
*VCVS for the op-amp input stage
E1 VoPls VCM ViPls ViMns 10000
E2 VCM VoMns ViPls ViMns 10000

*RC filter stage
XPls VoPls VbufferInPls 0 RCfilter
XMns VoMns VbufferInMns 0 RCfilter

*Buffer Stage
XPlsBuffer VbufferInPls plsVout Buffer
XMnsBuffer VbufferInMns mnsVout Buffer
*Power Supplies
VCM VCM 0 DC 1.5v AC 0 0


*RC Filter subckt for RC/2pi = 1KHZ
.SUBCKT RCfilter in out btm
R1 in out 1K
C1 out btm 159e-9
.ENDS RCfilter

*Buffer subckt using VCVS
.SUBCKT Buffer in out
Ebuffer out 0 in 0 1
.ENDS Buffer
```

The plots for the above ckt are on the next page. Notice that there is not a 40db/Decade fall off because this model of an op-amp doesn’t have any circuit components to cause it in simulation. It is still a ‘fake’ op-amp, but it does model Aol, f3db, fu, and proper Phase Margine for the useful range of operation of the op-amp.

Problem 35.5 continued



Solution: 35.6

Anti alising filter should not limit the SNR of data converter, so SNR of anti alising filter should be greater than SNR of data converter. Beside filter, data converter has other noise sources, due to non-idealities of components used.

SNR of data converter = 6.02N +1.76 dB
(where quantization noise = $V_{LSB}/\sqrt{12}$)

if noise performance is dominated by thermal noise, in this case:
SNR of anti alising filter = $20\log 10 \, {}^{Vdd/2\sqrt{2}}\!\big/_{\sqrt{KT/C}}$
where, T=temperature
and K=Boltzman's Constant =$1.38*10^{-23}$ J/K

SNR (filter) > SNR (data converter)

Choosing T=298K

$$20\log_{10}(8.27*10^{9}\sqrt{C}) > 6.02*12+1.76 \text{ dB}$$
$$C>367.3 \text{ fF}$$

Minimum value of integration capacitor should be much higher than 367.3fF.

Solution for 35.7 by Sugato Mukherjee e-mail:msugato@ieee.org

Q: Repeat problem 35.6 if the op-amp used in the filter has a linear output swing of 80% of the power supply voltage.
Ans: Assuming that the noise performance of the filter is dominated by thermal noise, the filter SNR is given by

$$SNR(filter) = 20\log_{10}\frac{0.8\times\frac{Vdd}{2\sqrt{2}}}{\sqrt{\frac{kT}{C}}} \text{ (from equation 35.23)}$$

where C=value of integration capacitor
Vdd=1.5V
k=Boltzman's constant= $1.38X10^{-23}$ J/K
T=temperature =298K
Putting these values in the above equation, we get

$$SNR(filter) = 20\log_{10}(6.616\times10^{9}\times\sqrt{C})$$

Now the SNR for a 12 bit data converter considering ideal behavior is given by SNR(ADC-12bit)=6.02X12 +1.76 (using equation 28.27 and assuming that the quantization noise is given by $\frac{V_{LSB}}{\sqrt{12}}$ i.e no oversampling)
SNR(ADC-12 bit)=74dB
Now, $SNR(filter) \geq SNR(ADC)$
$\therefore 20\log_{10}(6.616\times10^{9}\times\sqrt{C}) \geq 74$
which gives $C \geq 573.9\,fF$
Since we do not want the anti-aliasing filter SNR to limit the SNR of our data converter(which has other non-idealities associated with it), practical choice of C must be much higher than the minimum value of 573.9fF.

Solution by:
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Problem 35.8

Show using the topology shown in Fig. 33.22 (and the same SPICE models), how using the two MOSFETs linearizes the change in resistance with VDS.

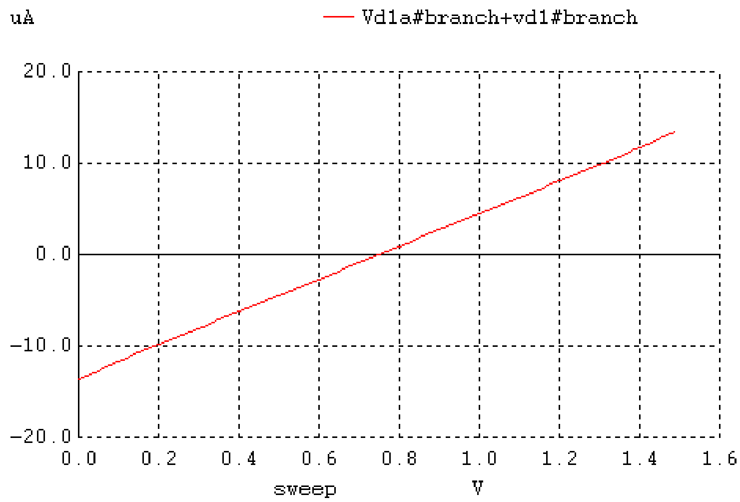
Solution:

First of all, refer to the topology in Fig. 33.22. For this simulation, I tied the sources of both MOSFETs to Vcm=0.75V. I then swept the drain voltage of the first MOSFET from 0 to 1.5 volts. I attached a VCVS (Eda) to the other MOSFET, and set the gain such that the drain of the second MOSFET was swept from 1.5 down to 0 volts. The netlist for this simulation is shown below.

```
M1  Vd1  Vg VCM 0 nmos W=5 L=100
M1a Vd1a Vg VCM 0 nmos W=5 L=100

Vg   Vg   0   DC 2
Vd   Vd   0   DC 1.5
VCM  VCM  0   DC 0.75
Vd1  Vd   Vd1 DC 0
Vd1a Vd1a Vda DC 1.5
Eda  Vda 0 0 Vd 1

.DC Vd 0.5 1 0.01

.control
destroy all
run
let RDS1=1/deriv(Vd1#branch+Vd1a#branch)
let RDS11=1/deriv(vd1#branch)
plot RDS1 RDS11
plot Vd1a#branch+vd1#branch
.endc
```

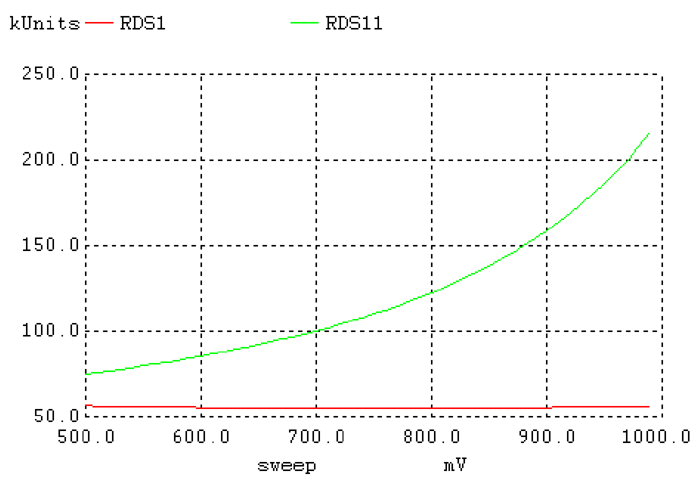
Notice that the voltage across the first MOSFET is being swept from –0.75V to 0.75 volts, while the voltage across the second MOSFET is being swept from 0.75 to –0.75 volts. For this simulation, notice that I set the gate voltage to 2 volts for this simulation, which could be increased to increase the linearity of the current through the set of MOSFETs. I picked this value because it was large enough to keep the MOSFETs always operating in the triode region. For a discussion of why this topology is used, see the discussion on MOSFET-C integrators in the textbook.

When I ran this simulation, I summed the currents through the two MOSFETs and the result is plotted below.



(Note: The voltage at the bottom for 0-1.5V corresponds to VDS= -0.75 to 0.75V.)

This graph shows that over this range of VGS, the current change is almost exactly linear. This equivalent resistance is the reciprocal of the derivative of the current through the MOSFETs. Since the current through the MOSFETs is essentially linear, this means that the resistance of the MOSFETs will be essentially constant, with a value of 1/(slope of IV graph above). I plotted the equivalent resistance of the single MOSFET together with the resistance of the MOSFET pair on the graph below to compare the two.



Over the range from 500mV to 1V, the resistance is essentially constant at 55kohms, which is what we want in order to minimize distortion.

Problem 35.9

Repeat Ex. 35.4 using a MOSFET-C filter. Use the MOSEFET SPICE model given in Ch. 33. After performing the AC simulations, try a transient simulation with an input sinusoid at 1MHz. Show how the output of the filter becomes distorted as the amplitude of the input signal increases. Determine the filters SNDR when the input signal has a frequency of 1MHz and an amplitude of VDD peak to peak.

As in Ex. 35.4, the op-amp's DC gain is set to 10,000, f_u set to 10 MHz and F_{3dB} is 1kHz. The circuit shown below is the Spice model used to simulate an op-amp with finite f_u.

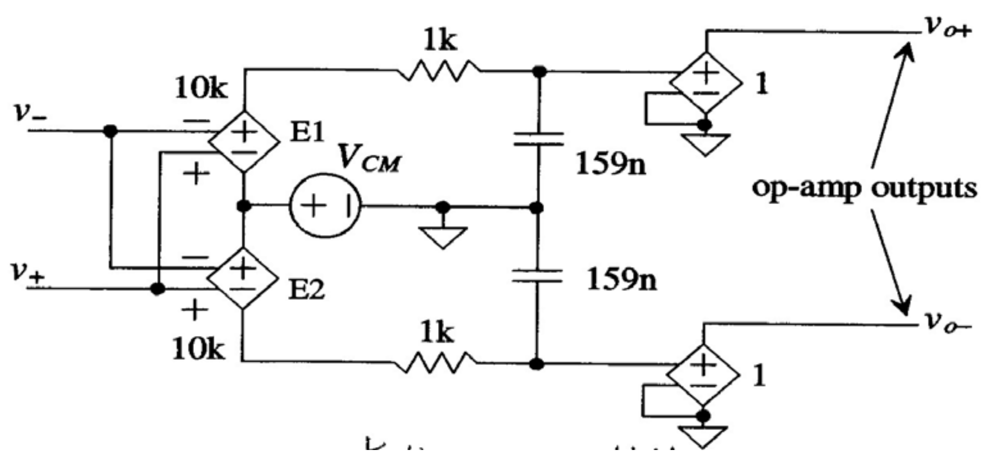


Fig1. SPICE modeling of a differential op-amp with finite bandwidth.

The MOSFET-C integrator is used here. Four long length transistors operated in the triode region replace the R_I and R_F of the active-RC filter. EKV device model is selected for those NMOS transistors. The minimum length is 0.15u for the process the model represented.

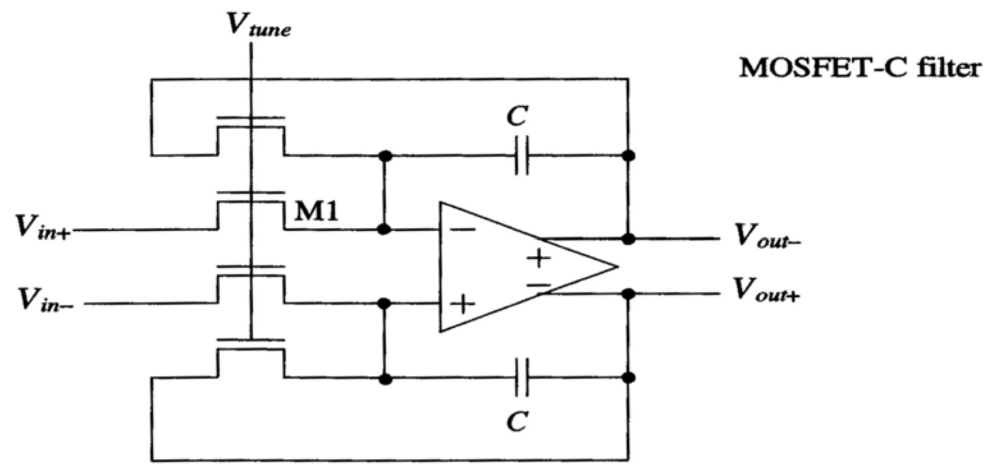
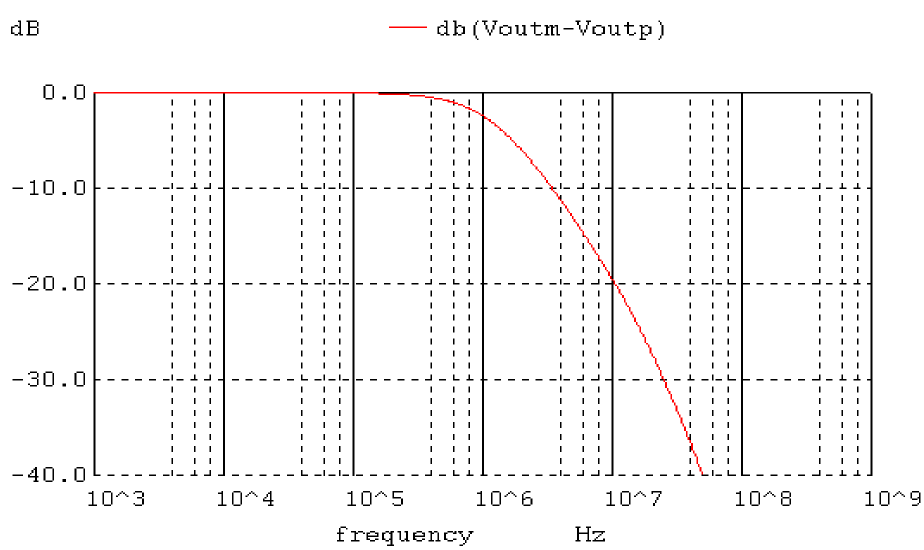


Fig2. A MOSFET-C filter.

AC SPICE Simulation

Fig.3 shows the magnitude and phase responses of the above MOSFET-C filter from the AC simulation. The f_{3dB} is slightly over 1 MHz with Vtune = 0.6V. The f_{3dB} of the filter could be easily adjusted by tuning the Vtune upwards or downwards. The magnitude response also shows that at 10 MHz, the response transitions to 40 dB/decade from the initial 20 dB/decade due to the effect of op-amp's closed-loop pole at this frequency.



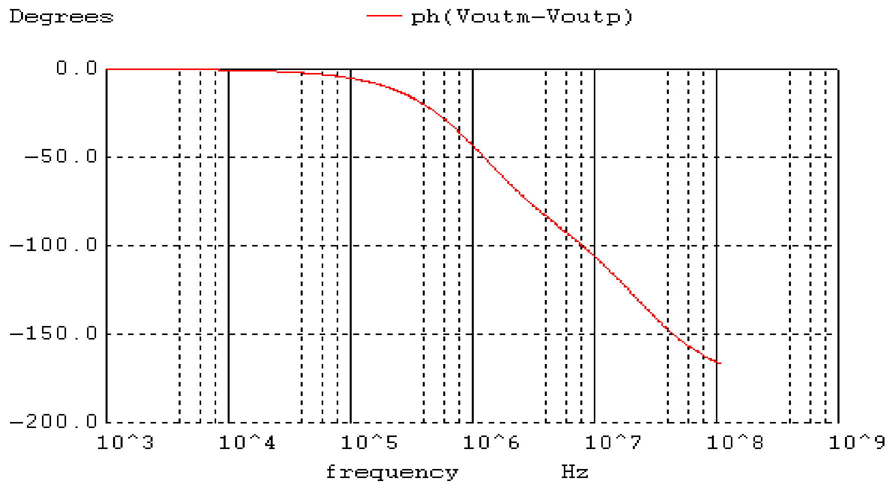
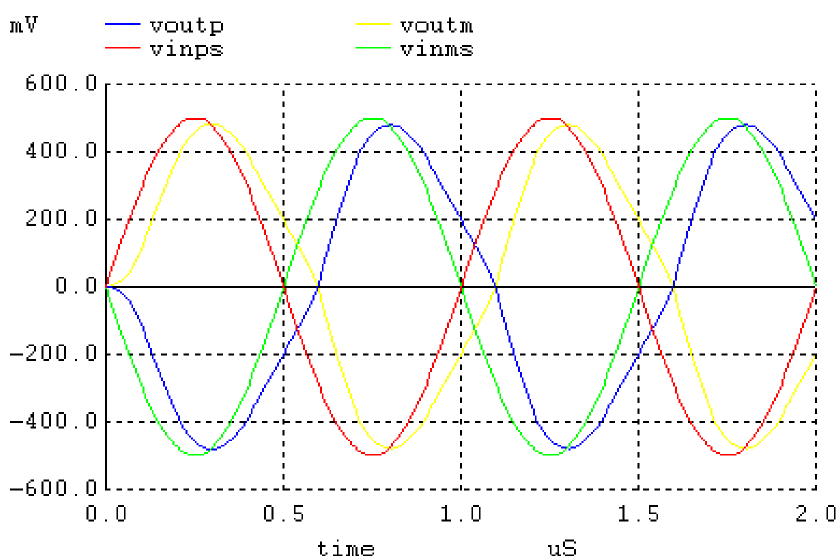


Fig3. The magnitude and phrase responses of the MOSFET-C filter.

Transient SPICE Simulation

Fig.4 shows transient simulation results of a 0.5V and a 1V sinewaves applied to the filter at 1 MHz. The output of the filter is starting to decrease as 1 MHz is approaching the 3 dB frequency of the filter. The output of the filter also becomes distorted as the amplitude of the input signal increases (from 0.5V to 1V).



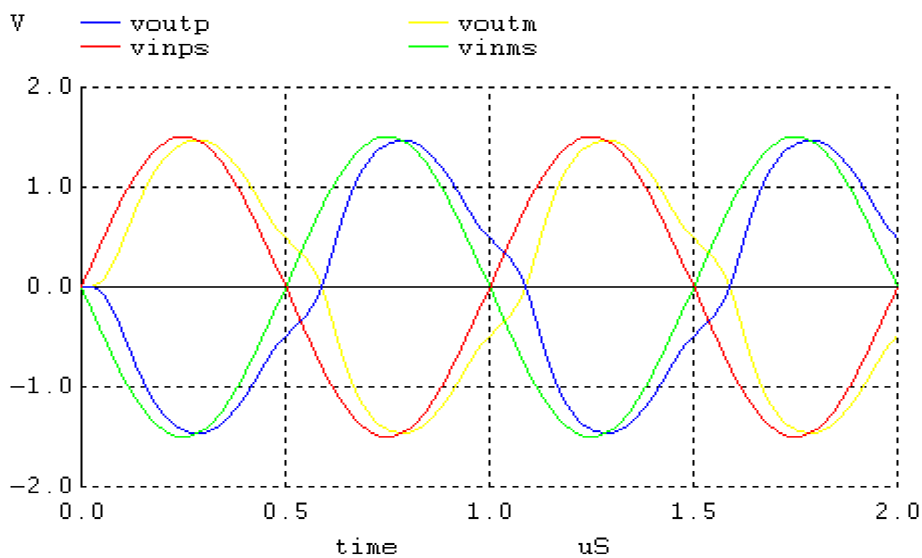


Fig4. The transient simulation results of the MOSFET-C filter.

Determine the filter's SNDR

The signal-to-noise plus distortion ratio is defined as

$$SNDR = 20\log\frac{V_p/\sqrt{2}}{V_{Qe+D,RMS}}$$

Where $V_{Qe,RMS}$ is the RMS quantization noise voltage from an output spectrum. To calculate this value, we sum the mean-squared contribution from each component (after removing the input tone from the spectrum) and then take the square root of the results.

$$V_{Qe+D,RMS} = \frac{1}{\sqrt{2}}\sqrt{\sum_{k=0}^{M-1} V_{DFT}^2(k \cdot f_{RES})}$$

The *spec* command (spectral analysis command) in SPICE is used to take the DFT (discrete Fourier Transform) of Vout over a frequency rang (from 0 to 5 MHz in this simulation). The voltage spectrum for the output of the filter is shown in Fig 5. The SNDR from the SPICE simulation is 3.1727e+2 dB which is small because of the nonlinear property of the MOFET resistors. The major benefit of the MOSFET-C filter over the active–RC filter is its ability to tune.

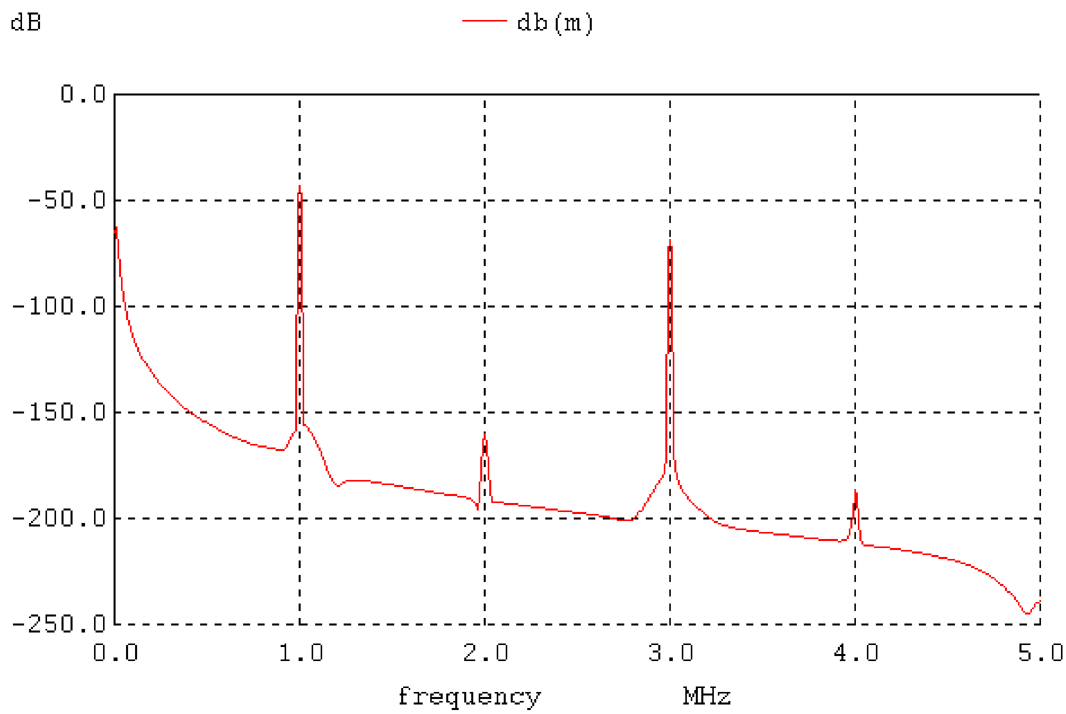


Fig5. The output noise spectrum of the MOSFET-C filter.

SPICE Simulation Netlist for AC and Transient Simulation

```
.control
destroy all
run
set units=degrees
*plot ph(Voutm-Voutp)
*plot db(Voutm-Voutp) ylimit 0 -40
plot  vinps vinms voutp voutm
*let vout=voutp-voutm
*plot vout
.endc

*.ac dec 100 1k 100MEG
.tran .01u 2u UIC

.options reltol=0.1 vntol=1m abstol=1u

*VCM VCM 0 DC 0.75
VCM VCM 0 DC 0
Vtune Vtune 0 DC 0.6
vbb vbb 0 DC -0.5

*Set Vin to 1V (Vin+ - Vin- = 1V)
Vin     Vinps   VCM   DC   0  AC  0.5    SIN 0  0.5  1000k
Vina    Vinms   VCM   DC   0  AC  -0.5   SIN 0  -0.5 1000k

Mftop Voutp Vtune  Vinm  vbb   NMOS  L=5u W=10u
Mitop Vinps Vtune  Vinm  vbb   NMOS  L=5u W=10u
Mibot Vinms Vtune  Vinp  vbb   NMOS  L=5u W=10u
Mfbot Voutm Vtune  Vinp  vbb   NMOS  L=5u W=10u

Cfp Voutp Vinm   5p
Cfm Voutm Vinp   5p

*Use a VCVS for the op-amp
E1 Voutpp VCM Vinp Vinm 10k
E2 VCM Voutmm Vinp Vinm 10k
E3 Voutp 0 Voutppc 0 1
E4 Voutm 0 Voutmmc 0 1
Rpp Voutpp Voutppc 1k
Rmm Voutmm Voutmmc 1k
Cpp Voutppc 0 159n
Cmm Voutmmc 0 159n


.MODEL nmos nmos
.
.
.
.end
```

SPICE Simulation Netlist for Determining the filter's SNDR

```
.control
destroy all
run
set units=degrees
* Here Vout = Vout+ - Vout- = Voutm - Voutp

*plot ph(Voutm-Voutp)
*plot db(Voutm-Voutp) ylimit 0 -40
*plot  vinps vinms voutp voutm
let vout=voutp-voutm
*plot vout
linearize vout
spec 0 5MEG 10k  vout
let m=mag(vout)
plot db(m)

let m[0]=0
let m[100]=0

let noise=0.707*sqrt(mean(m*m)*length(m))
let sndr=db(0.5*1.414/noise)
print noise
print sndr
print length(m)
.endc

*.ac dec 100 1k 100MEG
.tran .1u .1m UIC

.options reltol=0.1 vntol=1m abstol=1u

*VCM VCM 0 DC 0.75
VCM VCM 0 DC 0
Vtune Vtune 0 DC 0.25
vbb vbb 0 DC -0.5

*Set Vin to 1V (Vin+ - Vin- = 1V)
Vin     Vinps   VCM   DC    0  AC  0  0    SIN 0  0.5  1000k
Vina    Vinms   VCM   DC    0  AC  0  0    SIN 0  -0.5 1000k

*Rftop Voutp Vinm 10k
*Ritop Vinps Vinm 10k
*Rfbot Voutm Vinp 10k
Mftop Voutp Vtune  Vinm  vbb   NMOS  L=5u W=10u
Mitop Vinps Vtune  Vinm  vbb   NMOS  L=5u W=10u
Mibot Vinms Vtune  Vinp  vbb   NMOS  L=5u W=10u
Mfbot Voutm Vtune  Vinp  vbb   NMOS  L=5u W=10u

Cfp Voutp Vinm   5p
Cfm Voutm Vinp  5p


*Use a VCVS for the op-amp
```

```
E1 Voutpp VCM Vinp Vinm 10k
E2 VCM Voutmm Vinp Vinm 10k
E3 Voutp 0 Voutppc 0 1
E4 Voutm 0 Voutmmc 0 1
Rpp Voutpp Voutppc 1k
Rmm Voutmm Voutmmc 1k
Cpp Voutppc 0 159n
Cmm Voutmmc 0 159n


.MODEL nmos nmos
.
.
.
.end
```

<u>EKV device model used in the simulation</u>

```
.MODEL nmos nmos
+ LEVEL=44
*** Setup Parameters
+ UPDATE=2.6
*** Process Related Model Parameters
+ COX=9.083E-3 XJ=0.15E-6
*** Intrinsic Model Parameters
+ VTO=0.4 GAMMA=0.71 PHI=0.97 KP=453E-6
+ E0=88.0E6 UCRIT=4.0E6
+ DL=-0.05E-6 DW=-0.02E-6
+ LAMBDA = 0.30 LETA=0.28 WETA=0
+ Q0=280E-6 LK=0.5E-6
*** Substrate Current Parameters
+ IBN=1.0 IBA=200E6 IBB=350E6
*** Intrinsic Model Temperature Parameters
+ TNOM=27.0 TCV=1.5E-3 BEX=-1.5 UCEX=1.7 IBBT=0
*** 1/f Noise Model Parameters
+ KF=1E-27 AF=1
*** Series Resistance and Area Calulation Parameters
+ HDIF=0.24e-6 ACM=3 RSH=5.0 RS=1250.526
+ RD=1250.526 LDIF=0.07e-6
*** Junction Current Parameters
+ JS=1.0E-6 JSW=5.0E-11 XTI=0 N=1.5
*** Junction Capacitances Parameters
+ CJ=1.0E-3 CJSW=2.0E-10 CJGATE=5.0E-10
+ MJ=0.5 MJSW=0.3 PB=0.9 PBSW=0.9 FC=0.5
*** Gate Overlap Capacitances
+ CGSO=3.0E-10 CGDO=3.0E-10 CGBO=3.0E-11
.end
```

EE515 -CMOS Mixed Signal IC Design -- Yantao Ma
-- yantaoma@rocketmail.com

Chapter 35.10 Derive the transfer function for the filter shown in fig35.16 if the transconductanctors have different gm. Sketch the block diagram, similar to the one seen in fig 35.6, for the filter?

[Answer]: If the transconductors have different gm, like gm1 and gm2 as shown in the following figure, we can sum the output current of 1st transconductor with that from 2nd one to generate the net output current through capacitor C.

$$g_{m1}(Vin+ - Vin-) - g_{m2}(Vout+ - Vout-) = j\omega C(Vout+ - Vout-)$$

or transfer function as following:

$$\frac{Vout+ - Vout-}{Vin+ - Vin-} = \frac{g_{m1}}{g_{m2} + j\omega C} = \frac{g_{m1}/g_{m2}}{1 + j\omega C/g_{m2}} = \frac{1/G_2}{1 + s/G_1G_2}$$

Where, $G_1 = g_{m1}/C = 1/(C/g_{m1})$, $G_2 = g_{m2}/g_{m1} = (1/g_{m1})/(1/g_{m2})$, $f3dB = G_1G_2/(2\pi)$

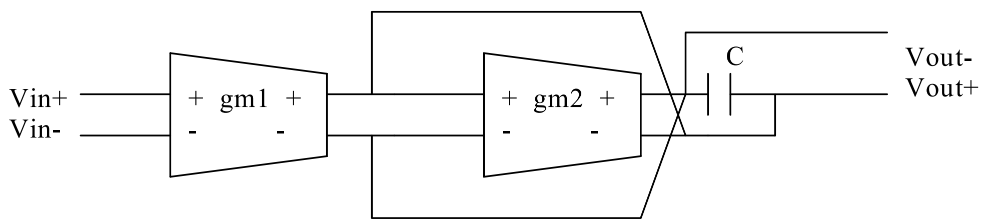


Figure 35.16 Implementing a first-order filter using transconductors

The block diagram, similar to the one seen in fig 35.6, for the filter is shown as following

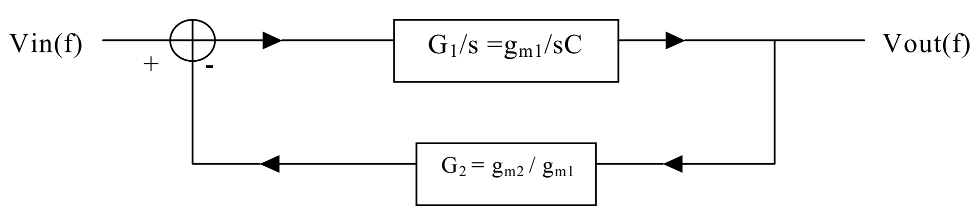


Figure 2. Block diagram for the first-order filter using transconductors

-- Yantao Ma
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Chapter 35.11

Derive the transfer function for the following first-order transconductor filter.

[Answer]: Assume all these three transconductors have different gm's, defined as gm_1 gm_2 and gm_3 as shown in the figure below:

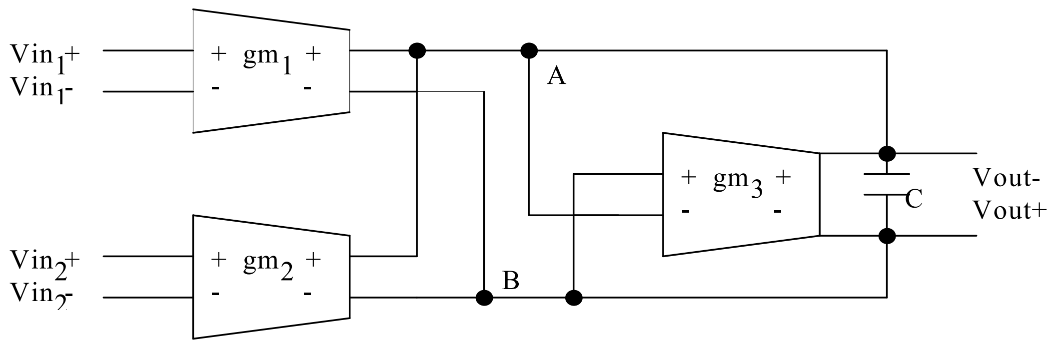

Figure 35.74 A first-order filter with two input transconductors

Define: $Vin1 = Vin_{1+} - Vin_1-$ $\quad$ $Vin2 = Vin_{2+} - Vin_2-$ $\quad$ $V_{out} = V_{out+} - V_{out}-$

As we know, the output of a single transcondutor is defined as gm (Vin_+ -Vin-).
By deploying Kirchhoff's Current Law (KCL) at either node A or B, we can easily obtain:

$$g_{m1}(Vin_{1+} - Vin_1-) + g_{m2}(Vin_{2+} - Vin_2-) - g_{m3}(V_{out+} - V_{out}-) = j\omega C(V_{out+} - V_{out}-) \rightarrow$$

Therefore, the Transfer equation for a first-order two-input filter can be stated as:

$$V_{out}(g_{m3} + j\omega C) = g_{m1} Vin_1 + g_{m2} Vin_2$$

Transfer function can be further simplified as following if $Vin_1 = Vin_2 = Vin$:

$$\frac{Vout}{Vin} = \frac{g_{m1} + g_{m2}}{g_{m3} + j\omega C} = \frac{g_{m1}/g_{m3} + g_{m2}/g_{m3}}{1 + j\omega C/g_{m3}}$$

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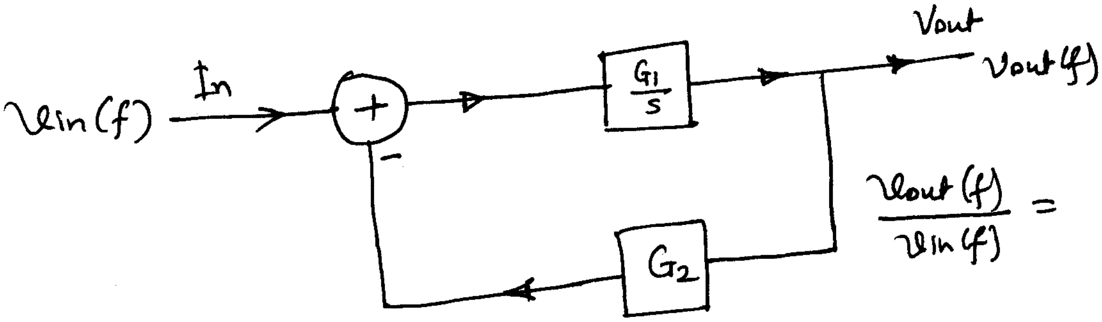
Solution of 35.12 by Pandurang K. Irkar

Prob 35.12 show the derivation details that result in equations. (35.44) and (35.46)

Soln : The general implementation of a lowpass first order filter.



$$\frac{v_{out}(f)}{v_{in}(f)} = \frac{1/G_2}{1 + s/G_1G_2}$$

The schematic diagram of a Discrete Analog Integrator (DAI)
(Ref. 31.78)

Basically ~~To be~~ begin with the output of the DAI is connected to the OPAMP through ϕ_1 switch. When the ϕ_1 switches are closed (ϕ_1 is high) at n-1 → swithes shut off), the charge stored on C_I is

$$Q_1 = C_I\left(V_{cm} - V_1[(n-1)T_s]\right) \quad — ①$$

When ϕ_2 switches turn on the charge stored on C_I becomes

$$Q_2 = C_I\left(V_{cm} - V_2\left[(n-\tfrac{1}{2})T_s\right]\right) \quad — ②$$

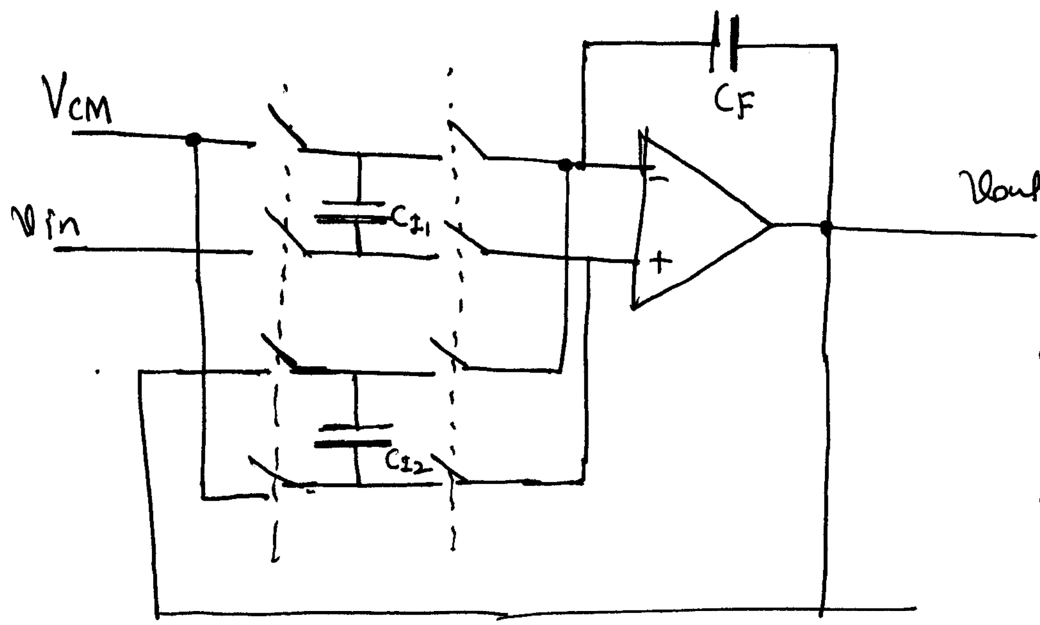
The difference ~~#~~ in these charges, $Q_2 - Q_1$ → Resulting in output voltage change. This change can be written as

$$\left(v_{out}[nT_s] - v_{out}[(n-1)T_s]\right)C_F = C_I\left(V_1[(n-1)T_s] - V_2[(n-1/2)]T_s\right) \quad — ③$$

Writing in Z-domain results in

$$v_{out}(z)\left(1-z^{-1}\right) = \frac{C_I}{C_F}\left(v_1(z)\cdot z^{-1} - v_2(z)z^{-1/2}\right) \quad ④$$

Depending upon the output connected to ϕ_1 or ϕ_2; we have different topologies. and one of them is as shown in following fig.



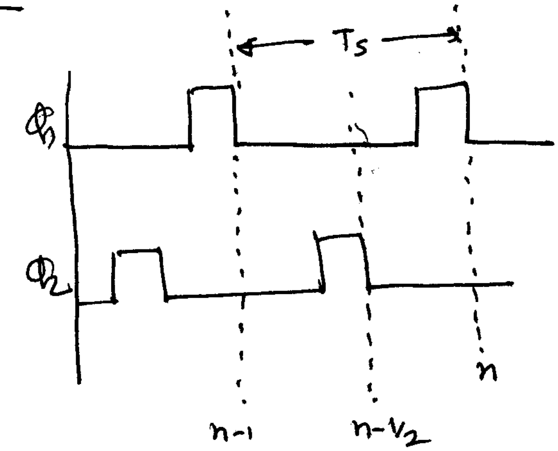


fig ②

Similarly as above procedure we can write the equation

for the ~~abv~~ fig. 2. topology

Begin with ϕ_1 and at n-1 shutting off, we can write

~~Charges~~

$$Q_1 = C_{I_1}\left(V_{CM} - V_{in}\left[(n+\tfrac{1}{2})T_s\right]\right) \quad —①$$

with ~~ϕ_2~~ C_{I_2}

$$\phi_1' = C_{I_2}\left(V_{out}(n\cancel{+\tfrac{1}{2}})T_s - V_{CM}\right) \quad —②$$

The output change across the feed back capacitor is

$$\left(V_{out}\left[(nT_s)\right] - V_{out}\left[(n-1)T_s\right]\right)C_F = C_{I_1}\left(V_{CM} - V_{in}\left((n+\tfrac{1}{2})T_s\right)\right)$$
$$- C_{I_2}\left(V_{out}(n\cancel{+\tfrac{1}{2}})T_s - V_{CM}\right)$$

writing into z domain

$$V_{out}(z) = \frac{z^{-1}}{1-z^{-1}}$$

$$V_{out}(z)\,(1-z^{-1})C_F = C_{I1}\left(V_{in}(z)z^{1/2}\right) - C_{I2}\left(V_{out}(z)\,\cancel{z^{-1}}\right)$$

$$V_{out}(z) = \frac{z^{-1}}{1-z^{-1}} \cdot \left[\frac{C_{I1}}{C_F} \cdot V_{in}(z) \cdot z^{1/2} - \frac{C_{I2}}{C_F} \cdot V_{out}(z)\right]$$

With this equation we can write for general block diagram

$$G_1 = \frac{C_{I1}}{C_F} \cdot f_s \quad \text{and} \quad G_2 = \frac{C_{I2}}{C_f} \cdot f_s \cdot \frac{1}{G_1} = \frac{C_{I2}}{C_{I1}}$$

$$f_{3dB} = \frac{G_1 G_2}{2\pi}$$

P. K. IRKAR

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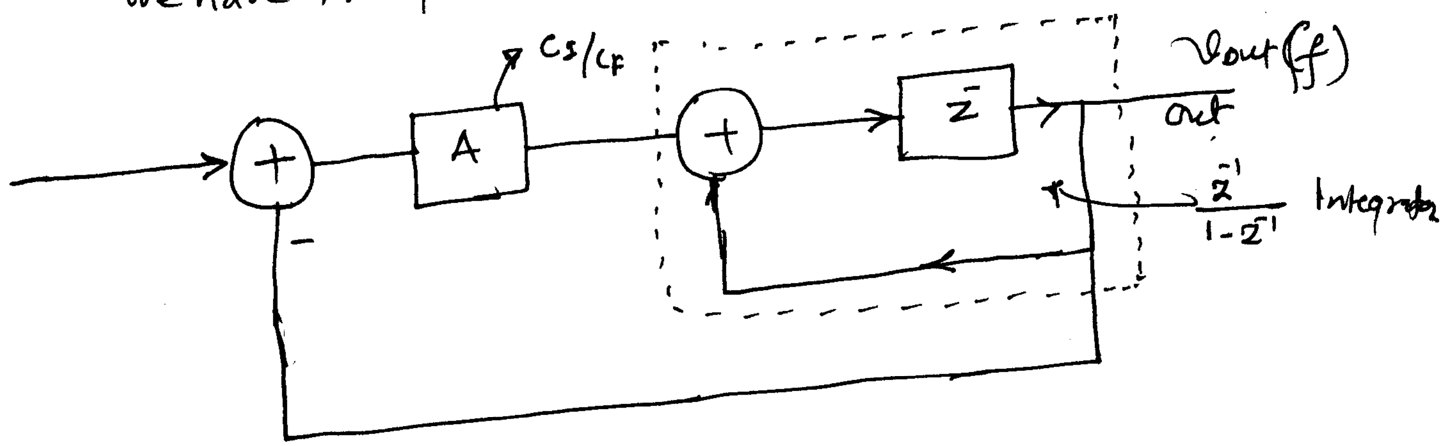
Q. 35.13 From the derivation of eq. (35.48) what ~~wh~~ would happen if we repeated Ex. 35.6 with an ~~p~~ input frequency of 101.59 MHz

Soln: The derived eqn 35.48 is as follows:

$$\frac{V_{out}(f)}{V_{in}(f)} = \frac{A z^{-1}}{A z^{-1} + 1 - z^{-1}} = \frac{A}{z - (1 - A)}$$

We have ~~th~~ replaced ~~ration~~ of C_I/C_F with the variable A.

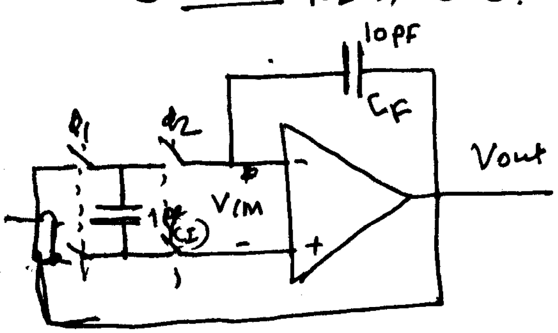


We can compare with Ex 35.6, ~~by assuming~~ f

Ex. 35.6 f_s = clock frequency = 100 MHz then

$$f_{3dB} = \frac{A \cdot f_s}{2\pi} \Rightarrow 1.59\ \text{MHz}$$

fig. 35.22 for Ex. 35.6.



With capacitance values and $R_{ee} \Rightarrow \frac{I_s}{C_I}$

$$f_{3dB} = 1.59\ \text{MHz}$$

$$A = \frac{1.59\ \text{MHz} \times 2\pi}{100\ \text{MHz}}$$

$$\boxed{A = 0.1}$$

Here in this ~~expemple~~ example if f_s, Clock frequency = 101.59 MHz.
assuming
the and the cut of freq same 1.59 MHz

A becomes

$$A = \frac{1.59\,\text{MHz} \times 2\pi}{101.59\,\text{MHz}}$$

$$A = 0.009$$

We can write the magnitude response as

$$\left|\frac{v_{out}}{v_{in}}\right| = \frac{A}{\sqrt{\left(\cos 2\pi f/f_s - 1 + A\right)^2 + \sin^2 2\pi f/f_s}}$$

But if. ~~for~~ the ~~cut~~ clock frequency = 101.59 MHz

$$\text{The } R_{se} = \frac{T_s}{C_I} \Rightarrow \frac{0.0098 \times 10^{-6}}{1\,\text{pF}} = 0.0098 \times 10^{6}$$

$$f_{3db} = \frac{1}{2\pi R_{se} \times C} = \frac{1}{2\pi \times 0.0098 \times 10^{6} \times 10 \times 10^{-12}} = \cancel{0.0061 \times 10^{6}} = \underline{1.62 \times 10^{6}}$$

Hence the output 1.59 MHz will be slightly higher than the 1.62 MHz (actual cut off freqn). This is shown by simulation also.

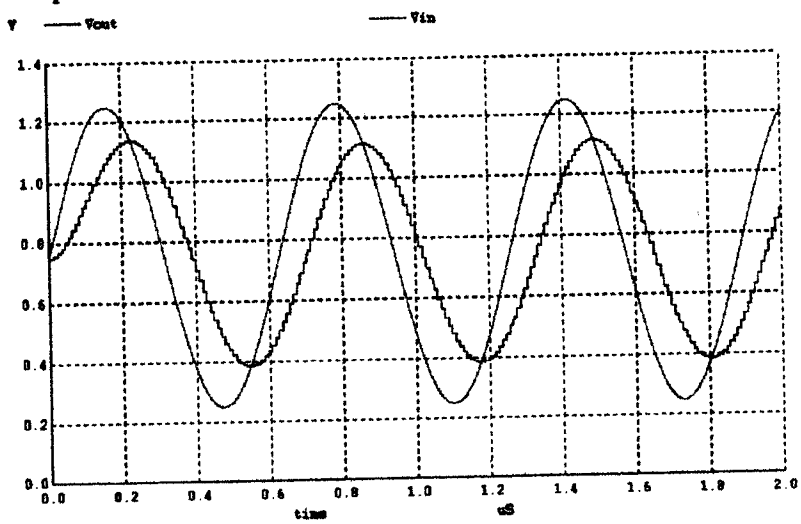
If I give the input 1.62×10^{6} the I expect the same output as to 35.6. ~~the~~ But the output is low approximately equal to 1.1 peak comparing to 1.3 in fig 35.6.

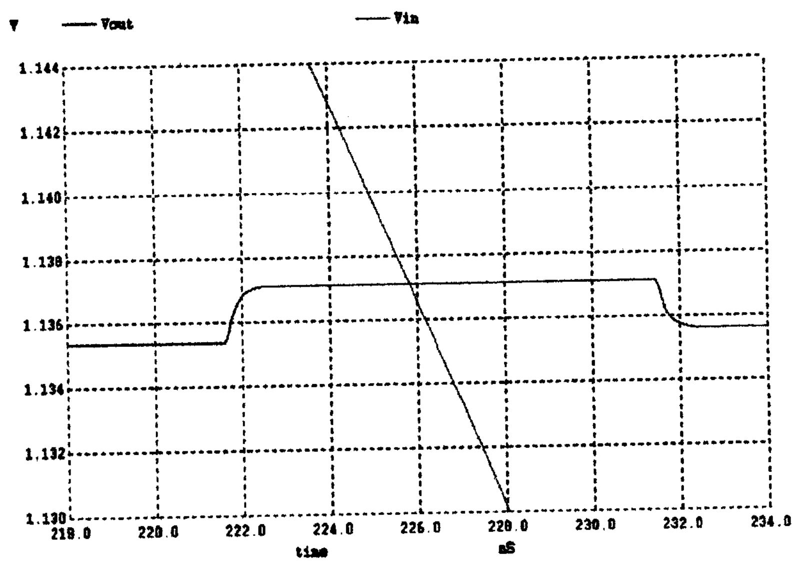
This is what the alising effect makes sense.

Repeatation of problem 35.6 with clock frequency 101.59MHz

```
.control
destroy all
run
plot Vout Vin
.endc


* Op-amp using VCVS
Eamp Vout 0 Vcom Vinm 100MEG


*Input power and references
Vswit Vswit 0 DC 0.75
Vcom Vcom 0 DC 0.75

*Input Signal
Vin   Vin   0 DC 0 Sin 0.75 .5 1.59MEG

*Clock Signals
Vphi1  phi1  0 DC 0  Pulse 0 1.5  0   200p  200p  4n 9.843n
Vphi2  phi2  0 DC 0  Pulse 0 1.5  5n  200p  200p  4n 9.843n
R2 phi1 0 1MEG
R3 phi2 0 1MEG

*switched capacitors
CI Vtop Vbot 1p
*load capacitor
CF Vout Vinm 10p

.tran 1n 2000n 0 1n UIC

*switches
S1 Vout  Vtop phi1 Vswit switmod
S2 Vin   Vbot phi1 Vswit switmod
S3 Vtop  Vinm phi2 Vswit switmod
S4 Vbot  Vcom phi2 Vswit switmod
.model switmod SW RON=100

.end
```

Output with 101.59MHz clock frequency



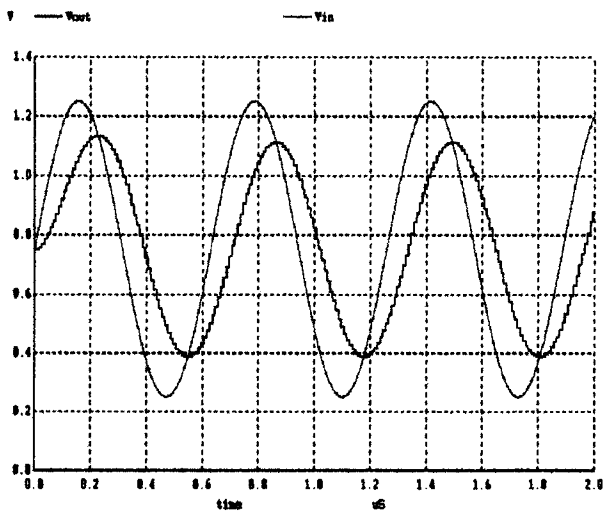


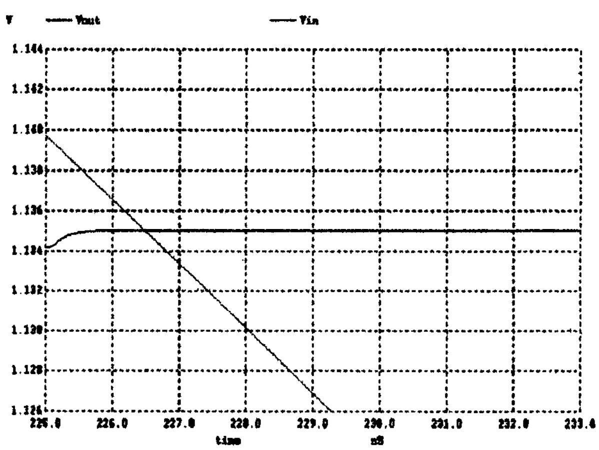
Close look at the peak voltage

Input freq^n = 1.59 MHz

peak vtg = 1.137

Output with 100 MHz clock frequency



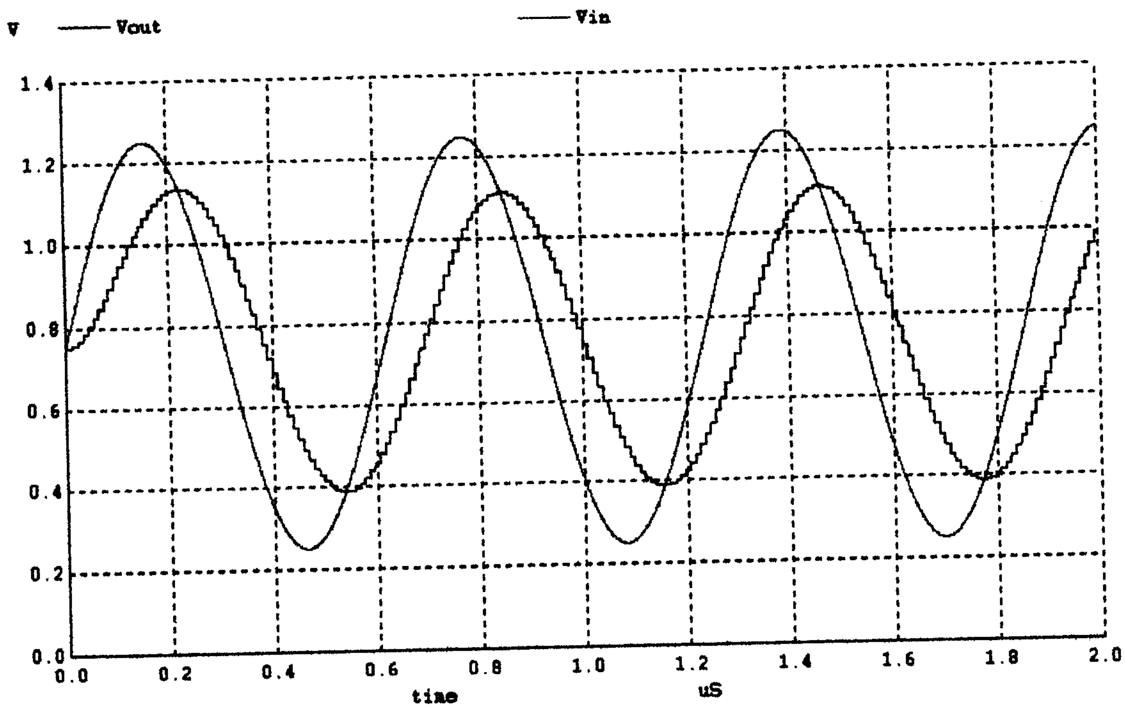


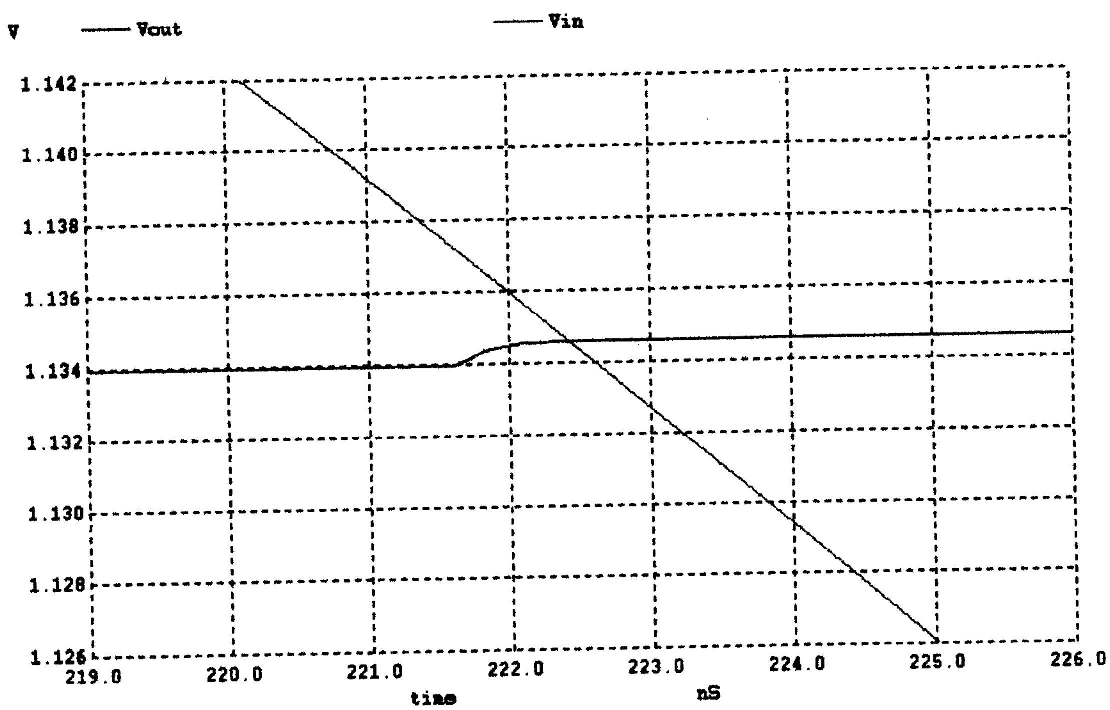
Close look at peak voltage

Input frequency = 1.59 MHz

peak vtg = 1.135

Output with input signal frequency 1.62MHz





Close look of peak voltage

peak Vtg = 1.1345 V.

Solution for 35.14 by Sugato Mukherjee e-mail:msugato@ieee.org

Q. Show that if the values of A and B are restricted to 1,0.5,0.25,0.125 etc that the circuit of Figure 35.75 can be used to implement multiplication by coefficients that aren't directly powers of two. How would a multiply by 0.75 be implemented? A multiply by 0.9375? A multiply by 0.5625?

Ans. If the values of A and B are restricted to 1,0.5,0.25,0.125 etc, multiplication by A and B can be simply implemented with a shifter. Eg. a multiply by 0.25 is achieved by two right shifts of the digital word. If we incorporate another adder block in the system, then we can achieve multiplication by values that are not powers of two with minimal hardware complexity. The hardware requirements are simply shift registers and adders. Let us now mathematically examine how this is possible.

Looking at Figure 35.75, we see that Out = (A-B) In

Then if we choose A=1 (no shift) and B=0.25 (two right shifts), then Out = 0.75 In. Thus we have achieved a multiplication by 0.75.

For multiplying by 0.9375 we observe that 0.9375 = 1 - 0.0625.

Now 0.0625 = $(2)^{-4}$ So setting A=1(no shift) and B=0.0625(4 right shifts) achieves multiplication by 0.9375.

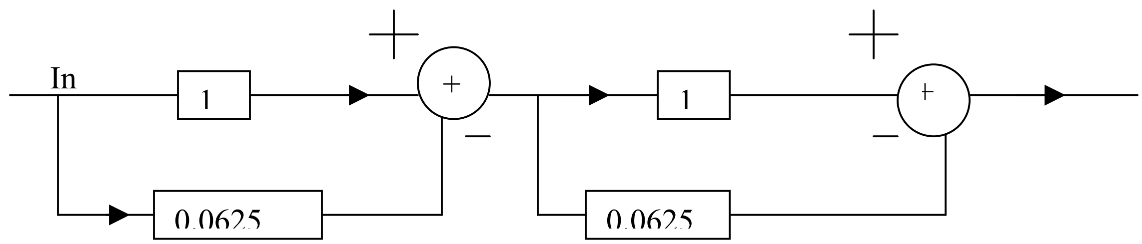
For multiplying with 0.5625, we observe that 0.5625 = $(0.75)^2$. So we can cascade two multipliers each with a multiplying factor of 0.75 to achieve the desired result. Also realizing that binary subtraction is addition of 2's complement numbers, we see that the block diagram of Figure 35.75 need not be restricted to subtractions only. Subtraction can be converted to addition by setting the carry bit of the first (least significant) stage = 0 (instead of 1 needed to convert a number to 2's complement for subtraction purpose) and not logically inverting the B input to the adder (inversion needed to convert the digital representation of B into 2's complement for subtracting purpose). All we have added to the circuit hardware are some two-input multiplexers which are controlled by a signal which decides whether we add B to A or subtract B from A. So if we have Out=(A+B)In then we can say that 0.5625= 0.5+0.0625=$(2)^{-1}$ + $(2)^{-4}$. So choosing A=0.5 and B=0.0625 achieves multiplication by 0.5625.

Solution: 35.15:

- Multiply by 0.8789

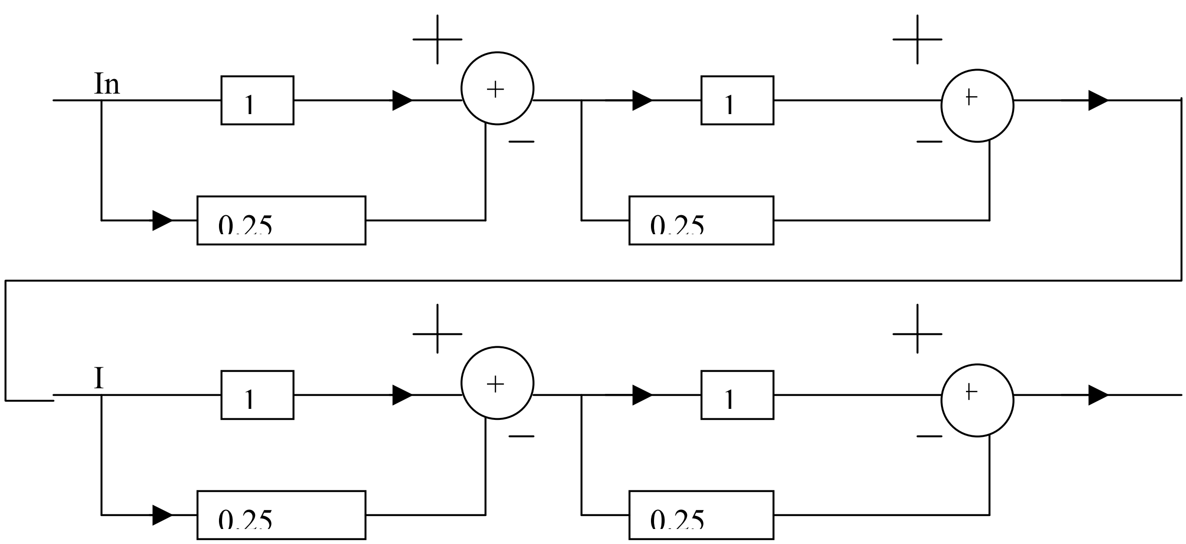
From figure 37.75 (of problem 35.14) Given A and B are restricted to 0.5, 0.25, 0.125 ….
(Implemented with shift registers)

Choosing A=1 and B=0.0625
A-B=0.9375
And $(A-B)^2$=0.8789
So by cascading two multipliers we could get multiplication by 0.8789



- Multiply by 0.3164

If A=1, and B=0.25
A-B=0.75
And $(A-B)^4$=0.3164



Problem 35.16

Jake Anderson
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Show the details of how the gains, G's, are derived in Fig. 35.30

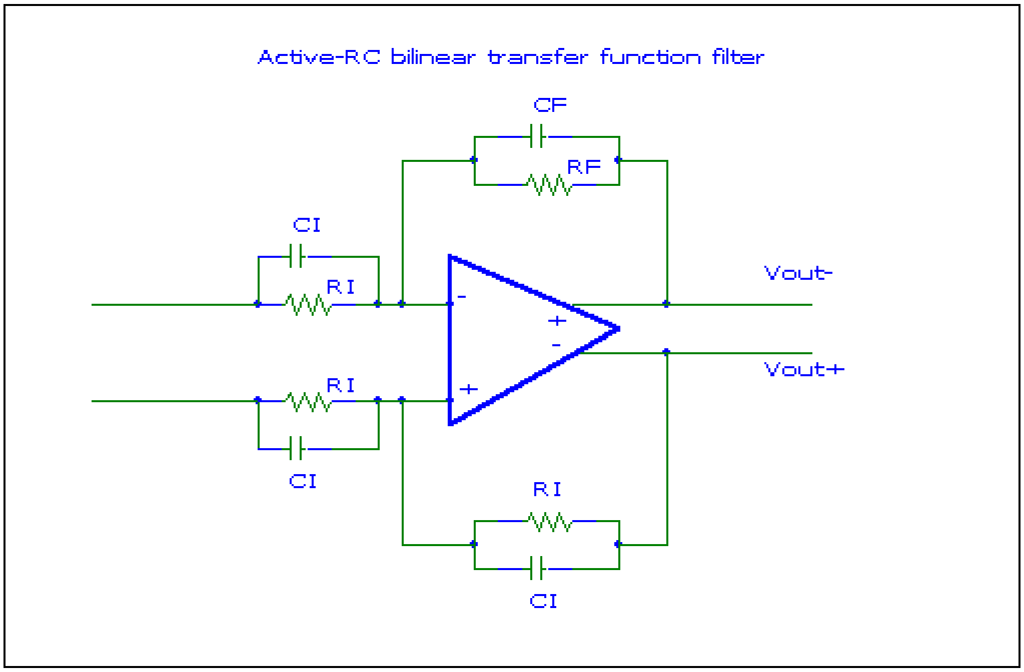

Figure 35.30

It is easier to derive the gains using a single-ended topology shown below.

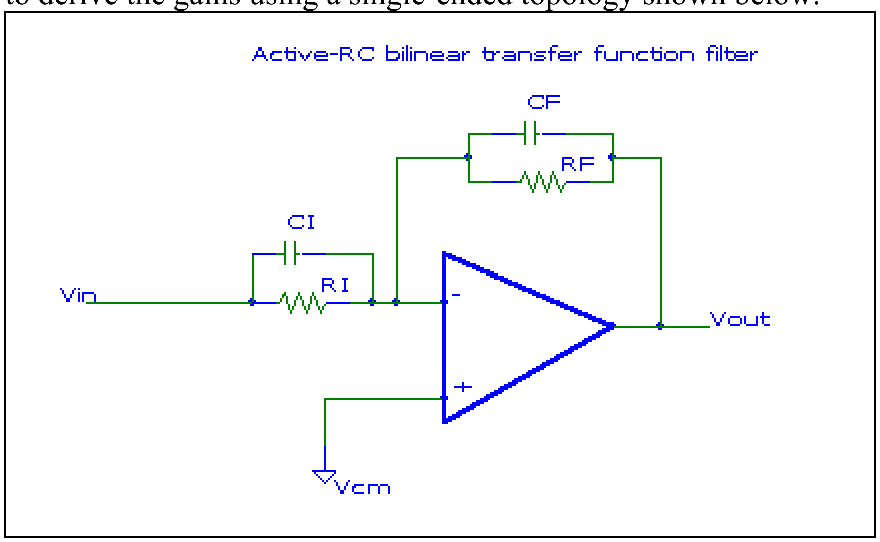

Figure1

$$Z_{in} = R_I \,//\, X_I = \frac{R_I}{1 + sR_I C_I} \qquad\qquad Z_{Feedback} = Z_F = R_F \,//\, X_F = \frac{R_F}{1 + sR_F C_F}$$

The Vout in Figure 1 is actually –Vout.
The input current and the feedback current are equal so that

$$\frac{V_{in}}{Z_{in}} = \frac{V_{out}}{Z_F}$$

$$\frac{V_{out}}{V_{in}} = \frac{Z_F}{Z_{in}} = \left(\frac{R_F}{1+sR_F C_F}\right)\left(\frac{1+sR_I C_I}{R_I}\right) = \frac{R_F}{R_I}\frac{1+sR_I C_I}{1+sR_F C_F}$$

This equation can be compared to equation 35.52, and the gains are calculated below.

$$\frac{V_{out}}{V_{in}} = \frac{R_F}{R_I}\frac{1+sR_I C_I}{1+sR_F C_F} = \frac{1}{G_2}\frac{1+\frac{s}{1/G_3}}{1+\frac{s}{G_1 G_2}}$$

$$---> G_2 = \frac{R_I}{R_F}$$

$$---> G_3 = R_I C_I$$

$$\frac{1}{G_1 G_2} = R_F C_F$$

$$G_1 \frac{R_I}{R_F} = \frac{1}{R_F C_F}$$

$$---> G_1 = \frac{1}{R_I C_F}$$

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35.17) *In Fig. 35.35 a filter section has a transfer function that can be written*

$$H(z) = (1 + A) * \frac{z - A/(1 + A)}{z}$$

For this transfer function generate a z-plane plot and a magnitude plot similar to what is seen in Fig. 35.27.

Soln:

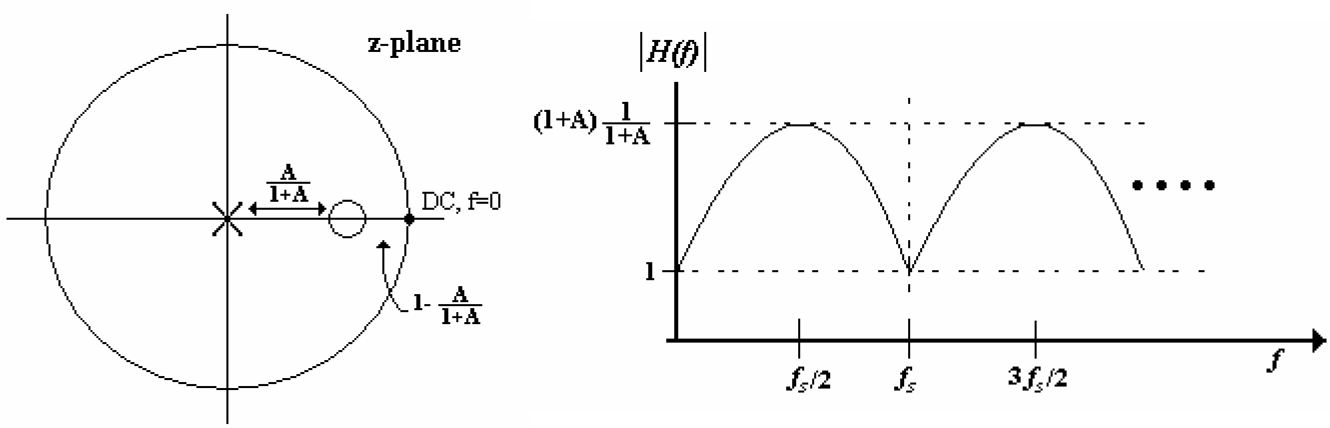
pole=> 0

zero=> $(1 + A) * [z - \dfrac{A}{1 + A}] = 0$

$$(1 + A) * z = A$$

$$z = \frac{A}{A + 1}$$

Z-plane and magnitude plot are shown below:



Magnitude of |H(f)| was found by taking the distance from the starting point on the unit circle (at DC, f=0) of the zero divided by the distance from the starting point of the pole:

$$|H(f)| = (1 + A) \cdot \frac{1 - \dfrac{A}{1 + A}}{1} = (1 + A) \cdot \frac{1}{1 + A}$$

We can also solve this problem by transforming z in the transfer function and then taking the magnitude and solving for the values shown in the above magnitude graph:

$$z = e^{j2\pi \frac{f}{f_s}} = \cos 2\pi \frac{f}{f_s} + j \sin 2\pi \frac{f}{f_s}$$

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$$H(f) = (1 + A)\left(\cos 2\pi \frac{f}{f_s} + j \sin 2\pi \frac{f}{f_s}\right) - A$$

Grouping the real terms together and taking the magnitude we get the following:

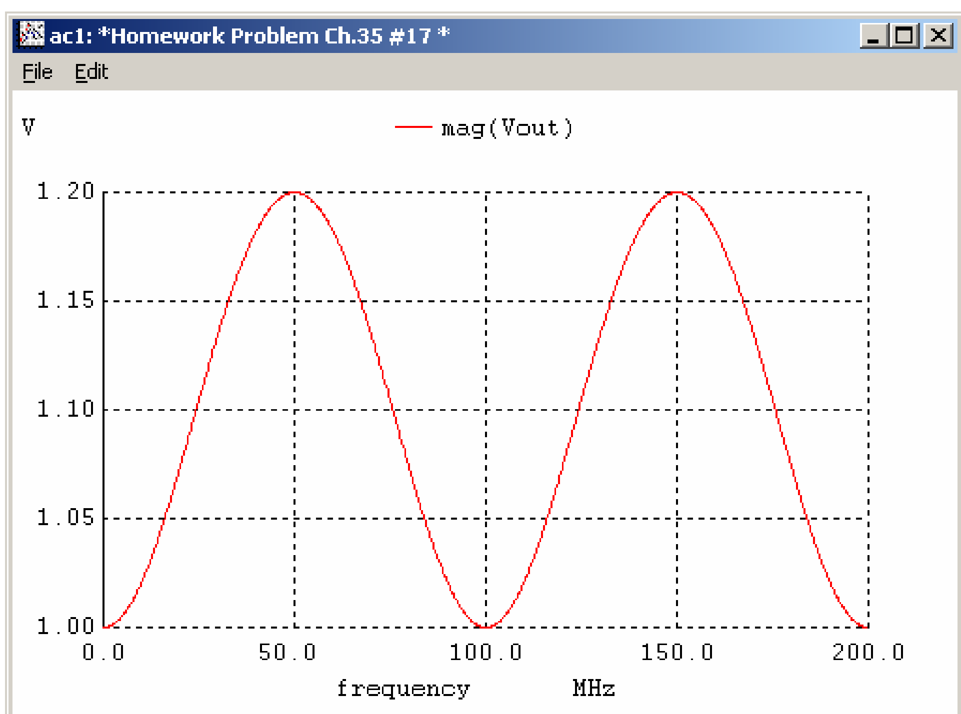
$$|H(f)| = \sqrt{((1+A)\cdot \cos 2\pi \frac{f}{f_s} - A)^2 + (\sin 2\pi \frac{f}{f_s}(1+A))^2}$$

Plugging in for *f* with A=.1 we get the following with for the magnitude:

$f=f_s/2$ ➔ 1.2
$f=f_s$ ➔ 1
$f=3f_s/2$ ➔ 1.2

A simulation with WINSPICE verifies the solution.

```
*Homework Problem Ch.35 #17 *

.AC LIN 1000 1k 200MEG

*WinSPICE command scripts
.control
destroy all
run
plot mag(Vout)
.endc

Vin     Vin     0       DC      0       AC      1
Vina    Vina    0       DC      0       AC      0.090909
R1      vin     0       1k
R2      Vina    0       1

*Delays using transmission lines and terminations
TZ1     Voutd   0       Vina    0       TD=10n  ZO=50
RZ1     Voutd   0       50

Esum    Vout    0       Vin     Voutd   1.1
R3      Vout    0       1k

.end
```

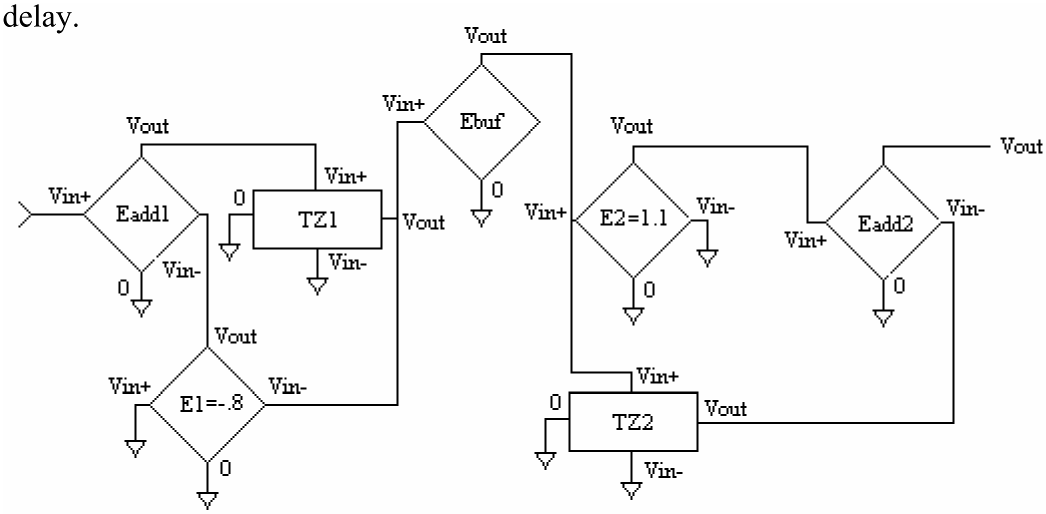


Ben Rivera
brivera@ieee.org

35.18) *Plot the time-domain output of the filter in Fig. 35.37 when the input is a zero to one step function.*

Soln:

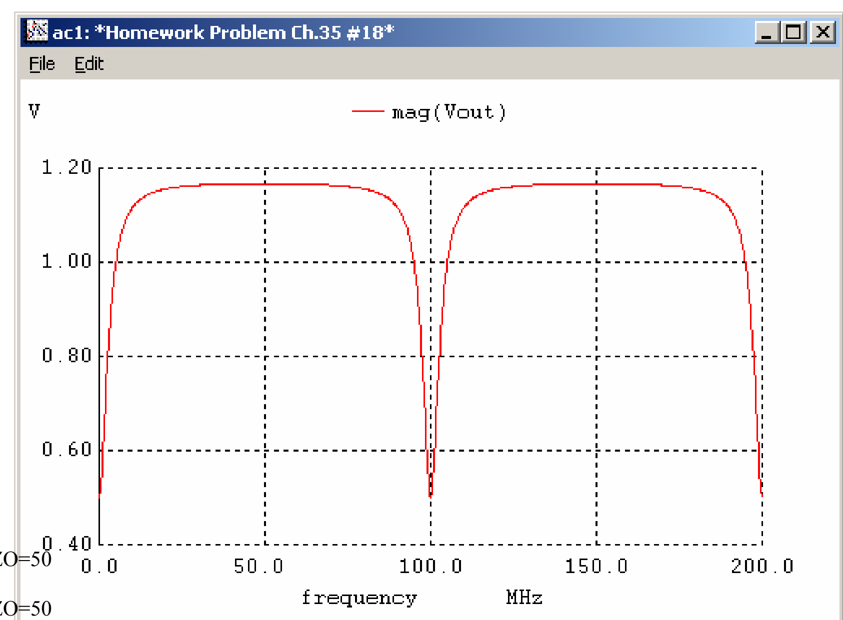
To model the circuit in WINSPICE we use voltage-controlled voltage sources for the adders and the multipliers. The z^{-1} blocks are modeled as transmission lines with a time delay.



We can write the transfer function as: $H(z) = \dfrac{1.1z - 1}{z^2 - .8z}$

The spice simulation is shown below to verify operation:

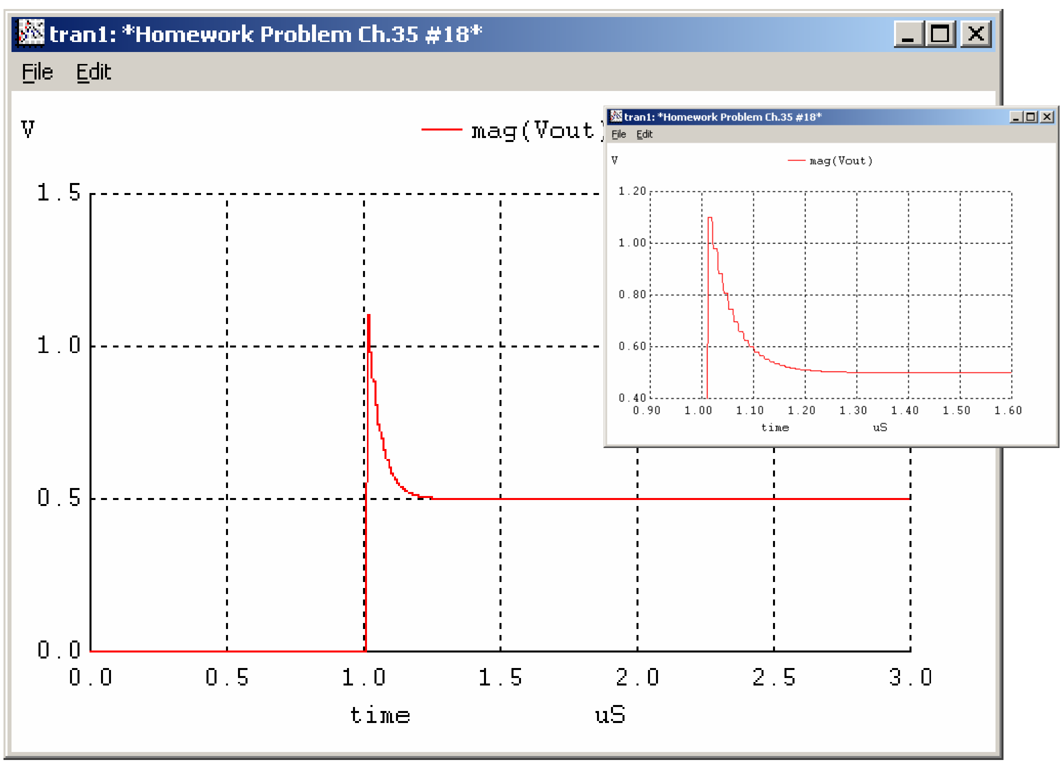
```
*Homework Problem Ch.35 #18*

.AC LIN 1000 1k 200MEG

*WinSPICE command scripts
.control
destroy all
run
plot mag(Vout)
.endc

Vin     Vin     0       DC      0       AC      1

Eadd1   Vint    0       Vin     Vf1     1
Eadd2   Vout    0       Vin1    Vtd2    1

*Multipliers
E1      Vf1     0       Vout1   0       -.8
E2      Vin1    0       Vout2   0       1.1

*Delays using transmission lines and terminations
TZ1     Vout1   0       Vint    0       TD=10n  ZO=50
RZ1     Vout1   0       50
TZ2     Vtd2    0       Vout2   0       TD=10n  ZO=50
RZ2     Vtd2    0       50

*Buffer to ensure no loading between the two delays
Ebuf    Vout2   0       Vout1   0       1

.end
```



Ben Rivera
brivera@ieee.org

The problem asked for a step input from 0 to 1, we can change the input in the netlist and do a .tran simulation:

```
*Homework Problem Ch.35 #18*

.tran 1n 3u 1n

*WinSPICE command scripts
.control
destroy all
run
plot mag(Vout)
.endc

Vin     Vin     0     pulse(0 1 1u 2n 2n 2u 4u)

Eadd1   Vint    0     Vin     Vf1     1
Eadd2   Vout    0     Vin1    Vtd2    1

*Multipliers
E1      Vf1     0     Vout1   0       -.8
E2      Vin1    0     Vout2   0       1.1

*Delays using transmission lines and terminations
TZ1     Vout1   0     Vint    0       TD=10n   ZO=50
RZ1     Vout1   0     50
TZ2     Vtd2    0     Vout2   0       TD=10n   ZO=50
RZ2     Vtd2    0     50

*Buffer to ensure no loading between the two delays
Ebuf    Vout2   0     Vout1   0       1

.end
```



Note at steady state, (1.5u) we get half the input voltage, this agrees with the transfer function if we set f=0 then z=1 and we get .1/.2=.5

Problem 35.19

Jake Anderson
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Design a first-order canonic digital filter that is clocked at 100MHz and has a transfer function in the frequency domain given by,

$$H(f) = \frac{1}{1 + j\dfrac{f}{4MHz}}$$

Begin by calculating A_1 from Figure 35.39

$$f_{3dB,pole} = 4MHz = \frac{f_s(1-A_1)}{2\pi} = \frac{100MHz(1-A_1)}{2\pi} --> A_1 = 0.7487$$

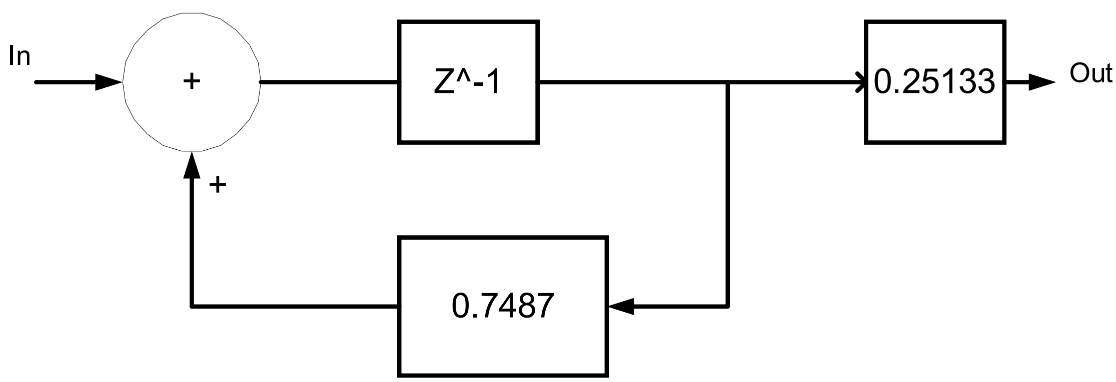
Now calculating B_o+B_1

$$A_{DC} = \frac{B_o + B_1}{1 - A_1} --> B_o + B_1 = 0.25133$$

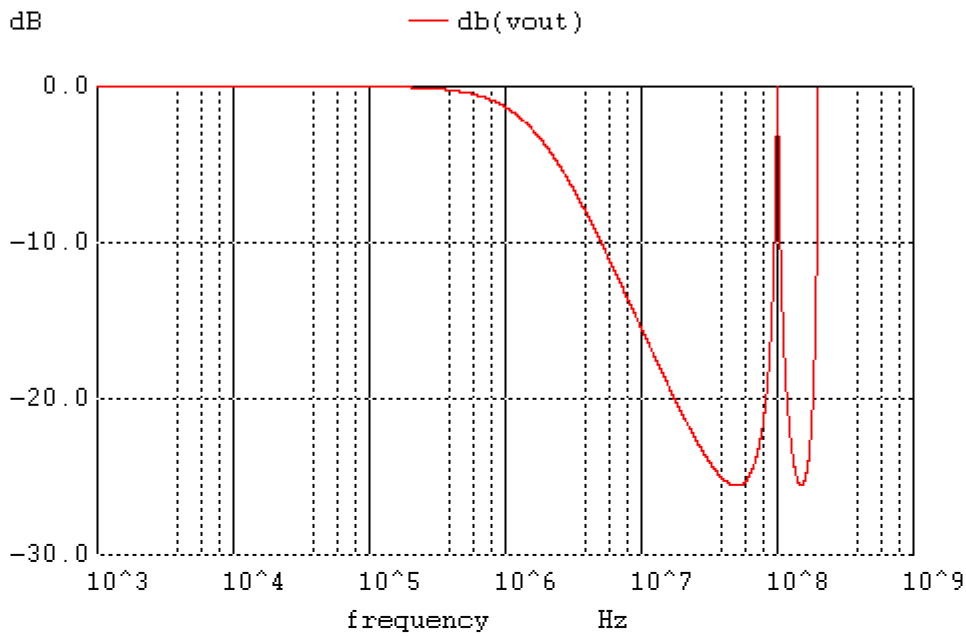
Like in example 35.10, we will put the zero at infinity so it doesn't efect the transfer function.

$$f_{3dB,pole} = \infty = \frac{f_s}{2\pi}\left(1 + \frac{B_1}{B_o}\right) --> B_o = 0 --> B_1 = 0.25133$$

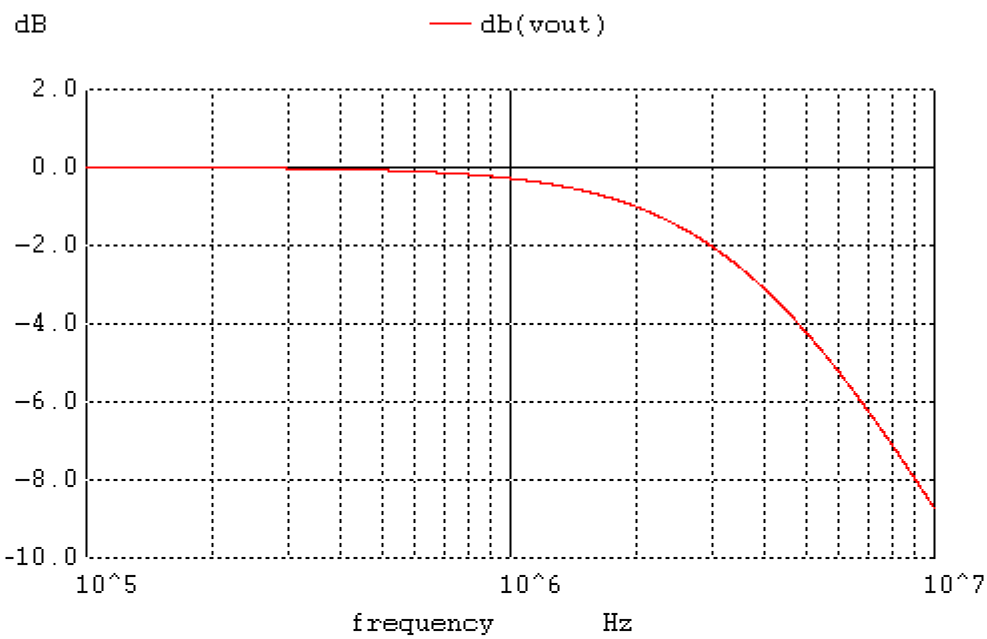
The sketch of the filter is shown below



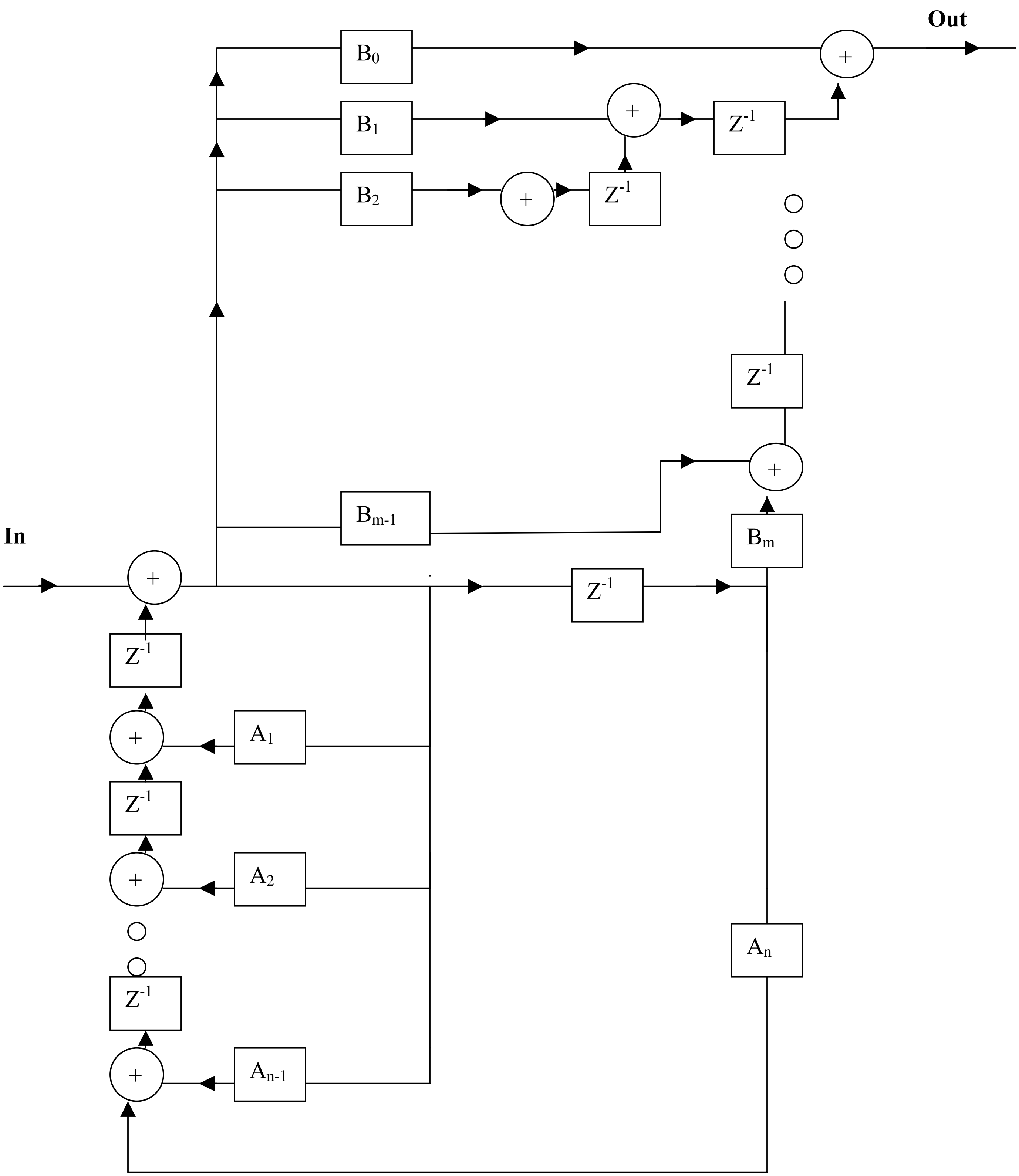
Note that this is the exact same filter as the one seen in Fig 35.26 except we have combined multipliers so B_1=A, the A of Fig 35.26.
Using the same netlist for Fig35-28 alt.cir, accept the 0.1 in the netlist is changed to 0.25133 gives the simulation for this filter. The Frequency response is shown on the next page. f_{3db} is four Mega Hertz.



Below is a zoom in, to see more easily the f_{3db} is at 4MHz



Solution 35:20.
Digital filter of fig. 35.42 using only two input adders:



Solution for 35.21 by Sugato Mukherjee e-mail:msugato@ieee.org

Q. Is it possible to tune the gain, Q, and cut-off frequency of the lowpass biquad independently? If so how? Give examples using the simulation netlist used to generate Fig. 35.48.

Ans: It is possible to tune the gain, Q, and cut-off frequency of the lowpass biquad independently. This can be shown by examining the design equations for the active RC implementation of the lowpass biquad. The general form (s-domain) of the second order lowpass filter is given by

$$H(f) = \frac{a_0}{s^2 + \frac{(2\pi f_0)s}{Q} + (2\pi f_0)^2}$$

Looking at equations 35.89 to 35.93, we find that $a_2=a_1=0 \Rightarrow G_3=G_6=0$. Let us now find the expression for Q using equations 35.92 and 35.93. Substituting the value for f_0 from 35.93 in 35.92, we get

$$Q = \frac{\sqrt{G_1G_4G_5}}{G_1G_2} = \sqrt{\frac{G_4G_5}{G_1{G_2}^2}}$$

$\omega_0 = \sqrt{G_1G_4G_5}$ ($\omega_0=2\pi f_0$)

Gain = G_1G_4

Also for the active RC implementation, putting the values for G_1 to G_6, we get

$$Q = \sqrt{\frac{{R_{F1}}^2C_{F1}}{R_{F2}C_{F2}R_{I2}}} \quad \text{....(1)}$$

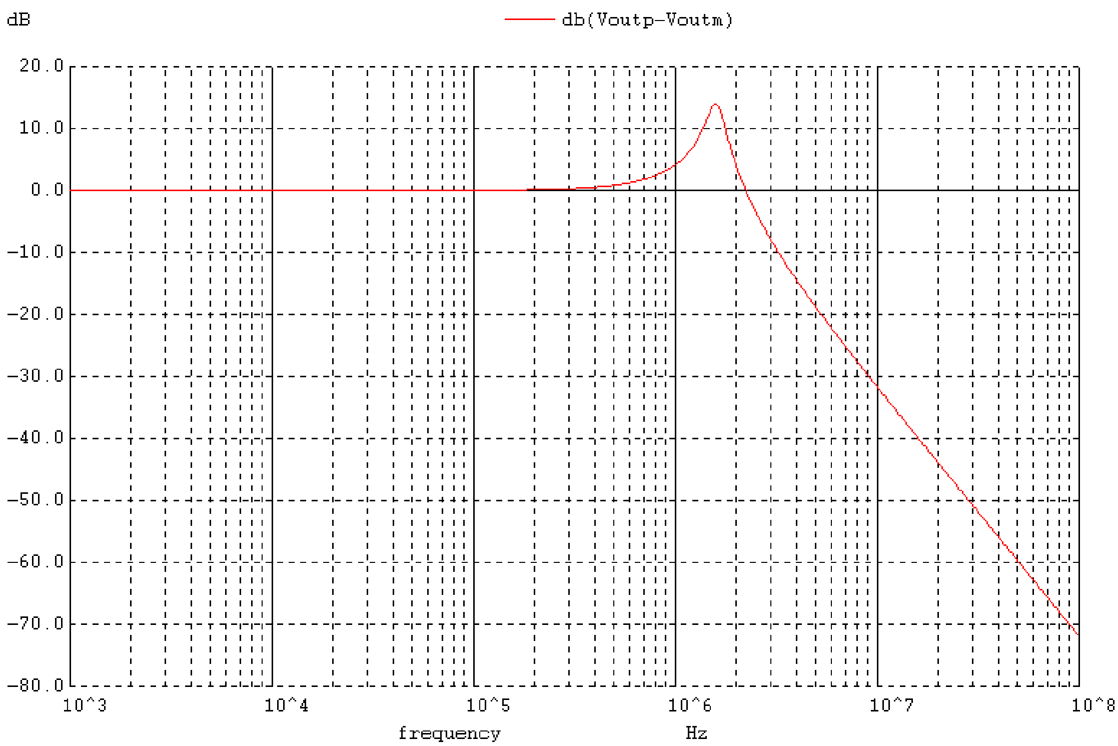
$$\omega_0 = \frac{1}{\sqrt{R_{F2}C_{F2}R_{I2}C_{F1}}} \quad \text{...(2)}$$

$$Gain = \frac{1}{R_{I1}C_{F1}R_{I2}C_{F2}} \quad \text{...(3)}$$

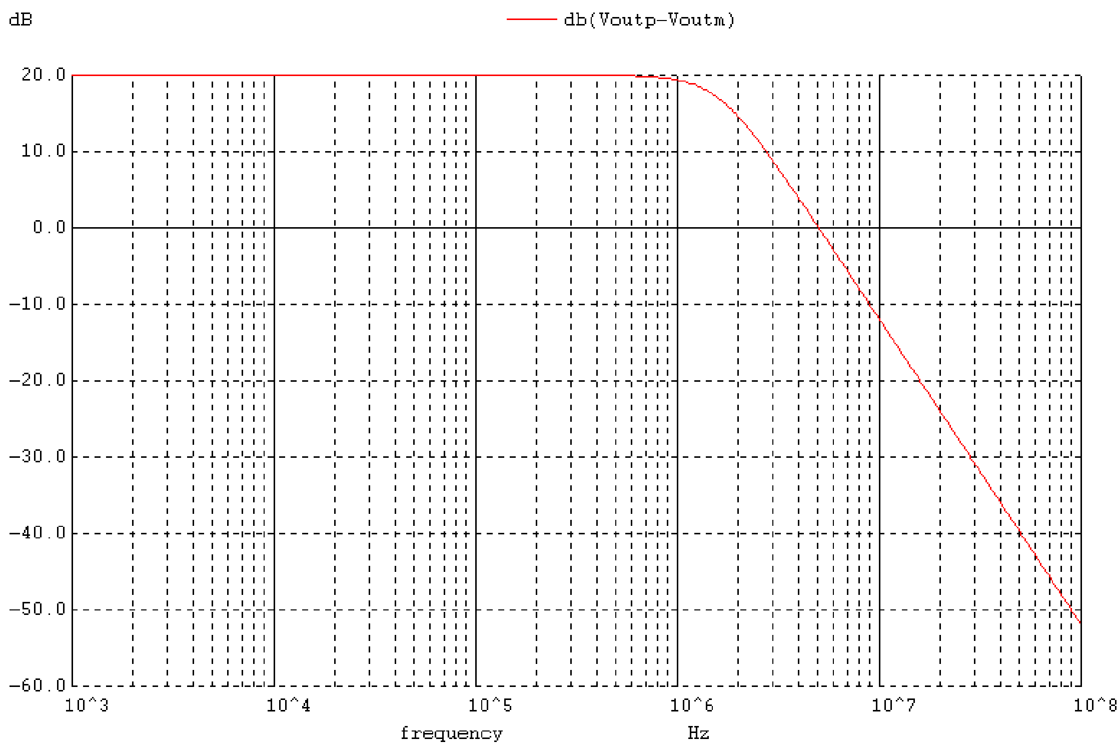
From (1), (2) and (3), we see that for a given cut-off frequency, we can adjust Q by changing R_{F1} and adjust the gain by changing R_{I1}.

To illustrate this point we will use the netlist used to generate Fig. 35.48. The cut-off frequency for this example was 1.59MHz , Q=0.707, Gain=1. Let us proceed to show that we can change the Q of this filter keeping the gain and cut-off frequency constant and then change the gain of the filter keeping the Q and the cut-off frequency constant. The netlist used to generate Fig. 35.48 is reproduced next for convenience. In this netlist if we change R_{F1} from 7.07K to 50K, then Q becomes 5 instead of 0.707 and the magnitude response of the filter should now exhibit a peaking behavior but the DC gain and the cut-off frequency should remain unchanged. Also, next if we change the value of R_{I1} from 10K to 1K, we should get a DC gain of 10 instead of 1 with the same Q (=0.707) and cut-off frequency as the original filter. The simulation waveforms are shown to validate the above observations.

```
*Figure 35.48 CMOS: Mixed-Signal Circuit Design *

*WinSPICE command scripts
*#destroy all
*#run
*#set units=degrees
*#plot ph(Voutp-Voutm)
*#plot db(Voutp-Voutm)

.ac dec 100 1k 100MEG

VCM VCM 0 DC 0.75

*Set Vin to 1V (Vin+ - Vin- = 1V)
Vin     Vinps  VCM   DC      0         AC 0.5
Vina    Vinms        VCM             DC      0         AC -0.5

Rftop1 Voutm1  Vinm1 7.07k
Ritop1 Vinps   Vinm1 10k
Ribot1 Vinms   Vinp1 10k
Rfbot1 Voutp1  Vinp1 7.07k

Cftop1 Voutm1  Vinm1 10p
Cfbot1 Voutp1  Vinp1 10p

*Use a VCVS for the op-amp
E11 Voutm1 VCM Vinp1 Vinm1 100MEG
E21 VCM Voutp1 Vinp1 Vinm1 100MEG

Rf2top Voutm  Vinm1 10k
Ri2top Voutm1 Vinm2 10k
Ri2bot Voutp1 Vinp2 10k
Rf2bot Voutp  Vinp1 10k

Cfp2 Voutp Vinm2 10p
Cfm2 Voutm Vinp2 10p

*Use a VCVS for the op-amp
E12 Voutp VCM Vinp2 Vinm2 100MEG
E22 VCM Voutm Vinp2 Vinm2 100MEG

.end
```



DC gain =1, cut-off frequency =1.59 MHz, Q=5. The above figure can be compared against Fig. 35.48 in the book to verify that Q can be tuned independently for a given gain and cut-off frequency.



DC gain =10, cut-off frequency =1.59 MHz, Q=0.707. The above figure can be compared against Fig. 35.48 in the book to verify that the gain can be tuned independently for a given Q and cut-off frequency.

This is known as orthogonal tuning. Orthogonal tunability increases the flexibility of a design by providing more degrees of freedom for adjusting system parameters.

Solution by:
Curtis Cahoon
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Problem 35.22
What happens to the poles in the biquadratic equation, Eq. (35.80), if the Q is less than 0.5? Is the f_{max} equation in Fig. 34.45 valid?

Solution

First of all, we recognize that the poles in a biquadratic transfer function occur where the equation in the denominator is equal to zero. The equation for the denominator in the standard biquadratic transfer function is shown below.

$$P(f) = s^2 + (2\pi f_0/Q)s + (2\pi f_0)^2$$

If the Q of the filter is set equal to 0.5, the equation can be rewritten in the following way (since 1/0.5 = 2)

$$P(f) = s^2 + 2(2\pi f_0)s + (2\pi f_0)^2$$

Which is simply $(s + 2\pi f_0)^2$, which means that the filter will have a double pole at $s = -2\pi f_0$. If we remember the discriminant of a quadratic function ($b^2 - 4ac$) we see that this corresponds to the case where $b^2 - 4ac = 0$. This results in a repeated real value for the roots of our equation. Since the filter has only real poles at this point, this transfer function that can be realized by a cascade of two first-order filters (see section 35.2.2 in the chapter).

Now let's see what will happen if we have a lower Q value. Having a lower value for Q corresponds to a larger coefficient for the linear term in the denominator of our transfer function. Having a larger linear term coefficient results in $b^2 - 4ac > 0$, which means that we will have two real poles in our transfer function. These roots will always be negative, which means that the filter will also always be stable (recalling from control system theory that when all poles are less than 0, the system will be stable). Also, this type of transfer function can be realized with the cascade of two first-order filters.

Finally, lets find when the equation in Fig. 34.45 is valid. It states in the discussion above the figure that the equation is only valid when Q is greater than 0.707. This is because the filter will only experience peaking when Q is greater than this value. This corresponds to the frequency at which the peaking will occur if Q is higher than that value. Since no peaking occurs for $Q<0.707$, this equation is not valid and thus doesn't apply. Notice that if we make Q very high, Fmax will approach f_0.

Problem 35.23

Compare the size of the elements used in Exs. 35.11 and 35.12. Is there a benefit to using an active element for monolithic implementation?

Yes, using active-RC biquad filter (Ex 35.12) is easier for the monolithic implementation. As shown in the Ex. 35.12, it only need to set $C_{I1}=C_{I2}=0$, $C_{F1}=C_{F2}=10pF$, and $R_{I2}=R_{F2}=10k$. These capacitors and resistors are typical values and easy to fabricate in a CMOS process. However, for LRC circuit shown in Ex 35.11, having the similar frequency characteristic, we need to make C=100pF, L=100uH, and R=1.4K. Both C and L are relatively big for any standard CMOS process. For example, in a given process, the thickness between metal1 and substrate is 1.5um, for a 1 um-wide piece of metal, the inductance is

$$L(nH/mm) = \frac{1.25}{\frac{1}{1.5} + 1.393 + 0.667 \quad In(\frac{1}{1.5} + 1.44)} = 0.6nH/mm$$

In order to get L=100uH, we need to place166, 666 um-long metal1 on the chip. This is impossible to manufacture. So, the big benefit of active –RC filter over the LRC filter is reducing the value of the elements.

EE515 -CMOS Mixed Signal IC Design

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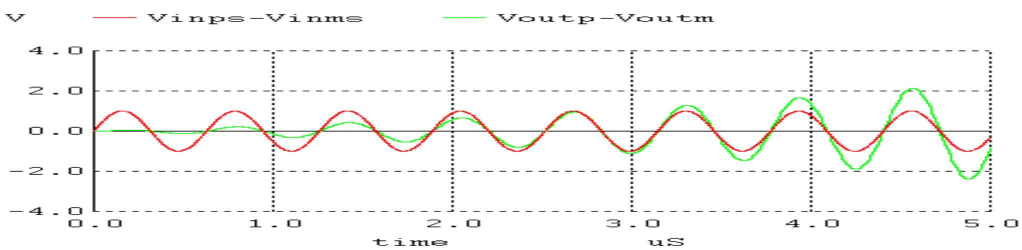
Chapter 35.24

Show, using the simulations from Ex35.17 that increasing the switch resistance, and thus the spectral content present in a switched capacitor circuit, can help to stabilize high-Q switched-capacitor bandpass filters.

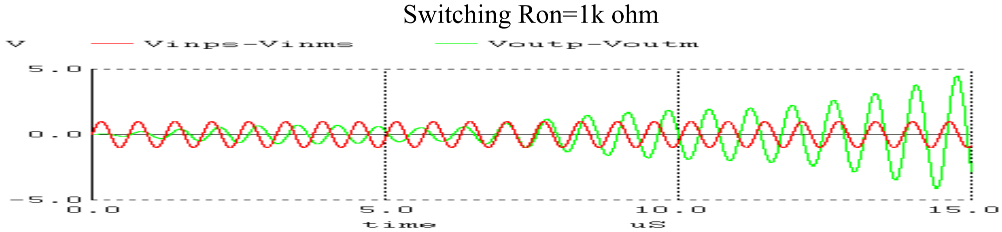
[Answer]: Simulations results indicate that indeed high-Q switched-capacitor bandpass filter gets improvement on stability gradually when switching resistance increases. The following simulations were based on configuration of Fig35.58. (Green line is output).

Further analysis is provided in next page.

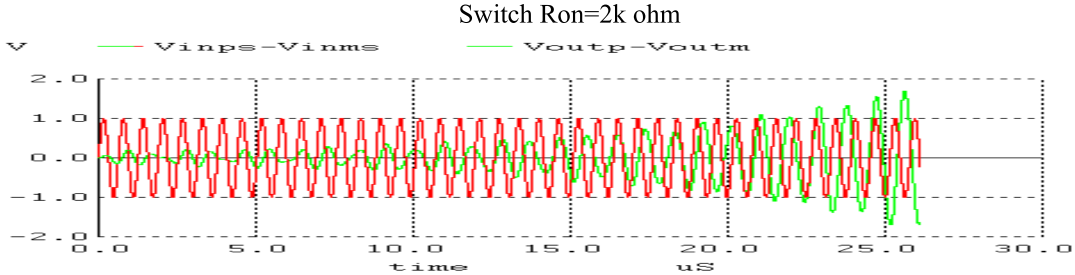
Switching Ron=100 ohm



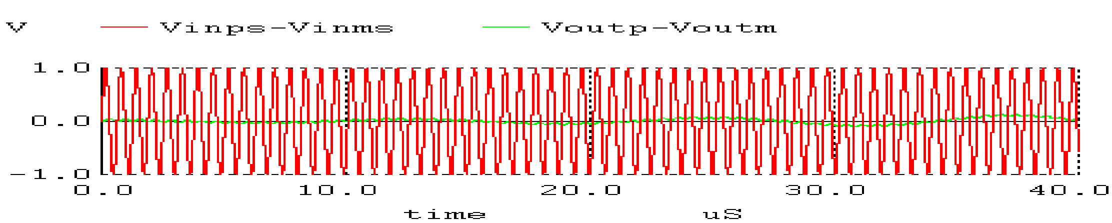
Switching Ron=1k ohm



Switch Ron=2k ohm



Switch Ron=20k ohm



[Analysis]: There are several effects by increasing switching resistance.

1). Bigger switching resistance imposes lossy line throughout circuit; voltage drops on switches help to reduce positive feedback gain when filter is unstable and oscillating;
2). Bigger switching resistance reduces the switching noise, smoothes voltage abrupt changes (higher frequency components) when on/off.
3). Bigger Switching resistance results in larger time constant at each switching operation. Output would be attenuated at initial cutoff frequency (f_o) instead of oscillating. →

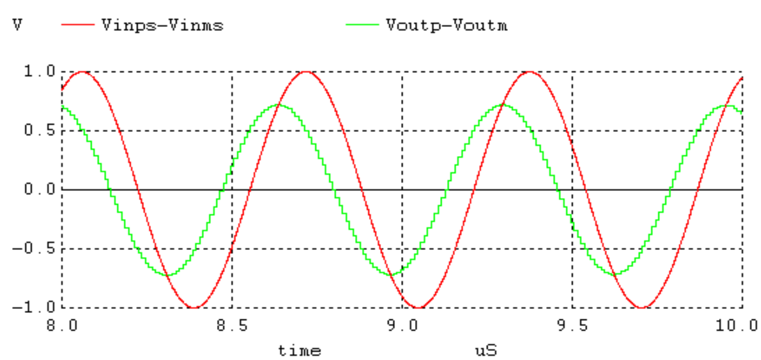
Moreover, it leads to another key impact:

Bandpass filter Cutoff frequency (f_o) is decreased as switching resistance increase; further helps poles move away from right-hand plane after oscillation.

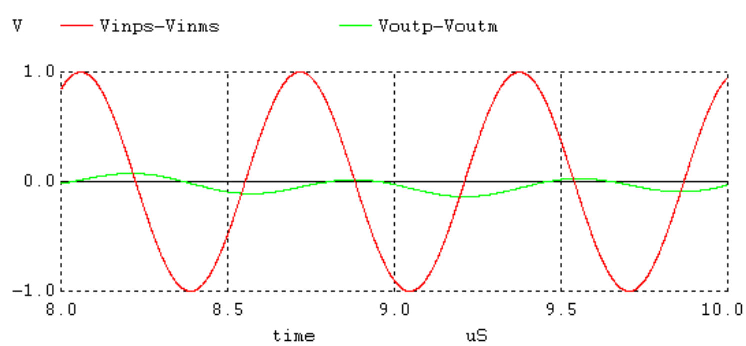
$f_o = 1/2\pi \text{ sqrt}(1/C_{F1}R_{I2}C_{F2}R_{F2})$ drops as R_{I2} and R_{F2} increase.

[Simulation]: Due to the fact that this circuit can only be simulated using a transient analysis, we will input a sinewave at a known frequency and verify we get the desired output.

Switching resistance Ron=100 ohm, input frequency = 1.52MHz = f_{3dB} initially



Switching resistance Ron=10k ohm, same input frequency =1.52MHz



Clearly, same input signal gets attenuated after switching resistance increase to 10k from 100. Therefore, cutoff frequency fo dropped as switching resistance increase.

EE515 -CMOS Mixed Signal IC Design -- Yantao Ma

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Chapter 35.25

Redesign and simulate the operation of the filter discussed in Ex35.17, with a Q of 5, while trying to minimize the difference between C_{I1} and C_{F2}. Suggest a possible modification to the filter topology (similar to how we add G_{2Q} in Figure 35.54) to reduce this component spread.

[Answer]:

We will re-design the system to minimize the difference between C_{I1} and C_{F2} after adding R_{F1Q} as High-Q compensation.

As in Example 35.17 suggested params are as following Q=20 f_o = 1.59MHz:

C_{I1} = 0.4pf C_{F1} = 2pf C_{F2} = 5pf C_{I21} = 0.2pf

C_{I21Q} = 0.19pf C_{I12} = 0.125pf C_{I22} = 0.8pf

Re-design: Bandpass filter design key parameters: (fs = 100MHz)

1). $Q = R_{F1}\cdot \text{sqrt}(C_{F1}/R_{I2}C_{F2}R_{F2}) = \text{sqrt}(C_{I12}\,C_{I22}\,C_{F1}/C_{F2})\,/C_{I21} = C_{F1}/10(C_{I21}-C_{I21Q})$

with $R_{F1} = 1/(C_{I21}\,fs)$

$R_{I2} = 1/(C_{I12}\,fs)$

$R_{F2} = 1/(C_{I22}\,fs)$

2). $f_o = 1/\{2\pi\,\text{sqrt}(1/C_{F1}R_{I2}C_{F2}R_{F2})\} = fs/\{2\pi\,\text{sqrt}(C_{I12}C_{I22}/C_{F1}C_{F2})\}$ =1.59MHz

$\rightarrow C_{I12}C_{I22}/C_{F1}C_{F2} = 0.01$

3). Passband Gain $Av = 1$

$a_1 = 2\pi f_o/Q = C_{I1}/R_{I2}C_{F1}C_{F2} = 2\pi\cdot 1.59\text{MHz}/Q = 1/R_{F1}C_{F1}$

$\rightarrow C_{I1}\,C_{I12}\,fs\,/C_{F1}C_{F2} = C_{I21}\,fs\,/\,(C_{F1}Q) = 10\text{x}10^6/Q$ or

$\rightarrow C_{I1}\,C_{I12}\,/C_{F1}C_{F2} = C_{I21}\,/\,(C_{F1}Q) = 0.1/Q$

In summary: $C_{I1}\,C_{I12}\,/C_{F1}C_{F2} = C_{I21}\,/\,(C_{F1}\,Q) = 0.1/Q = 0.01C_{I1}/C_{I22}$

$\rightarrow C_{I1} = 10\,C_{I22}/Q$ (determined by Q, fs, fo)

$\rightarrow C_{I12}C_{I22}/C_{F1}C_{F2} = 0.01$ (determined by fs, fo)

$\rightarrow C_{I21} = 0.1\,C_{F1}$ (determined by fs amd fo)

Design Q to drop from 20 to 5 while keep fo @ 1.59MHz and Av=1 by setting C_{I1}=1.6pf, C_{I12} = 0.25pf as twice larger than that of Q=20 for a_1;

C_{I21} = 0.6pf and C_{I21Q} = 0.48pf, C_{F1} = 4pf, C_{I22} = 0.8pf for Q with the consideration of minimize the difference between C_{I1} and C_{F2}. (Now C_{I1}= 1.6pf and C_{F2} = 5pf)

Further discussion:

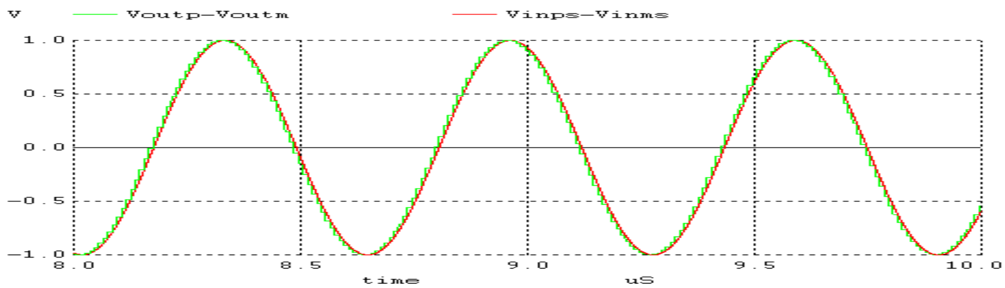
1). C_{I1} can be brought further close to C_{F2} at the price of sacrificing C_{F1} if maintaining same fs, fo, and Q.

2). Determined by Q, fs, and fo, C_{I1} should be twice larger than C_{I22} when Q=5, fs=100MHz, fo=1.59MHz, it explained the reason why Figure 35.59 simualtion indicated that Q=11.36 @page443 in textbook.

Simulations:

(Simulation case for fo and Passband Gain *Av*)

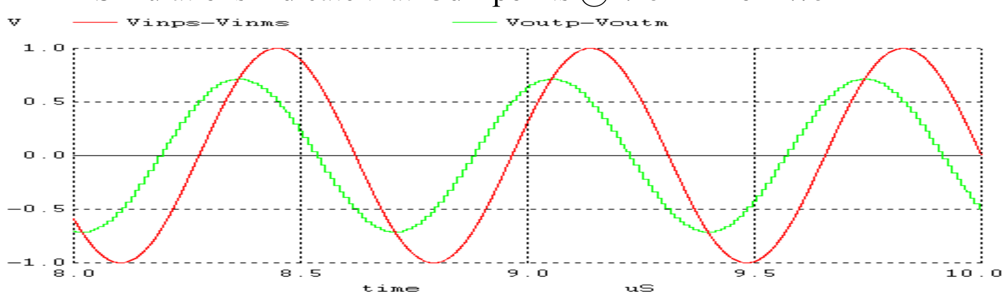
Simulation1 indicates: fo~=1.595MHz, *Av* =1 as desired

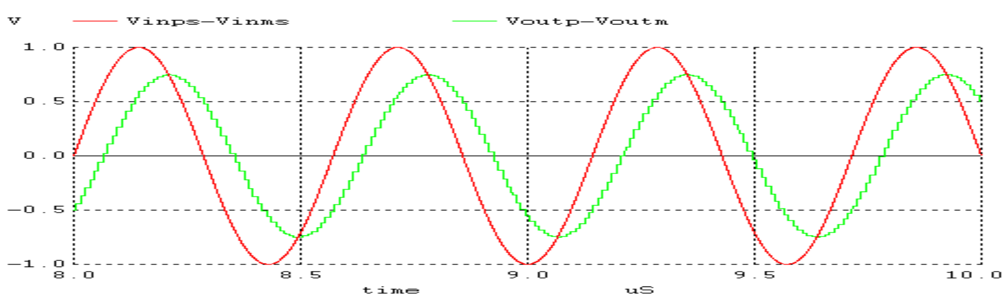


(Simulation case for f3dB and Q)

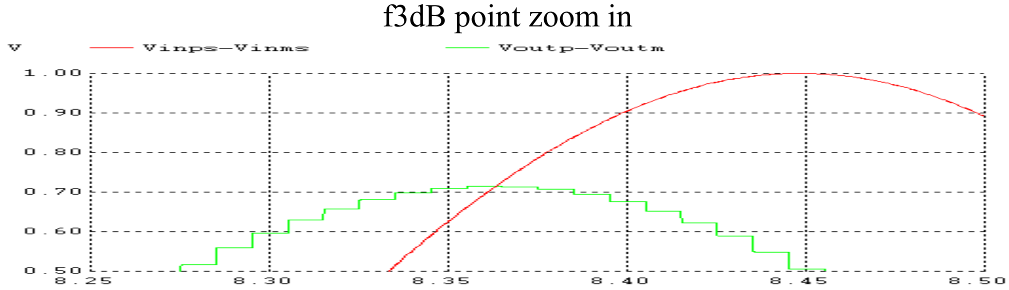
Simulation2 indicates f3dB BW = [1.45MHz, 1.75MHz] as compared to 1.43MHz as designed. Results in Q~= 5.6 vs ideal target Q=5

Simulations indicate that f3dB points @1.45MHz or 1.75MHz

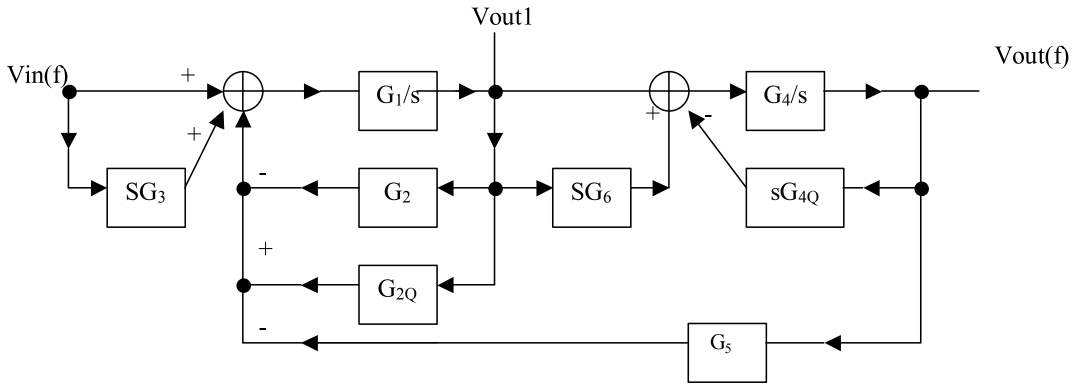


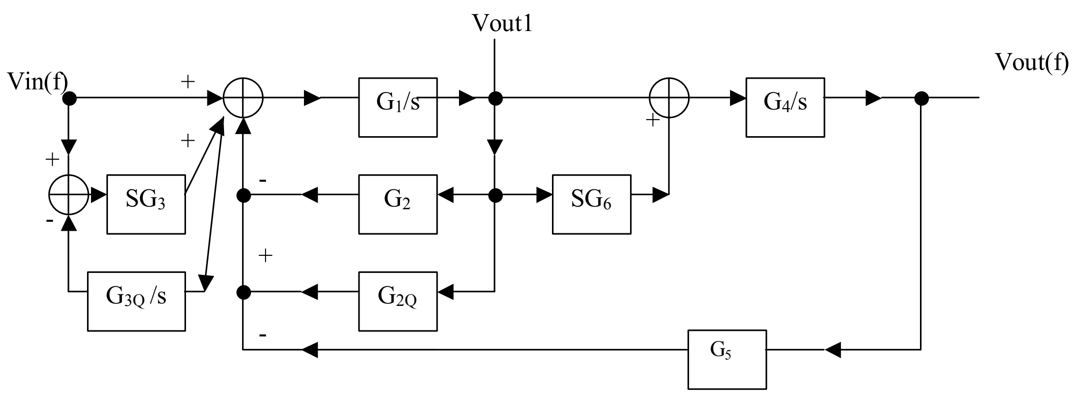


f3dB point zoom in



Suggest Topology:





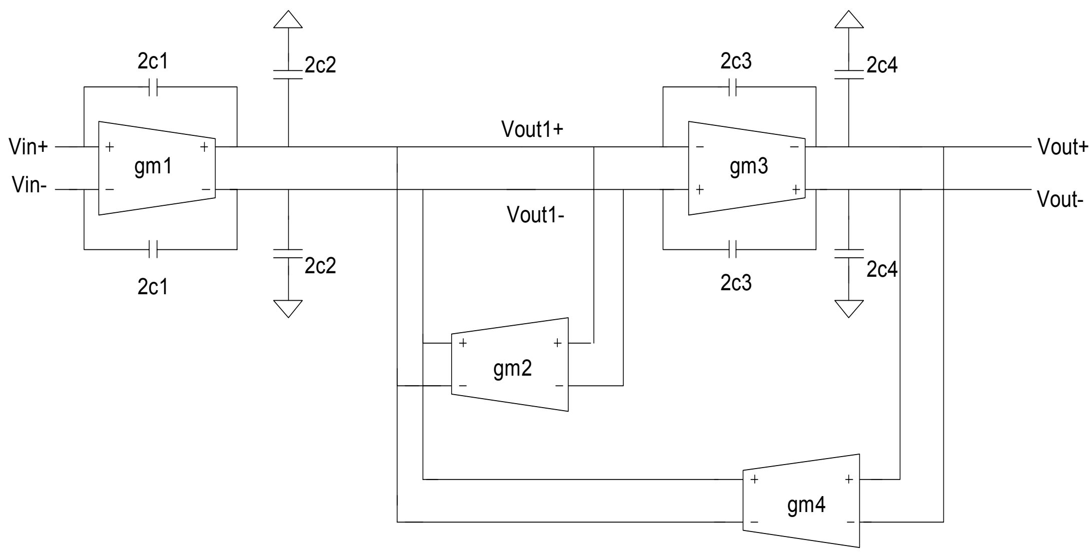
Simulation Scripts—SPICE

```
*Problem 35.25 temp-sol CMOS: Mixed-Signal Circuit Design --Yantao Ma*

*WinSPICE command scripts
*#destroy all
*#run
*#plot Vinps-Vinms Voutp-Voutm
.tran 1n 10u 8u 1n UIC

*Input power and references
Vtrip Vtrip 0 DC 0.75
VCM VCM 0 DC 0.75

*Input Signal
Vinps    Vinps   0 DC 0 Sin 0.75  500m 1.45MEG
Vinms    Vinms   0 DC 0 Sin 0.75 -500m 1.45MEG

*Clock Signals
Vphi1  phi1  0 DC 0  Pulse 0 1.5   0    200p  200p  4n 10n
Vphi2  phi2  0 DC 0  Pulse 0 1.5   5n   200p  200p  4n 10n
R2 phi1 0 1MEG
R3 phi2 0 1MEG

S1top1      Voutm1     N1          phi1 VTRIP switmod
S2top1      N1         VCM         phi2 VTRIP switmod
Citop21     N1         N3          0.6p
Citp21Q     N1         N2          0.48p
S3top1      VCM        N2          phi1 VTRIP switmod
S4top1      N2         Vinm1       phi2 VTRIP switmod
Citop1      Vinps   Vinm1          1.6p
Cibot1      Vinms   Vinp1          1.6p
S1bot1      Voutp1     N4          phi1 VTRIP switmod
S2bot1      N4         VCM         phi2 VTRIP switmod
Cibot21     N4         N2          0.6p
Cibt21Q     N4         N3          0.48p
S3bot1      VCM        N3          phi1 VTRIP switmod
S4bot1      N3         Vinp1       phi2 VTRIP switmod

Cftop1 Voutm1  Vinm1 4p
Cfbot1 Voutp1   Vinp1 4p

*Use a VCVS for the op-amp
E11 Voutm1 VCM Vinp1 Vinm1 200MEG
E21 VCM Voutp1 Vinp1 Vinm1 200MEG

S1top2      Voutp      N5          phi1 VTRIP switmod
S2top2      N5         VCM         phi2 VTRIP switmod
Citop22 N5 N2          0.8p
S3top2      Voutm1     N6          phi1 VTRIP switmod
S4top2      N6         VCM         phi2 VTRIP switmod
Citop12     N6         N8          0.25p
S5top2      VCM        N7          phi1 VTRIP switmod
S6top2      N7         Vinm2       phi2 VTRIP switmod
S1bot2      Voutm      N10         phi1 VTRIP switmod
S2bot2      N10        VCM         phi2 VTRIP switmod
Cibot22     N10        N3          0.8p
S3bot2      Voutp1     N9          phi1 VTRIP switmod
S4bot2      N9         VCM         phi2 VTRIP switmod
Cibot12     N9         N7          0.25p
S5bot2      VCM        N8          phi1 VTRIP switmod
S6bot2      N8         Vinp2       phi2 VTRIP switmod

Cfp2 Voutp Vinm2 5p
Cfm2 Voutm Vinp2 5p

*Use a VCVS for the op-amp
E12 Voutp VCM Vinp2 Vinm2 200MEG
E22 VCM Voutm Vinp2 Vinm2 200MEG

.model switmod SW RON=100
.end
```

Problem 35.26

Derive the transfer function of the transconductor-C biquad shown in Fig. 35.63. Can this filter be orthogonally tuned? If so how?

The figure below shows implementation of a biquad filter using transconductors without crossing wires. Signals are summed using current.



Lets sum the currents at the V_{out1+} first,

$$g_{m1}(V_{in+} - V_{in-}) - g_{m2}(V_{out1+} - V_{out1-}) + \frac{V_{in+} - V_{out1+}}{1/s2c_1} - \frac{V_{out1+}}{1/s2c_2} + g_{m4}(V_{out+} - V_{out-}) = 0$$

where $V_{out+} = -V_{out-}$, $V_{out1+} = -V_{out1-}$ and $V_{in+} = -V_{in-}$. Also,

$$\frac{V_{in+}}{1/s2c_1} = \frac{2V_{in+}}{1/sc_1} = \frac{V_{in+} - V_{in-}}{1/sc_1}$$

$$(V_{out1+} - V_{out1-}) \cdot (s(C_1 + C_2) + g_{m2}) = g_{m4}(V_{out+} - V_{out-}) + (V_{in+} - V_{in-}) \cdot (sC_1 + g_{m1})$$

so,

$$(V_{out1+} - V_{out1-}) = \frac{(V_{in+} - V_{in-}) \cdot (sC_1 + g_{m1}) + (V_{out+} - V_{out-})g_{m4}}{s(C_1 + C_2) + g_{m2}}$$

Summing the currents at V_{out+},

$$g_{m3}(V_{out1+} - V_{out1-}) + \frac{V_{out1+} - V_{out+}}{1/s2C_3} - \frac{V_{out+}}{1/s2C_4} = 0$$

$$g_{m3}(V_{out1+} - V_{out1-}) + s2C_3(V_{out1+} - V_{out+}) - s2C_4 \cdot V_{out+} = 0$$

$$(g_{m3} + sC_3)(V_{out1+} - V_{out1-}) - s(C_3 + C_4)(V_{out+} - V_{out-}) = 0$$

Replace $(V_{out1+} - V_{out1-})$,

$$(g_{m3} + sC_3)\frac{(V_{in+} - V_{in-}) \cdot (sC_1 + g_{m1}) + g_{m4}(V_{out+} - V_{out-})}{s(C_1 + C_2) + g_{m2}} - s(C_3 + C_4)(V_{out+} - V_{out-}) = 0$$

$$(g_{m3} + sC_3)[(V_{in+} - V_{in-})(sC_1 + g_{m1}) + g_{m4}(V_{out+} - V_{out-})] - s(C_3 + C_4)[s(C_1 + C_2) + g_{m2}](V_{out+} - V_{out-}) = 0$$

$$(g_{m3} + sC_3)(sC_1 + g_{m1})(V_{in+} - V_{in-}) + \{g_{m4}(g_{m3} + sC_3) - s(C_3 + C_4)[s(C_1 + C_2) + g_{m2}]\}(V_{out+} - V_{out-}) = 0$$

$$\frac{V_{out+} - V_{out-}}{V_{in+} - V_{in-}} = \frac{(g_{m3} + sC_3)(sC_1 + g_{m1})}{s(C_3 + C_4)[s(C_1 + C_2) + g_{m2}] - g_{m4}(g_{m3} + sC_3)}$$

$$\frac{V_{out+} - V_{out-}}{V_{in+} - V_{in-}} = \frac{s^2 C_1 C_3 + s(C_3 g_{m1} + C_1 g_{m3}) + g_{m1} g_{m3}}{s^2 (C_3 + C_4)(C_1 + C_2) + s(g_{m2}(C_3 + C_4) + g_{m4} C_3) + g_{m3} g_{m4}}$$

$$\frac{V_{out+}-V_{out-}}{V_{in+}-V_{in-}}=\frac{s^2\frac{C_1C_3}{(C_3+C_4)(C_1+C_2)}+s\frac{(C_3g_{m1}+C_1g_{m3})}{(C_3+C_4)(C_1+C_2)}+\frac{g_{m1}g_{m3}}{(C_3+C_4)(C_1+C_2)}}{s^2+s\frac{g_{m2}}{(C_1+C_2)}+\frac{C_3g_{m3}}{(C_1+C_2)(C_3+C_4)}+\frac{g_{m3}g_{m4}}{(C_3+C_4)(C_1+C_2)}}$$

The transfer function of the biquad is given by,

$$\frac{V_{out+}-V_{out-}}{V_{in+}-V_{in-}}=\frac{s^2G_1G_3G_4G_6+s(G_1G_3C_4+G_1G_4G_6)+G_1G_4}{s^2+s(G_1G_2+G_1G_4G_5C_6)+G_1G_4G_5}$$

So, finally we got,

$$G_1=\frac{g_{m1}}{(C_1+C_2)} \qquad G_2=\frac{g_{m2}}{g_{m1}} \qquad G_3=\frac{C_1}{g_{m1}}$$

$$G_4=\frac{g_{m3}}{(C_3+C_4)} \qquad G_5=\frac{g_{m4}}{g_{m1}} \qquad G_6=\frac{C_3}{g_{m3}}$$

This filter can be orthogonally tuned. The pole and zero could be adjusted by changing each transconductor’s g_m independently. For instance, G_1/G_3 can be tuned by changing g_{m1}, G_2/G_5 can be adjusted by changing g_{m2} and g_{m4}, and G_6/G_4 can be tuned by changing g_{m3}.

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Problem 35.27

How would a "high-Q" biquad be implemented using transconductors? Repeat Ex. 35.15 using the transconductor based biquad.

Solution

On page 446 we can see the schematic for the transconductor-C implementation of a biquadratic transfer function. The discussion on how to transform the standard active RC biquad filter into a practical "high-Q" design is on page 438. In this discussion we work with a simplified form of our filter, assuming that it will either have a bandpass or lowpass response. In order to do this, we assume that the gain G_6 from the standard equation derived for a biquad response is equal to zero. This is equivalent to removing C_3 from our schematic. In the modified biquad filter, $C_3 = 0$.

We can now refer to equation 35.96 and the gain equations under the schematic on page 446 to compute the transfer function for this filter. Before this is done, however, remember that we need an easy way to make this a "high-Q" filter without making our gain G_2 too small to be practically implemented. In the filter shown in the discussions on pages 438-439, this gain is implemented using an extra positive feedback resistor (R_{F1Q}) around the first op-amp. This allows a current to be subtracted from the current flowing through the resistor (R_{F1}), and allows the resistors to be smaller, comparable in magnitude to the other resistors. The values for these resistors are obtained by multiplying the gain G_2 by (Q-1)/Q, and subtracting that new gain G_{2Q} from G_2 and substituting it into our original equation. This can be performed easily by multiplying the gain g_{m2} by (Q-1)/Q. Below are the equations showing how we plug in our gains, and finally our simplified transfer function that we will use in the second part of this problem.

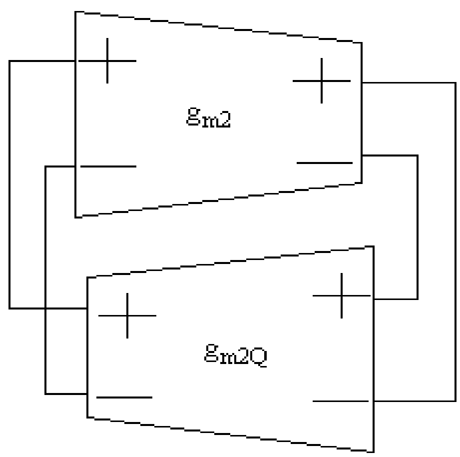
$$\frac{V_{out}}{V_{in}} = \frac{s\left(\left(\frac{g_{m1}}{(C_1+C_2)}\right)\bullet\left(\frac{C_1}{g_{m1}}\right)\bullet\left(\frac{g_{m3}}{(C_4)}\right)\right)+\left(\frac{g_{m1}}{(C_1+C_2)}\right)\bullet\left(\frac{g_{m3}}{(C_4)}\right)}{s^2+s\left(\frac{g_{m1}}{(C_1+C_2)}\right)\bullet\left(\frac{g_{m2}}{g_{m1}}-\frac{g_{m2}\bullet\left(\frac{Q-1}{Q}\right)}{g_{m1}}\right)+\left(\frac{g_{m1}}{(C_1+C_2)}\right)\bullet\left(\frac{g_{m3}}{(C_4)}\right)\bullet\left(\frac{g_{m4}}{g_{m1}}\right)}$$

$$\frac{V_{out}}{V_{in}} = \frac{s\left(\frac{g_{m3}C_1}{(C_1+C_2)C_4}\right)+\left(\frac{g_{m1}g_{m3}}{(C_1+C_2)C_4}\right)}{s^2+s\left(\frac{g_{m2}}{(C_1+C_2)}\right)\bullet\left(1-\frac{(Q-1)}{Q}\right)+\left(\frac{g_{m3}g_{m4}}{(C_1+C_2)C_4}\right)}$$

The way we can implement this filter is to put an extra transconductor in parallel with g_{m2} called g_{m2Q} except the input terminals of the transconductor are switched to subtract from the current being fed back by g_{m2}. In this way, we can make g_{m2} have any value we want as long as we make g_{m2Q} the right size using the following equation:

$$g_{m2Q} = g_{m2} \bullet \left(\frac{Q-1}{Q} \right)$$

This eliminates the problem of large component spread that can be a problem in the design of a "high-Q" filter. The extra transconductor is attached around g_{m2} in the following way.



Ex. 35.15 reads the following:
Use an active-RC filter (*In our case a transconductor-C filter*) to implement a filter with the response shown in Fig. 35.51 (*where Q is equal to 20*).

In order to do this, we need to make the constant term in our transfer function equal to zero. If we look at the equation above, we see that this can be done with the elimination of the transconductor g_{m1}. The simplified transfer function is shown below.

$$\frac{V_{out}}{V_{in}} = \frac{s\left(\frac{g_{m3}C_1}{(C_1+C_2)C_4}\right)}{s^2 + s\left(\frac{g_{m2}}{(C_1+C_2)}\right) \bullet \left(1 - \frac{(Q-1)}{Q}\right) + \left(\frac{g_{m3}g_{m4}}{(C_1+C_2)C_4}\right)}$$

Now we can follow the same approach used in example 35.15 to determine our values for g_{m2}, g_{m3}, g_{m4}, C_1, C_2, and C_4. Since we want the passband gain to be equal to one, the center frequency equal to 1.59 MHz, and Q equal to 20, we can form the following equation to determine our values.

$$2\pi f_0 = 10\times 10^6$$

$$Q = 20$$

$$a_1 = \frac{2\pi f_0}{Q} = \frac{10\times 10^6}{20} = 5\times 10^5 = \frac{g_{m3}C_1}{(C_1 + C_2)C_4} = \frac{1}{20}\left(\frac{g_{m2}}{(C_1 + C_2)}\right)$$

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{g_{m3}g_{m4}}{(C_1 + C_2)C_4}}$$

To simplify things, $g_{m2} = g_{m3} = g_{m4} = 10$uA/V. With a Q equal to 20, this means that our transconductor g_{m2Q} will have a value of 9.5uA/V. Solving the other equations gives us values of $C_1 = 0.05$pF, $C_2 = 0.95$pF, and $C_4 = 1$pF. This gives us values that are all close to the same values. If we were more concerned about matching capacitor values, we could set the capacitor values first and recalculate the capacitor values.

Solution for 35.28 by Sugato Mukherjee e-mail:msugato@ieee.org

Q: Repeat Ex. 35.13 using a digital filter.

Ans: We have to design a digital bandpass filter with center frequency f_o = 1.59MHz and Q=0.707. This can be done with the digital biquad filter whose general form is shown in Figure 35.64. The general form (s-domain) of the second order bandpass filter is given by

$$H(f) = \frac{a_1 s}{s^2 + \frac{(2\pi f_0)s}{Q} + (2\pi f_0)^2} \quad \ldots\ldots.(1)$$

Looking at equations 35.111 to 35.116 we can write that

$a_2=B_0=0$

$a_0=0 \Rightarrow (B_0+ B_1+ B_2) = 0 \Rightarrow B_1= - B_2$

$a_1=f_s B_1$

Let us take the sampling frequency f_s to be 100MHz which is much above the required center frequency of 1.59MHz so that equation 35.110 holds true.

Now we need to compute the coefficients A_1, A_2 and B_1 in accordance with our filter specifications.

Using equation 35.115 we have for our filter $\frac{2\pi(1.59)}{0.707\times 100} = (2 - A_1)$

which gives A_1=1.859

Using the value of A_1 in equation 35.116 we get

$\sqrt{1 - 1.859 - A_2} = \frac{2\pi(1.59)}{100}$ which gives A_2 = -0.869

$a_1=f_s B_1$ decides the "pass-band gain" of the filter. Putting $s=j\omega$ in (1) and evaluating the magnitude of the transfer function at $\omega=\omega_0=2\pi f_0$ we get

$$\left|H(j\omega_0)\right| = \frac{\omega_0 a_1}{\sqrt{(\omega_0{}^2 - \omega_0{}^2) + \frac{\omega_0{}^2\omega_0{}^2}{Q^2}}} = \frac{a_1 Q}{\omega_0} \ldots\ldots.(2)$$

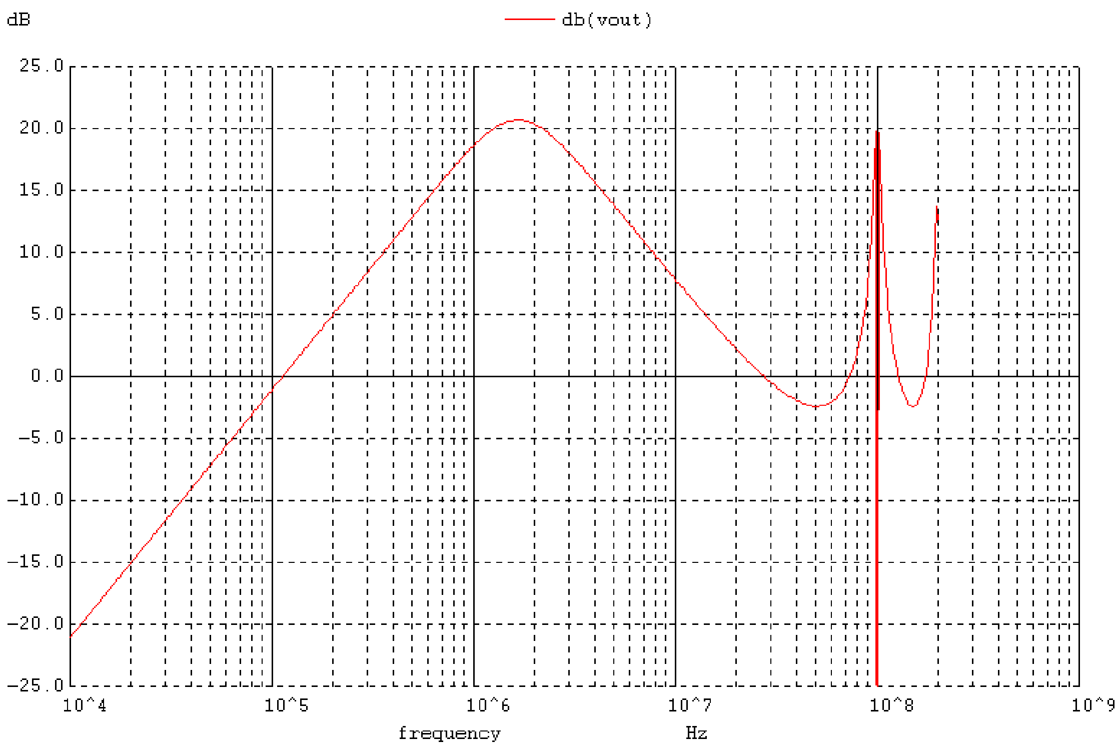
Taking our pass-band gain as 10, putting the values of a_1, ω_0 and Q we get

$$B_1 = \frac{10\times 2\pi(1.59)}{0.707\times 100} = 1.413$$

Thus we have all the design parameters needed for the band-pass filter. The filter netlist and the simulation results are shown next. For SPICE simulation, transmission lines are used as the delay elements and voltage-controlled-voltage-sources are used for the multipliers and adders. Note that we get our desired band-pass function only for input signal frequencies lower than approximately $\frac{f_s}{2}$ = 50MHz. For higher input signal frequencies , equation 35.110 is not valid.

Netlist used in simulation

```
* Solution for 35.28*

.AC DEC 100 10k 200MEG

*WinSPICE command scripts
*#destroy all
*#run
*#set units=degrees
*#plot db(vout) ylimit 25 -25

Vin     Vin     0       DC      0       AC      1

*Adders
Eadd1           Voadd1          0               Vin             Voadd2          1
Eadd2           0               Voadd2          Voa1            Voa2            1
Eadd3           Vout            0               Vob1            Vob2            1

*Delays using transmission lines and terminations
TZ1     Vod1    0       Voadd1          0       TD=10n          ZO=50
RZ1     Vod1    0       50
*Add buffer to ensure that the two delays don't load each other
Ebuf1   Vod11 0         Vod1    0       1
TZ2     Vod2    0       Vod11 0         TD=10n          ZO=50
RZ2     Vod2    0       50

*Multipliers
EB2     Vob2    0       Vod2    0       1.413
EB1     Vob1    0       Vod1    0       1.413
EA1     Voa1    0       Vod1    0       1.859
EA2     Voa2    0       Vod2    0       0.869

*Put load resistors in to avoid floating nodes
RL      Vout            0       1G
Radd1   Voadd1          0       1G
Radd2   Voadd2          0       1G
Roa1    Voa1            0       1G
Roa2    Voa2            0       1G

.end
```



The above figure shows the magnitude plot for the frequency response of the digital band-pass filter. Note that the gain at the center frequency is ~10 (=20dB).

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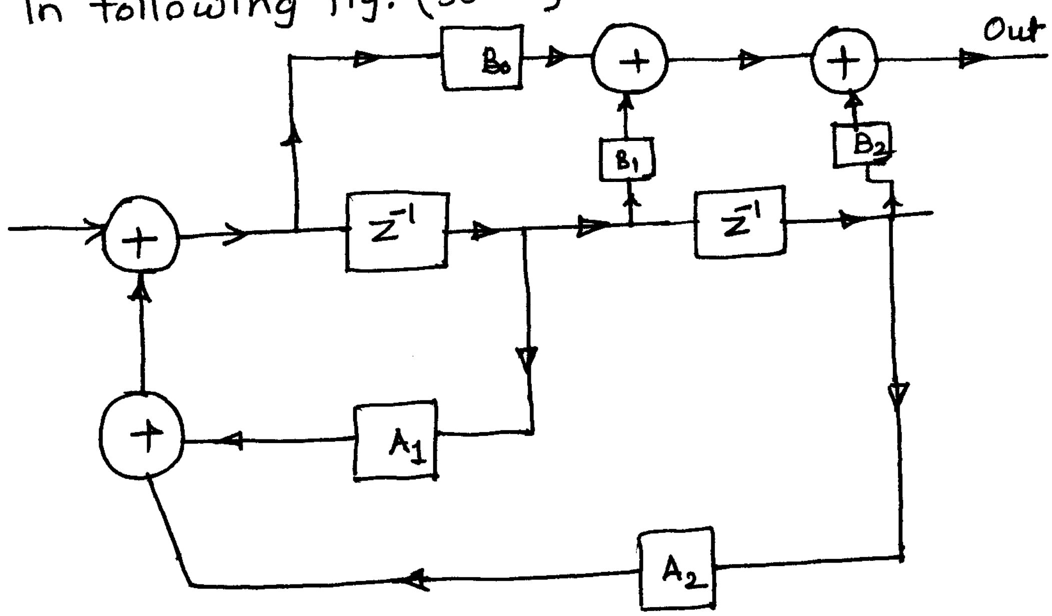
Solution for 35.29 by Pandurang Irkar

Prob. 35.29

Repeat Ex. 35.14 using a digital filter.

Soln : Referring to Ex. 35.14 (& 35.11 & 35.13). We have to design a digital band pass filter with center frequency $f_0 = 1.59\,MHz$ and $Q = 20$. It can be done with digital Biquad form shown in following fig. (35.64)



Writing the transfer function

$$H(f) = \frac{a_1 s}{s^2 + \left(\frac{2\pi f_0}{Q}\right)s + (2\pi f_0)^2} \quad \text{———} \ (*)$$

The equation from 35.110 to 35.116 gives that

$$a_2 = B_0$$
$$a_1 = f_s(2B_0 + B_1)$$
$$a_0 = f_s^2(B_0 + B_1 + B_2)$$
$$\frac{2\pi f_0}{Q} = f_s(2 - A_1)$$

$$f_0 = \frac{f_s}{2\pi}\sqrt{(1-A_1-A_2)}$$

From ✱

$$\boxed{a_2 = B_0 = 0}$$

$a_0 = 0 \Rightarrow B_0 + B_1 + B_2 = 0$

$$\boxed{B_1 = -B_2}$$

$$\boxed{a_1 = f_s \cdot B_1} \longrightarrow \text{Pass Band gain.}$$

For the center frequency ⇒ 1.59 MHz, We can take sampling frequency 100 MHz which can satisfy the Nyquist critera completely.

We need to Calculate the coefficients A_1, A_2 and B_1 with the specifications $f_0 = 1.59$ MHz and $Q = 20$

From equation 35.115

~~35.115~~

$$\frac{2\pi f_0}{Q} = f_s(2 - A_1)$$

$$\frac{2\pi \times 1.59}{20 \times 10} = 2 - A_1$$

$$\boxed{A_1 = 1.9950}$$

From equation 35.116

$$f_0 = \frac{f_s}{2\pi} \cdot \sqrt{(1-A_1-A_2)}$$

putting the above value of A in 35.116

We get

$$\boxed{A_2 = 1.0049}$$

To find B_1 ; We know $a_1 = f_s \cdot B_1$ → decides the pass band gain

~~Byt~~ putting $s = j\omega$ in eqn (*) and taking the magnitude

$\because \omega_0 = 2\pi f_0$.

$$|H(j\omega)| = \frac{\omega_0 a_1}{\sqrt{(\omega_0^2 - \omega_0^2) + \frac{\omega_0^2 \omega_0^2}{Q^2}}} = \frac{a_1 Q}{\omega_0} \Rightarrow (**)$$

put $a_1 = f_s B_1$ in eqn (**) and equating to a pass band gain $\approx \underline{\underline{20}}$ (Assumed)

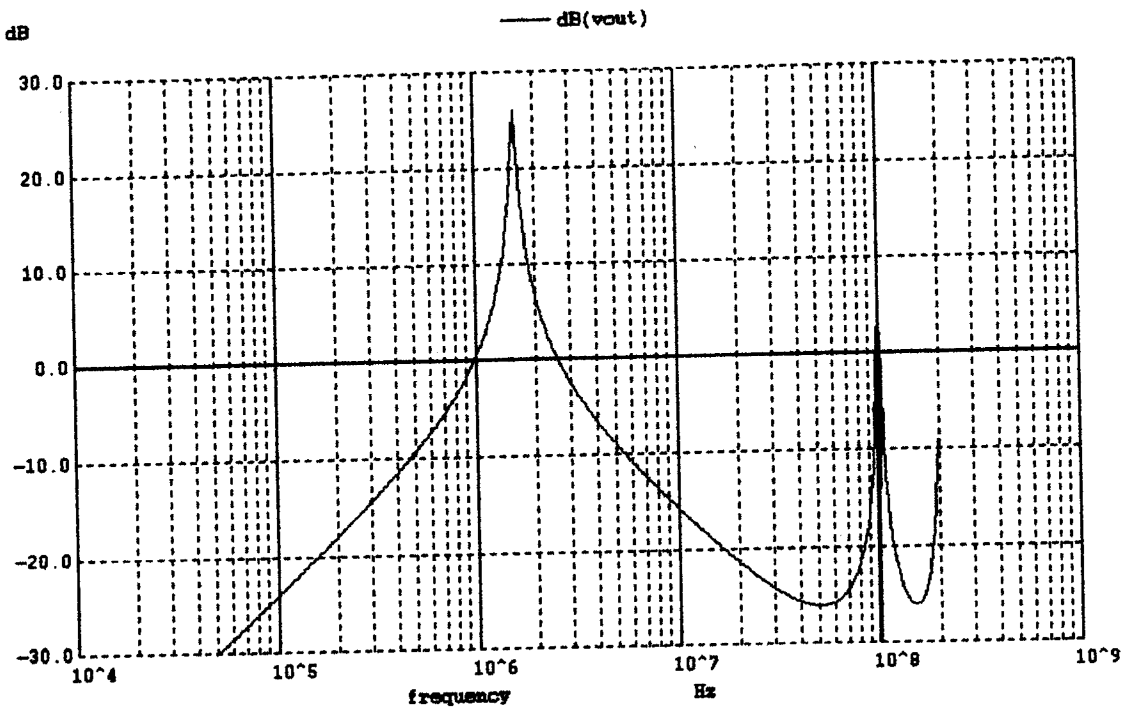
$$20 = \frac{1.59 \times B_1 \times 20}{2\pi \cdot 159}$$

$$\boxed{B_1 = 0.099}$$

Thus we found the coefficients. ~~for ou~~ The netlist and simulated results are shown on the following pages. The simulated results shows the effect of high Q i.e. sharp ~~select~~ selectivity of frequency.

Biquad Bandpass Digital filter

```
.control
destroy all
run
set units=degrees
plot dB(vout) ylimit 25 -25
.endc

.AC DEC 100 10k 200MEG

*Input Signal
Vin Vin 0 DC 0 AC 1

*Adders
Eadd1 Voadd1 0 Vin Voadd2 1
Eadd2 0  Voadd2  Voa1 Voa2 1
Eadd3 Vout 0 Vob1 Vob2 1

*Delays Using transmission line and termination
TZ1 Vod1 0 Voadd1 0 TD=10n ZO=50
RZ1 Vod1 0 50

*Add buffer to avoid loading
Ebuf1 Vod11 0 Vod1 0 1
TZ2 Vod2 0 Vod11 0 TD=10n ZO=50
RZ2 Vod2 0 50

*multipliers
EA1 Voa1 0 Vod1 0 1.9950
EA2 Voa2 0 Vod2 0 1.0049
EB1 Vob1 0 Vod1 0 0.099
EB2 Vob2 0 Vod2 0 0.099

* Load resistors
RL Vout 0 1G
Radd1 Voadd1 0 1G
Radd2 Voadd2 0 1G
Roa1 Voa1 0 1G
Roa2 Voa2 0 1G
.end
```



With Q=20 and Gain of Passband=20, we have here Gain =26dB at center frequency

Problem 35.30

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Show, using biquad sections, how the following lowpass ladder filter would be implemented.

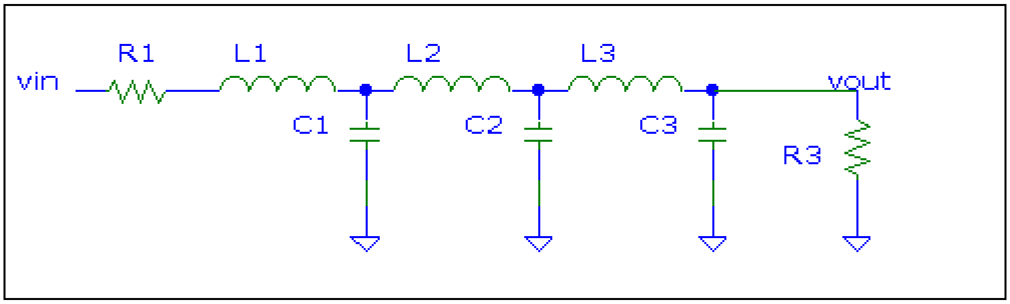

Fig 35.76

To implement biquad sections for Fig 35.76, the stages can be broken up in to three sections. Each section will have a transfer function that can be implemented using a biquadratic filter. The three sections of the filter are shown below in Fig1.

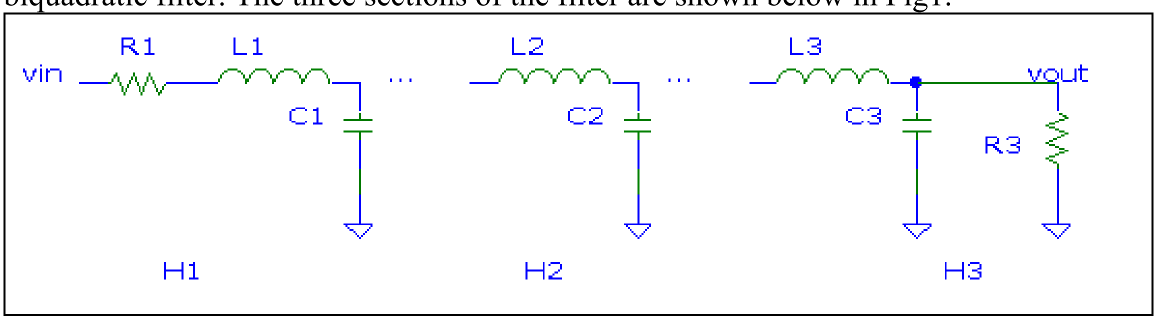

Fig 1

Each stage has a transfer function (H1, H2, and H3) that can be implemented with a biquadratic filter.

The transfer functions and Q's are:

$$H_1 = \frac{vout_1}{vin} = \frac{1/L_1C_1}{s^2 + sR_1/L_1 + 1/L_1C_1} \qquad Q_1 = \frac{1}{R_1}\sqrt{\frac{L_1}{C_1}} \qquad f_o = \frac{1}{2\pi\sqrt{L_1C_1}}$$

The second transfer function, H_2, is the same as the H_1 but the input resistance, R_2, is 0. This gives the transfer function shown below and a Q of infinity.

$$H_2 = \frac{vout_2}{vout_1} = \frac{1/L_2C_2}{s^2 + 1/L_2C_2} \qquad Q_2 = \infty \qquad f_o = \frac{1}{2\pi\sqrt{L_2C_2}}$$

$$H_3 = \frac{vout}{vout_2} = \frac{1/L_3C_3}{s^2 + s/R_3L_3 + 1/L_3C_3} \qquad Q_3 = R_3\sqrt{\frac{C_3}{L_3}} \qquad f_o = \frac{1}{2\pi\sqrt{L_3C_3}}$$

problem 35.30 continued…

• *Implementation of a biquad section for H_1*

The thing to do is compare the biquad transfer function, equation 35.80, with the desired transfer function to easily see what the biquadratic transfer function components need to be. This is shown below.

$$BiquadTF_1 = H_1 = \frac{a_2 s^2 + a_1 s + a_o}{s^2 + \left(\frac{2\pi f_o}{Q_1}\right)s + (2\pi f_o)^2} = \frac{1/L_1C_1}{s^2 + sR_1/L_1 + 1/L_1C_1}$$

Comparing the $biquadTF_1$ with H_1 it is easy to see that,

$$a_2 = a_1 = 0 \qquad a_o = 1/L_1C_1 \qquad \left(\frac{2\pi f_o}{Q_1}\right) = R_1/L_1 \qquad (2\pi f_o)^2 = 1/L_1C_1$$

• *Implementation of a biquad section for H_2*

Using the same approach,

$$BiquadTF_2 = H_2 = \frac{a_2 s^2 + a_1 s + a_o}{s^2 + \left(\frac{2\pi f_o}{Q_2}\right)s + (2\pi f_o)^2} = \frac{1/L_2C_2}{s^2 + 1/L_2C_2}$$

looking above, it is easy to see that,

$$a_2 = a_1 = 0 \qquad a_o = 1/L_2C_2 \qquad (2\pi f_o)^2 = 1/L_2C_2$$

$\left(\frac{2\pi f_o}{Q_2}\right) = 0$, which occurs because for this section, remember, Q_2 is infinite.

• *Implementation of a biquad section for H_3*

$$BiquadTF_3 = H_3 = \frac{a_2 s^2 + a_1 s + a_o}{s^2 + \left(\frac{2\pi f_o}{Q_3}\right)s + (2\pi f_o)^2} = \frac{1/L_3C_3}{s^2 + s/R_3L_3 + 1/L_3C_3}$$

and it can be seen that the components for this biquad filter will be,

$$a_2 = a_1 = 0 \qquad a_o = 1/L_3C_3 \qquad \left(\frac{2\pi f_o}{Q_3}\right) = \frac{1}{R_3L_3} \qquad (2\pi f_o)^2 = 1/L_3C_3$$

As we read in pages 429-448 of the book, Biquadratic Filters can be made by using Active-RC implementation, Switched-Capacitor implementation, Transconductor-C implementation, or digitally.

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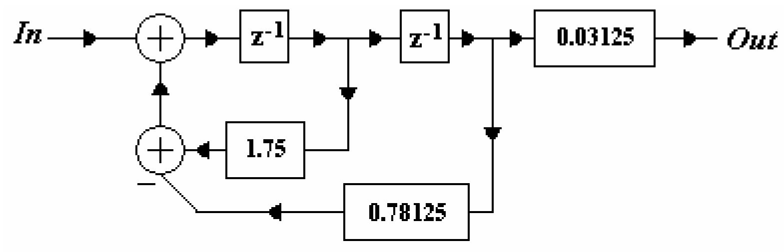
35.31) *Show how to implement the multipliers used in Ex. 35.20.*

Soln:

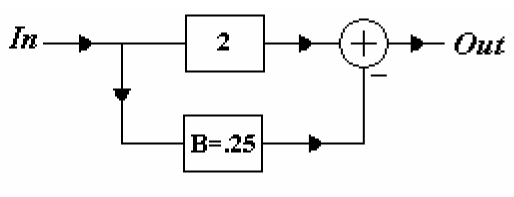
The block diagram with the multipliers needed to implement is shown:



We can see that we need to implement multipliers with the following values of 1.75, 0.78125 and 0.03125.

For A_1=1.75, 1.75=1*(2) - 0.25
A_2=0.78125, 0.78125=1 - 0.125 + .03125
A_3=0.03125 we will simply shift the word to the right five times

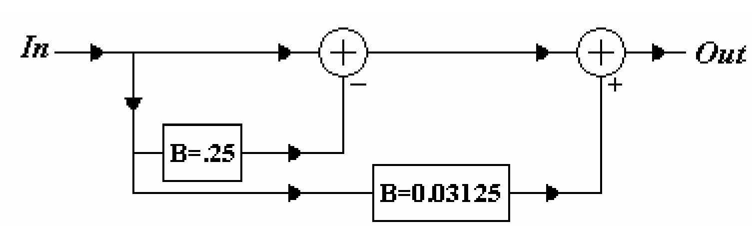
The implementation with one adder is shown for A_1



Following step-by-step through the adder we get:

Input	1
Multiply by 2	2 (add a zero to the two's complement of the input)
Multiply by 0.25	0.25 (shift to the right by 2)
Subtract 2 – 0.25	=1.75

We can do the same for the next multiplier, the implementation with two adders is shown for A_2.



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Following step-by-step through the adder we get:

Input	1	
Subtract by 0.25	0.75	
Multiply by 0.01325	0.03125	(shift word to the right five times)
Add 0.75 + 0.03125	0.78125	

For the A_3 multiplier we can simply shift the word to the right five times before passing it on to the output.

Solution by:
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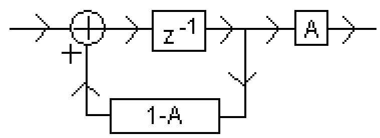
Problem 35.32
Show that the filter shown in Fig. 35.77 can be implemented using a single multiplier.

Solution
First of all, let's take a look at the figure.



Now let's eliminate the feedback loop, using the basic feedback equation where G(z) is the forward gain, and H(z) is the feedback gain.

$$\frac{G(z)}{1 \mp G(z)H(z)} \qquad \text{(EQ. 1)}$$

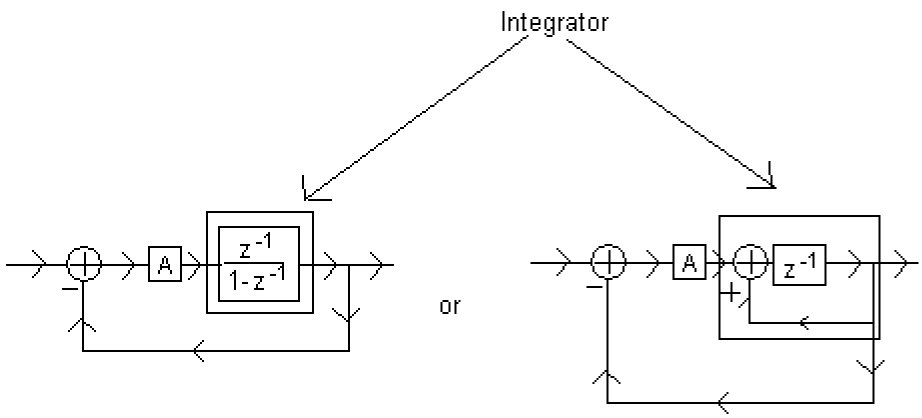
Using this equation, and multiplying the entire equation by A (the gain at the output of the filter) we obtain the following transfer function.

$$\frac{Az^{-1}}{1 - z^{-1} + Az^{-1}} \qquad \text{(EQ. 2)}$$

Now if we divide both the numerator and denominator by the quantity $1\text{-}z^{-1}$, we obtain the following equation for our transfer function.

$$\frac{\dfrac{Az^{-1}}{1 - z^{-1}}}{1 + \dfrac{Az^{-1}}{1 - z^{-1}}} \qquad \text{(EQ. 3)}$$

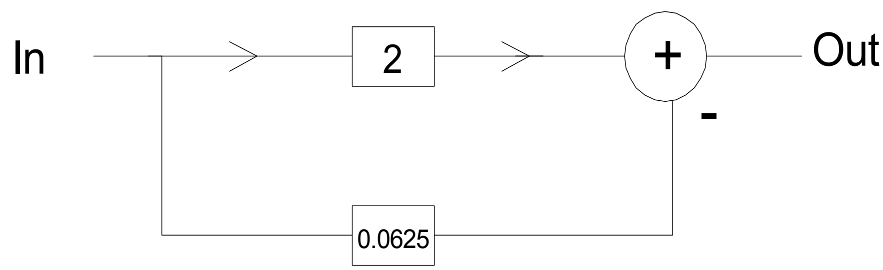
If we examine this equation closely, we find that this can be interpreted as an equation of the form of (EQ. 1) above, where $G(z)=Az^{-1}/(1-z^{-1})$, and $H(z)=1$. This means we can draw a block diagram of the filter where the multiplier (A) is in the loop, with an additional forward gain of $z^{-1}/(1-z^{-1})$, with a unity feedback. This drawing is shown below, with an alternative representation to the right of it. Notice that both implementations are equivalent, and both implement a single multiplier with a gain of A.


Integrator
A
z -1
1- z -1
or
A
z -1

Problem 35.33

Show how the output of a single-bit, noise-shaping modulator would be multiplied by 1.9375. Make sure that the detail on converting the modulator's output to two's complement is show.

This multiplier can be implemented using a single adder along with the associated multiplication factors as shown below,



$$A=1.9375= 2 - 0.0625$$

For example, suppose the output of a single-bit, noise-shaping modulator is 1. To begin the multiplying, simply change the output into a two's complement number,

1 -> 01

To multiply a word by 2, we just simply add a zero to the end of the word,

01 - > 010

To multiply by 0.0625, simply insert four zeros in between the sign-bit and remaining part of the word (when the word is positive),

01 - > 000 001