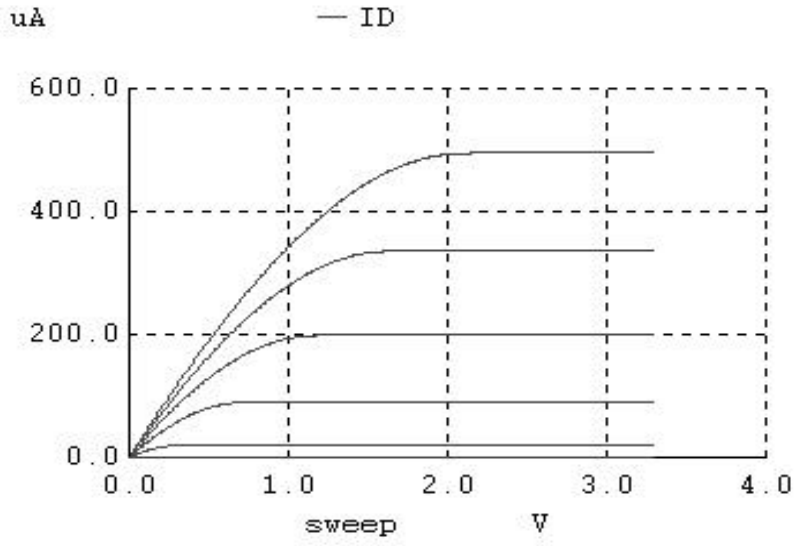
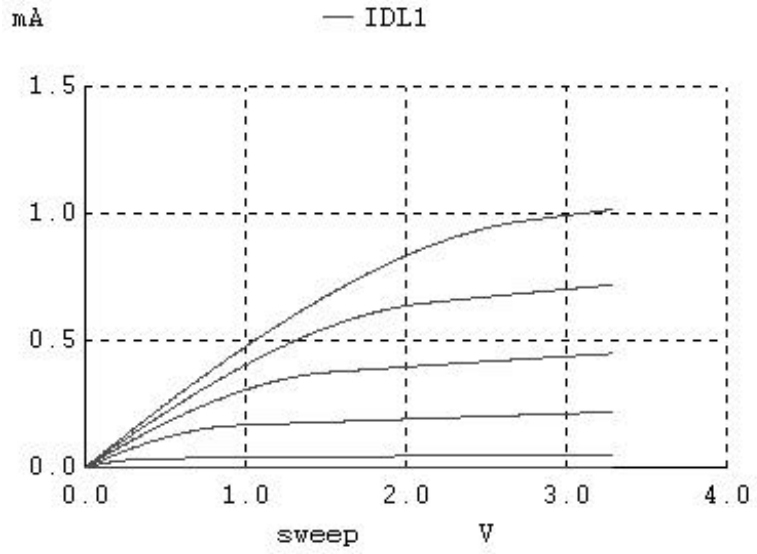
Problem 33.1 Regenerate the plots shown in Fig. 33.1 using an L of 5 μm and a W of 15 μm. Do the curves look similar? Could we use the Level 1 model with long L devices?





The two plots above are the result of using the SPICE netlist for Figure 33.1 and changing L and W to 5 μm and 15 μm, respectively. The plots do not look the same. Modern submicron devices are engineered to drop large voltages over small distances. Increasing the channel length doesn't cause an increase in the depletion layer thickness between the channel and the drain. It only increases the channel (that portion that is not depleted) charge.

Tyler J. Gomm
tjgomm@micron.com

33.2 Can we use a native MOSFET in an application where we need a small threshold voltage? What are the limitations?

The native MOSFET can be used in certain applications requiring a small, or even negative, threshold voltage. The MOSFET is laid out as shown in Fig. 33.4, creating a depletion device with a very low threshold voltage.

This device can also be used to create a capacitor with better capacitance range (see Fig. 33.4c). Note that this style of capacitor should not be used when a true bipolar capacitor is required.

A significant limitation of this device as a transistor is the finite output resistance. The N+ active areas are essentially shorted together by the n-well, lowering the output resistance. This reduces the usefulness of the transistor in analog designs where high output impedance is necessary for good linear response.

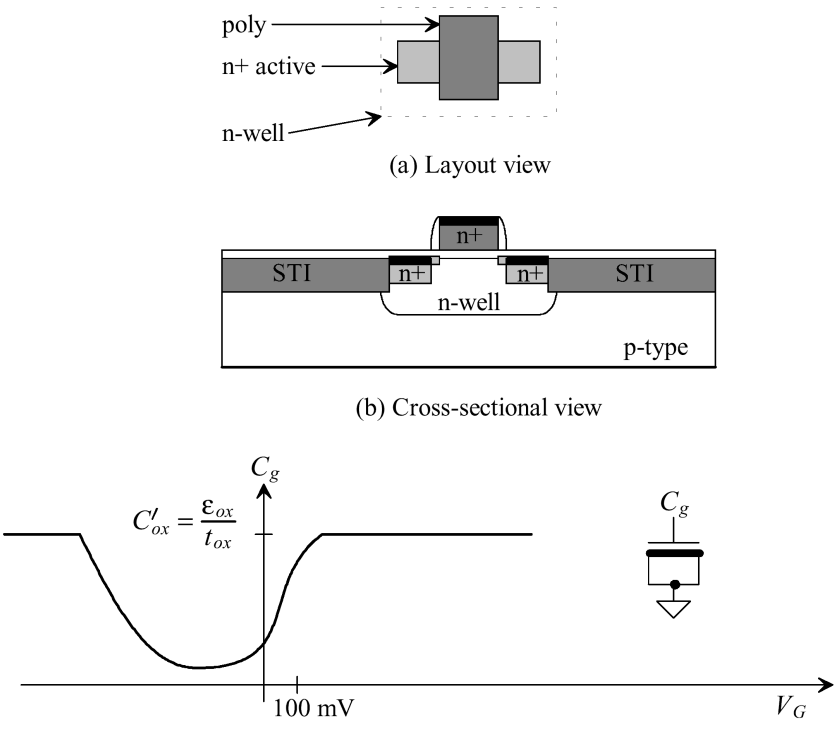


Figure 33.4 The Native or Natural MOSFET.

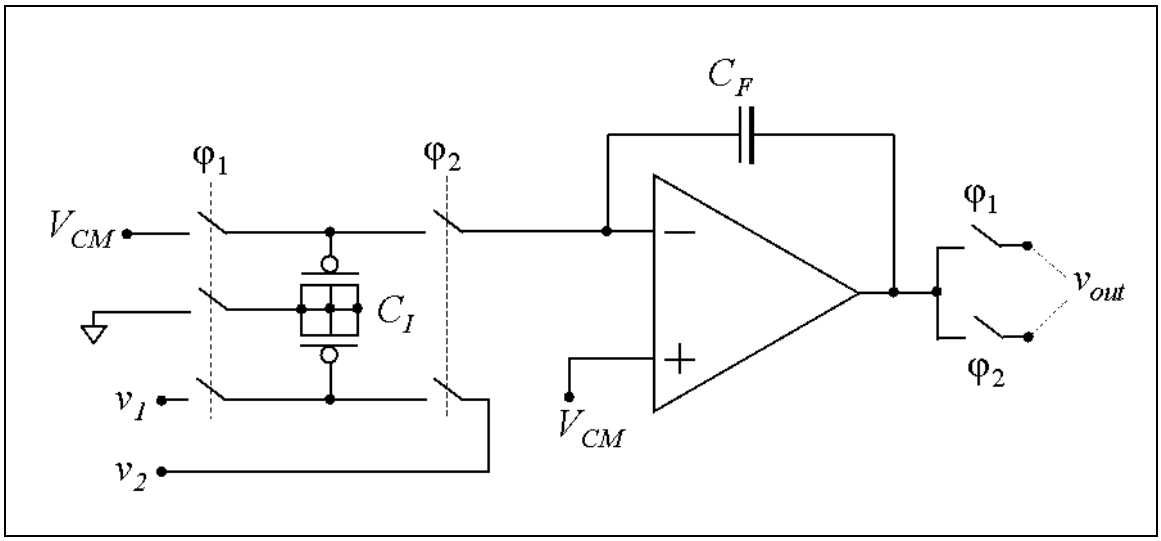
David Goldman

EE 515 – CMOS Mixed-Signal IC Design

Problem 33.3

Question: Sketch the implementation of a floating capacitor that uses a MOSFET switch to connect the source/drain/bulk to ground. Show the capacitor used in a DAI, Fig. 31.78. Assume the switch connected to the capacitor is clocked with the φ_1 clock (why?). Explain the operation of the circuit.

Answer: A DAI implemented with a floating capacitor is shown below.



The operation of this circuit can be described in two states; namely, φ_1 is the charging state and φ_2 is the state that transfers charge to the output. During the charging state (φ_1 closed), the floating capacitor's source/drain/body is connected through a resistive MOSFET switch to ground. If v_1 and v_2 are greater than V_x (see Fig. 33.5 on page 240 of the textbook for a definition of V_x) then C_I will charge. The φ_1 switch is then opened.

When the state changes to φ_2 closed, the charge on the floating capacitor will flow to v_{out}. In this state, φ_1 must be open to prevent the capacitor's charge from moving to ground. Other than the floating capacitor, the DAI operates in the same way as described in the textbook.

Gexin

Problem 33.4: Sketch the practical layout of a 10K n+ poly resistor using a silicide block.

Solution for 33.4:

From table 33.1, the square resistance for n+ poly resistor using silicide block is 3ohm/sq. For a 10K resistor, about 3333 squares are needed.

To achieve better matching, in general, the resistor's width and length should be at least 10 and 100 times the minimum feature size of the process, respectively. Assume $L_{\min} = 0.15um$, here the length is chosen 3um.

The sketched layout is shown below:
Here is the layout for 1K ohm resistor cell.

This is the layout for 10K ohm. It consists of 10 resistor cells.

Brandon Roth

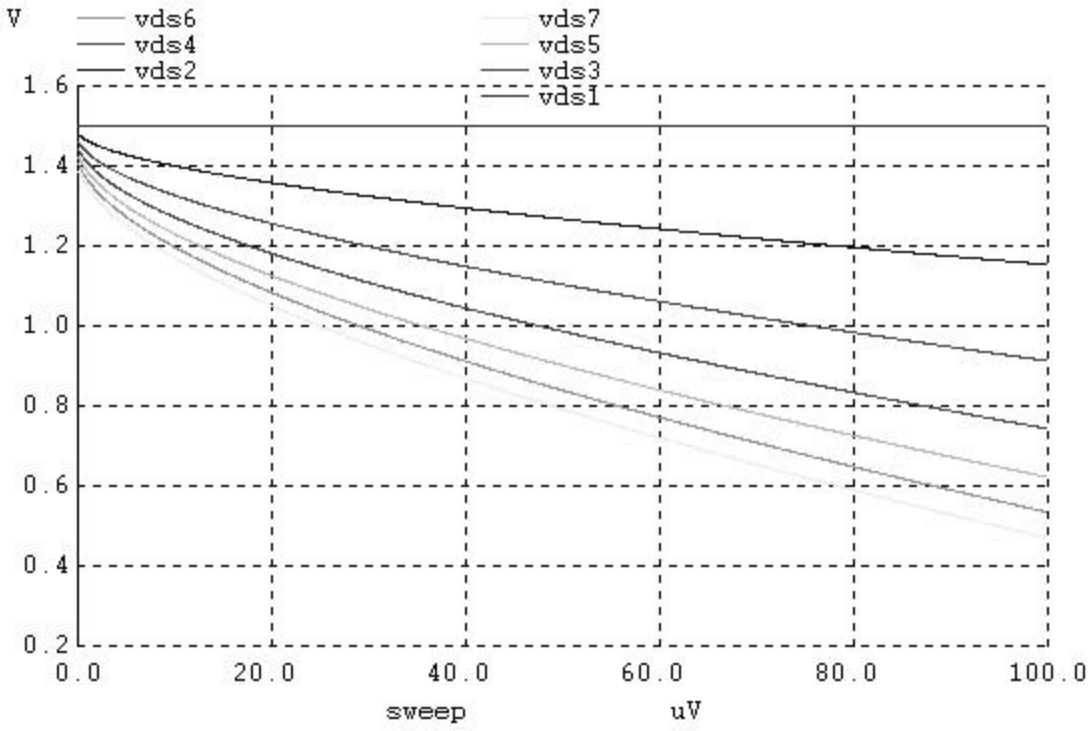
33.5 Verify the error in Fig. 33.18 is due to differing device drain-source voltages. Show that using an even longer length device can result in less error.

In the netlist that generates Fig. 33.18 the error for each binary weighted current is calculated by first scaling the binary weighted current to the reference current. Then the difference of the scaled current from the reference is divided by the reference current and multiplied by 100. The result is the percentage error from the reference current. This is calculated for each binary weighted current in the W-2W current mirror.

Each branch of the current mirror has the same gate voltage, but different source voltages. Each successive branch has a higher source voltage where the first branch has a source voltage equal to zero. Therefore each VGS and VDS is different.

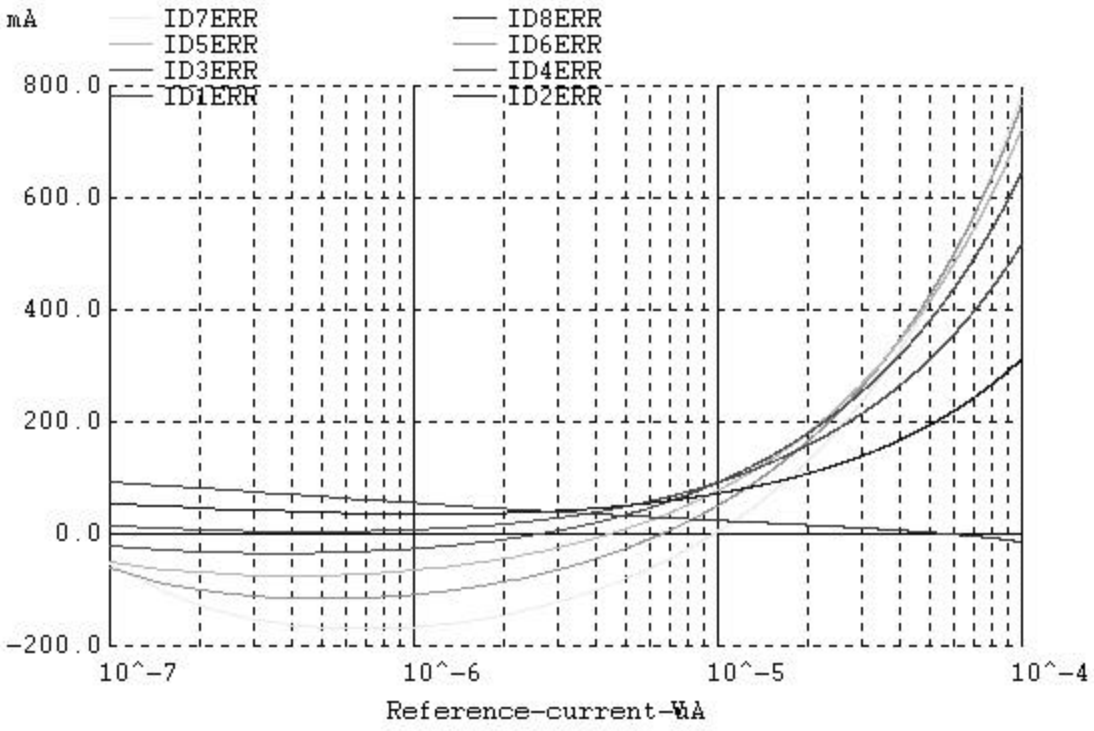
The currents are scaled or weighted by the changing values of VGS. As seen in an ID vs VDS MOSFET characterization curve, as VGS increases the current ID increases. Assuming that the current mirror is biased so that all the MOSFETs are in the saturation region, as VDS varies the current remains the same for the ideal MOSFET where the output resistance is infinite. Then it follows if the currents for each binary weighted branch are then scaled up by the corresponding binary factor, the result should be equal to the reference current. However, figure 33.18 shows error in these scaled currents. This error is due to the output resistance of the MOSFET's not being infinite (there is a slope in the ID vs. VDS curve), so that changing VDS causes changes in ID.

In the figure below VDS is plotted for each branch. This figure does show that VDS is varying between the branches. Then from the previous discussion, if the current for any given branch is not equal to the reference current after being scaled, the error is due to the current varying with VDS and not remaining constant (non-ideal MOSFETs).



Varying VDS for each binary weight branch.

If a longer length device is used then the error for each branch current is reduced. Comparing the figure below to Fig. 33.18, the error has decreased from 2 percent to 0.8 percent by increasing the length from 5um to 50um. Increasing the length results in smaller changes in the current with changes in VDS, in other words higher output resistance.



Percentage error from ideal current for each binary weighted branch.

EE515: CMOS Mixed-Signal IC Design

Problem 33.6
Jim Slupe

33.6 If the drawn area of a source implant is 100 m^2 what is the actual area if a scale factor of 0.15 um is used?

Answer: Since the scaling factor is being applied to an area, the formula would be:

$$\text{actual area} = (\text{drawn area}) \times (\text{scaling factor})^2$$

Substituting the terms given here:

$$\text{actual area} = 100 \text{ meters} \times (0.15 \text{ um} \times 0.15 \text{ um})$$

$$\text{actual area} = 2.25 \times 10^{-12} \text{ m}^2$$

33.7
Jeremy Rice

Find tphl & tplh for the inverter and nand gate shown in fig 33.90
I assumed an L of .5 for this problem

To do this, use eqn's

33.3 $Rn = 10k \cdot \frac{L}{W}$

33.4 $Rp = 20k \cdot \frac{L}{W}$

For the inverter, because the p is twice the size of the n, and rp is twice that of rn, tplh=tphl

$$tphl = 10k \cdot \frac{.5}{20} \cdot 1 \cdot 10^{-12}$$ =250ps

For the nand gate, tplh is the two p's in parallel driving 1pF, and tphl is the two n's in series driving 1pF

$$tplh = 20k \cdot \frac{.5}{40 \cdot 2} \cdot 1p = 125ps$$

$$tphl = 10k \cdot \frac{.5 \cdot 2}{20} \cdot 1p = 500ps$$

EE515: CMOS Mixed-Signal IC Design
Brian Bergeson
Problem 33.8
brian_bergeson@amis.com

Problem 33.8:

Using Winspice results tabulate the output amplitude of the circuit in Fig. 33.32 against capacitive load.?

Solution:

Capacitive_load	Output Amplitude
0F	2.85V
10fF	2.82V
20fF	2.78V
100fF	2.60V
200fF	2.40V
500fF	1.93V
1pF	1.37V (amplitude becomes < VDD as cap load reaches 1pF)
2pF	900mV
5pF	475mV
10pF	245mV

The outputs of Fig. 33.32 are each driven by a Charge-pump clock driver (see Fig. 33.31). The peak amplitude of this clock driver approaches 2*VDD=2*1.5V=3.0V. The amplitude of the output signals approaches this limit when they have little or no capacitive loading. As their capacitive loading increases, the amplitude of the output signals decreases (see table of Cap_load vs. Out_Amp above). The charge supplied to each load comes from a 1pF cap inside the clock drivers (see Fig. 33.31). As the capacitive loads reach 1pF the amplitude of the outputs becomes less than VDD. This is because the capacitive loads are equal in capacitance to the capacitors that supply their charge. The cap loads take as long to charge up, as do the caps supplying their charge. The amplitude of the outputs continue to become smaller than VDD as the capacitive loads become greater than the caps that supply there charge.

In order to drive a load of 1pF (or more) to an amplitude of VDD (or more), the charge supplying caps, inside the clock drivers, must be increased accordingly.

EE515: CMOS Mixed-Signal IC Design
Question 33.10
Richard Friel
Rich_Friel@AMIS.COM

Question: #33.10

Modify the design of the digital input buffer shown in Fig. 33.39 using the topology shown in fig. 33.78. Show that the circuit still functions as expected using simulations.

Solution:

Spice model for Fig 33.40.

```
****** Figure 33.40 CMOS: Mixed-Signal Circuit Design *

*#destroy all
*#run
**#plot vin vref vout voutb
*#plot vout voutb

X1 Vin Vo1 Vdd invert
X2 Vref Vo2 Vdd invert
X3 Vo2 Vo2 Vdd invert
X4 Vo1 Vo2 Vdd invert
X5 Vo2 Vo1 Vdd invert
X6 Vo1 Vo1 Vdd invert
X7 Vo1 Vout Vdd invert
X8 Vo2 Voutb Vdd invert

Vdd     Vdd 0 DC 1.5
Vin Vin 0 DC 0 pulse 0.5 1.0 5n .1n .1n 2n 5n
Vref Vref 0 DC .75

*.tran .1n 25n 0 .1n
.dc Vin  0 1.5 .001 Vref 0.7 0.95 0.2
.options scale=0.15u

.subckt invert Vin Vout Vdd
M1      Vout Vin 0 0 NMOS  L=1 W=10
M2      Vout Vin Vdd Vdd PMOS  L=1 W=20
.ends

*** SPICE Models

*** Models created by Daniel Foty.
*** (c) 2001, Gilgamesh Associates and EPFL - All rights reserved.
*** These models are provided without warranty or support.
*** These models represent a completely fictitious 0.15um process, and do
***   NOT correspond to any real silicon process.  They are provided expressly for
***   use in the examples provided in this text, and should not be used for any
***   real silicon product design.
```

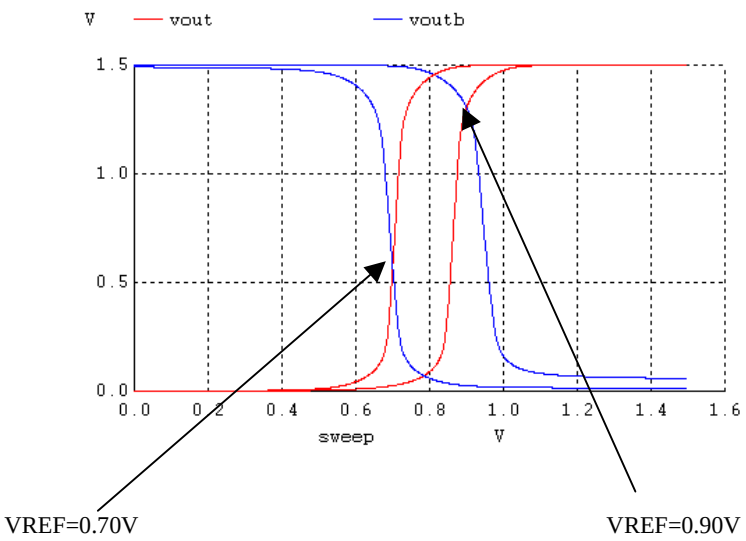
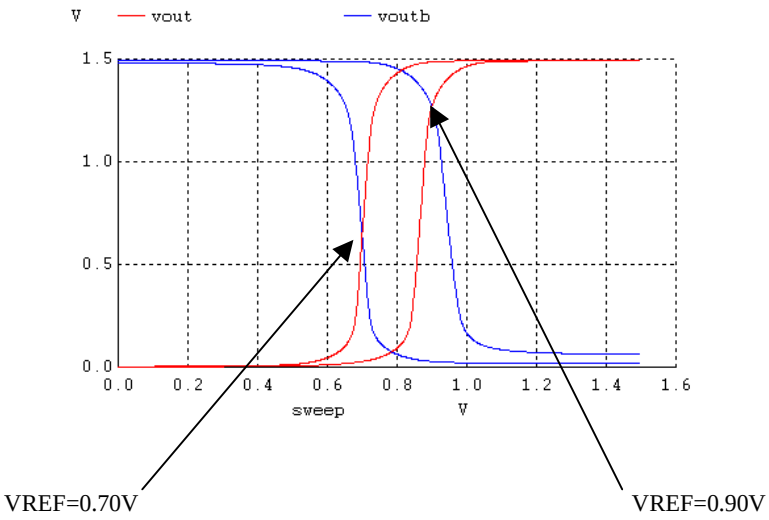


Fig 33.40

To implement Fig 33.78 into the above spice code, insert the following spice code to implement Fig. 33.78. The resistors must be greater than or equal to 100K-Ohms or the current feedback is to large.

r1 vout mid 100k
r2 voutb mid 100k
xne1 vout mid vdd invert
xne2 voutb mid vdd invert

If the above spice code is implemented, the resulting simulation result is:



The simulation result is the the same. The switch point for Vref=0.70V is about 100mV higher than in the previous example but now common-mode noise elimination has been implemented to balance the outputs of the op-amp.

33.11 Show, using simulations, that the circuits in Fig. 33.47 do indeed behave as counters.

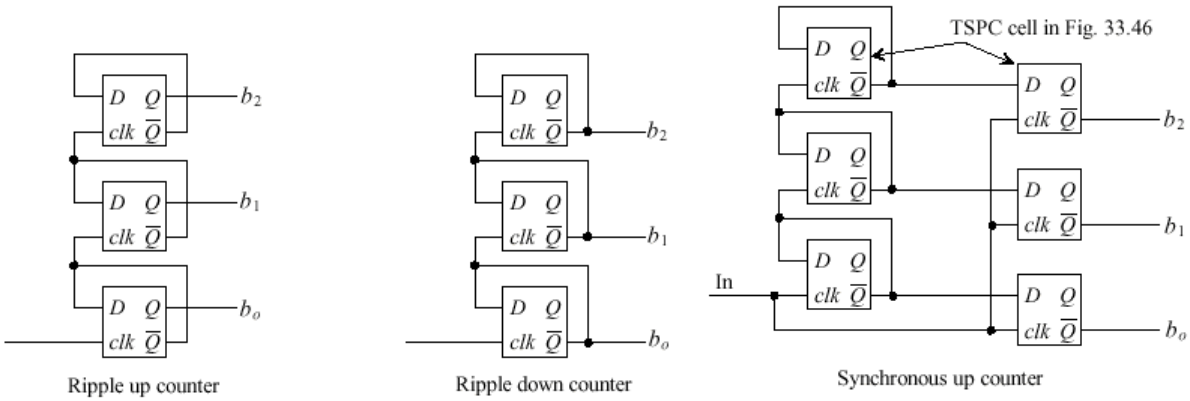


Figure 33.47

Solution:
The netlists for these three simulations and their outputs are given below:

```
* Problem 33.11 CMOS: Mixed-Signal Circuit Design - ripple up *

*#destroy all
*#run
**#plot phi phib
**#plot vdd#branch
*#let Iavg=mean(vdd#branch)
*#let b0=vout+2
*#let b1=vout2+4
*#let b2=vout3+6
*#let b0n=vout4+2
*#let b1n=vout5+4
*#let b2n=vout6+6
*#plot clk b0n b1n b2n
**#plot clk b0 b1 b2 b0n b1n

Vdd   Vdd 0 DC 1.5
Vclk clk 0 DC 0 pulse 0 1.5 0 .1n .1n 4.9n 10n

X1 Vout Vout clk vdd dtspc
X2 Vout2 Vout2 Vout vdd dtspc
X3 Vout3 Vout3 Vout2 vdd dtspc
X4 Vout Vout4 vdd invrt
X5 Vout2 Vout5 vdd invrt
X6 Vout3 Vout6 vdd invrt
CL Vout 0 30f
CL2 Vout2 0 30f
**CL3 Vout3 0 30f

.tran .2n 80n 0n .2n
.option ITL4=100 scale=0.15u reltol=0.10 vntol=20m abstol=2n

.subckt invrt Vinv Voutv Vdd
M10 Voutv Vinv 0 0 NMOS L=1 W=10 PD=20
M11 Voutv Vinv Vdd Vdd PMOS L=1 W=20 PD=40
.ends

.subckt dtspc Vin Vout clk Vdd
M1 1 Vin 0 0 NMOS  L=1 W=10 PD=20
```

```
M2 1 clk 2 Vdd PMOS L=1 W=20 PD=40
M3 2 Vin Vdd Vdd PMOS L=1 W=20 PD=40
M4 3 clk 0 0 NMOS L=1 W=10 PD=20
M5 4 1 3 0 NMOS L=1 W=10 PD=20
M6 4 clk Vdd Vdd PMOS L=1 W=20 PD=40
M7 5 4 0 0 NMOS L=1 W=10 PD=20
M8 Vout clk 5 0 NMOS L=1 W=10 PD=20
M9 Vout 4 Vdd Vdd PMOS L=1 W=20 PD=40
.ends

.MODEL nmos nmos  level=1 VTO=0.4 GAMMA=0.71 PHI=0.97 KP=453E-6
+ CJ=1.0E-3 CJSW=2.0E-10 MJ=0.5 MJSW=0.3 PB=0.9 tox=40e-10

.MODEL pmos pmos  level=1 VTO=-0.4 GAMMA=0.69 PHI=0.87 KP=92.15E-6
+ CJ=1.3E-3 CJSW=2.5E-10 MJ=0.5 MJSW=0.35 PB=0.9 tox=40e-10

*** SPICE Models

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*** These models are provided without warranty or support.
*** These models represent a completely fictitious 0.15um process, and do
***   NOT correspond to any real silicon process.  They are provided
expressly for
***   use in the examples provided in this text, and should not be used for
any
***   real silicon product design.

*** NMOS EKV MOSFET Model ************************************************
*** Level=44 in WinSPICE and ELDO, Level=55 in ADM/HSPICE, Level=5 in PSPICE,
*** Level=EKV in Spectre
*** Lmin=0.15u Wmin=1.05u (If Scale=0.15u then Lmin=1 and Wmin=7)
*---------------
.MODEL nmos1 nmos
+ LEVEL=44

*** Setup Parameters
+ UPDATE=2.6

*** Process Related Model Parameters
+ COX=9.083E-3 XJ=0.15E-6

*** Intrinsic Model Parameters
+ VTO=0.4 GAMMA=0.71 PHI=0.97 KP=453E-6
+ E0=88.0E6 UCRIT=4.0E6
+ DL=-0.05E-6 DW=-0.02E-6
+ LAMBDA = 0.30 LETA=0.28 WETA=0
+ Q0=280E-6 LK=0.5E-6

*** Substrate Current Parameters
+ IBN=1.0 IBA=200E6 IBB=350E6

*** Intrinsic Model Temperature Parameters
+ TNOM=27.0 TCV=1.5E-3 BEX=-1.5 UCEX=1.7 IBBT=0

*** 1/f Noise Model Parameters
+ KF=1E-27 AF=1

*** Series Resistance and Area Calculation Parameters
+ HDIF=0.24e-6 ACM=3 RSH=5.0 RS=1250.526
```
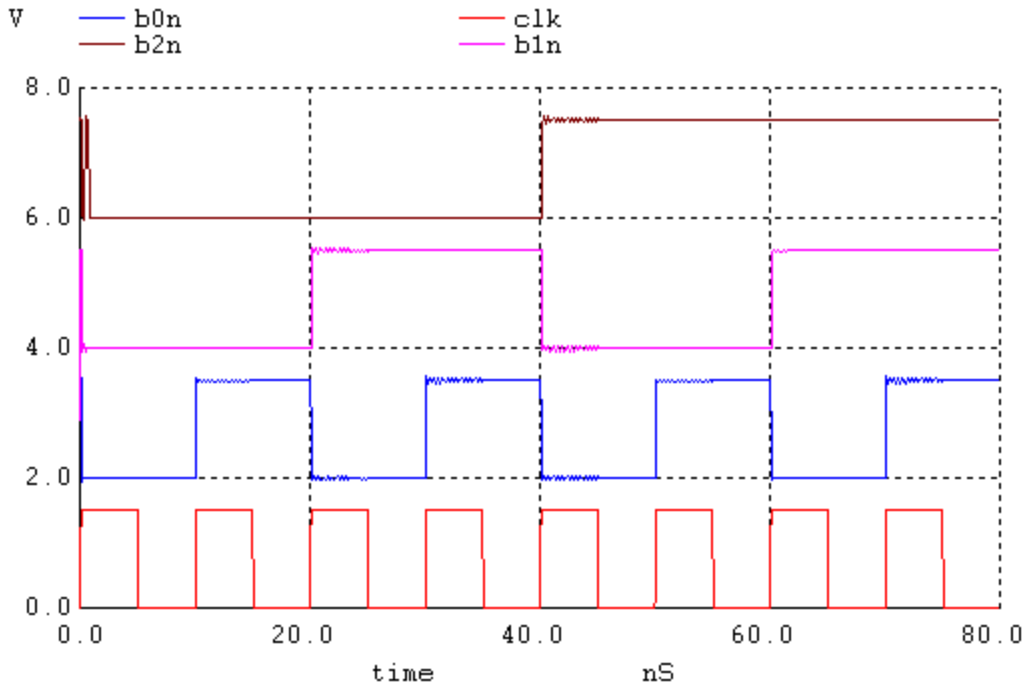

```
+ RD=1250.526 LDIF=0.07e-6

*** Junction Current Parameters
+ JS=1.0E-6 JSW=5.0E-11 XTI=0 N=1.5

*** Junction Capacitances Parameters
+ CJ=1.0E-3 CJSW=2.0E-10 CJGATE=5.0E-10
+ MJ=0.5 MJSW=0.3 PB=0.9 PBSW=0.9 FC=0.5

*** Gate Overlap Capacitances
+ CGSO=3.0E-10 CGDO=3.0E-10 CGBO=3.0E-11

*** PMOS EKV MOSFET Model ************************************************
*** Level=44 in WinSPICE and ELDO, Level=55 in ADM/HSPICE, Level=5 in PSPICE,
*** Level=EKV in Spectre
*** Lmin=0.15u Wmin=1.05u (If Scale=0.15u then Lmin=1 and Wmin=7)
*---------------
.MODEL pmos1 pmos
+ LEVEL  = 44

*** Setup Parameters
+ UPDATE = 2.6

*** Process Related Model Parameters
+ COX=9.083E-3 XJ=0.15E-6

*** Intrinsic Model Parameters
+ VTO=-0.4 GAMMA=0.69 PHI=0.87 KP=92.15E-6
+ E0=51.0E6 UCRIT=18.0E6
+ DL=-0.05E-6 DW=-0.03E-6
+ LAMBDA=1.1 LETA=0.45 WETA=0
+ Q0=200E-6 LK=0.6E-6

*** Substrate Current Parameters
+ IBN=1.0 IBA=0.0 IBB=300E6

*** Intrinsic Model Temperature Parameters
+ TNOM=25.0 TCV=-1.4E-3 BEX=-1.4 UCEX=2.0 IBBT=0.0

*** 1/f Noise Model Parameters
+ KF=1.0E-28 AF=1

*** Series Resistance and Area Calculation Parameters
+ HDIF=0.24E-6 ACM=3 RSH=5.0 RS=3145.263
+ RD=3145.263 LDIF=0.07e-6

*** Junction Current Parameters
+ JS=1.0E-7 JSW=5.0E-12 XTI=0 N=1.8

*** Junction Capacitances Parameters
+ CJ=1.3E-3 CJSW=2.5E-10 CJGATE=5.5E-10
+ MJ=0.5 MJSW=0.35 PB=0.9 PBSW=0.9 FC=0.5

*** Gate Overlap Capacitances
+ CGSO=3.2E-10 CGDO=3.2E-10 CGBO=3.0E-11

.end
```



This is the ripple-up counter output.

```
* Problem 33.11 CMOS: Mixed-Signal Circuit Design - ripple down *

*#destroy all
*#run
**#plot phi phib
**#plot vdd#branch
*#let Iavg=mean(vdd#branch)
*#let b0=vout+2
*#let b1=vout2+4
*#let b2=vout3+6
*#plot clk b0 b1 b2

Vdd   Vdd 0 DC 1.5
Vclk clk 0 DC 0 pulse 0 1.5 0 .1n .1n 4.9n 10n

X1 Vout Vout clk vdd dtspc
X2 Vout2 Vout2 Vout vdd dtspc
X3 Vout3 Vout3 Vout2 vdd dtspc
CL Vout 0 30f

.tran .2n 160n 0n .2n
.option ITL4=100 scale=0.15u reltol=0.05 vntol=10m abstol=1n

.subckt dtspc Vin Vout clk Vdd
M1 1 Vin 0 0 NMOS  L=1 W=10 PD=20
M2 1 clk 2 Vdd PMOS L=1 W=20 PD=40
M3 2 Vin Vdd Vdd PMOS L=1 W=20 PD=40
M4 3 clk 0 0 NMOS L=1 W=10 PD=20
M5 4 1 3 0 NMOS L=1 W=10 PD=20
M6 4 clk Vdd Vdd PMOS L=1 W=20 PD=40
M7 5 4 0 0 NMOS L=1 W=10 PD=20
M8 Vout clk 5 0 NMOS L=1 W=10 PD=20
M9 Vout 4 Vdd Vdd PMOS L=1 W=20 PD=40
.ends

.MODEL nmos nmos  level=1 VTO=0.4 GAMMA=0.71 PHI=0.97 KP=453E-6
+ CJ=1.0E-3 CJSW=2.0E-10 MJ=0.5 MJSW=0.3 PB=0.9 tox=40e-10

.MODEL pmos pmos  level=1 VTO=-0.4 GAMMA=0.69 PHI=0.87 KP=92.15E-6
+ CJ=1.3E-3 CJSW=2.5E-10 MJ=0.5 MJSW=0.35 PB=0.9 tox=40e-10

*** SPICE Models

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expressly for
***   use in the examples provided in this text, and should not be used for
any
***   real silicon product design.

*** NMOS EKV MOSFET Model ************************************************
*** Level=44 in WinSPICE and ELDO, Level=55 in ADM/HSPICE, Level=5 in PSPICE,
*** Level=EKV in Spectre
*** Lmin=0.15u Wmin=1.05u (If Scale=0.15u then Lmin=1 and Wmin=7)
*---------------
.MODEL nmos1 nmos
+ LEVEL=44
```
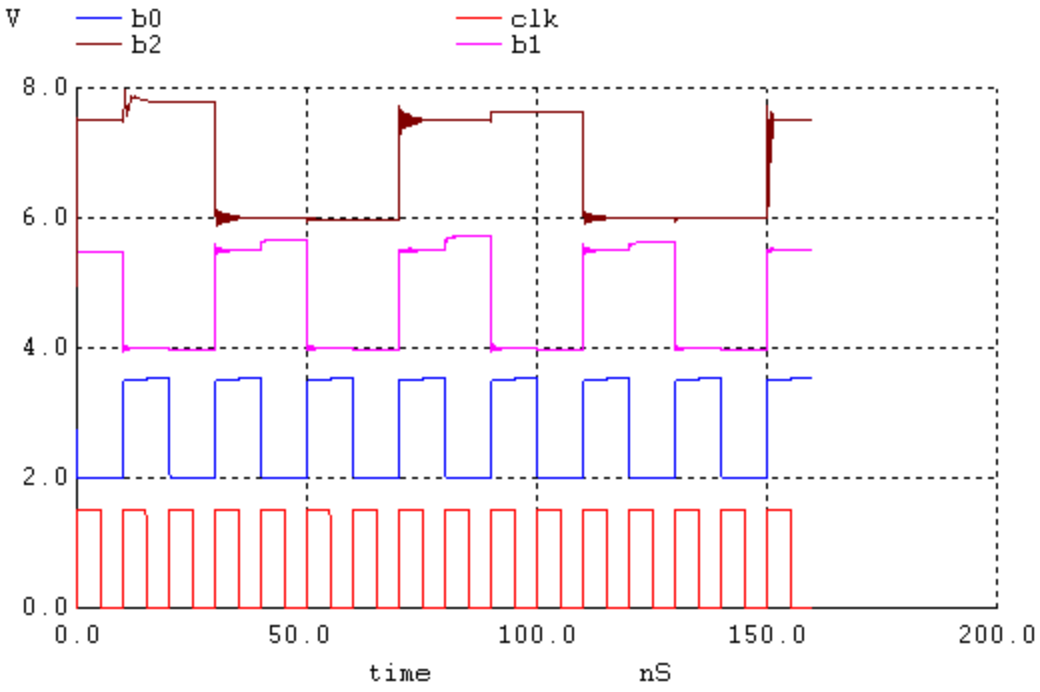

```
*** Setup Parameters
+ UPDATE=2.6

*** Process Related Model Parameters
+ COX=9.083E-3 XJ=0.15E-6

*** Intrinsic Model Parameters
+ VTO=0.4 GAMMA=0.71 PHI=0.97 KP=453E-6
+ E0=88.0E6 UCRIT=4.0E6
+ DL=-0.05E-6 DW=-0.02E-6
+ LAMBDA = 0.30 LETA=0.28 WETA=0
+ Q0=280E-6 LK=0.5E-6

*** Substrate Current Parameters
+ IBN=1.0 IBA=200E6 IBB=350E6

*** Intrinsic Model Temperature Parameters
+ TNOM=27.0 TCV=1.5E-3 BEX=-1.5 UCEX=1.7 IBBT=0

*** 1/f Noise Model Parameters
+ KF=1E-27 AF=1

*** Series Resistance and Area Calculation Parameters
+ HDIF=0.24e-6 ACM=3 RSH=5.0 RS=1250.526
+ RD=1250.526 LDIF=0.07e-6

*** Junction Current Parameters
+ JS=1.0E-6 JSW=5.0E-11 XTI=0 N=1.5

*** Junction Capacitances Parameters
+ CJ=1.0E-3 CJSW=2.0E-10 CJGATE=5.0E-10
+ MJ=0.5 MJSW=0.3 PB=0.9 PBSW=0.9 FC=0.5

*** Gate Overlap Capacitances
+ CGSO=3.0E-10 CGDO=3.0E-10 CGBO=3.0E-11

*** PMOS EKV MOSFET Model ************************************************
*** Level=44 in WinSPICE and ELDO, Level=55 in ADM/HSPICE, Level=5 in PSPICE,
*** Level=EKV in Spectre
*** Lmin=0.15u Wmin=1.05u (If Scale=0.15u then Lmin=1 and Wmin=7)
*---------------
.MODEL pmos1 pmos
+ LEVEL  = 44

*** Setup Parameters
+ UPDATE = 2.6

*** Process Related Model Parameters
+ COX=9.083E-3 XJ=0.15E-6

*** Intrinsic Model Parameters
+ VTO=-0.4 GAMMA=0.69 PHI=0.87 KP=92.15E-6
+ E0=51.0E6 UCRIT=18.0E6
+ DL=-0.05E-6 DW=-0.03E-6
+ LAMBDA=1.1 LETA=0.45 WETA=0
+ Q0=200E-6 LK=0.6E-6

*** Substrate Current Parameters
+ IBN=1.0 IBA=0.0 IBB=300E6
```

```
*** Intrinsic Model Temperature Parameters
+ TNOM=25.0 TCV=-1.4E-3 BEX=-1.4 UCEX=2.0 IBBT=0.0

*** 1/f Noise Model Parameters
+ KF=1.0E-28 AF=1

*** Series Resistance and Area Calculation Parameters
+ HDIF=0.24E-6 ACM=3 RSH=5.0 RS=3145.263
+ RD=3145.263 LDIF=0.07e-6

*** Junction Current Parameters
+ JS=1.0E-7 JSW=5.0E-12 XTI=0 N=1.8

*** Junction Capacitances Parameters
+ CJ=1.3E-3 CJSW=2.5E-10 CJGATE=5.5E-10
+ MJ=0.5 MJSW=0.35 PB=0.9 PBSW=0.9 FC=0.5

*** Gate Overlap Capacitances
+ CGSO=3.2E-10 CGDO=3.2E-10 CGBO=3.0E-11

.end
```

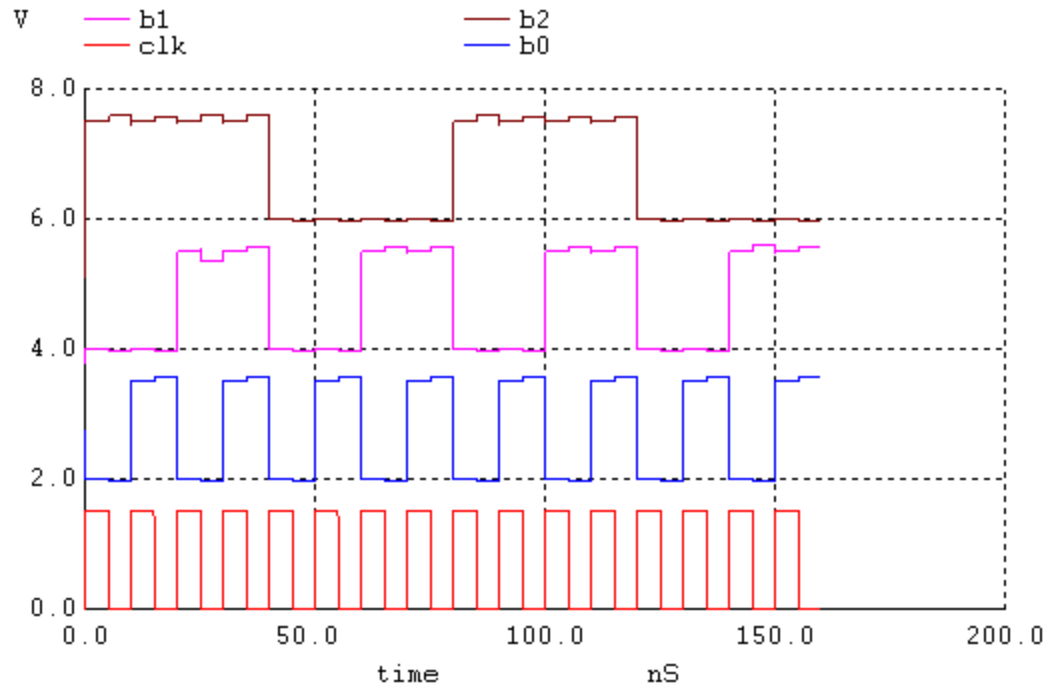


This is the output for a ripple-down counter.

```
* Problem 33.11 CMOS: Mixed-Signal Circuit Design - synchronous up *

*#destroy all
*#run
**#plot phi phib
**#plot vdd#branch
*#let Iavg=mean(vdd#branch)
*#let b0=vout4+2
*#let b1=vout5+4
*#let b2=vout6+6
*#plot clk b0 b1 b2

Vdd   Vdd 0 DC 1.5
Vclk clk 0 DC 0 pulse 0 1.5 0 .1n .1n 4.9n 10n

X1 Vout Vout clk vdd dtspc
X2 Vout2 Vout2 Vout vdd dtspc
X3 Vout3 Vout3 Vout2 vdd dtspc
X4 Vout Vout4 clk vdd dtspc
X5 Vout2 Vout5 clk vdd dtspc
X6 Vout3 Vout6 clk vdd dtspc
CL Vout 0 30f
CL2 Vout2 0 30f
CL3 Vout3 0 30f
CL4 Vout4 0 30f
CL5 Vout5 0 30f
CL6 Vout6 0 30f

.tran .2n 160n 0n .2n
.option ITL4=100 scale=0.15u reltol=0.2 vntol=20m abstol=4n

.subckt dtspc Vin Vout clk Vdd
M1 1 Vin 0 0 NMOS  L=1 W=10 PD=20
M2 1 clk 2 Vdd PMOS L=1 W=20 PD=40
M3 2 Vin Vdd Vdd PMOS L=1 W=20 PD=40
M4 3 clk 0 0 NMOS L=1 W=10 PD=20
M5 4 1 3 0 NMOS L=1 W=10 PD=20
M6 4 clk Vdd Vdd PMOS L=1 W=20 PD=40
M7 5 4 0 0 NMOS L=1 W=10 PD=20
M8 Vout clk 5 0 NMOS L=1 W=10 PD=20
M9 Vout 4 Vdd Vdd PMOS L=1 W=20 PD=40
.ends

.MODEL nmos nmos  level=1 VTO=0.4 GAMMA=0.71 PHI=0.97 KP=453E-6
+ CJ=1.0E-3 CJSW=2.0E-10 MJ=0.5 MJSW=0.3 PB=0.9 tox=40e-10

.MODEL pmos pmos  level=1 VTO=-0.4 GAMMA=0.69 PHI=0.87 KP=92.15E-6
+ CJ=1.3E-3 CJSW=2.5E-10 MJ=0.5 MJSW=0.35 PB=0.9 tox=40e-10

*** SPICE Models

*** Models created by Daniel Foty.
*** (c) 2001, Gilgamesh Associates and EPFL - All rights reserved.
*** These models are provided without warranty or support.
*** These models represent a completely fictitious 0.15um process, and do
***   NOT correspond to any real silicon process.  They are provided
expressly for
***   use in the examples provided in this text, and should not be used for
any
***   real silicon product design.
```

```
*** NMOS EKV MOSFET Model ************************************************
*** Level=44 in WinSPICE and ELDO, Level=55 in ADM/HSPICE, Level=5 in PSPICE,
*** Level=EKV in Spectre
*** Lmin=0.15u Wmin=1.05u (If Scale=0.15u then Lmin=1 and Wmin=7)
*---------------
.MODEL nmos1 nmos
+ LEVEL=44

*** Setup Parameters
+ UPDATE=2.6

*** Process Related Model Parameters
+ COX=9.083E-3 XJ=0.15E-6

*** Intrinsic Model Parameters
+ VTO=0.4 GAMMA=0.71 PHI=0.97 KP=453E-6
+ E0=88.0E6 UCRIT=4.0E6
+ DL=-0.05E-6 DW=-0.02E-6
+ LAMBDA = 0.30 LETA=0.28 WETA=0
+ Q0=280E-6 LK=0.5E-6

*** Substrate Current Parameters
+ IBN=1.0 IBA=200E6 IBB=350E6

*** Intrinsic Model Temperature Parameters
+ TNOM=27.0 TCV=1.5E-3 BEX=-1.5 UCEX=1.7 IBBT=0

*** 1/f Noise Model Parameters
+ KF=1E-27 AF=1

*** Series Resistance and Area Calculation Parameters
+ HDIF=0.24e-6 ACM=3 RSH=5.0 RS=1250.526
+ RD=1250.526 LDIF=0.07e-6

*** Junction Current Parameters
+ JS=1.0E-6 JSW=5.0E-11 XTI=0 N=1.5

*** Junction Capacitances Parameters
+ CJ=1.0E-3 CJSW=2.0E-10 CJGATE=5.0E-10
+ MJ=0.5 MJSW=0.3 PB=0.9 PBSW=0.9 FC=0.5

*** Gate Overlap Capacitances
+ CGSO=3.0E-10 CGDO=3.0E-10 CGBO=3.0E-11

*** PMOS EKV MOSFET Model ************************************************
*** Level=44 in WinSPICE and ELDO, Level=55 in ADM/HSPICE, Level=5 in PSPICE,
*** Level=EKV in Spectre
*** Lmin=0.15u Wmin=1.05u (If Scale=0.15u then Lmin=1 and Wmin=7)
*---------------
.MODEL pmos1 pmos
+ LEVEL  = 44

*** Setup Parameters
+ UPDATE = 2.6

*** Process Related Model Parameters
+ COX=9.083E-3 XJ=0.15E-6

*** Intrinsic Model Parameters
```

```
+ VTO=-0.4 GAMMA=0.69 PHI=0.87 KP=92.15E-6
+ E0=51.0E6 UCRIT=18.0E6
+ DL=-0.05E-6 DW=-0.03E-6
+ LAMBDA=1.1 LETA=0.45 WETA=0
+ Q0=200E-6 LK=0.6E-6

*** Substrate Current Parameters
+ IBN=1.0 IBA=0.0 IBB=300E6

*** Intrinsic Model Temperature Parameters
+ TNOM=25.0 TCV=-1.4E-3 BEX=-1.4 UCEX=2.0 IBBT=0.0

*** 1/f Noise Model Parameters
+ KF=1.0E-28 AF=1

*** Series Resistance and Area Calculation Parameters
+ HDIF=0.24E-6 ACM=3 RSH=5.0 RS=3145.263
+ RD=3145.263 LDIF=0.07e-6

*** Junction Current Parameters
+ JS=1.0E-7 JSW=5.0E-12 XTI=0 N=1.8

*** Junction Capacitances Parameters
+ CJ=1.3E-3 CJSW=2.5E-10 CJGATE=5.5E-10
+ MJ=0.5 MJSW=0.35 PB=0.9 PBSW=0.9 FC=0.5

*** Gate Overlap Capacitances
+ CGSO=3.2E-10 CGDO=3.2E-10 CGBO=3.0E-11

.end
```



This is the output of the synchronous up counter.
QED

Bob Moehrke EE515 (bmoehrke@amis.com)

Question 33.12

Verify the operation of the element in Fig. 33.50 as a 1-bit adder.

A one bit adder has the following truth table:

Cin	Ain	Bin	Cout	Sout
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

This can be summarized as is done in the corrected version of equation 33.16:

$$sout = ain * bin * cin + (ain + bin + cin) * coutbar$$

and equation 33.17:

$$cout = ain * bin + cin * (ain + bin)$$

The one-bit adder shown in figure 33.50 uses precharge-evaluate logic. It is broken up into two stages--the first to output cout and the second to output sout. These outputs are valid when clk is high. Looking at the operation of the first stage, one can see that when clk is low, coutbar is precharged high (making cout low). When clk goes high, coutbar will stay high due to parasitic caps unless the right combination of inputs is present. If this combination is present, since there is a path to ground, coutbar will be pulled low (making cout high). Using this knowledge, one can easily by inspection, figure out all of these input combinations that will make coutbar low (cout high):

$$cout = ain * bin + cin * (ain + bin)$$

This is exactly the same as equation 33.17. So the first stage appears to be correct.

Looking at the operation of the second stage, one can see that when clkbar is high (clk low), soutbar is precharged low (making sout high). When clk goes high (clkbar goes low), soutbar will stay low due to parasitic caps unless the right combination of inputs is present. If this combination is present, since there is a path to VDD, soutbar will be pulled high (making sout low). Again, one can easily by inspection, figure out all of these input combinations that will make soutbar high (sout low):

$$soutbar = (ainbar + binbar + cinbar) * (ainbar * binbar * cinbar + cout)$$

complementing both sides of the equation:

$$sout = ain * bin * cin + (ain + bin + cin) * coutbar$$

This is exactly the same as the corrected version of equation 33.16. So both stages working together will perform the function of a 1-bit adder described by the truth table above.

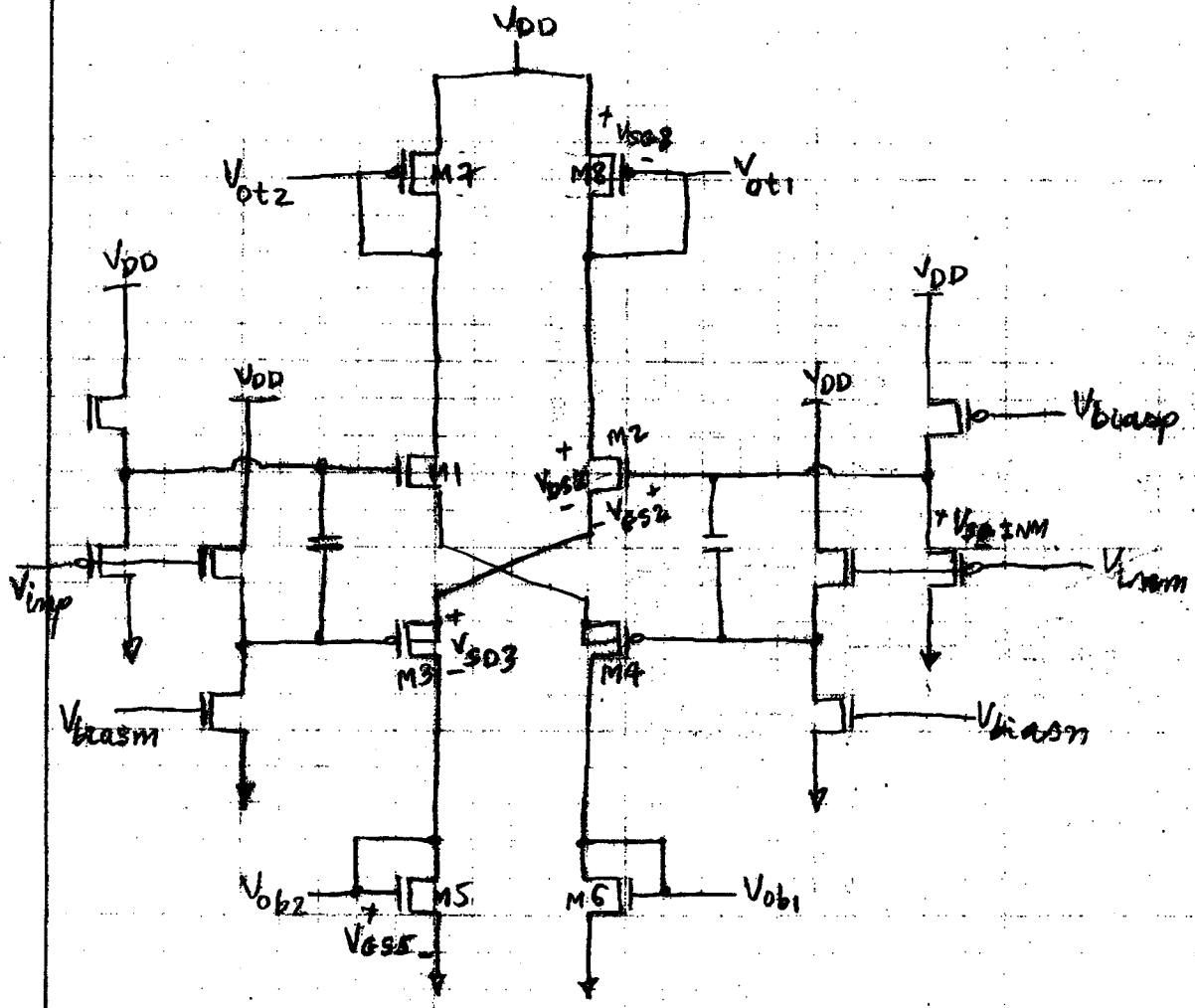
33.13
Jeremy Rice

Do the capacitors in Fig. 33.51 slow down the operation of the diff amp? why?

No. The purpose of the caps is not to provide a pole in the transfer function of the op amp, but rather to ensure the circuit operates correctly over the entire supply range on the input. The caps will provide a pole and a zero, but they will be at ~ gm/C which would take entirely too large of a capacitance to make it a good choice for compensation.

When the input common-mode voltage is close to the positive supply, the p-channel inputs will shut off, but the capacitors will prevent the gates of M1 and M2 from being charged to VDD, and the capacitors provide a signal path to these devices. The inverse is true when the input common-mode voltage approaches VSS, the caps prevent the gates of M3 and M4 from being pulled to ground and still allow signal path to these devices.

Problem 33.14 Estimate the input common-mode range of the diff-amp shown in Fig. 33.51.



For negative input CMR, $V_{DD} = 1.5V$, $V_{SD} = V_{DS} = \Delta V = .1V$

$V_{THN} = V_{THP} = .4V$

$$V_{IMIN} = -V_{SGINM} + V_{GS2} + V_{SD3} + V_{GS5}$$

$$= -(\Delta V + V_{THP}) + (\Delta V + V_{THN}) + \Delta V + (\Delta V + V_{THN})$$

$$= 2\Delta V + V_{THN} = 2(.1V) + .4V = .6V$$

For positive input CMR

$$V_{IMAX} = V_{DD} - V_{SG8} - V_{DS2} + V_{GS2} - V_{SGINM}$$

$$= V_{DD} - 2\Delta V - V_{THP} = 1.5V - .2V - .4V = .9V$$

Tyler J. Gomm
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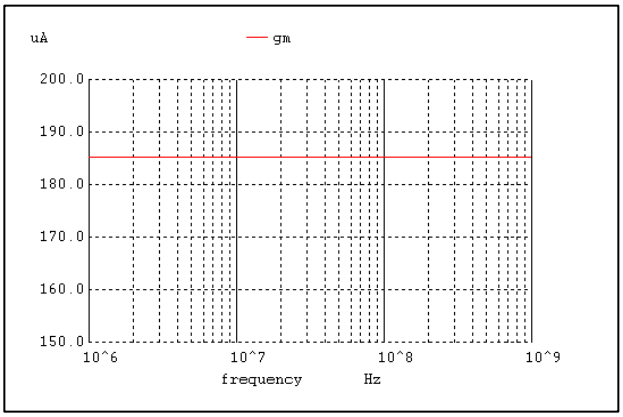
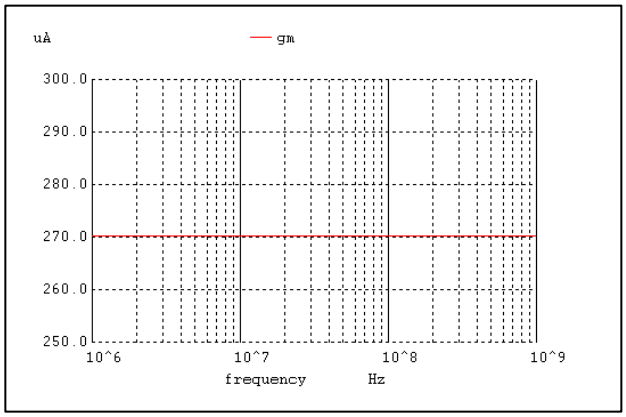
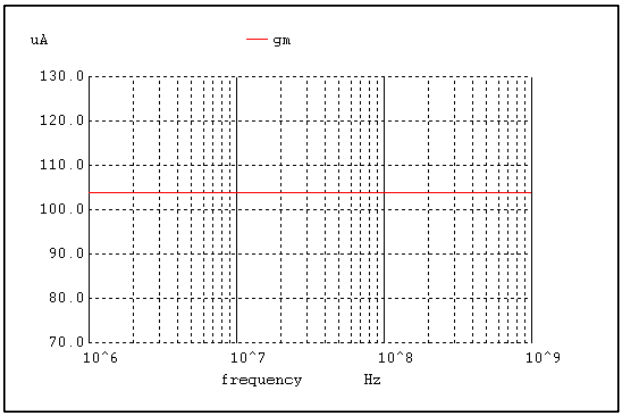
33.15 Regenerate the plots shown in Figs. 33.54 and 33.55 if the drain-source voltages of the MOSFET's are increased to 1.5 V. Why did the transconductance increase?

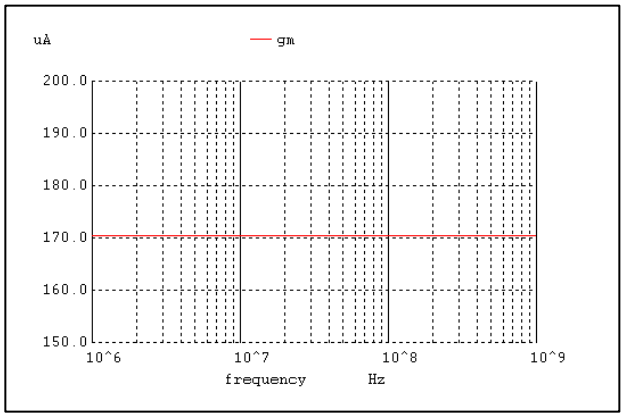
The following figures show the original Fig. 33.54 results (left) and the modified version with V_{DS} increased from 0.1 V to 1.5 V (right). The transconductance has increased from ~185 µA/V to ~270 µA/V.





The next figures show the original Fig. 33.55 (left) and the modified version with V_{SD} increased from 0.1 V to 1.5 V. The PMOS small-signal transconductance has increased from ~104 µA/V to ~170 µA/V.





Both of the original plots reflect g_m with the transistors operating in the triode region. With the increased voltages, the devices operate in the saturation region:

$$V_{DS} > V_{GS} - V_{THN}$$

Therefore, the transconductance increases because the device has moved from the triode region to the saturation region.

Remember that g_m can be determined using the circuit shown in Fig. 9.1 (from Chap. 9 of the first book). The small-signal model is shown in Fig. 9.2.

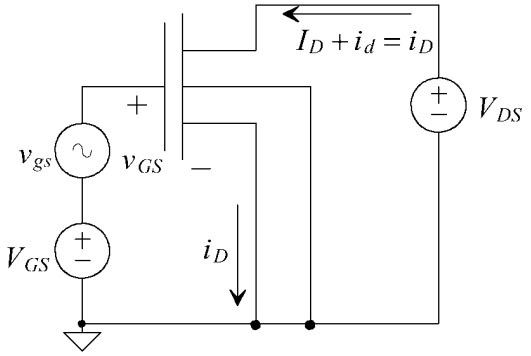


Figure 9.1 Circuit used to determine the forward transconductance.

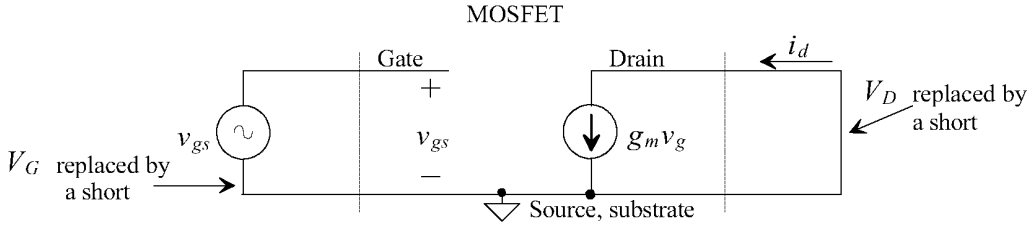


Figure 9.2 Small-signal model of the circuit in Fig. 9.1.

The transconductance is simply a gain factor in the voltage-controlled current source. Therefore, because i_d increases (while holding v_{gs} constant) as the transistor moves from triode to saturation, the gain has increased.

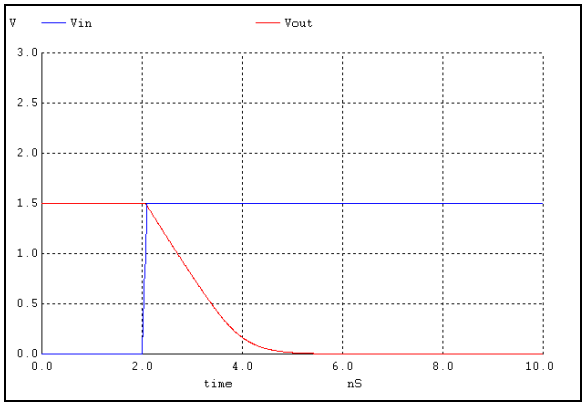
David Goldman

EE 515 – CMOS Mixed-Signal IC Design

Problem 33.16

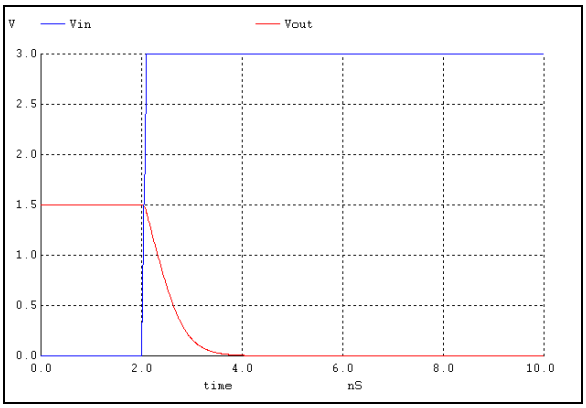
Question: Show, using simulations, that a MOSFET's transition frequency does increase with increasing gate-source voltage and decreasing length.

Answer: Figure 33.25 (plotted below) is the impulse response of a MOSFET at a given operating point.

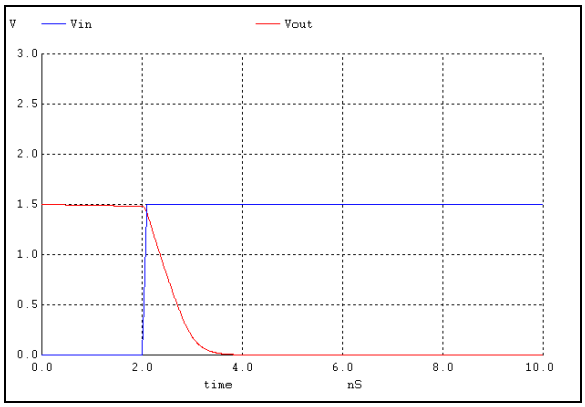


In the preceding plot, V_{GS} = 1.5 V and L = 1 μm; and, the propagation delay (τ_{PHL}) is about 1 ns. This represents a transition frequency of $1/\tau_{PHL} = 1/10^{-9}$ s = 1 GHz.

When V_{GS} is increased to 3.0 V and the length remains at L = 1 μm, the propagation delay is about 0.5 ns (shown below), which corresponds to a frequency of $0.5/10^{-9}$ s or 2 GHz.



The next plot shows the result of decreasing the channel length by one half, while the V_{GS} is returned to the value of the first plot. So, V_{GS} = 1.5 V and L = 0.5 μm.



Again, the plot above depicts a propagation delay of about 0.5 ns or a transition frequency of 2 GHz, which is twice as much as the first plot. Therefore, when V_{GS} increases or L decreases, the transition frequency increases.

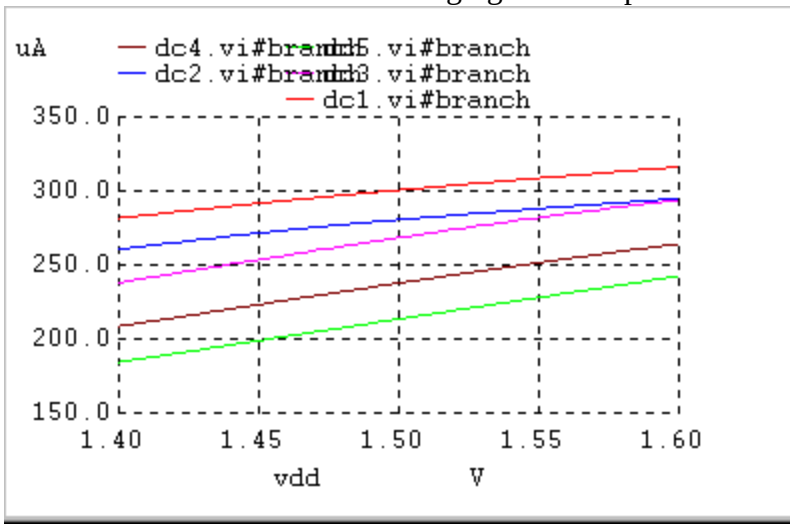
Gexin

Problem 33.17: Do any of the MOSFETs in Fig. 33.58 move into the triode region if the resistor's value is decreased to 1K? Verify your answers with simulation.

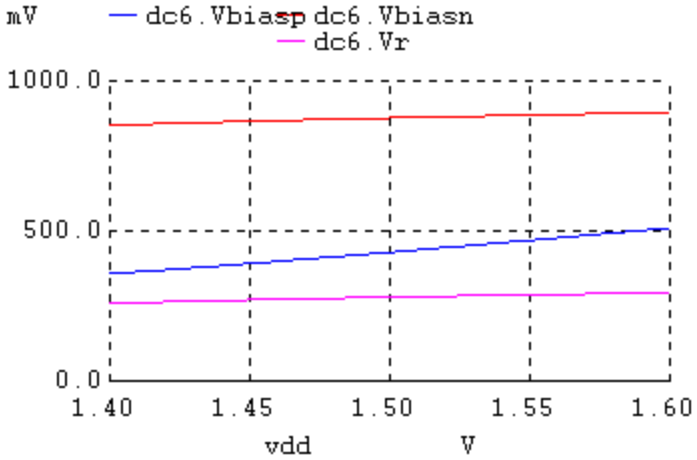
Solution for Problem 33.17:

If the resistor is decreased to 1K, then the current following through resistor and MOSFETs (M1 ~ M4) will be increased. That means the gate voltage of M3 and M4 (V_{biasp}) will be decreased, and at the meantime the gate voltage of M1 and M2 (V_{biasn}) will be increased. This implies that the MOSFETS M2 and M3 may enter triode region, since the gate-drain voltage of M2 and M3 may exceed the threshold voltage V_T, which is about 0.4V.

Simulation shows the current changing with temperature



The following simulations show V_{biasp}, V_{biasn} and the voltage across resistor V_r at T=27.



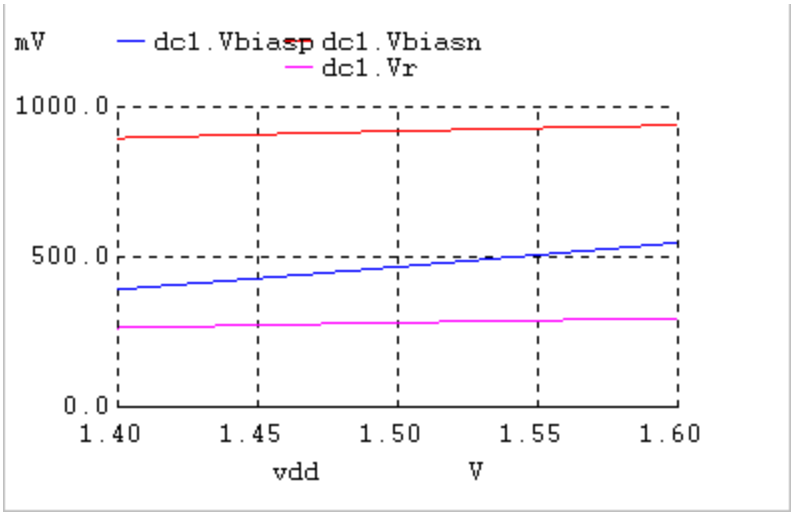
From the second simulation, we can get the following results:

When Vdd=1.5V:
Vbiasn=877mV
Vbiasp=430mV
Vr=280mV

Thus the gate-drain voltage for M2 is $V_{gd2} = V_{biasn} - V_r = 597mV$, which is greater than V_T. Thus M2 will work in triode region.

For M3, the gate-drain voltage is $V_{dg3} = V_{biasn} - V_{biasp} = 447mV$, which is also greater than V_T. Thus M3 will work in triode region.

Here shows the simulation for V_{biasp}, V_{biasn} and the voltage across resistor V_r at T=0.

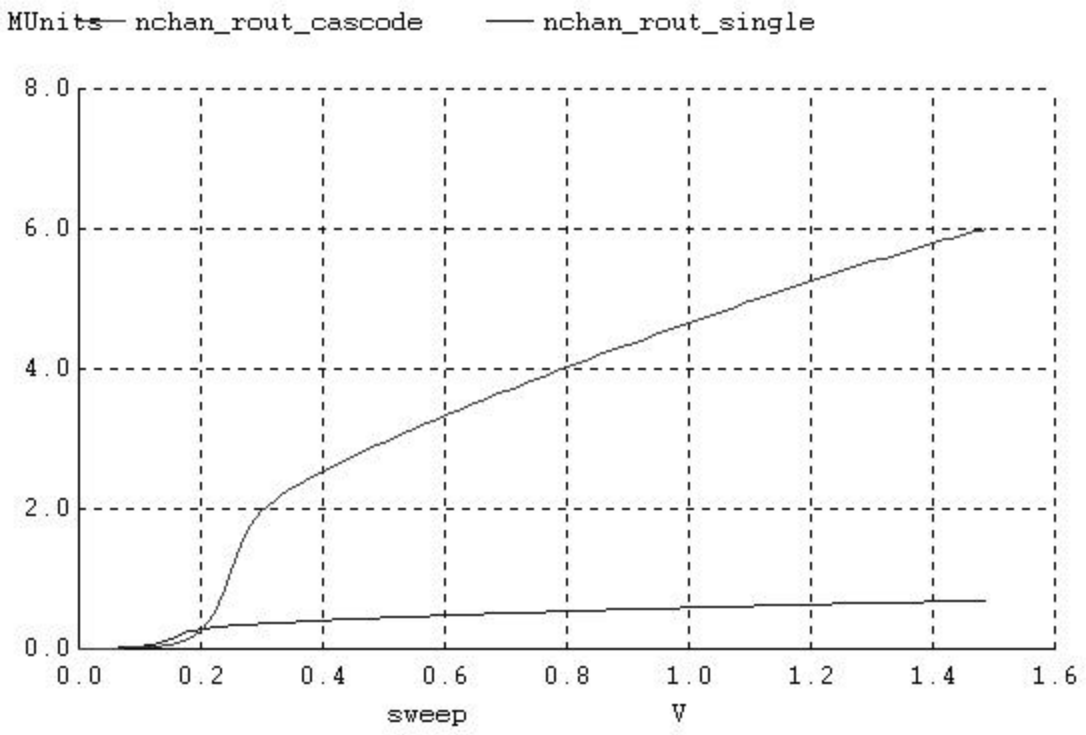


Brandon Roth

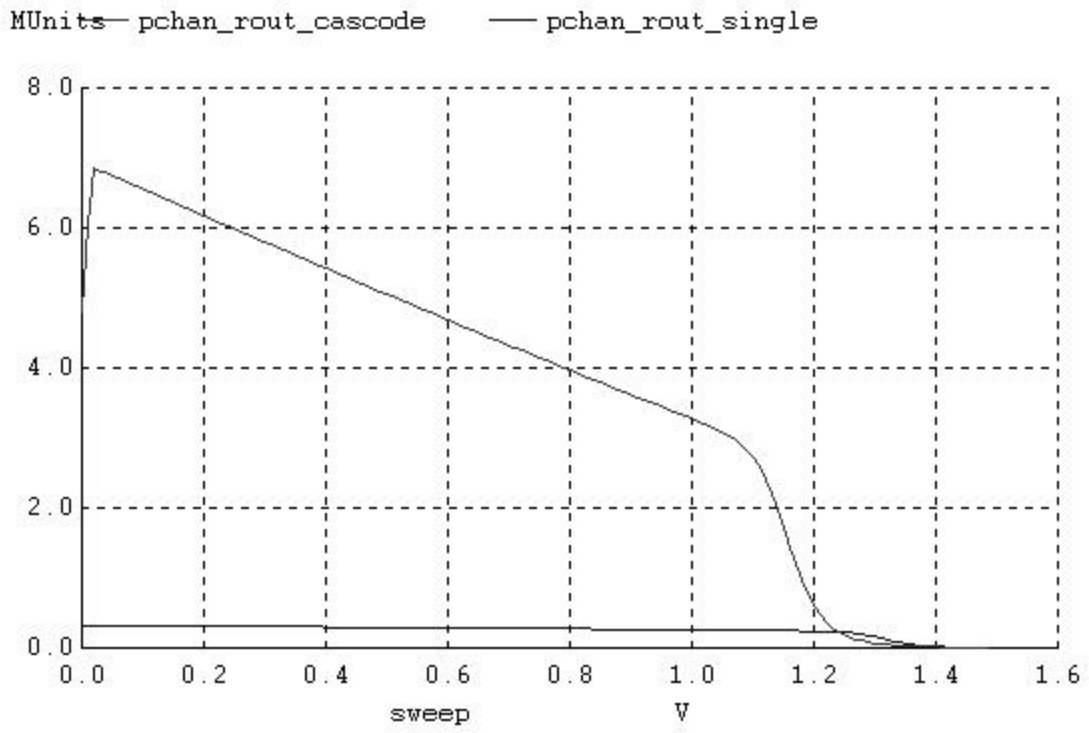
33.18 Compare the cascode current mirror performance shown in Fig. 33.61 to a basic current mirror. Show the increases in output resistance when using a cascode and compare the minimum voltages across the mirrors.

To show the difference in performance between a basic current mirror (single MOSFET) and a cascode current mirror the output resistance is compared. Current mirrors with higher output resistance have better performance, because changes in VDS have less effect on the current when operating in the saturation region. The ideal current mirror would have MOSFET's with infinite resistance when in saturation.

Each graph below has the output resistance for the single and cascode current mirrors, one graph for the n-channel mirrors and one for the p-channel mirrors. From the graphs, as VDS increases the output resistance increases.



N-channel output resistance.

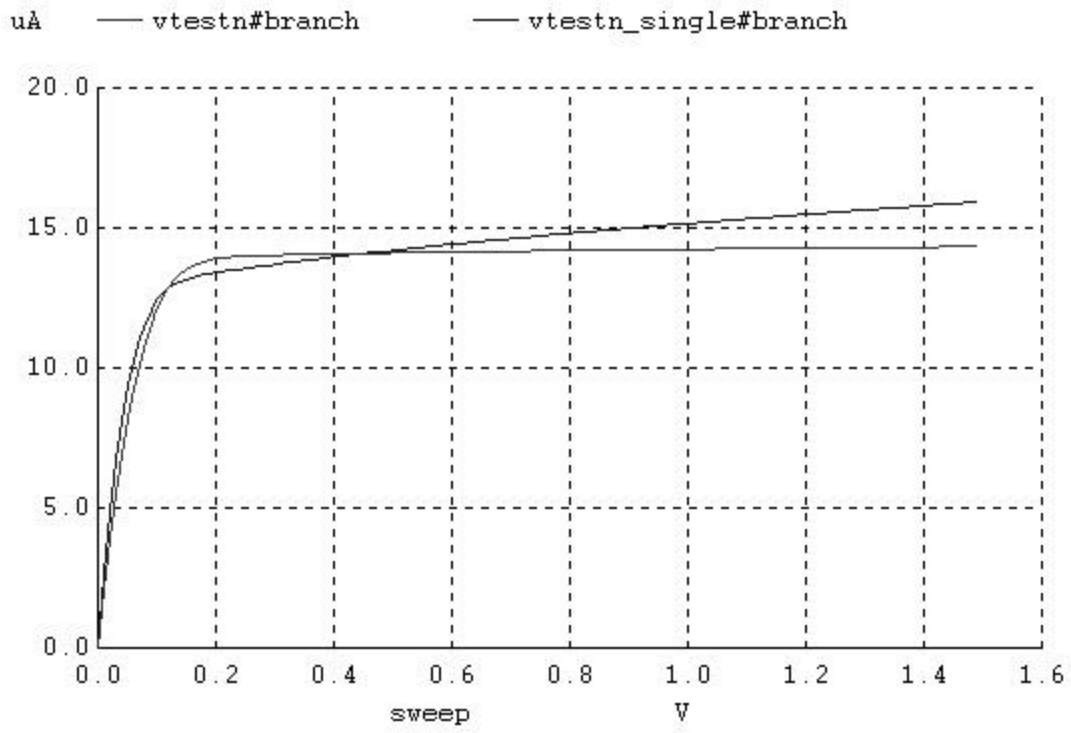


P-channel output resistance.

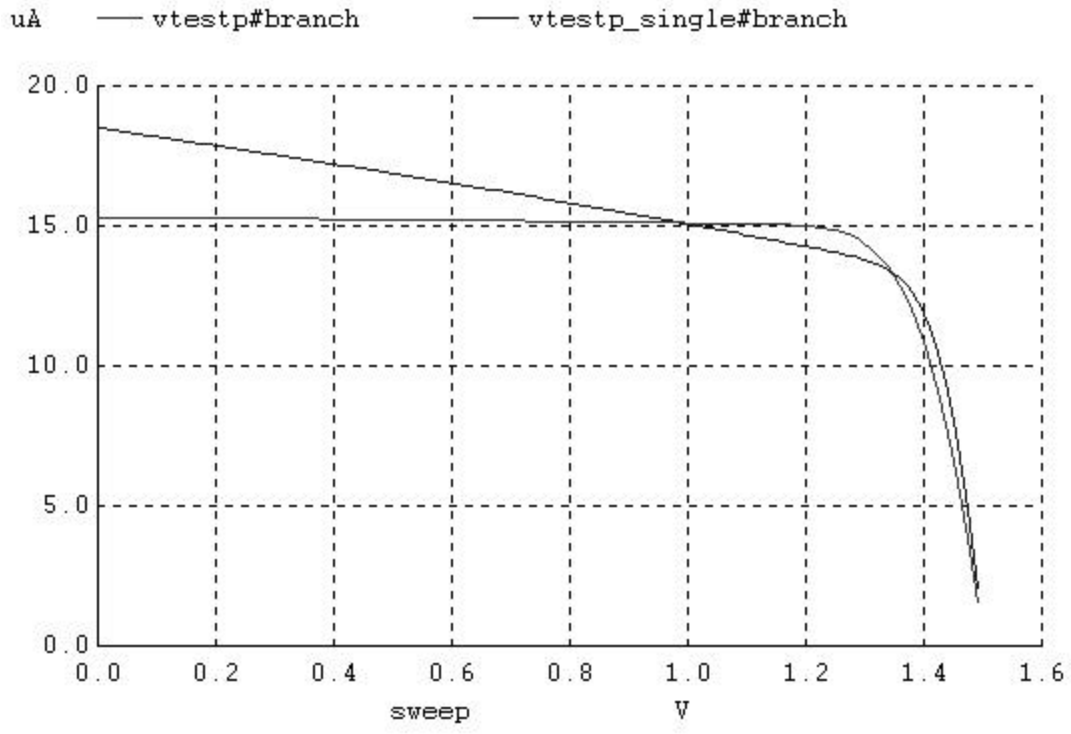
The table below shows the output resistance from the graphs when VDS is equal to 1.0V. Both cascode mirrors have significantly higher output resistance.

	Cascode Mirror	Basic (Single) Mirror
n-channel	4.66 Mega-ohms	600 Kilo-ohms
p-channel	3.28 Mega-ohms	260 Kilo-ohms

The minimum voltage across the mirrors is higher for the cascode mirrors than the single MOSFET mirrors, because there is more than one MOSFET to keep in the saturation region. This is evident in the graphs below where the slope of the line for the single current mirrors begins to decrease sooner indicating saturation. Note that for the p-channel the minimum voltage required for the cascode is a larger negative number.



N-channel ID vs. VDS



P-channel ID vs. VDS

The netlist was generated by adding a basic current mirror, removing the temperature behavior analysis, and adding the output resistance calculation to the netlist from Fig. 33.61. The netlist is listed below up to the EKV model information. The same EKV model was used as in Fig. 33.61.

```
* Problem 33.18 CMOS: Mixed-Signal Circuit Design *

Vdd Vdd 0 DC 1.5
Vtest Vtest 0 DC 0

X1 Vbias1 Vbias2 Vbias3 Vbias4 Vbiasn Vbiasn2 Vbiasp Vbiasp2 Vdd bias
X2 Vbias1_single Vbias2_single Vbiasn_single Vbiasn2_single Vbiasp_single Vbiasp2_single
Vdd bias_single

***Cascode Mirror***
M1 N1 Vbias1 Vdd Vdd PMOS L=2 W=40
M2 Vtestp Vbias2 N1 Vdd PMOS L=2 W=40
Vtestp Vtestp Vtest DC 0

M3 N2 Vbias4 0 0 NMOS L=2 W=20
M4 Vtestn Vbias3 N2 0 NMOS L=2 W=20
Vtestn Vtest Vtestn DC 0

***Single Device/Basic Mirror***
M5 Vtestp_single Vbias1_single Vdd Vdd PMOS L=2 W=40
Vtestp_single Vtestp_single Vtest DC 0

M6 Vtestn_single Vbias2_single 0 0 NMOS L=2 W=20
Vtestn_single Vtest Vtestn_single DC 0

.DC Vtest 0 1.5 .01
*#distroy all
*#run
*#plot vtestn#branch vtestn_single#branch
*#plot vtestp#branch vtestp_single#branch

***Output Resistance Plots***
*#let nchan_rout_cascode = abs(1/deriv(vtestn#branch))
*#let pchan_rout_cascode = abs(1/deriv(vtestp#branch))
*#let nchan_rout_single = abs(1/deriv(vtestn_single#branch))
*#let pchan_rout_single = abs(1/deriv(vtestp_single#branch))
*#plot nchan_rout_cascode nchan_rout_single
*#plot pchan_rout_cascode pchan_rout_single

.options scale=0.15u

***BIAS Circuit for Cascode Mirror***
.subckt bias Vbias1 Vbias2 Vbias3 Vbias4 Vbiasn Vbiasn2 Vbiasp Vbiasp2 Vdd

M1 Vbiasn Vbiasn 0 0 NMOS L=2 W=20
M2 Vbiasp Vbiasn Vr 0 NMOS L=1 W=80
M3 Vbiasn Vbiasp Vdd Vdd PMOS L=2 W=40
M4 Vbiasp Vbiasp Vdd Vdd PMOS L=2 W=40
R1 Vr Vi 10k RMOD
Vi Vi 0 DC 0
.model RMOD R TC1=0.0024
M5 Vsu Vsu Vdd Vdd PMOS L=20 W=10
M6 Vsu Vsu 0 0 NMOS L=5 W=10
M7 Vdd1 Vsu Vbiasn 0 NMOS L=1 W=10
Vdd1 Vdd Vdd1 DC 0
```

```
*Generate Vbiasn2
M8 Vbiasn2 Vbiasp Vdd Vdd PMOS L=2 W=40
M9 Vbiasn2 Vbiasn2 N1 0 NMOS L=2 W=20
M10 N1 N1 0 0 NMOS L=2 W=20

*Generate Vbiasp2
M11 Vbiasp2 Vbiasn 0 0 NMOS L=2 W=20
M12 Vbiasp2 Vbiasp2 N2 Vdd PMOS L=2 W=40
M13 N2 N2 Vdd Vdd PMOS L=2 W=40

*Generate Vbias1 Vbias2
M14 Vbias2 Vbiasn 0 0 NMOS L=2 W=20
M15 Vbias2 Vbias2 Vdd Vdd PMOS L=8 W=40
M16 N3 Vbias1 Vdd Vdd PMOS L=2 W=40
M17 Vbias1 Vbias2 N3 Vdd PMOS L=2 W=40
M18 Vbias1 Vbiasn 0 0 NMOS L=2 W=20

*Generate Vbias3 Vbias4
M19 Vbias3 Vbiasp Vdd Vdd PMOS L=2 W=40
M20 Vbias3 Vbias3 0 0 NMOS L=8 W=20
M21 Vbias4 Vbiasp Vdd Vdd PMOS L=2 W=40
M22 Vbias4 Vbias3 N4 0 NMOS L=2 W=20
M23 N4 Vbias4 0 0 NMOS L=2 W=20

.ends

***BIAS Circuit for Single Mirror***
.subckt bias_single Vbias1_single Vbias2_single Vbiasn_single Vbiasn2_single Vbiasp_single
Vbiasp2_single Vdd

M1 Vbiasn_single Vbiasn_single 0 0 NMOS L=2 W=20
M2 Vbiasp_single Vbiasn_single Vr 0 NMOS L=1 W=80
M3 Vbiasn_single Vbiasp_single Vdd Vdd PMOS L=2 W=40
M4 Vbiasp_single Vbiasp_single Vdd Vdd PMOS L=2 W=40
R1 Vr Vi 10k RMOD
Vi Vi 0 DC 0
.model RMOD R TC1=0.0024
M5 Vsu Vsu Vdd Vdd PMOS L=20 W=10
M6 Vsu Vsu 0 0 NMOS L=5 W=10
M7 Vdd1 Vsu Vbiasn_single 0 NMOS L=1 W=10
Vdd1 Vdd Vdd1 DC 0

*Generate Vbiasn2
M8 Vbiasn2_single Vbiasp_single Vdd Vdd PMOS L=2 W=40
M9 Vbiasn2_single Vbiasn2_single N1 0 NMOS L=2 W=20
M10 N1 N1 0 0 NMOS L=2 W=20

*Generate Vbiasp2
M11 Vbiasp2_single Vbiasn_single 0 0 NMOS L=2 W=20
M12 Vbiasp2_single Vbiasp2_single N2 Vdd PMOS L=2 W=40
M13 N2 N2 Vdd Vdd PMOS L=2 W=40

*Generate Vbias1
M14 Vbias1_single Vbiasn_single 0 0 NMOS L=2 W=20
M15 Vbias1_single Vbias1_single Vdd Vdd PMOS L=2 W=40
M17 N1 Vbias1_single Vdd Vdd PMOS L=2 W=40
M18 N1 Vbiasn_single 0 0 NMOS L=2 W=20

*Generate Vbias2
M19 Vbias2_single Vbiasp_single Vdd Vdd PMOS L=2 W=40
M20 Vbias2_single Vbias2_single 0 0 NMOS L=2 W=20
```

```
M21 N4 Vbiasp_single Vdd Vdd PMOS L=2 W=40
M22 N4 Vbias2_single 0 0 NMOS L=2 W=20

.ends
```

EE515: CMOS Mixed-Signal IC Design

Problem 33.19
Jim Slupe

33.19 What happens in Fig. 33.65 to the current flowing in the push-pull amplifier if we increase the lengths of MC1 and MC2?

Answer: As the length of the bias transistors MC1 and MC2 are increased they will tend to choke off the output transistors. Figure 33.66 is a realizable version of figure 33.65 and I use it to model 33.65. I implemented the bias circuitry of figures 33.58 and 33.60 in conjunction with figure 33.66 to produce the following abbreviated SPICE listing (SPICE transistor model not shown) that is partly illustrated in figure 5:

```
* Problem 33.19 CMOS: Mixed-Signal Circuit Design *

Vdd Vdd 0 DC 1.5
Vina Vina 0 DC 0

.DC Vina 0 1.5 .02

X1 Vbias1 Vbias2 Vbias3 Vbias4 Vbiasn Vbiasn2 Vbiasp Vbiasp2 Vhigh Vlow Vdd bias

M31 N31 Vot1 Vdd Vdd PMOS L=2 W=40
M32 N32 Vbias2 N31 Vdd PMOS L=2 W=40
MC1 N33 Vbiasp2 N32 Vdd PMOS L=2 W=20
MC2 N32 Vbiasn2 N33 0 NMOS L=2 W=10
M35 N33 Vbias3 N34 0 NMOS L=2 W=20
M36 N34 Vob1 0 0 NMOS L=2 W=20
M37 Vout N32 Vdd Vdd PMOS L=2 W=400
M38 Vout N33 Vresistor 0 NMOS L=2 W=200
R31 Vresistor 0 100

Vob1 Vob1 Vina DC 0
Vot1 Vina Vot1 DC 0

.control
destroy all
run
run
run
plot Vresistor Vob1 Vot1 Vout vs Vina
.endc

.options scale=0.15u
```

```
.subckt bias Vbias1 Vbias2 Vbias3 Vbias4 Vbiasn Vbiasn2 Vbiasp Vbiasp2 Vhigh Vlow
Vdd

M1 Vbiasn Vbiasn 0 0 NMOS L=2 W=20
M2 Vbiasp Vbiasn Vr 0 NMOS L=1 W=80
M3 Vbiasn Vbiasp Vdd Vdd PMOS L=2 W=40
M4 Vbiasp Vbiasp Vdd Vdd PMOS L=2 W=40
R1 Vr Vi 10k RMOD
Vi Vi 0 DC 0
.model RMOD R TC1=0.0024
M5 Vsu Vsu Vdd Vdd PMOS L=20 W=10
M6 Vsu Vsu 0 0 NMOS L=5 W=10
M7 Vdd1 Vsu Vbiasn 0 NMOS L=1 W=10
Vdd1 Vdd Vdd1 DC 0

*Generate Vbiasn2
M8 Vbiasn2 Vbiasp Vdd Vdd PMOS L=2 W=40
M9 Vbiasn2 Vbiasn2 N1 0 NMOS L=2 W=20
M10 N1 N1 0 0 NMOS L=2 W=20

*Generate Vbiasp2
M11 Vbiasp2 Vbiasn 0 0 NMOS L=2 W=20
M12 Vbiasp2 Vbiasp2 N2 Vdd PMOS L=2 W=40
M13 N2 N2 Vdd Vdd PMOS L=2 W=40

*Generate Vbias1 Vbias2
M14 Vbias2 Vbiasn 0 0 NMOS L=2 W=20
M15 Vbias2 Vbias2 Vdd Vdd PMOS L=8 W=40
M16 Vhigh Vbias1 Vdd Vdd PMOS L=2 W=40
M17 Vbias1 Vbias2 Vhigh Vdd PMOS L=2 W=40
M18 Vbias1 Vbiasn 0 0 NMOS L=2 W=20

*Generate Vbias3 Vbias4
M19 Vbias3 Vbiasp Vdd Vdd PMOS L=2 W=40
M20 Vbias3 Vbias3 0 0 NMOS L=8 W=20
M21 Vbias4 Vbiasp Vdd Vdd PMOS L=2 W=40
M22 Vbias4 Vbias3 Vlow 0 NMOS L=2 W=20
M23 Vlow Vbias4 0 0 NMOS L=2 W=20

.ends
```

Note: I added Vresistor between the source of the 200/2 NMOS transistor of figure 33.66 and ground in order to determine the current that flowed through the output stage of the push-pull amplifier versus the variation in length of MC1 and MC2

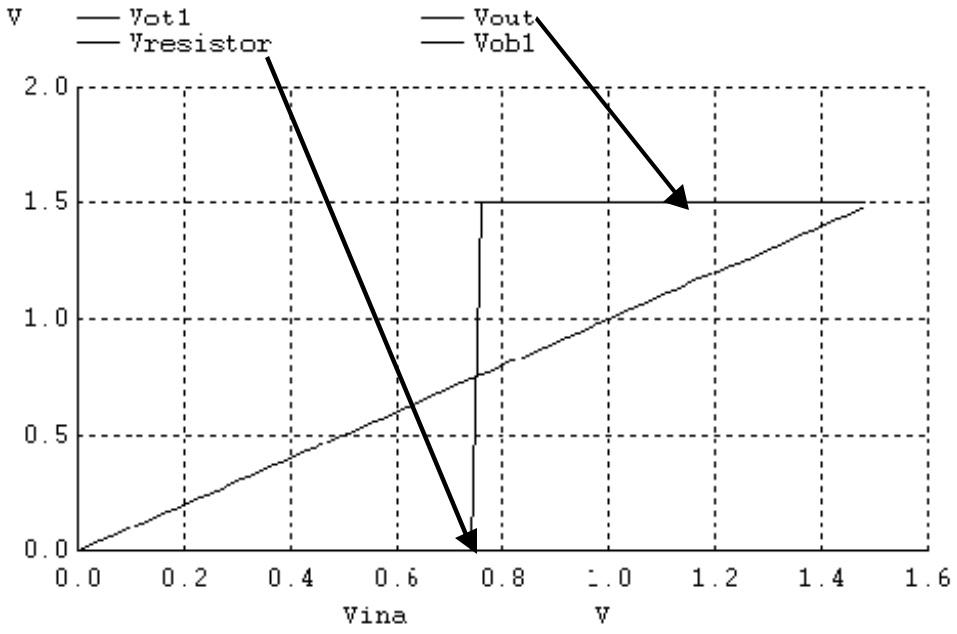


Figure 1

Figure 1 shows the result with a voltage ramp applied to Vot1 and Vob1 of figure 5.

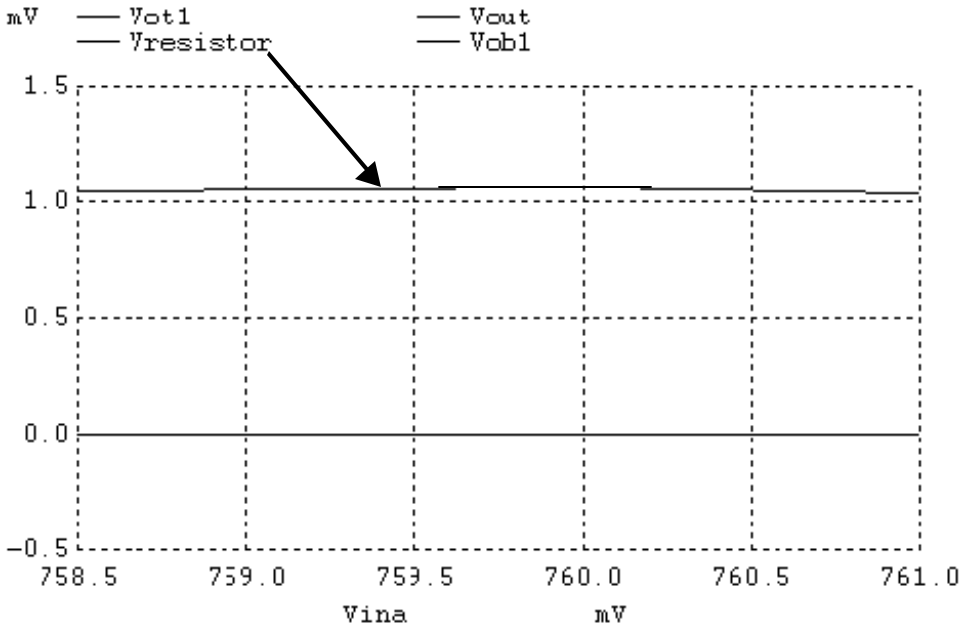


Figure 2

Figure 2 shows the voltage developed (1 mV) across the resistor in the drain to ground path of the 200/2 NMOS transistor of the output stage of the push-pull amplifier of figure 5. Here the W/L ratios of MC1 and MC2 were 20/2 and 10/2 respectively.

Now by increasing the length of MC1 and MC2 by a factor of ten to 20/20 and 10/20 respectively, one sees that the speed of the output stage of the push-pull amplifier is significantly reduced (as shown in figure 3).

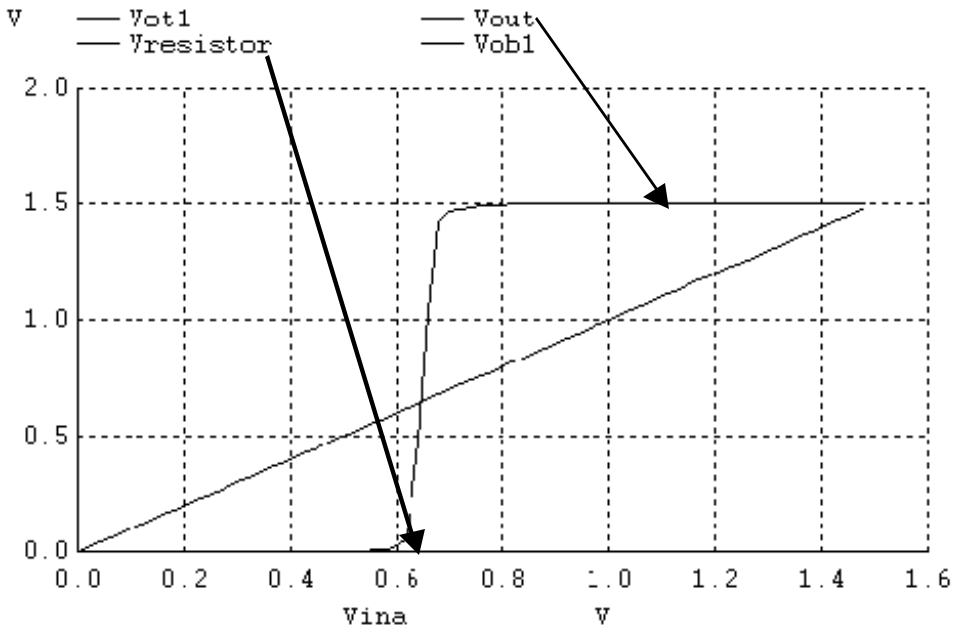


Figure 3

In addition, the current through the resistor is also reduced (1 uV / 100 ohms) as shown in figure 4.

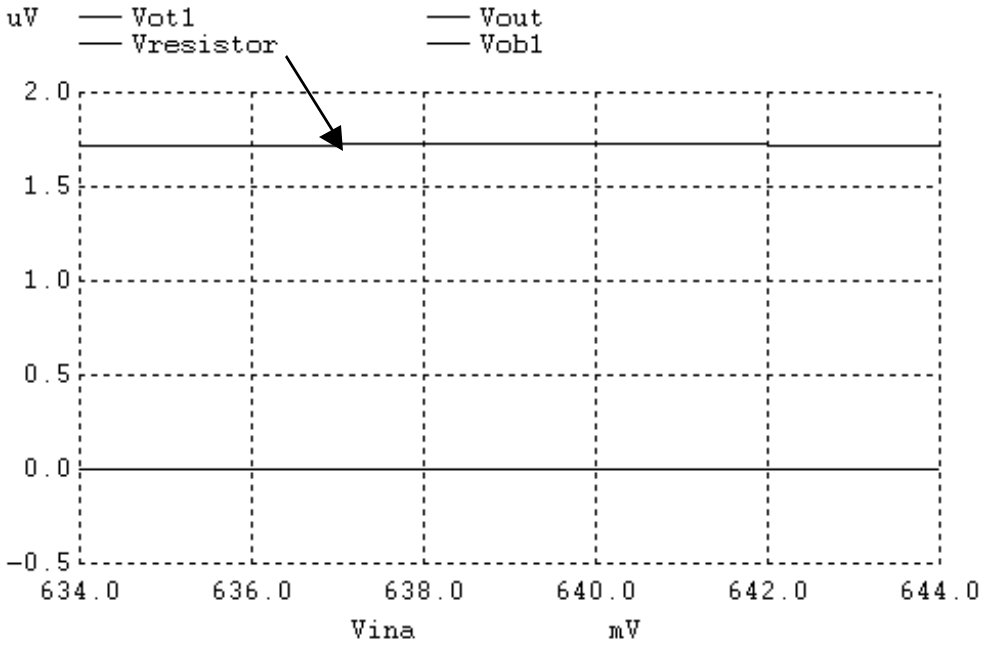


Figure 4

Extrapolation of the aforementioned result leads to the conclusion that: If the channel length of MC1 and MC2 are increased enough, one could "choke off" the output stage of the push-pull amplifier and supports the argument that the frequency of operation is significantly reduced.

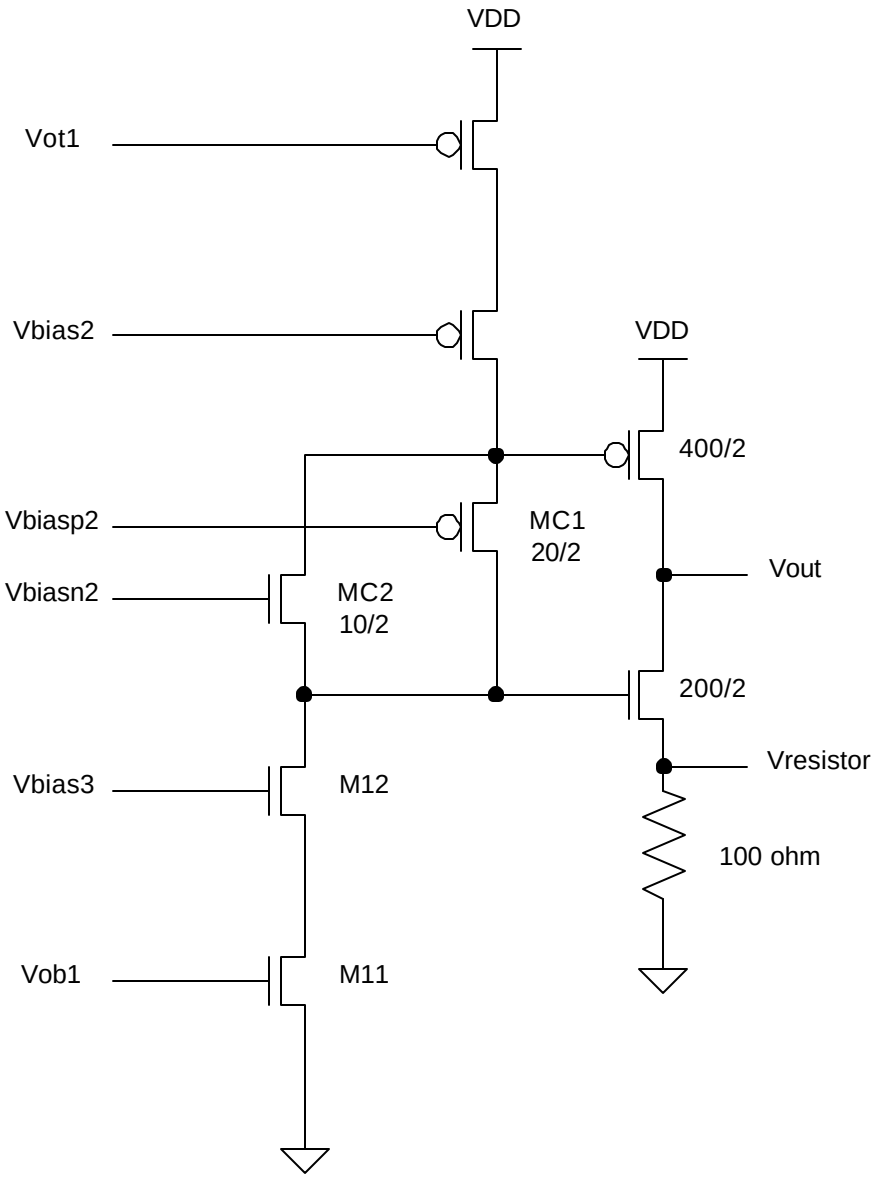
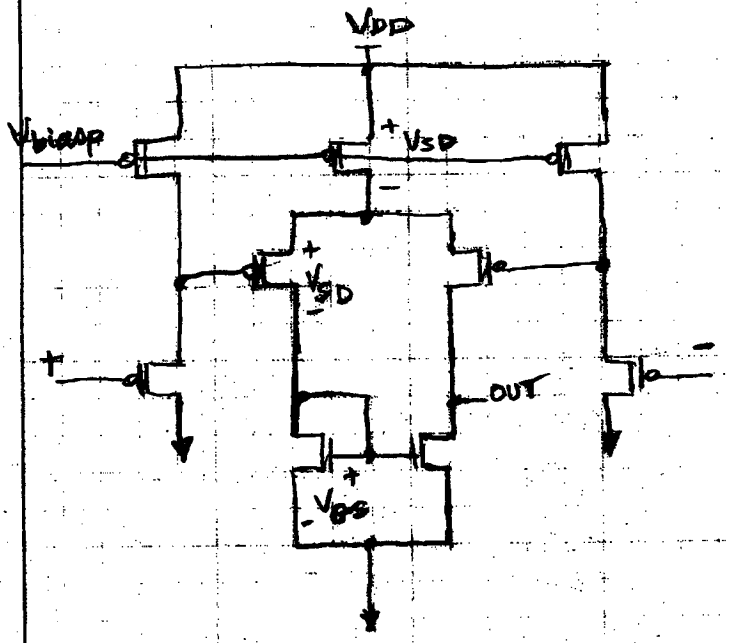


Figure 5

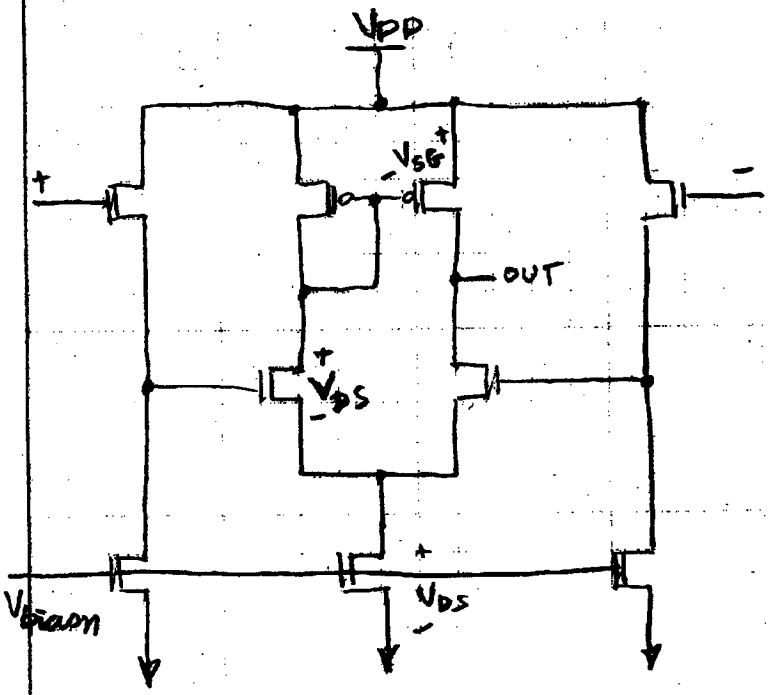
Figure 5 shows the modification to Figure 33.66 that was done to simulate the results obtained. A small resistor was placed in series with the output stage in order to measure the voltage drop caused by current flow through the output stage.

Problem 33.20 Estimate the minimum V_{DD} allowed for proper operation of the diff-amps shown in Fig. 33.69



$$V_{DD} = V_{SD} + V_{SD} + V_{GS}$$

$$= .1V + .1V + .5V = .7V$$



$$V_{DD} = V_{SG} + V_{DS} + V_{DS}$$

$$= .5V + .2V = .7V$$

EE515: CMOS Mixed-Signal IC Design
Brian Bergeson
Problem 33.21
brian_bergeson@amis.com

Problem 33.21:

If, in Fig. 33.70, VGS=VSG=0.5V and deltaV=VDS,min=0.1V, what is the minimum allowable power supply voltage, VDD, for proper op-amp operation.

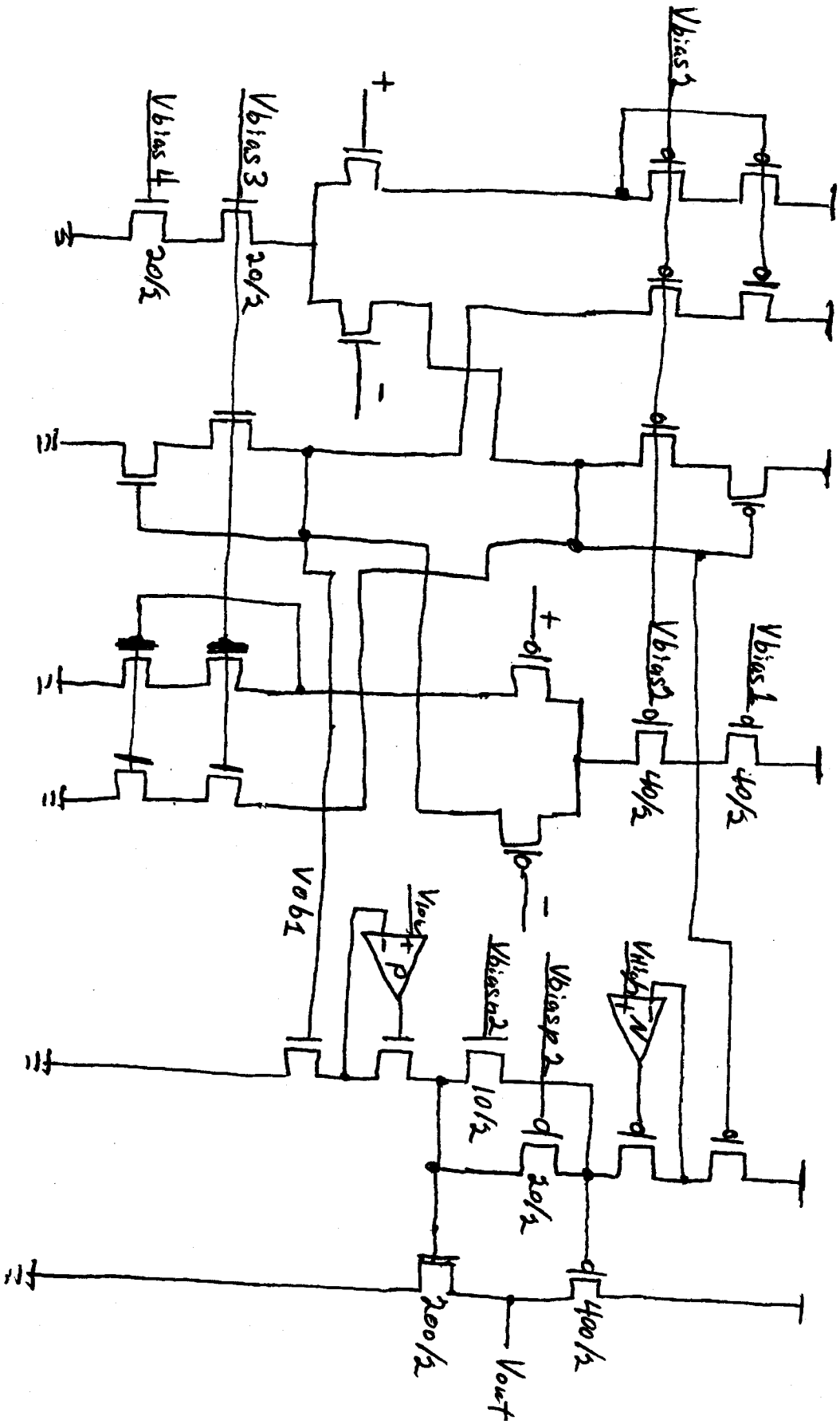
Solution:

The minimum allowable VDD for proper op-amp operation would be the sum of the VGS's and VDS's through the "worst case" path through the op-amp. The worst case path would be the path with the highest voltage drop from VDD to GND, assuming VDS=0.1V and VGS=0.5V. In Fig 33.70, this path would be from the right most VDD, through the Vbiasp2 transistor, to the right most GND. The sum of the VGS's and VDS's through this path would be:

VGS+VDS+VGS=0.5V+0.1V+0.5V=1.1V

On page 290 it states that, for this op-amp topology in a typical process run, the minimum VDD would approach 1V. The exact number would depend on the values for VGS and VDS. For the case when VGS=0.5V and VDS=0.1V, the minimum VDD is actually 1.1V.

33.22



EE515: CMOS Mixed-Signal IC Design
Question 33.23
Richard Friel
Rich_Friel@AMIS.COM

Question: #33.23

Resketch Fig. 33.79 for the cases when the thermal noise is averaged. Show the cases with K=1,2,4,8, and 16.

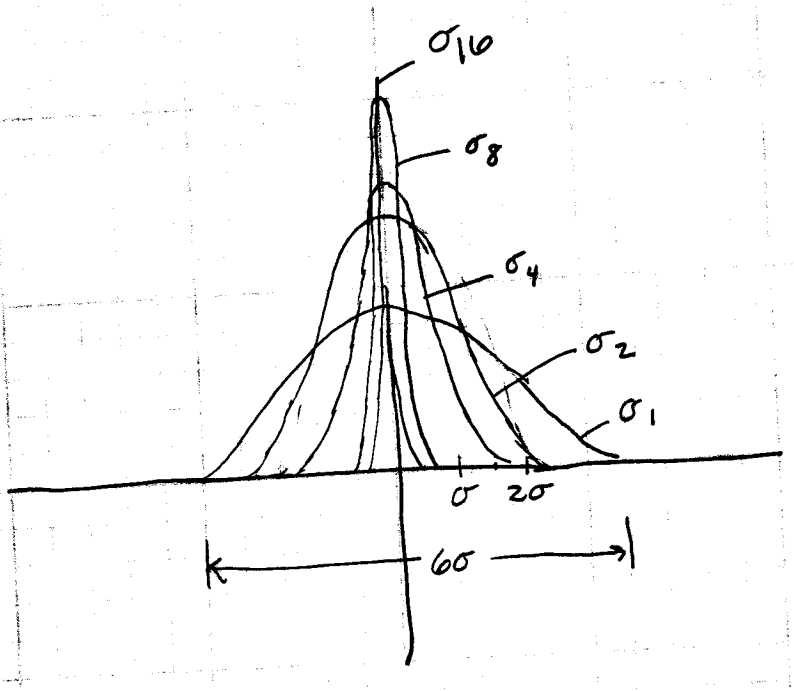
Solution:

Using Eq. 33.30 for averaging K samples of a random variable, results in a reduction of its RMS value:

$$\sigma_{K,therm} = \frac{\sigma_{therm}}{\sqrt{K}}, or, \sigma^2_{K,therm} = \frac{\sigma^2_{K,therm}}{K} \qquad \text{Eq. 33.30}$$

As shown in the figure on the next page, the shape of the Gaussian PDF get taller and narrower as we average the random signal. The area remains contant and equal to one.

33.23)



Eq 33.30 $\sigma_{k,therm} = \frac{\sigma}{\sqrt{k}}$

for $k=1$ $\sigma_{k_1} = \sigma/\sqrt{1} = \sigma_k$

$k=2$ $\sigma_{k_2} = \sigma/\sqrt{2} = .707\sigma$

$k=4$ $\sigma_{k_4} = \sigma/\sqrt{4} = .5\sigma$

$k=8$ $\sigma_{k_8} = \sigma/\sqrt{8} = .353\sigma$

$k=16$ $\sigma_{k_{16}} = \sigma/\sqrt{16} = .25\sigma$

EACH curve HAS SAME AREA, DIFFERENT MAGNITUDES

33.24 Suppose a MOSFET is used as a switch connecting an input signal to a capacitor. The MOSFET can be modeled, for noise purposes while the switch is on, as a simple resistor, Fig. 33.82. When the capacitor is charged, zero current flows in the MOSFET. Is the noise in the circuit due to thermal or 1/f (flicker) noise? Why? Note that each time the MOSFET turns on we can think that an RMS noise voltage of SQRT(kT/C) is sampled on the capacitor.

Solution:
When zero current flows, the noise will be due to thermal noise. Thermal noise is not a function of current, but rather temperature and the capacitance.