Ben Rivera
brivera@ieee.org

34.1) We can approach this problem in one of two ways, either by utilizing the equations given in the book or using circuit analysis, we'll do both.

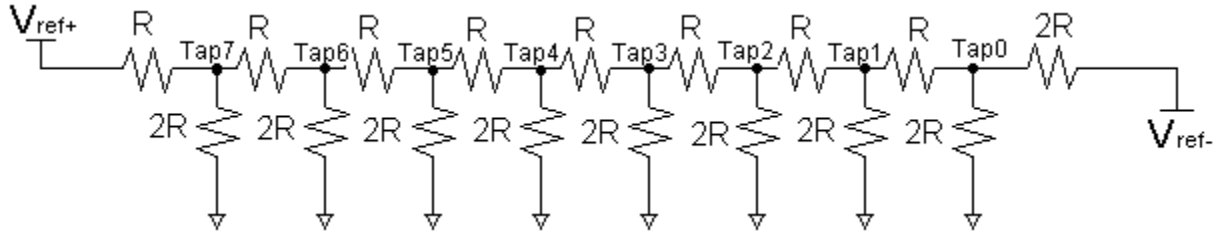
$$V_{TAPX} = \frac{2^X}{2^N} \bullet (V_{REF+} - V_{REF-}) + V_{REF-} \quad \text{EQ(34.1)}$$

8-Bit R-2R DAC

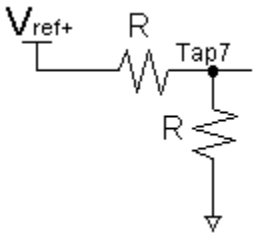
N	X	V_{TAPX}
8	0	.00586
8	1	.01172
8	2	.02343
8	3	.04687
8	4	.09375
8	5	.1875
8	6	.375
8	7	.75

Using circuit analysis will require a little more work but will give more of an understanding how the circuit is working.

Schematic of the circuit is shown with just the resistors, Vref+=1.5V and Vref-=0, in the circuit.



Starting from the left we have the 2R resistors in parallel which gives us an R in series with the R between the two Tap voltages and continuing all the way we are left with a simple voltage divider.



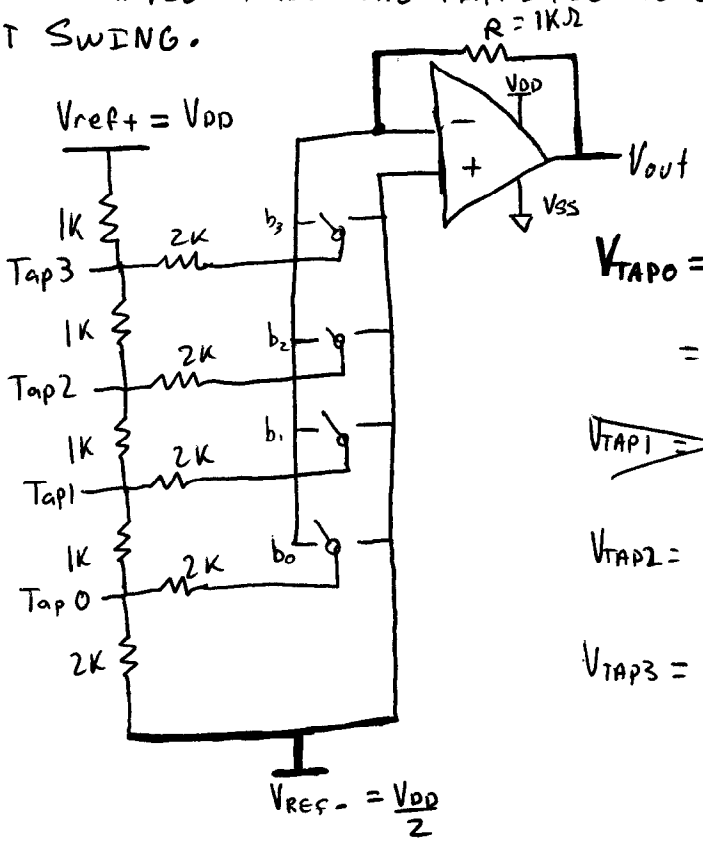
V_{tap7}=1.5/2=.75V
V_{tap6}=.75/2=.375V
V_{tap5}=.375/2=.1875V
V_{tap4}=.1875/2=.09375V
V_{tap3}=.09375/2=.04687V
V_{tap2}=.04687/2=.02343V
V_{tap1}=.02343/2=.01172V
V_{tap0}=.01172/2=**.00586V**

This result agrees with the value for the LSB of the circuit: 1LSB=$1.5/2^8$=.00586V

(34.2)

Jake Anderson
janderson@boisestate.edu

GIVE AN EXAMPLE OF HOW THE TRADITIONAL CURRENT MODE DAC WILL HAVE LIMITED OUTPUT SWING.



$V_{DD} = 5V$

(34.1) $V_{TAPx} = \frac{2^x}{2^N}(V_{REF+} - V_{REF-}) + V_{REF-}$

$V_{TAP0} = \frac{2^0}{2^4}\left(\frac{V_{DD}}{2}\right) + \frac{V_{DD}}{2}$

$= \frac{V_{DD}}{32} + \frac{V_{DD}}{2} = 2.65625V$

~~$V_{TAP1} = \frac{V_{DD}}{2} + V_{DD}$~~ $V_{TAP1} = \frac{V_{DD}}{2} + \frac{V_{DD}}{16} = 2.8125V$

$V_{TAP2} = \frac{V_{DD}}{2} + \frac{V_{DD}}{8} = 3.125V$

$V_{TAP3} = \frac{V_{DD}}{2} + \frac{V_{DD}}{4} = 3.75V$

The maximum current draw is when each switch is connected the inverting input.

This current is

$$I_{MAX} = \frac{V_{TAP0} + V_{TAP1} + V_{TAP2} + V_{TAP3} - 4V_{REF-}}{2K\Omega}$$

$$= \frac{2.65625 + 2.8125 + 3.125 + 3.75 - 4 \cdot 5/2}{2K\Omega} = 1.1718mA$$

$I_{min} = 0$, when all the switches are connected to the non inverting input.

$$\frac{V_{REF-} - V_{OUT_{min}}}{1K\Omega} = I_{max}$$

$$V_{OUT_{min}} = V_{REF-} - I_{MAX}(1K\Omega) = \frac{V_{DD}}{2} - (1.1718)(1) = 1.328$$

$V_{OUT_{max}} = V_{REF} - I_{min}(R)$

$= 5/2 - 0 = \frac{VDD}{2}$

So for this standard current mode DAC

V_{out} ranges from (1.328 — 2.5 Volts)

If the DAC has more bits it only causes the minimum Vout to decrease, but it doesn't change $V_{out\,max} = V_{REF}$.

The op-amp can't have its output go below the power supply Vss = 0 V.

Solution 34.3:

By applying superposition theorem, for fig. 3.2
Voltage at R-2R tap we can write as,

$$V_{(R\text{-}2R)_{n\text{-}1}} = \frac{b_{(N-1)}V_{REF}^{+} + \overline{b_{(N-1)}}V_{REF}^{-}}{2^1} + \frac{b_{(N-2)}V_{REF}^{+} + \overline{b_{(N-2)}}V_{REF}^{-}}{2^2} + \ldots\ldots\ldots + V_{REF}^{-}$$

For 8 bit DAC, N=8, and $V_{REF}^{+} = 1.5V$, $V_{REF}^{-} = 0V$,

So voltage at $V_{(R\text{-}2R)}$ tap would be:

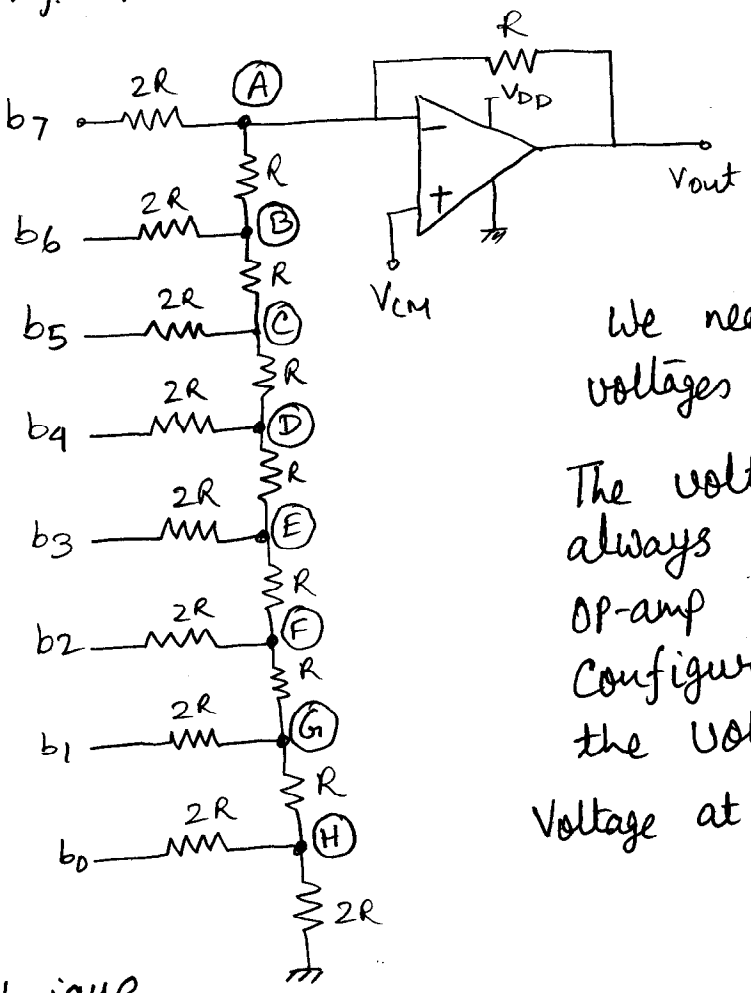
tap no.	$V_{(R\text{-}2R)}$ tap	$V_{(R\text{-}2R)}$ tap, if b_0, ……., b_7 =1
0	$\frac{3}{2}(\frac{b_0}{2^8})$	5.86mV
1	$\frac{3}{2}(\frac{b_0}{2^8}+\frac{b1}{2^7})$	17.58mV
2.	$\frac{3}{2}(\frac{b_0}{2^8}+\ldots+\frac{b2}{2^6})$	41mV
3	$\frac{3}{2}(\frac{b_0}{2^8}+\ldots.+\frac{b3}{2^5})$	87.88mV
4	……..	181.63mV
5	…….	369.13mV
6	……	750mV
7	$\frac{3}{2}(\frac{b_0}{2^8}+\ldots\ldots\ldots+\frac{b7}{2})$	1.5V

SOLUTION FOR 34.4 by

SUGATO MUKHERJEE
e-mail : msugato@ieee.org

Q: For the wide-swing current mode DAC shown in Fig. 34.3 what are the voltages at the taps along the R-2R string assuming 8-bits, $V_{REF+} = 1.5V$, $V_{REF-} = 0$, and a digital input code of 0000 0000 ?

Ans: Fig. 34.3 is redrawn as shown for 8 bit case



We need to calculate the voltages at nodes A to H.

The voltage at node A is always held at V_{CM} by the op-amp working in feedback configuration irrespective of the voltage values at $b_7 - b_0$.

Voltage at b_i = V_{REF+} if bit $i = 0$
= V_{REF-} if bit $i = 1$
$i = 0, 1, 2, \ldots 7$

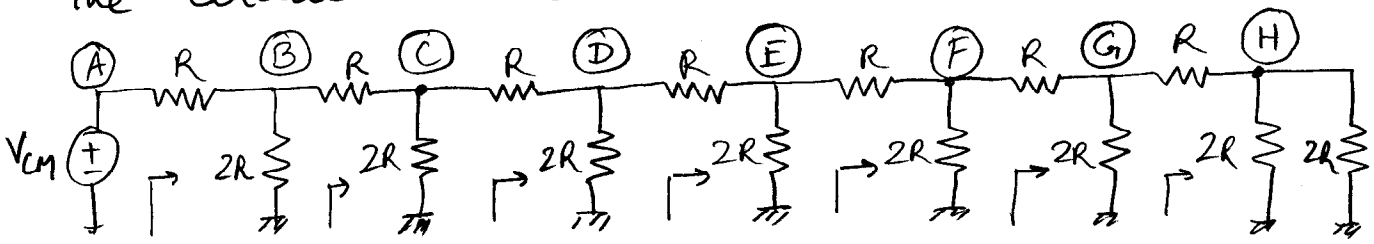
Technique

To solve this problem, we use the superposition theorem. $b_7 - b_0$ are 8 independent sources along with node A which is always held at V_{CM} by the op-amp. At each node from B to H, we superpose the effect of these 9 independent sources individually and then sum the individual effects to determine the expression for the voltage at each node. We then calculate the voltage value at each node for the given digital input code "0000 0000".

Independent source V_{CM}

We ground all other independent sources (ie $b_0 - b_7$).

The circuit becomes:



We find that the resistance looking to the right of A, B, ..., G is 2R to ground.

Voltage at A = V_{CM}

Voltage at B = $\frac{V_{CM}}{2}$ →

" " C = $\frac{V_{CM}}{4}$ →

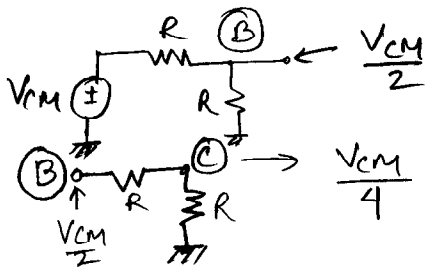
" " D = $\frac{V_{CM}}{8}$

" " E = $\frac{V_{CM}}{16}$

" " F = $\frac{V_{CM}}{32}$

" " G = $\frac{V_{CM}}{64}$

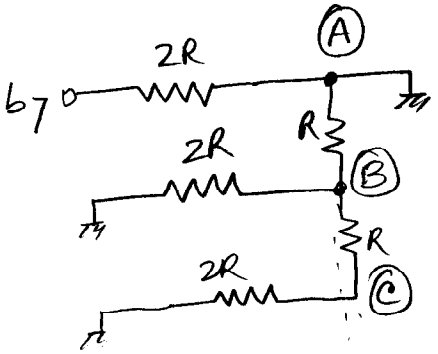
" " H = $\frac{V_{CM}}{128}$

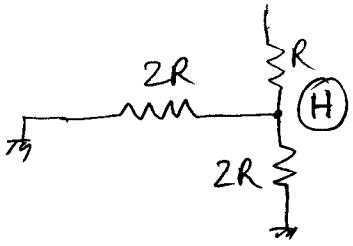


Independent source b_7

We ground all other independent sources (V_{CM}, $b_0 - b_6$)

We find that the contribution of b_7 at nodes A - H is zero.





Independent source b_6

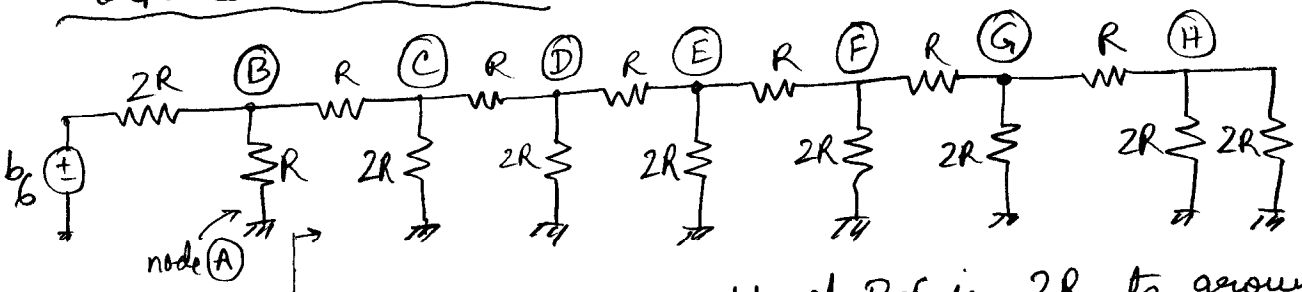
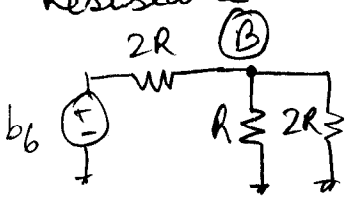


Fig b_6

Resistance looking to the right of B-G is 2R to ground.

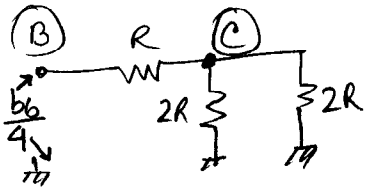


$$\text{Voltage at B} = b_6 \cdot \frac{R // 2R}{2R + (R // 2R)}$$

$$= b_6 \cdot \frac{\frac{2R}{3}}{2R + \frac{2R}{3}}$$

$$= b_6 \cdot \frac{\frac{2R}{3}}{\frac{8R}{3}}$$

$$= \frac{b_6}{4}$$



$$\text{Voltage at C} = \frac{b_6}{4} \cdot \frac{2R // 2R}{R + (2R // 2R)}$$

$$= \frac{b_6}{4} \cdot \frac{R}{R+R}$$

$$= \frac{b_6}{8}$$

Similarly, Voltage at D = $\frac{b_6}{16}$

E = $\frac{b_6}{32}$

F = $\frac{b_6}{64}$

G = $\frac{b_6}{128}$

H = $\frac{b_6}{256}$

Independent source b_5

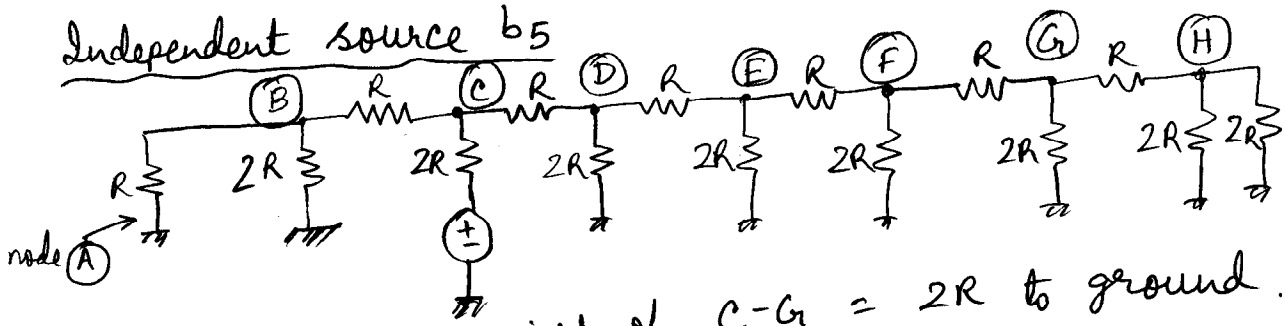
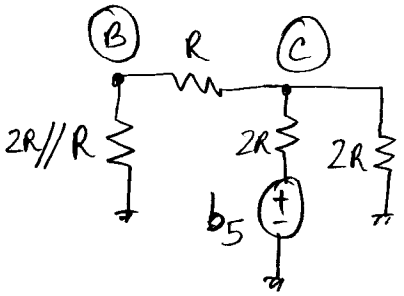


Fig b_5

Resistance looking right of C-G = 2R to ground.



Resistance looking left of C = R//2R to ground

$= \frac{2R}{3} + R = \frac{5R}{3}$ to ground

Voltage at C $= b_5 \cdot \frac{2R // \frac{5}{3}R}{2R + 2R // \frac{5}{3}R}$

$= b_5 \cdot \frac{\frac{10R}{3} / \left(\frac{11}{3}\right)}{2R + \frac{10R}{11}}$

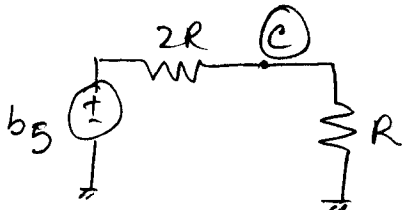
$= b_5 \cdot \frac{10}{32}$

Now $2R // \frac{5}{3}R$

$= \frac{10R}{11}$

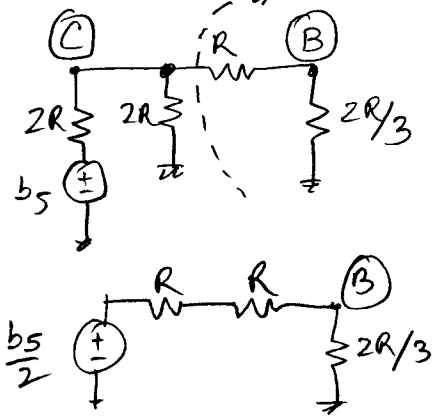
$\simeq R$.

If we make this approximation, then the voltage at C becomes



$b_5 \cdot \frac{R}{R+2R} = \frac{b_5}{3}$.

Voltage at B



Thevenizing the circuit to the right of B, we get

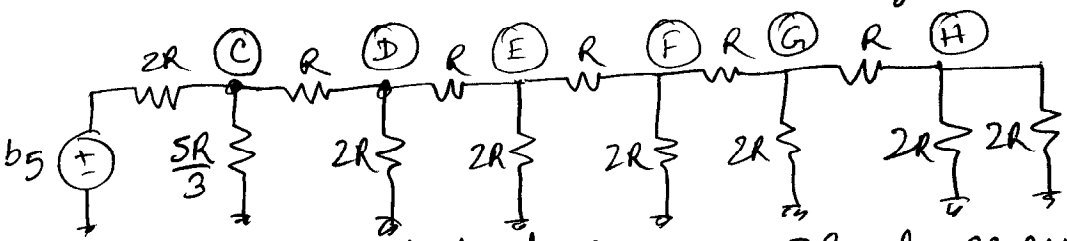
$V_{Th} = b_5 \cdot \frac{2R}{2R+2R} = \frac{b_5}{2}$

$R_{Th} = 2R // 2R = R$.

Voltage at B $= \frac{b_5}{2} \cdot \frac{\frac{2R}{3}}{2R + \frac{2R}{3}}$

$= \frac{b_5}{2} \cdot \frac{\frac{2R}{3}}{\frac{8R}{3}}$

Voltage at B $= \frac{b_5}{8}$.



Resistance looking right of C-G = 2R to ground.

Looking at the previous analysis for b_6, we know that the voltage at D-H will be $\frac{V_c}{2}, \frac{V_c}{4}, \frac{V_c}{8}, \frac{V_c}{16}, \frac{V_c}{32}$

where V_c = voltage at C.

The exact expression for the voltage at C $= \frac{5}{16} b_5$

The approximate expression is $\frac{b_5}{3}$

Voltage at	Exact	Approx.
D	$\frac{5b_5}{32}$	$\frac{b_5}{6}$
E	$\frac{5}{64} b_5$	$\frac{b_5}{12}$
F	$\frac{5}{128} b_5$	$\frac{b_5}{24}$
G	$\frac{5}{256} b_5$	$\frac{b_5}{48}$
H	$\frac{5}{512} b_5$	$\frac{b_5}{96}$

Independent source b_4

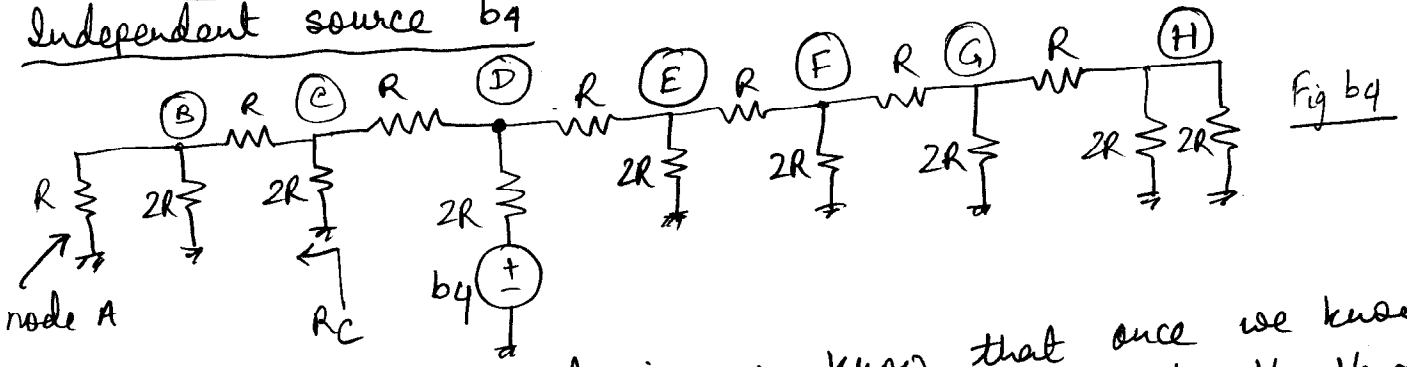
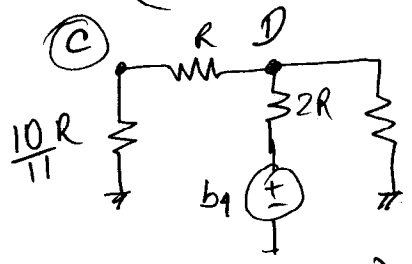


Fig b_4

From previous analysis, we know that once we know the voltage at D, (E, F, G, H) will have $\frac{V_D}{2}$, $\frac{V_D}{4}$, $\frac{V_D}{8}$, $\frac{V_D}{16}$ resp.

Also, resistance looking left of C $= [(R//2R)+R]//2R$ to ground

$$R_C = \left(\frac{2R}{3}+R\right)//2R = \frac{5R}{3}//2R = \frac{10}{11}R \simeq R.$$



$2R$ (circuit to right of D)

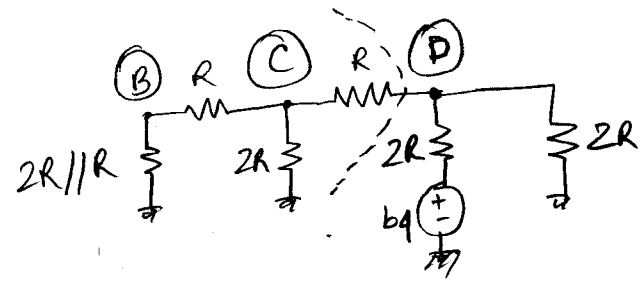
$$V_D = b_4 \cdot \frac{\left(R+\frac{10R}{11}\right)//2R}{2R+\left[\left(R+\frac{10R}{11}\right)//2R\right]} \simeq b_4 \cdot \frac{(R+R)//2R}{2R+[(R+R)//2R]} = b_4 \cdot \frac{R}{2R+R}$$

$$V_D = \frac{b_4}{3}$$

Exact expression for $V_D = \frac{21}{64} b_4$

	Exact	Approx.
$V_E =$	$\frac{21}{128} b_4$	$\frac{b_4}{6}$
$V_F =$	$\frac{21}{256} b_4$	$\frac{b_4}{12}$
$V_G =$	$\frac{21}{512} b_4$	$\frac{b_4}{24}$
$V_H =$	$\frac{21}{1024} b_4$	$\frac{b_4}{48}$

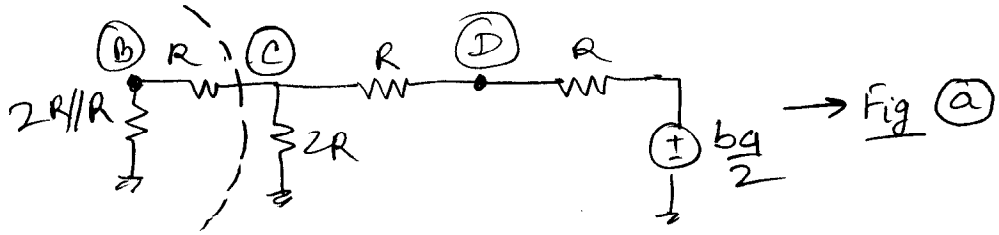
To find V_B



Thevenizing the elements at node D we get.

$$V_{TH} = b4 \cdot \frac{2R}{2R+2R} = \frac{b4}{2}$$

$$R_{TH} = 2R//2R = R.$$

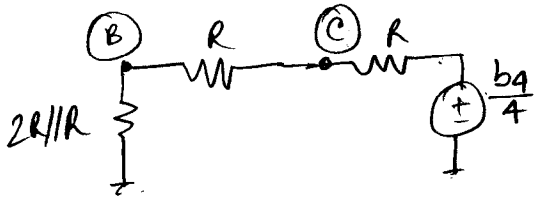


→ Fig (a)

Thevenizing elements at node C (and right of it), we get

$$V_{TH} = \frac{b4}{2} \cdot \frac{2R}{2R+2R} = \frac{b4}{4}$$

$$R_{TH} = 2R//2R = R.$$



$$V_B = \frac{b4}{4} \cdot \frac{2R//R}{2R+(2R//R)}$$

$$= \frac{b4}{4} \cdot \frac{\frac{2R}{3}}{2R+\frac{2R}{3}} = \frac{b4}{4} \cdot \frac{1}{4}$$

$$\boxed{V_B = \frac{b4}{16}}$$

To find V_C Referring to Fig (a) above,

$$V_C = \frac{b4}{2} \cdot \frac{2R//(R+2R//R)}{2R+[2R//\{R+2R//R)]} = \frac{b4}{2} \cdot \frac{2R//5R/3}{2R+(2R//5R/3)}$$

$$= \frac{b4}{2} \cdot \frac{(10/11\,R)}{2R+10/11\,R} \leftarrow R_C \qquad R_C = \frac{10}{11}R \simeq R.$$

$$\boxed{V_C \text{ (exact)} = \frac{b4}{2} \cdot \frac{10}{32} = \frac{5b4}{32}}$$

$$\boxed{V_C \text{ (approx.)} = \frac{b4}{2} \cdot \frac{R}{2R+R} = \frac{b4}{2} \cdot \frac{1}{3} = \frac{b4}{6}}$$

Independent source b_3

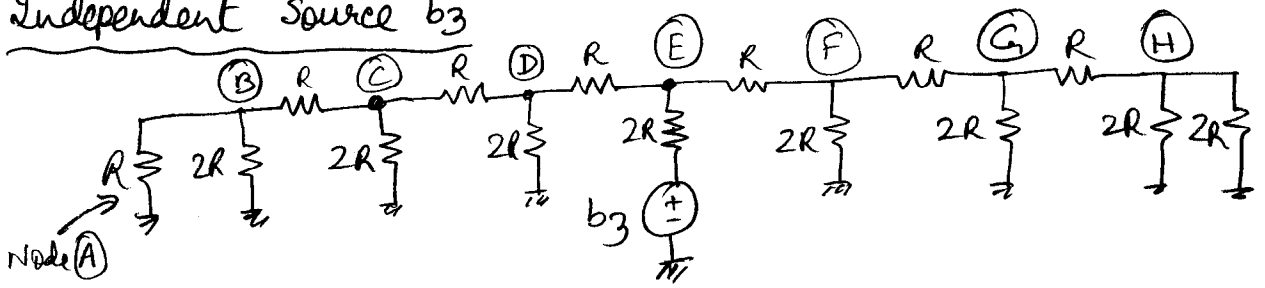
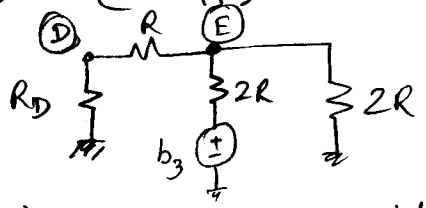


fig. b_3

We know $R_E = \frac{10R}{11} \simeq R$.

$R_D = \left(R + \frac{10R}{11}\right) // 2R = \frac{42}{43} R \simeq R$.

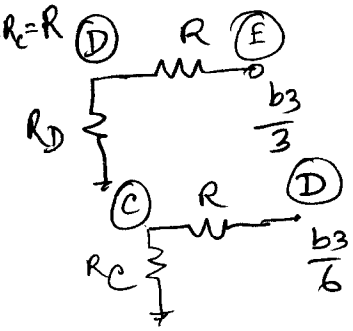


Using $R_D = \frac{42}{43}R$, $V_E = b_3 \cdot \frac{2R // \left(R + \frac{42R}{43}\right)}{2R + \left[2R // \left(R + \frac{42R}{43}\right)\right]} = b_3 \cdot \frac{\frac{170}{171} R}{2R + \frac{170}{171} R}$

$= b_3 \cdot \frac{170}{512} = b_3 \cdot \frac{85}{256}$

Using $R_D = R$, $V_E = b_3 \cdot \frac{2R // 2R}{2R + (2R // 2R)} = \frac{b_3}{3}$

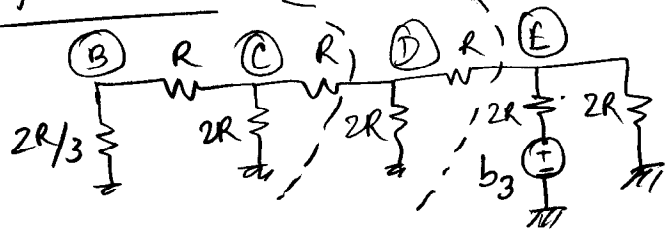
Using $V_E = \frac{b_3}{3}$, $R_D = R_C = R$



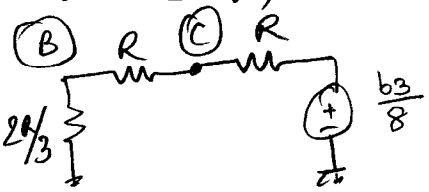
$V_D = \frac{b_3}{6}$

$V_C = \frac{b_3}{12}$

To find V_B



Thevenizing successively at (E) and (D) & (C), we get.



$V_B = \frac{b_3}{8} \cdot \frac{2R/3}{2R + \frac{2R}{3}} = \frac{b_3}{8} \cdot \frac{1}{4}$

$\boxed{V_B = \frac{b_3}{32}}$

Looking at the symmetry of the circuit referring to Fig $b_3/b_4/b_5$, we can write (extrapolate) the results for independent sources b_2, b_1, b_0 using the approximation $R_C = R_D = R_E = R_F = R_G \simeq R$. The exact expression for the voltages is also given for comparison purpose.

Exact values: $R_C = \frac{10R}{11}$, $R_D = \frac{42R}{43}$, $R_E = \frac{170R}{171}$, $R_F = \frac{682}{683}R$, $R_G = \frac{2730}{2731}R$

Node	Exact Expression	Approximate Expression
A	V_{CM}	V_{CM}
B	$\frac{V_{CM}}{2} + \frac{b_6}{4} + \frac{b_5}{8} + \frac{b_4}{16} + \frac{b_3}{32} + \frac{b_2}{64} + \frac{b_1}{128} + \frac{b_0}{256}$	$\frac{V_{CM}}{2} + \frac{b_6}{4} + \frac{b_5}{8} + \frac{b_4}{16} + \frac{b_3}{32} + \frac{b_2}{64} + \frac{b_1}{128} + \frac{b_0}{256}$
C	$\frac{V_{CM}}{4} + \frac{b_6}{8} + \frac{5b_5}{16} + \frac{5}{32}b_4 + \frac{5}{64}b_3 + \frac{5}{128}b_2 + \frac{5}{256}b_1 + \frac{5}{512}b_0$	$\frac{V_{CM}}{4} + \frac{b_6}{8} + \frac{b_5}{3} + \frac{b_4}{6} + \frac{b_3}{12} + \frac{b_2}{24} + \frac{b_1}{48} + \frac{b_0}{96}$
D	$\frac{V_{CM}}{8} + \frac{b_6}{16} + \frac{5}{32}b_5 + \frac{21}{64}b_4 + \frac{21}{128}b_3 + \frac{21}{256}b_2 + \frac{21}{512}b_1 + \frac{21}{1024}b_0$	$\frac{V_{CM}}{8} + \frac{b_6}{16} + \frac{b_5}{6} + \frac{b_4}{3} + \frac{b_3}{6} + \frac{b_2}{12} + \frac{b_1}{24} + \frac{b_0}{48}$
E	$\frac{V_{CM}}{16} + \frac{b_6}{32} + \frac{5}{64}b_5 + \frac{21}{128}b_4 + \frac{85}{256}b_3 + \frac{85}{512}b_2 + \frac{85}{1024}b_1 + \frac{85}{2048}b_0$	$\frac{V_{CM}}{16} + \frac{b_6}{32} + \frac{b_5}{12} + \frac{b_4}{6} + \frac{b_3}{3} + \frac{b_2}{6} + \frac{b_1}{12} + \frac{b_0}{24}$
F	$\frac{V_{CM}}{32} + \frac{b_6}{64} + \frac{5}{128}b_5 + \frac{21}{256}b_4 + \frac{85}{512}b_3 + \frac{341}{1024}b_2 + \frac{341}{2048}b_1 + \frac{341}{4096}b_0$	$\frac{V_{CM}}{32} + \frac{b_6}{64} + \frac{b_5}{24} + \frac{b_4}{12} + \frac{b_3}{6} + \frac{b_2}{3} + \frac{b_1}{6} + \frac{b_0}{12}$
G	$\frac{V_{CM}}{64} + \frac{b_6}{128} + \frac{5}{256}b_5 + \frac{21b_4}{512} + \frac{85b_3}{1024} + \frac{341b_2}{2048} + \frac{1365b_1}{4096} + \frac{1365b_0}{8192}$	$\frac{V_{CM}}{64} + \frac{b_6}{128} + \frac{b_5}{48} + \frac{b_4}{24} + \frac{b_3}{12} + \frac{b_2}{6} + \frac{b_1}{3} + \frac{b_0}{6}$
H	$\frac{V_{CM}}{128} + \frac{b_6}{256} + \frac{5b_5}{512} + \frac{21b_4}{1024} + \frac{85b_3}{2048} + \frac{341b_2}{4096} + \frac{1365b_1}{8192} + \frac{5461b_0}{16384}$	$\frac{V_{CM}}{128} + \frac{b_6}{256} + \frac{b_5}{96} + \frac{b_4}{48} + \frac{b_3}{24} + \frac{b_2}{12} + \frac{b_1}{6} + \frac{b_0}{3}$

For an input code of "0000 0000", $b_7 - b_0$ are $V_{REF+} = 1.5V$.

Node	Exact Voltage	Approx. Voltage	% Error
A	0.750 V	0.750 V	0
B	1.119 V	1.119 V	0
C	1.298 V	1.359 V	4.70
D	1.375 V	1.406 V	2.25
E	1.391 V	1.406 V	1.08
F	1.352 V	1.359 V	0.52
G	1.238 V	1.242 V	0.32
H	0.994 V	0.996 V	0.20

Solution by:
Curtis Cahoon
curtis_cahoon@ieee.org

Problem 34.5

Question: Can the op-amp shown in Fig. 34.36 be used in a fully differential implementation of the DACs shown in Figs. 34.1-34.3? Why or why not?

Answer: No, the op-amp of figure 34.36 cannot be used to implement an R2R DAC, because the amplifier does not have an output buffer, and therefore cannot drive a reasonable resistive load on an IC. This is because an op-amp with reasonably high gain has a very high output resistance (on the order of mega ohms). If we add a typical resistive load in the feedback path of the op-amp in these topologies, it will load the output of the amplifier and it will kill the gain, and thus not operate correctly. If an output buffer is added, the gain will not be reduced, but the output current drive capability will be increased, thus enabling the amplifier to drive the resistive loads used in the DAC topologies.

Problem 34.6

Show the detailed derivation of eqs.(34.12)-(34.14).

For a binary-weighted DAC, the midscale transition has the worst-case DNL condition caused by resistor mismatch. In a worst-case scenario, assume the 2R resistor of the MSB input has a maximum mismatch of ΔR and all other resistors have a maximum mismatch of - ΔR.

The equation 34.9 shows the current flowing in the feedback resistor Rf,

$$I_F = -\frac{V_{REF+} - V_{REF-}}{2R} + \frac{V_{REF+} - V_{REF-}}{2R} \left[1 \ \overline{b_{N-1}} + \frac{1}{2} \ \overline{b_{N-2}} + \ldots + + \frac{1}{2^{n-1}} \ \overline{b_0} \right]$$

The step error of this current caused by resistor mismatch at the midscale transition is

$$\begin{aligned}
\Delta I &= (I_{N-2} + I_{N-3} + \ldots + I_0) - I_{N-1} \\
&= \frac{V_{REF+} - V_{REF-}}{2(R - \Delta R)}\left(\frac{1}{2^1} + \frac{1}{2^2} + \ldots + \frac{1}{2^{N-1}}\right) - \frac{V_{REF+} - V_{REF-}}{2(R + \Delta R)} \\
&= \frac{V_{REF+} - V_{REF-}}{2(R - \Delta R)}\left(\frac{1}{2^1} + \frac{1}{2^2} + \ldots + \frac{1}{2^{N-1}} + \frac{1}{2^{N-1}} - \frac{1}{2^{N-1}}\right) - \frac{V_{REF+} - V_{REF-}}{2(R + \Delta R)} \\
&= \frac{V_{REF+} - V_{REF-}}{2(R - \Delta R)}\left(1 - \frac{1}{2^{N-1}}\right) - \frac{V_{REF+} - V_{REF-}}{2(R + \Delta R)}
\end{aligned}$$

Assuming Rf= R, the final output error (DNL) is approximately,

$$\begin{aligned}
DNL = \Delta I \cdot R &= \left[\frac{V_{REF+} - V_{REF-}}{2(R - \Delta R)}\left(1 - \frac{1}{2^{N-1}}\right) - \frac{V_{REF+} - V_{REF-}}{2(R + \Delta R)}\right] \ R \\
&= (V_{REF+} - V_{REF-})\left[\left(\frac{1}{2(R - \Delta R)} - \frac{1}{2^{N-1} \cdot 2(R - \Delta R)}\right) - \frac{1}{2(R + \Delta R)}\right] R \\
&= (V_{REF+} - V_{REF-})\left[\frac{1}{2(R - \Delta R)} - \frac{1}{2^N (R - \Delta R)} - \frac{1}{2(R + \Delta R)}\right] R \\
&= (V_{REF+} - V_{REF-})\left[\frac{R + \Delta R - R + \Delta R}{2(R - \Delta R)(R + \Delta R)} - \frac{1}{2^N (R - \Delta R)}\right] R \\
&= (V_{REF+} - V_{REF-})\left[\frac{\Delta R}{(R - \Delta R)(R + \Delta R)} - \frac{1}{2^N (R - \Delta R)}\right] R \\
&\cong (V_{REF+} - V_{REF-})\left[\frac{\Delta R}{R} - \frac{1}{2^N}\right]
\end{aligned}$$

For the DNL to be less than 1 LSB, the resistor-matching requirement is

$$DNL \le 1LSB = (V_{REF+} - V_{REF-}) / 2^N$$

$$(V_{REF+} - V_{REF-})[\frac{\Delta R}{R} - \frac{1}{2^N}] \le (V_{REF+} - V_{REF-}) / 2^N$$

$$[\frac{\Delta R}{R} - \frac{1}{2^N}] \le \frac{1}{2^N}$$

$$\frac{\Delta R}{R} \le \frac{2}{2^N}$$

Resistor mismatch = $\left|\frac{\Delta R}{R}\right| \le \frac{1}{2^{N-1}}$

-Yantao Ma

Chapter 34.7

Why would we want to use both current segments & binary-weighted currents to implement a current-mode DAC? (Why use segmentation?)

[Answer]: In general, segmentation achieves better DNL with less accurate components possible required.

- Use current Mode DAC: to achieve Rail-to-Rail Output swing while keeping input Nodes of Op-Amp fixed.
- Use current-segments & binary weighted current mode DAC: Efficient method of implement high-resolution DAC.
- To against normal current mode DAC major disadvantage:
  1. overall accuracy is determined largely by major MSB's.
  2. Monotonicity cannot be guaranteed
  3. Design is not practical when DAC N becomes large due to current elements (max) rises exponentially, which cause resistor matching extremely critical and challenging for manufacturing.
- Fundamental principle: By limiting & Equilizing maximum current elements (controlled by MSB/upper bits) with more fine current resolution levels (controlled by lower bits), a number of maximum and fine current elements can be switched to feedback resistor.
  This method guarantees monotonic operation and improves DNL within 1LSB because segment current used. The accuracy of segmented DAC is determined largely by the matching of maximum current elements.
  Precision can be improved by symmetrical layout techniques and additional calibriation techniques.

— yantaoma@rocketmail.com

pkirkar@rediffmail.com

Q. 348 Why do we subtract ΔA in Eq. (34.36)? Why not add the gain variation?

Ans: Referring to chapter 29. page 821.

Accuracy issues related to OPAMP:

It is quite difficult to implement standard OPAMPs within high resolution data converters because of the accuracy requirements. The nonideal characteristics of the opamp are well known and in many cases alone limit the accuracy of the data convertors.

Generalizing the concept for N-bit application with feedback theory.

$$A_{CL} = \frac{v_o}{v_i} \Rightarrow \frac{A_{OLDC}}{1 + A_{OLDC}\beta}$$

** It is well known that as A_{OL} increases, A_{CL} approaches towards $\frac{1}{\beta}$. i.e. ideal.

So it is assumed that the A_{CL} will be equal to the ideal value of $1/\beta$ minus some maximum deviation from ideal, ΔA then

$$A_{CL} = \frac{V_o}{v_i} = \frac{A_{OL}}{1 + A_{OL}\beta} = \frac{1}{\beta} \mp \Delta A \quad \text{— (*)}$$

and we know the maximum deviation would be $1/2$ LSB. Hence.

By solving (*) we can get

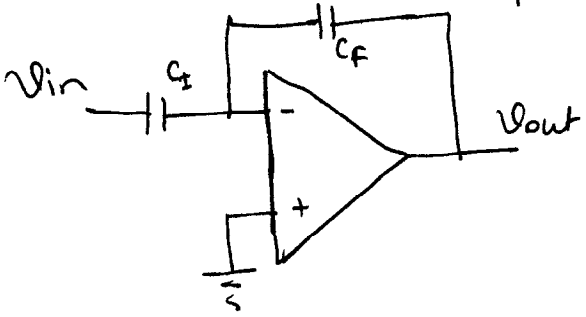
$$|A_{OL}| = 1/\beta \left(2^{N+1} + 1\right) = \frac{2^{N+1}}{\beta}$$

$$|A_{OL}| \geq \frac{2^{N+1}}{\beta}$$

$\therefore N \Rightarrow$ no of bits.
$\beta \Rightarrow$ feedback factor
$A \Rightarrow$ open loop gain
$A_{CL} \Rightarrow$ closed loop gain.

Referring to the equation 34.36

$$|A_{CL}| = \frac{C_I}{C_F} - \Delta A \Rightarrow \frac{A_{OLDC}}{1 + A_{OLDC} \cdot \frac{C_F}{C_F + C_I}}$$



$$\Delta A = \frac{\epsilon_I}{C_F} \cdot \frac{1/2\,LSB}{full\,scale\,i/p} \Rightarrow \frac{C_I}{C_F} \cdot \frac{1}{2^{N+1}}$$

Similar as previous discussion we get

$$|A_{OLDC}| \geq (1/\beta)\, 2^{N+1}$$

So mainly the reason to minus the ΔA from ideal close loop gain is well known and i.e. as A_{OLDC} increases then and then only we can approach to $A_{CL} = 1/\beta$. But

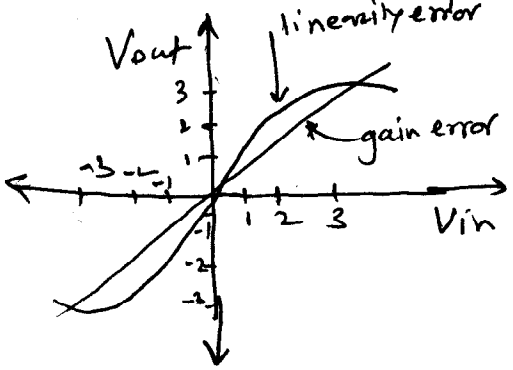
$$|A_{OLDC}| \geq \frac{1}{\beta} \cdot 2^{N+1}$$

Hence, there it can is notiable that for every bit increase in the resolution the open loop gain requirements double.

So the ideal $A_{CL} = 1/\beta$ which is possible only when $A_{OLDC} = \infty$ But to get $A_{OLDC} \simeq \infty$, N should be ∞ which is not practicable (from eqn) so always the closed loop gain of the amplifier will be equal to the $1/\beta$ minus some maximum deviation from the ideal, ΔA.

* Why not add the gain variation?

Ans: The amplifier must be able to linearity amplify the input over the input voltage range to within 1/2LSB. Nonlinearity as devices in the amplifier go into nonsaturation.



* Transfer curve shows nonlinearity introduced at both ends of i/p vtg. A gain error is much less harmful to an ADC's performance than Harmonic distortion (Nonlinearity)

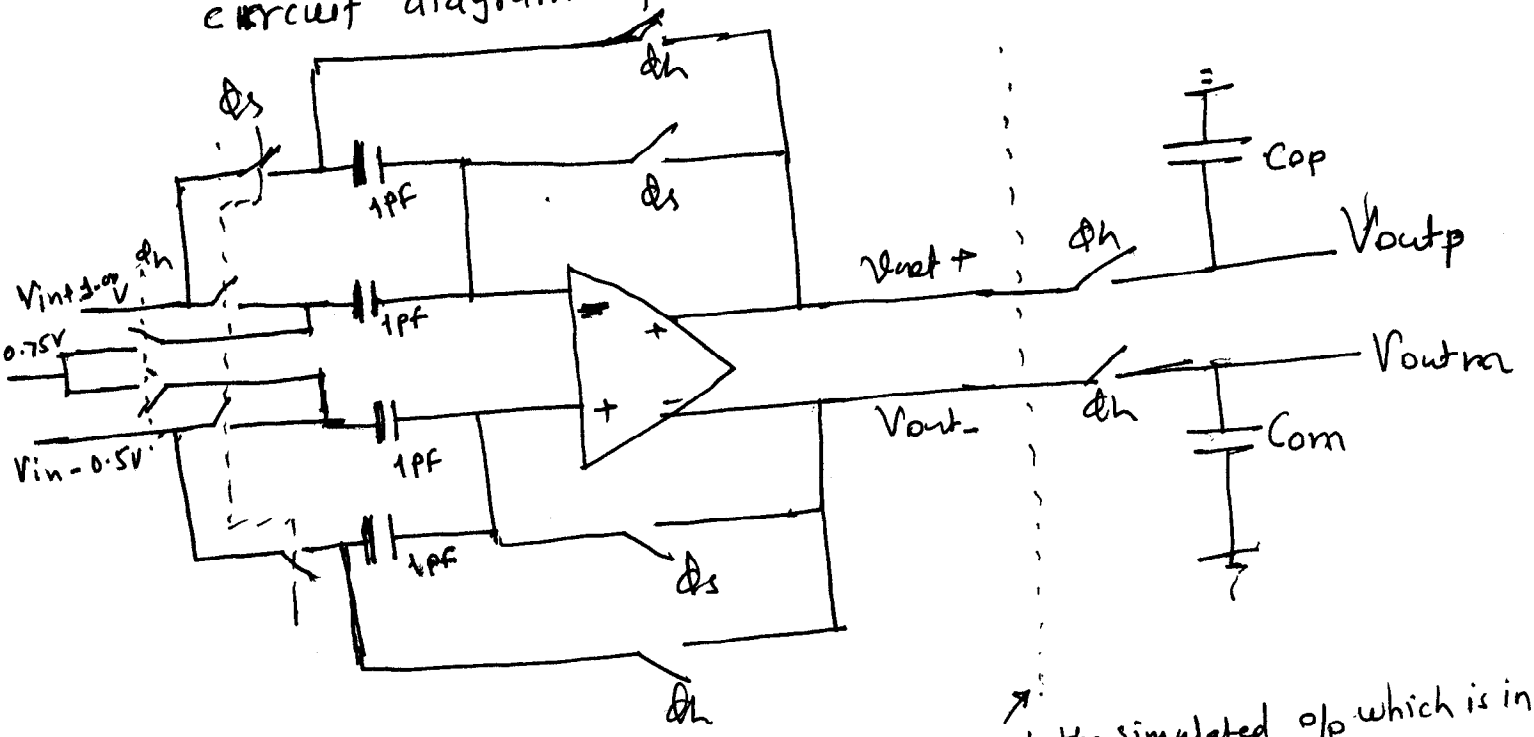
pkirkar@rediffmail.com

Q. 34.28

Repeat Ex. 34.18 if all capacitors are 1 PF (the ideal simulation) and verify that the error out of the stage is zero.

Ans:

circuit diagram of Ex. 34.18



We get the simulated o/p which is in terms of pulses. So after load capacitors we get the o/p without spikes.

The input voltage $V_{in+} - V_{in-} = 1.0 - 0.5 = 0.5\,V$

Ideally output should be equal to twice of input

i.e. 1 V

So the output at plus = 1.25 V

and output at minus = 0.25 V

The simulated results are shown in fig.

Error = $V_{ideal} - V_{outactual} \Rightarrow 1V - 1V \approx 0$.

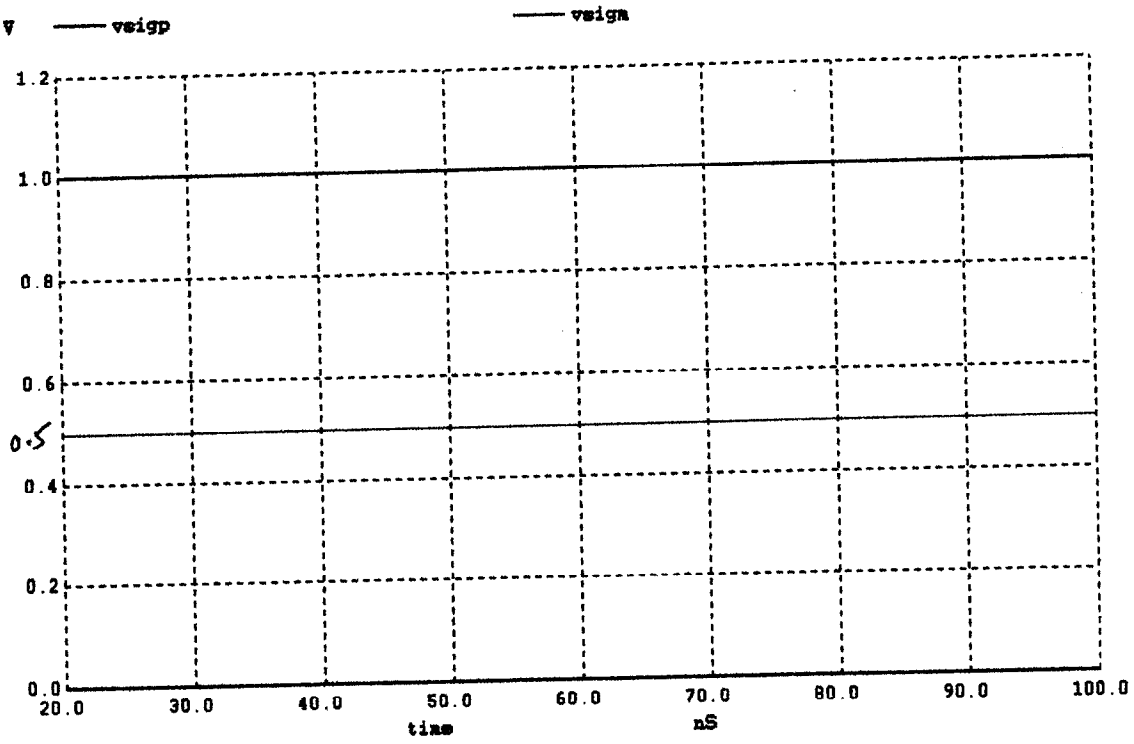
~~Input deck~~

Netlist

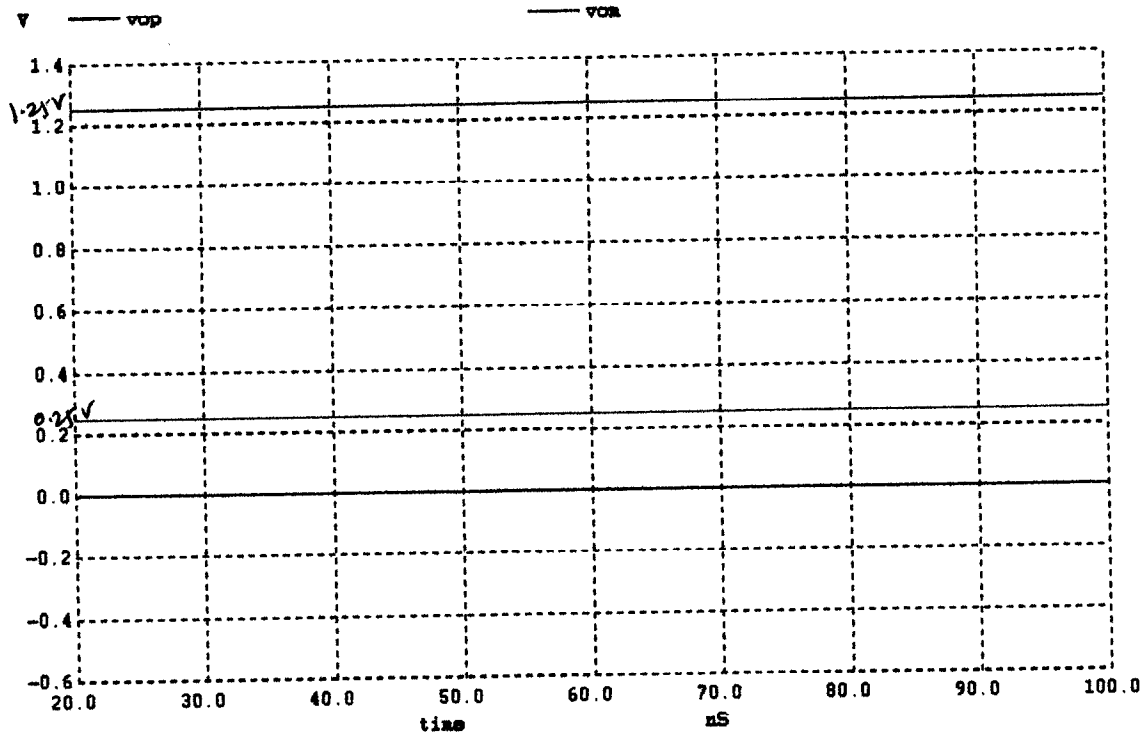
Sample and hold circuit

```
.control
destroy all
run
let Verror=Videal-(Vop-Vom)
plot Verror
.endc
.options scale=1u ABSTOL=10u VNTOL=10m RELTOL=.01

*Op-amp using VCVS
E1 Voutp Vcom Vplus Vminus 100MEG
E2 Vcom Voutm Vplus Vminus 100MEG
*Sample and hold capacitors
Cim Vminus Vcomm 1p
Cfm Vminus Vcenm 1p
Cip Vplus Vcomp 1p
Cfp Vplus Vcenp 1p
*Switches
S1 Vcenm Vsigp  phis Vswit switmod
S2 Vcomm Vsigp  phis Vswit switmod
S3 Vcomm Vcom   phih Vswit switmod
S4 Vcomp Vcom   phih Vswit switmod
S5 Vcomp Vsigm  phis Vswit switmod
S6 Vcenp Vsigm  phis Vswit switmod
S7 Voutp Vcenm  phih Vswit switmod
S8 Voutp Vminus phis Vswit switmod
S9 Voutm Vplus  phis Vswit switmod
S10 Voutm Vcenp phih Vswit switmod
S11 Voutp Vop   phih Vswit switmod
S12 Voutm Vom   phih Vswit switmod
*Load Capaitance
Cop Vop 0 10p
Com Vom 0 10p
*Supply voltage
VDD VDD 0 DC 1.5
*Reference voltages
Vswit Vswit 0 DC 0.75
Vcom  Vcom  0 DC 0.75
*Input Signals
Vsigp   Vsigp   0 DC 1.0
Vsigm   Vsigm   0 DC 0.5
*Ideal signal
Videal  Videal  0 DC 1
*Clock Signals
Vphis  phis  0 DC 0  Pulse 0 1.5  0   200p  200p  4n 10n
Vphih  phih  0 DC 0  Pulse 0 1.5  5n  200p  200p  4n 10n
Rs phis 0 1MEG
Rh phih 0 1MEG

.tran 2n 400n 0 2n UIC
.model switmod SW RON=1
.end
```

Input signals

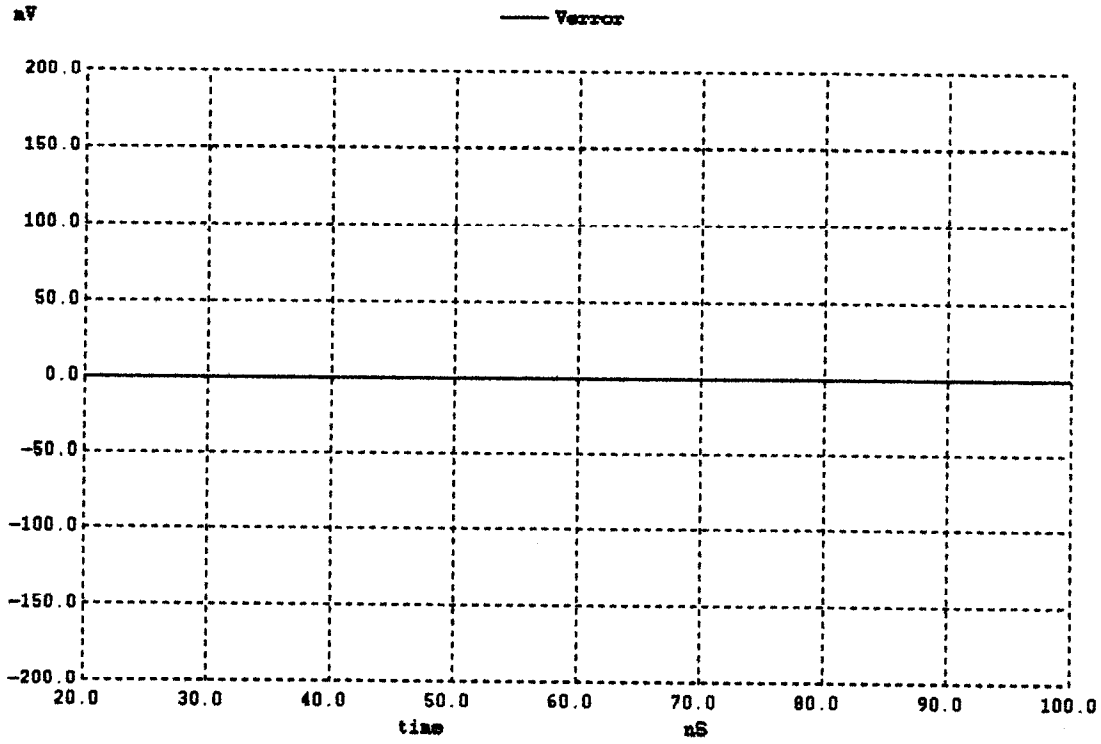


Output Signals



$V_{op} - V_{om} = 1.25 - .25 = 1V$

Error signal=Ideal signal-Actual signal



$$\text{Error} = V_{ideal} - V_{out}$$

$$= 1V - (V_{op} - V_{om})$$

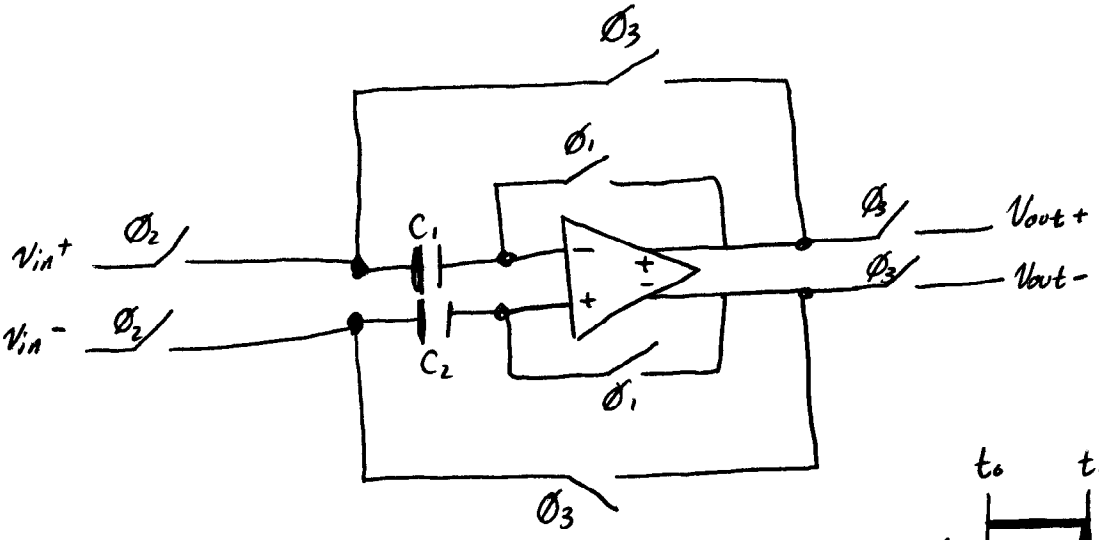
$$= 1V - (1.25 - 0.25)$$

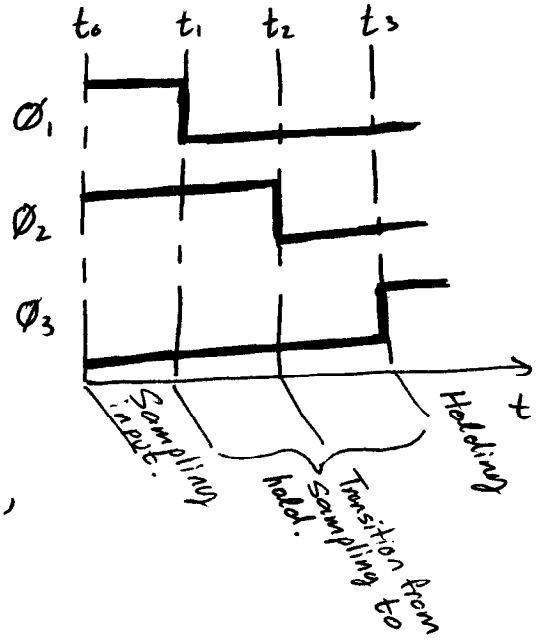
$$= \underline{0}$$

(34.9)

Jake Anderson
janderson@boisestate.edu

DOES MATCHING OF THE CAPACITORS MATTER IN THE S/H OF FIG 34.31?





To make it easier to analize. Let's have the input $V_{in} = V_{in}^+ - V_{in}^-$ be zero, or $V_{in}^+ = V_{in}^- = V_{cm}$.
So for this example, the circuit will be sampling $v_{in} = 0$.

For $t < t_1$

The charge stored on the storage capacitors, C_1 & C_2 is:

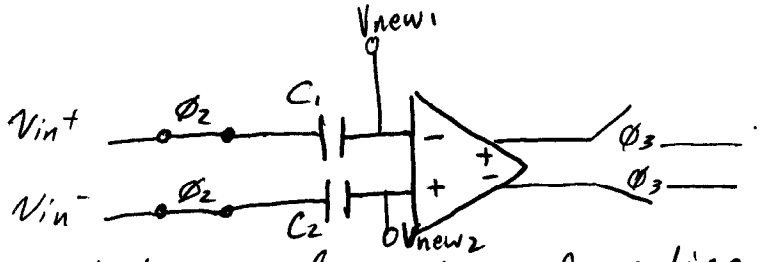
$$Q_1 = (V_{in}^+ - V_{cm})C_1 = (V_{cm} - V_{cm})C_1 = 0 = Q_{SAMPLED1}$$

$$Q_2 = (V_{in}^- - V_{cm})C_2 = (V_{cm} - V_{cm})C_2 = 0 = Q_{SAMPLED2}$$

For $t_1 < t < t_2$

At the beginning of this period, the $\emptyset_1$ switches turn off. Since the $\emptyset_1$ switches are the same size and the Bias voltages are all the same, they should both inject the same amount of charge, δQ, to the inputs (the top plates of the capacitor) of the op-amp.

The S/H circuit for this time ($t_1 < t < t_2$) is as shown below.



The op-amp is in open-loop gain configuration, making it very sensitive to differential input voltages.

The charge δQ (from charge injection of ϕ_1 switches turning off) is input to both inputs of the differential op-amp.

$$Q_{TOTAL\,1} = Q_{SAMPLED\,1} + \delta Q = \delta Q = (V_{in}^{+} - V_{new1})C_1 = (V_{cm} - V_{new1})C_1$$

$$Q_{TOTAL\,2} = Q_{SAMPLED\,2} + \delta Q = \delta Q = (V_{in}^{-} - V_{new2})C_2 = (V_{cm} - V_{new2})C_2$$

$$V_{new_1} = V_{cm} - \frac{\delta Q}{C_1} \quad + \quad V_{new_2} = V_{cm} - \frac{\delta Q}{C_2}$$

If $C_1 = C_2$ then $V_{new1} = V_{new2}$ and the signal from the ϕ_1 switches turning off is common to both inputs and would Ideally be rejected.

If $C_1 \neq C_2$ then the signals V_{new_1} & V_{new_2} aren't common & they, being different, could trigger the op-amp before the ϕ_3 switches turn on

Answer: Yes, it does matter that the input capacitors are well matched.

A similar case can be made for the ϕ_2 switches turning off.

Solution 34.10:

From fig. 34.34:

When ϕ_1 node is closed:

1. if Vos=0V, in this case

   Aol $\Rightarrow \propto$
   If everything is ideal, input terminal of error amplifier would be at same potencial.

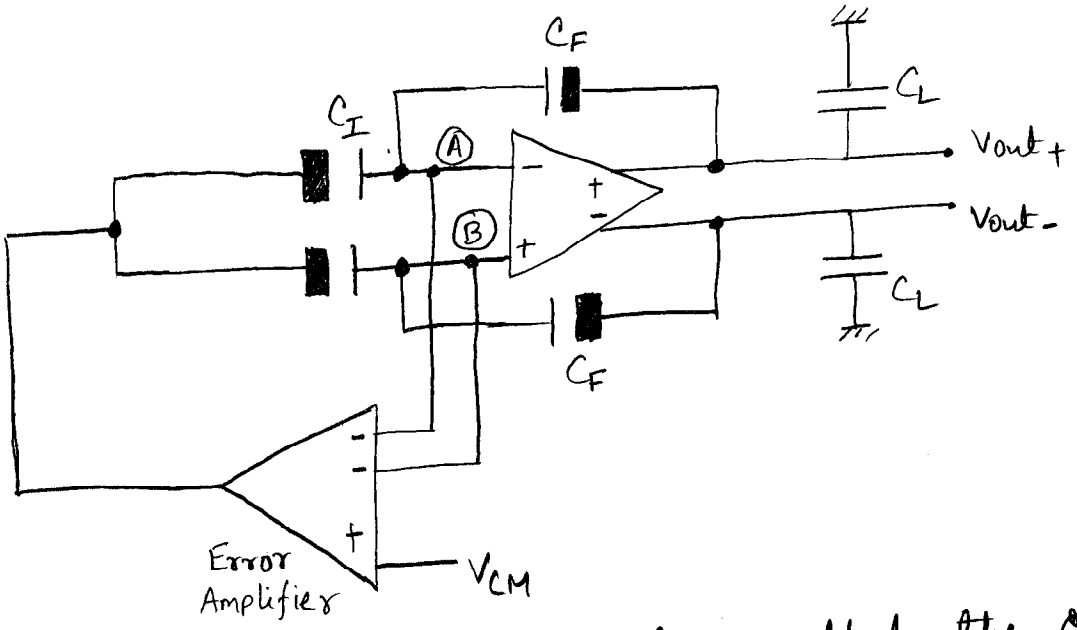
2. If things are not ideal, if there is capacitors mismatching and switching imperfection, and op-amp gain is Aol is not $\propto$, offset voltage would store on CI, when ϕ1 closes. And in this case input terminals of the error amplifier could be at different potential.

SOLUTION FOR 34.11

by SUGATO MUKHERJEE
e-mail : msugato@ieee.org

Q: When the ϕ_3 switches are closed in Fig. 34.34, is it possible for the inverting inputs of the error amplifier to be at different potentials? Again, neglect offsets.

Ans: With the ϕ_3 switches closed (ϕ_1, ϕ_2 switches open), fig 34.34 looks like



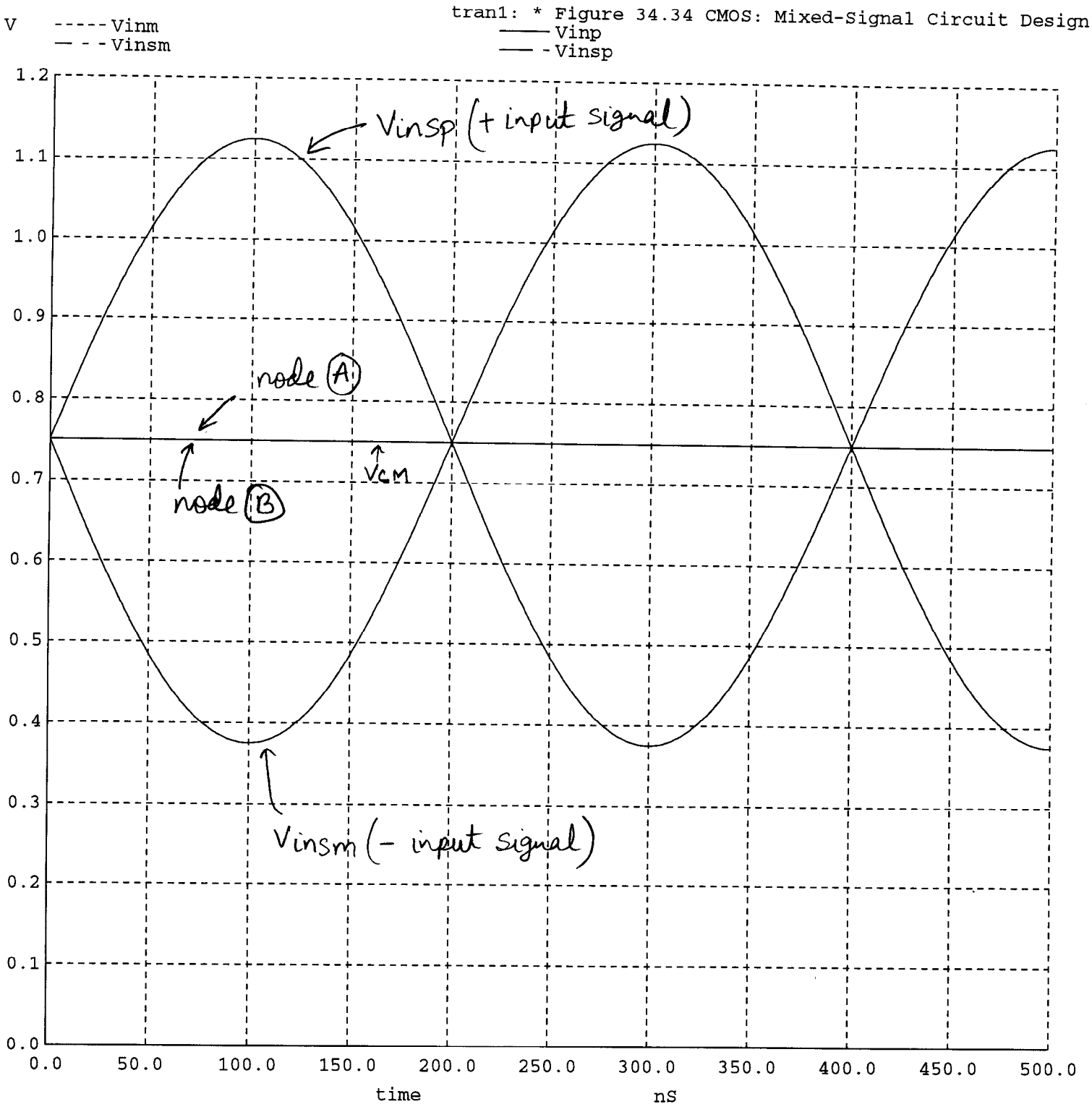
We see from the above figure that the op-amp is operating in a negative feedback configuration and hence the two inverting inputs of the error amplifier will always be at equal potential if we neglect op-amp offset.

If we have fully differential input signals and no error amplifier, the nodes (A) and (B) are held at V_{CM}.

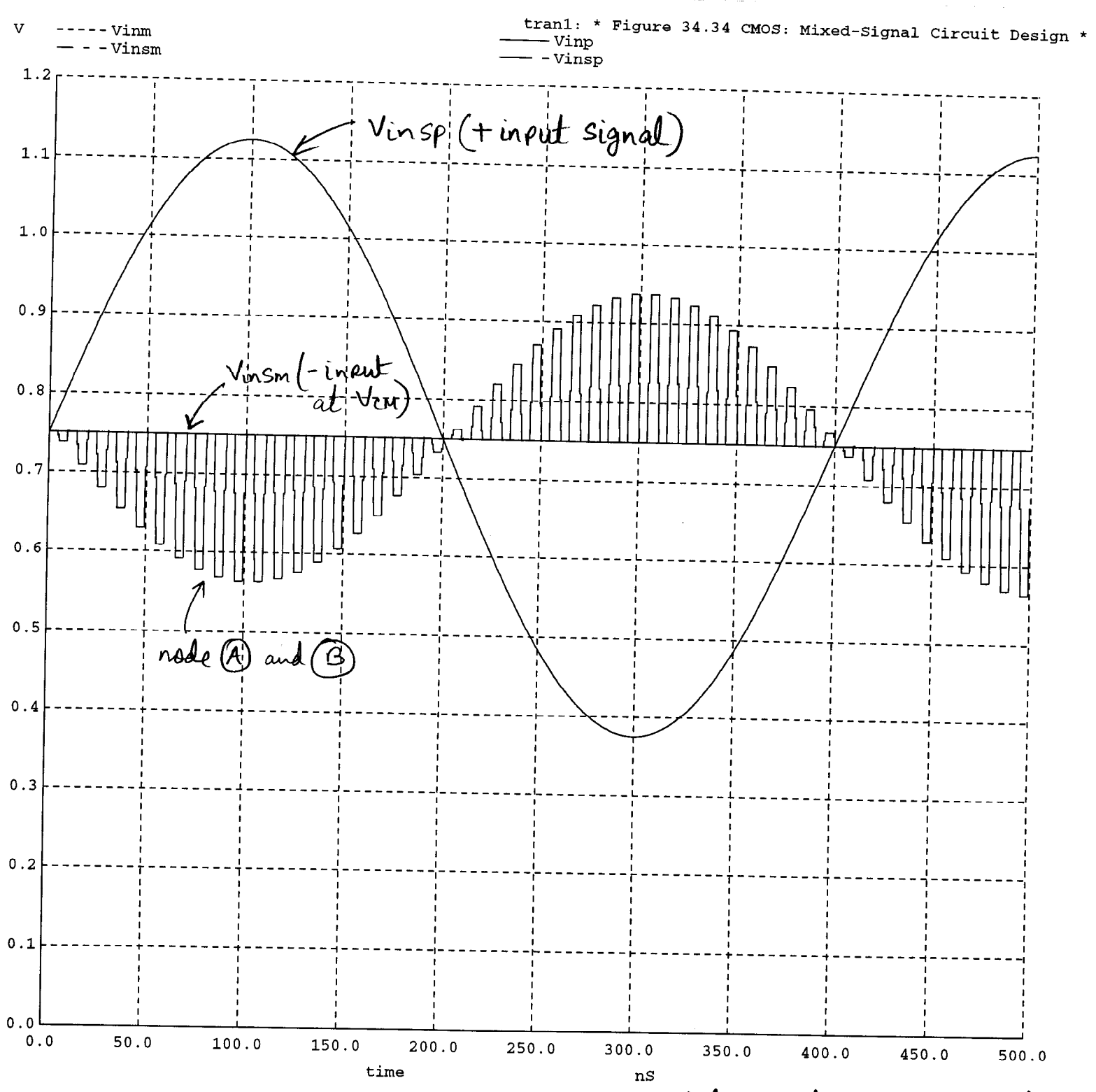
If we have single-ended input signal and an error amplifier with high gain, then also nodes (A) and (B) are at V_{CM}.

If we have single-ended input signal and do not connect the error amplifier, then nodes (A) and (B) vary with the input signal but are still always equal to each other.

The following SPICE plots illustrate the above statements



PLOT1: No error amplifier, fully differential inputs
Nodes (A) and (B) held at $V_{CM} = 0.75\,V$



PLOT 2: No error amplifier, single ended input, other input connected to V_{CM}

Nodes (A) and (B) vary with input signal but are always equal to each other.

Solution by:
Curtis Cahoon
curtis_cahoon@ieee.org

Problem 34.12

Question: Determine the output of the cyclic ADC of Fig. 34.38 if the input voltage is 0.41 Volts.

Answer: We follow the algorithm given in Ex. 34.9, in which we follow the cycle of comparing the input to the common-mode voltage, outputting a digital code, multiplying the voltage by 2, and feeding the resulting voltage back to the input to repeat the cycle. Below is a table showing this process, assuming that the converter is an 8-bit ADC. This process could be expanded or shortened depending on the resolution of the converter.

Cycle	Voltage	Vin>VCM?	Digtal Output	Subtract VCM?	New Voltage	Multiply by 2
0	0.41	no	0	no	0.41	0.82
1	0.82	yes	1	yes	0.07	0.14
2	0.14	no	0	no	0.14	0.28
3	0.28	no	0	no	0.28	0.56
4	0.56	no	0	no	0.56	1.12
5	1.12	yes	1	yes	0.37	0.74
6	0.74	no	0	no	0.74	1.48
7	1.48	yes	1	yes	0.73	1.46

Thus the 8-bit output word would be 0100 0101 (binary offset) or 69_{10}. This can be verified by finding the LSB (LSB=VDD/2^N) which is equal to 1.5V/256=0.005889V. We then multiply our digital output by 1 LSB to verify our result. Doing this we find that Vin=.404297. This is less than 1 LSB below our actual input, so we find that our result is correct.

Problem 34.13

Is kickback noise from the comparator a concern for the circuit of Fig. 34.39?

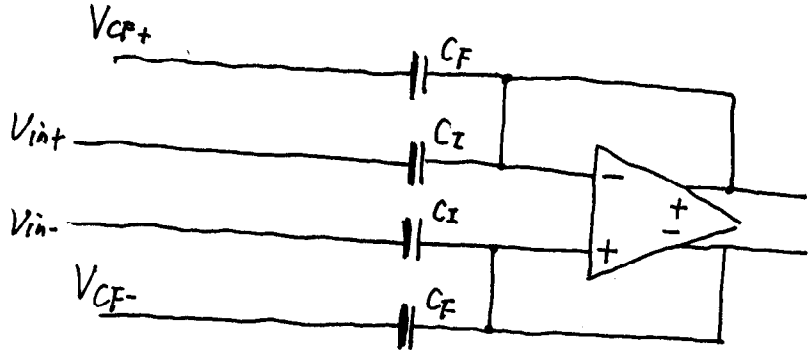
Yes, the comparator used in Fig. 34.39 has significant kickback noise resulting from the latch positive feedback. The decision circuit of a voltage comparator uses positive feedback to increase the gain of the decision element. The switch noise coming from the positive feedback stage will corrupt the input of the comparator and often limit its performance in the actual circuit.

In the sample-and-hold implementation of Fig. 34.39, if the kickback noise is not isolated, it will feed directly into the input voltage of the op-amp in S/H circuit through the input capacitor CI, and drastically affect the output of the sample-and-hold. In the Fig. 34.39, the switch $\phi 2$ is added in series with the comparator input to disconnect the comparator when comparator is clocked. Since the $\phi 2$ and $\phi 3$ are nonoverlapping, ideally, kickback noise will have very little effect to the input of the op-amp in the S/H.

Chapter 34. 14 - Yantao MA

Derive the transfer function from the circuit in Fig 34.39.

[solution]: ⇒ when ϕ_s close (ϕ_h open)

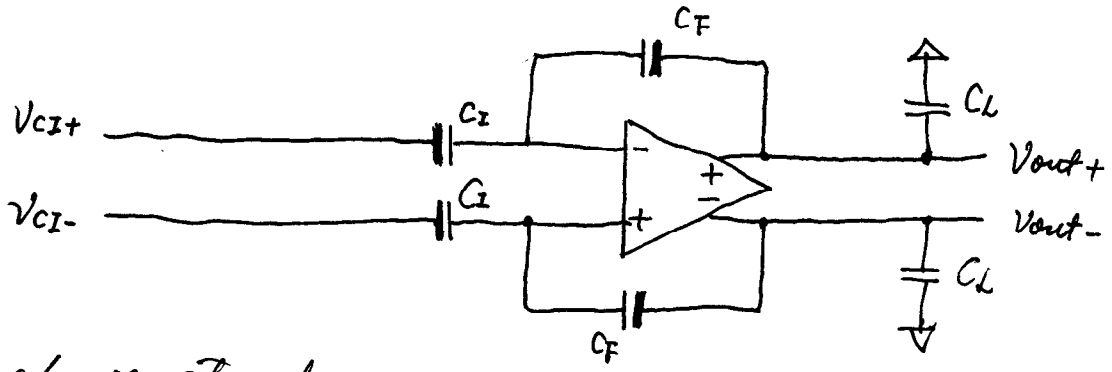


charge stored on C_I, C_F when ϕ_s close, ϕ_h open:

$$Q_I^{\phi_s} = C_I \cdot (V_{in+} - V_{cm} \pm V_{os})$$

$$Q_F^{\phi_s} = C_F \cdot (V_{CF+} - V_{cm} \pm V_{os})$$ (only consider + for now)

⇒ when ϕ_s open, ϕ_h close



charge stored on C_I, C_F now

$$Q_I^{\phi_h} = C_I \cdot (V_{CI+} - V_{cm} \pm V_{os})$$

$$Q_F^{\phi_h} = C_F \cdot (V_{out} - V_{cm} \pm V_{os})$$

since total amount of charge unchanged.

$$Q_I^{\phi_s} + Q_F^{\phi_s} \doteq Q_I^{\phi_h} + Q_F^{\phi_h}$$

(chapter 34.14 cont')

$$\Rightarrow \quad V_{out+} - V_{cm} \mp V_{os} =$$

$$\frac{C_I}{C_F}(V_{in+} - V_{cm} \mp V_{os}) + (V_{cf+} - V_{cm} \mp V_{os}) - \frac{C_I}{C_F}(V_{CI+} - V_{cm} \mp V_{os})$$

Considers fully-differential signal now:

$$\Rightarrow \quad V_{out} = V_{out+} - V_{out-}$$

$$= \boxed{\frac{C_I}{C_F}(V_{in} - V_{CI}) + V_{CF}}$$

where
$$\begin{cases} V_{in} = V_{in+} - V_{in-} \\ V_{CI} = V_{CI+} - V_{CI-} \\ V_{CF} = V_{cf+} - V_{CF-} \end{cases}$$

— yantao ma @ rocketmail.com

Ben Rivera
brivera@ieee.org

34.15) ***Repeat Ex. 34.16 for V_{in}=.41V. We begin by following the algorithm given in the example.***

Refer to Fig 34.50
Input value below $V_{cm}/2$ (=0.375V) our comparator outputs, *ab*, are 00 respectively.
Input value between $V_{cm}/2$ (=.375V) and $3V_{cm}/2$ (=1.125V) comparator outputs, *ab*, are 01 respectively.
Input value above $3V_{cm}/2$ (=1.125V) comparator outputs, *ab*, are 11 respectively.

From the book, Eq(34.59) or Eq(34.60), we can find the value for V_{out}. Note from the equations that we can never get a 00 followed by a 00, because we add Vcm, or a 11 followed by a 11, because we subtract Vcm, we can however, get repeated values for *ab* of 01.
For the digital outputs we follow Eq (34.67) to Eq (34.72).

V_{in}	Comparator Outputs, *ab*	V_{out}	Digital Output
.41 (n-1)	a=0 b=1	.07	b_7=1 c_7=0 b_8=0 MSB
.07 (n-2)	a=0 b=0	.89	b_6=1 c_6=0
.89 (n-3)	a=0 b=1	1.03	b_5=0 c_5=1
1.03 (n-4)	a=0 b=1	1.31	b_4=0 c_4=1
1.31 (n-5)	a=1 b=1	.37	b_3=0 c_3=0
.37 (b_2)	a=0 b=0	1.49	b_2=1 c_2=0
1.49 (b_1)	a=1 b=1	.73	b_1=0 c_1=0
.73 (b_0)	a=0 b=1	.71	b_0=1 c_0=0 LSB

Our digital output word is 0 1100 0101 (197dec)
We subtract V_{cm}-.5LSB from the output word to maintain accuracy 0 0111 1111 (127dec)

Digital Output
0 1100 0101 (binary offset)

V_{cm}-.5LSB
0 0111 1111 (binary offset)

```
  0 1100 0101
  1 1000 0000
+             1
1| 0 0100 0110
```

The 10^{th} bit is a don't care condition and we can throw it out so we are left with the digital output equal to 70(dec).
To verify, we multiply the digital output (70dec) by 1LSB, 70 * 1.5/256= .41V. This is the original input so the digital output is correct.

34.16 solution.

Jake Anderson, janderson@boisestate.edu

Determine the output of the Cyclic ADC if the input voltage is 0.41v. The comparators switch at 0.4(a 25mV offset) and 1.05 V (a 75mV offset).

The Digital output is calculated as shown below…

V_{in}	Comparator outputs, ab		V_{out}	Digital Out		
0.41	$a_{7=}$ 0	$b_{7=}$ 1	(0.41-0.375)*2 = 0.07	$Bit_{7=}$ 1	$c_{7=}$ 0	Bit_8=0
0.07	$a_{6=}$ 0	$b_{6=}$ 0	(0.07*2)+0.75 = 0.89	$Bit_{6=}$ 1	$c_{6=}$ 0	
0.89	$a_{5=}$ 0	$b_{5=}$ 1	(0.89-0.375)*2 = 1.03	$Bit_{5=}$ 0	$c_{5=}$ 1	
1.03	$a_{4=}$ 0	$b_{4=}$ 1	(1.03-0.375)*2 = 1.31	$Bit_{4=}$ 0	$c_{4=}$ 1	
1.31	$a_{3=}$ 1	$b_{3=}$ 1	(1.31-1.125)*2 = 0.37	$Bit_{3=}$ 0	$c_{3=}$ 0	
0.37	$a_{2=}$ 0	$b_{2=}$ 0	(0.37*2) + 0.75 =1.49	$Bit_{2=}$ 1	$c_{2=}$ 0	
1.49	$a_{1=}$ 1	$b_{1=}$ 1	(1.49-1.125)*2 = 0.73	$Bit_{1=}$ 0	$c_{1=}$ 0	
0.73	$a_{0=}$ 0	$b_{0=}$ 1	(0.73-0.375)*2 = 0.71	$Bit_{0=}$ 1	$c_{0=}$ 0	

The resulting Digital output from MSB to LSB is: 0 1100 0101

The Details for calculating the digital output are shown below, which are from equations 34.67-34.72. Equations 34.67-34.72 for an 8-bit ADC are:

$$Bit_0 = \overline{a}_0 b_0 = 1 \qquad c_0 = a_0 = 0$$

$$Bit_1 = \overline{a}_1 b_1 \oplus c_0 = 0 \qquad c_1 = \overline{a}_1 b_1 c_0 = 0$$

$$Bit_2 = \overline{a}_2 b_2 \oplus a_1 \oplus c_1 = 1 \qquad c_2 = \overline{a}_2 b_2 a_1 + c_1(\overline{a}_2 b_2 + a_1) = 0$$

$$Bit_3 = \overline{a}_3 b_3 \oplus a_2 \oplus c_2 = 0 \qquad c_3 = \overline{a}_3 b_3 a_2 + c_2(\overline{a}_3 b_3 + a_2) = 0$$

$$Bit_4 = \overline{a}_4 b_4 \oplus a_3 \oplus c_3 = 0 \qquad c_4 = \overline{a}_4 b_4 a_3 + c_3(\overline{a}_4 b_4 + a_3) = 1$$

$$Bit_5 = \overline{a}_5 b_5 \oplus a_4 \oplus c_4 = 0 \qquad c_5 = \overline{a}_5 b_5 a_4 + c_4(\overline{a}_5 b_5 + a_4) = 1$$

$$Bit_6 = \overline{a}_6 b_6 \oplus a_5 \oplus c_5 = 1 \qquad c_6 = \overline{a}_6 b_6 a_5 + c_5(\overline{a}_6 b_6 + a_5) = 0$$

$$Bit_7 = \overline{a}_7 b_7 \oplus a_6 \oplus c_6 = 1 \qquad c_7 = \overline{a}_7 b_7 a_6 + c_6(\overline{a}_7 b_7 + a_6) = 0$$

$$Bit_8 = a_7 \oplus c_7 = 0$$

Bit 8 is not used. So the output is $1100\ 0101_2$ (which is197_{10}).
If you subtract Vcm-½LSB (127_{10}) from the Digital output the result is:

$0100\ 0110_2$ (70_{10})

To check that the Digital output is correct, the Digital Output- Vcm multiplied by 1LSB[Volts] should give the same, or at least ½ LSB difference from the original input, which was 0.41 volts.

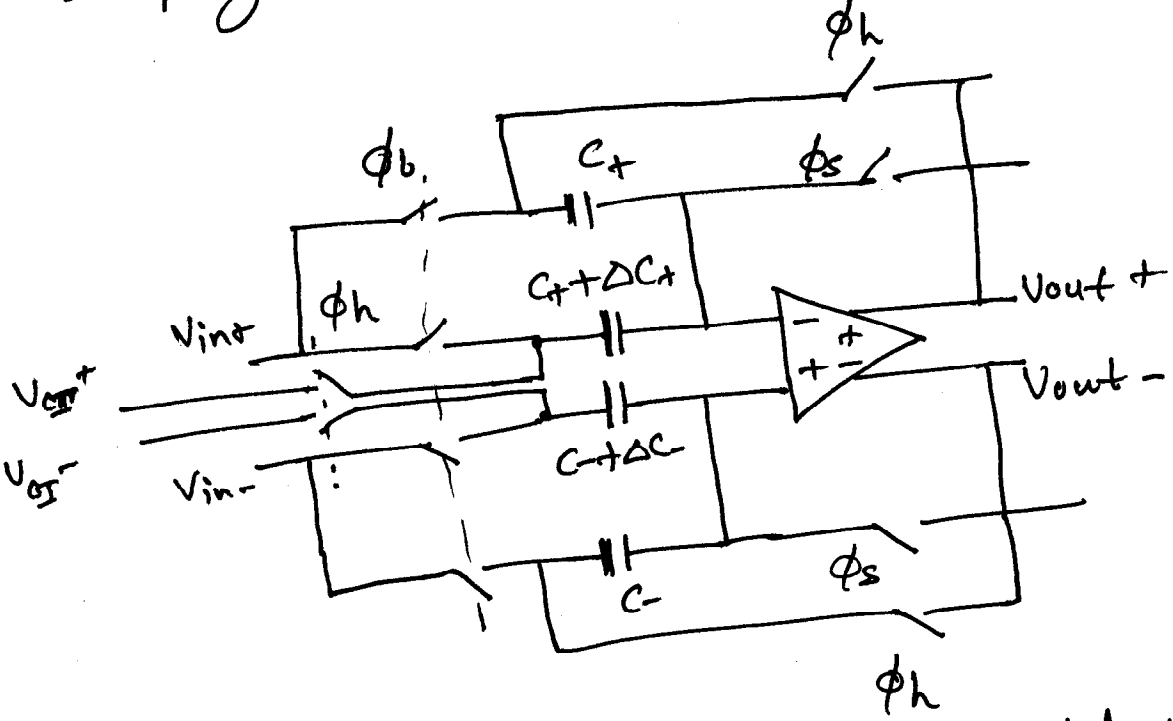
$V_{1LSB} = 1.5V/2^8 = 5.86mV$

70*5.86mV = 0.4102 Volts which is only 0.0002 greater than the input.

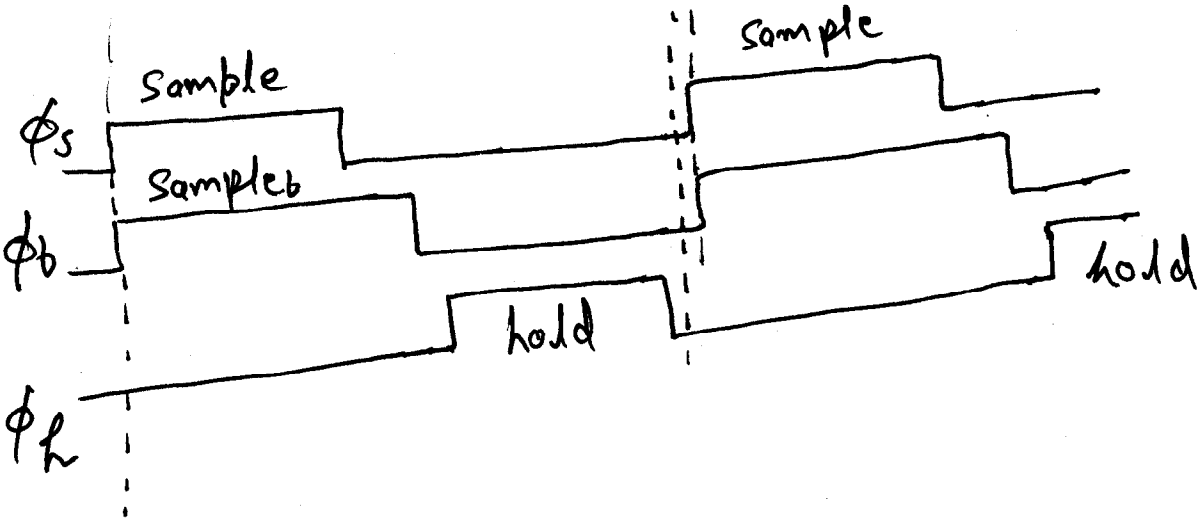
This results even with the comparator offsets not ideal. The ideal comparator for the same input voltage (0.41V) is analyzed in the previous problem.

Solution - 34.17

- Fig 34.54 would be as below if bottom plate sampling used.



and clock waveform for this ckt would be:

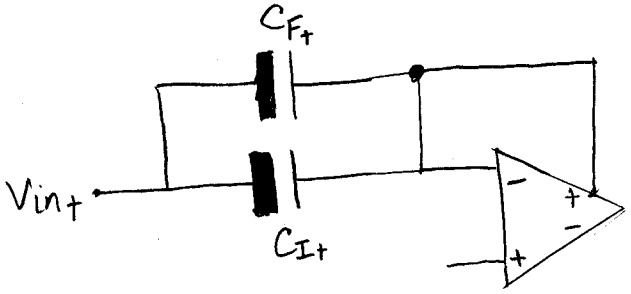


SOLUTION TO 34.18 by SUGATO MUKHERJEE

e-mail : msugato@ieee.org

Q: Show the derivation leading up to Eqn 34.83. Show using practical values for mismatch, how the squared mismatch terms are negligible.

Ans: Redrawing fig. 34.55 for the sampling phase (ϕ_s switches closed) we get the following figure. We draw all circuits only for the positive input knowing that the same equations hold true for the negative input when the input signals are fully differential.



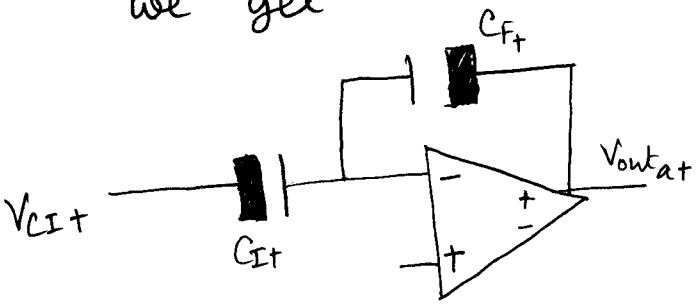
Sample phase

The total charge in the sample phase can be written as

$$Q_{sample} = (C_{I+} + C_{F+})(V_{in+} - V_{CM} \mp V_{OS})$$

where V_{OS} = offset voltage of op-amp

For the amplify phase, when ϕ_a switches are closed, we get



Amplify phase

The total charge

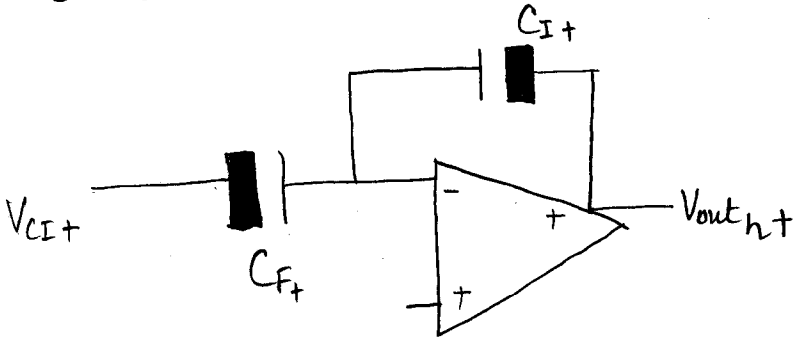
$$Q_{amp} = C_{I+}(V_{CI+} - V_{CM} \mp V_{OS}) + C_{f+}(V_{out_{a+}} - V_{CM} \mp V_{OS})$$

Since charge must be conserved, equating Q_{sample} and Q_{amp}, we get

$$C_{I+}(V_{in+} - V_{CI+}) + C_{f+}(V_{in+} - V_{out_{a+}}) = 0$$

or $$\boxed{V_{in+}(C_{f+} + C_{I+}) - C_{f+} V_{out_{a+}} = C_{I+} V_{CI+}} \quad \text{— eqn (a)}$$

In the hold phase when the ϕ_h switches are closed, the circuit becomes



Note that the C_{f+} and C_{I+} capacitors have interchanged their positions wrt the amplify phase.

Hold phase

Total charge in hold phase

$$Q_{hold} = C_{I+}(V_{outh+} - V_{CM} \mp V_{OS}) + C_{f+}(V_{CI+} - V_{CM} \mp V_{OS})$$

Equating Q_{hold} and Q_{amp} we get

$$C_{I+}.(V_{CI+} - V_{outh+}) + C_{f+}(V_{outa+} - V_{CI+}) = 0$$

or $$\boxed{C_{f+} V_{outa+} - C_{I+} V_{outh+} = V_{CI+}(C_{f+} - C_{I+})} \quad - \text{eqn (b)}$$

Adding eqns (a) and (b), we eliminate V_{outa+} and get

$$V_{in+}(C_{f+} + C_{I+}) - C_{f+}\cancel{V_{outa+}} + C_{f+}\cancel{V_{outa+}} - C_{I+} V_{outh+} = V_{CI+}(C_{f+} - \cancel{C_{I+}} + \cancel{C_{I+}})$$

or $$V_{outh+} = V_{in+}.\left(1 + \frac{C_{f+}}{C_{I+}}\right) - V_{CI+}.\frac{C_{f+}}{C_{I+}}$$

Putting $C_{I+} = C_+ + \Delta C_+$ and $C_{f+} = C_+$ where ΔC_+ indicates the mismatch between C_{f+} and C_{I+} we get

$$V_{outh+} = V_{in+}.\left(1 + \frac{C_+}{C_+ + \Delta C_+}\right) - V_{CI+} \cdot \frac{C_+}{C_+ + \Delta C_+}$$

$$\boxed{V_{outh+} = V_{in+}.\left(1 + \frac{1}{1 + \frac{\Delta C_+}{C_+}}\right) - V_{CI+}\left(\frac{1}{1 + \frac{\Delta C_+}{C_+}}\right)} \quad - \text{eqn (c)}$$

Now we know that $\frac{1}{1+x} = (1+x)^{-1} = 1 - x + x^2 - x^3 + \ldots$

(using binomial expansion)

$\therefore$ writing $\frac{1}{1+\frac{\Delta C_+}{C_+}} = \left(1+\frac{\Delta C_+}{C_+}\right)^{-1} = 1 - \left(\frac{\Delta C_+}{C_+}\right) + \left(\frac{\Delta C_+}{C_+}\right)^2 - \left(\frac{\Delta C_+}{C_+}\right)^3 + \ldots$

But ΔC_+ = mismatch between capacitors and is typically much less than C_+, the nominal capacitor value.

$\therefore \frac{\Delta C_+}{C_+} \ll 1$

Hence, the higher order terms $\left(\frac{\Delta C_+}{C_+}\right)^2$, $\left(\frac{\Delta C_+}{C_+}\right)^3$ etc are small and can be neglected.

Eg: if the typical capacitor mismatch in a process technology is 5%, then $\frac{\Delta C_+}{C_+} = 0.05$, $\left(\frac{\Delta C_+}{C_+}\right)^2 = 0.0025$, $\left(\frac{\Delta C_+}{C_+}\right)^3 = 0.000125$ etc.

Hence we can neglect the higher order terms and write

$$\frac{1}{1+\frac{\Delta C_+}{C_+}} \simeq 1 - \left(\frac{\Delta C_+}{C_+}\right)$$

Making the above substitution in eq^n (C), we get

$$V_{out_{h+}} = V_{in+}\left(1+1-\frac{\Delta C_+}{C_+}\right) - V_{CI+}\left(1-\frac{\Delta C_+}{C_+}\right)$$

$$V_{out_{h+}} = \left(2V_{in_+} - V_{CI+}\right) - \frac{\Delta C_+}{C_+}\left(V_{in+} - V_{CI+}\right)$$

which is Eq. 34.83.

Curtis Cahoon
curtis_cahoon@ieee.org

Problem 34.19

What happens to the error adjustment term in Equation 34.92 if the Capacitors in the Sample-and-Hold are perfectly matched?

Solution

First of all, here is Equation 34.92 from the book:

$$V_{avg+} - V_{avg-} = V_{outa+} - V_{outa-} - \underbrace{\frac{(V_{outa+} - V_{outh+}) - (V_{outa-} - V_{outh-})}{2}}_{\text{Error adjustment term}} \qquad (34.92)$$

It says in the paragraph above the equation in the book that if the capacitors are perfectly matched then $V_{outa+} = V_{outh+}$, and $V_{outa-} = V_{outh-}$, making the error adjustment term disappear, but let's verify with previous equations.

The V_{outa} and V_{outh} terms refer to V_{out} of the sample-and-hold when two of the three phases of the clock are high ($V_{outa} = V_{out}$ during amplify phase ϕ_a, and $V_{outh} = V_{out}$ during the hold phase ϕ_h). Let's see how V_{outa} and V_{outh} relate to each other. Also I will neglect V_{CI} terms, assuming $V_{CI+} = V_{CI-} = V_{cm}$,

(Equation 34.80) $\rightarrow$ $V_{outh+} = \cancel{V_{CI+}}^{\,0} + \frac{C_+}{C_+ + \Delta C_+} \cdot V_{outa+} - \cancel{\frac{C_+}{C_+ + \Delta C_+} \cdot V_{CI+}}^{\,0}$

Thus $V_{outh+} = \frac{C_+}{C_+ + \Delta C_+} V_{outa+}$ (the same equation applies to V_{outh-} and V_{outa-})

If the capacitors are perfectly matched, $\Delta C_+ = \Delta C_- = 0$, and $V_{outh+} = V_{outa+}$, thus making our error adjustment term equal to zero.

P. K. Irkar HW 1 prob: 34.20

Q. 34.20

Repeat Ex. 34.18 if all capacitors are 1 pf (the ideal situation) and verify that the error out of the stage is zero.

Ans:

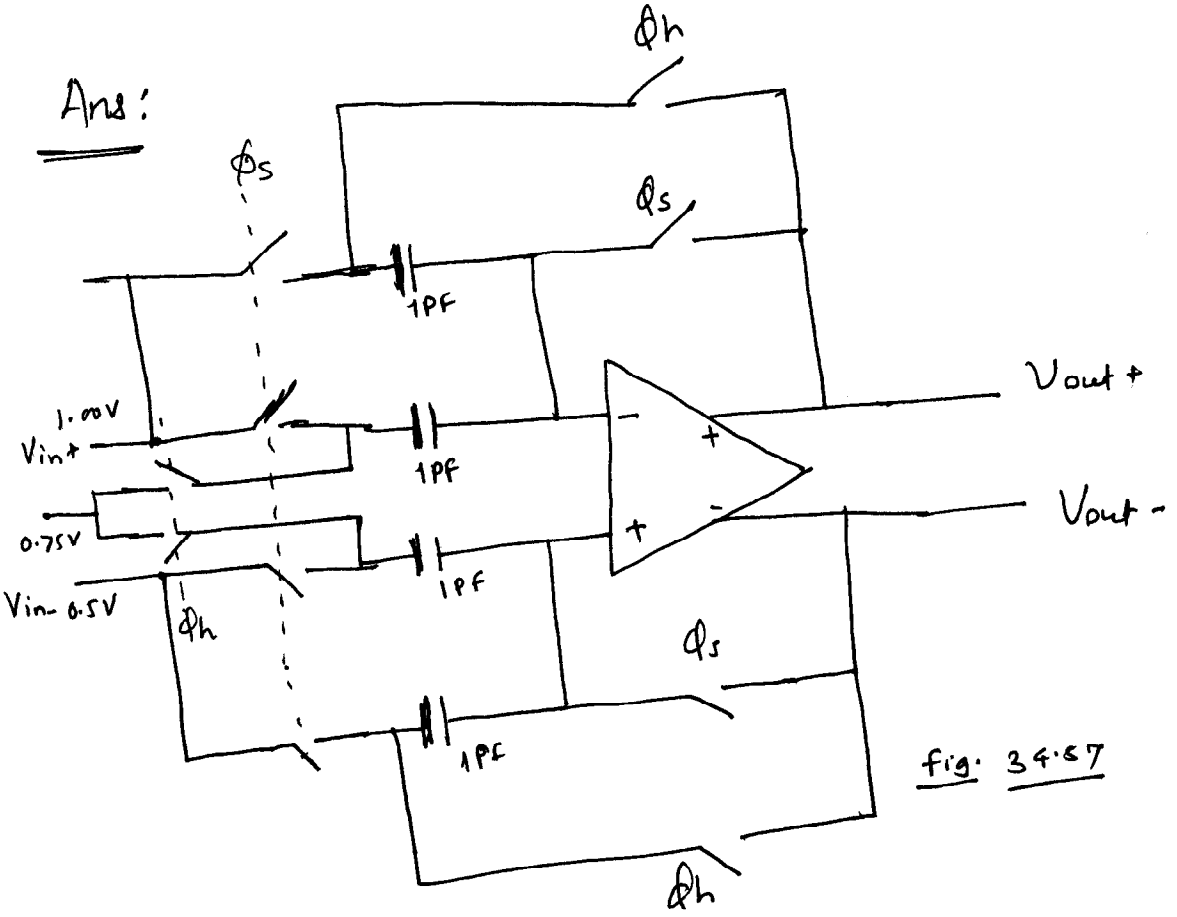


fig. 34.57

The capacitors are equal and input voltage $V_{in}^{+} - V_{in}^{-} \Rightarrow 0.5V$

Ideally the output is then 1V.

$V_{out}^{+} \simeq 1.25V$

$V_{out}^{-} = 0.25V$

$V_{out}^{+} - V_{out}^{-} \Rightarrow 1V$

Then error $\simeq$ Ideal output $-$ $(V_{out}^{+} - V_{out}^{-})$

$= 1V - 1V$

$= 0$

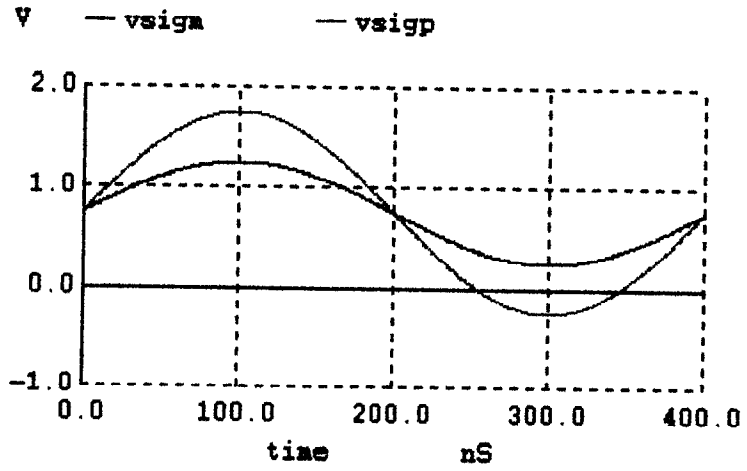
Simulation also shows the same as I've described above.

SPICE DECK : fig 34.57

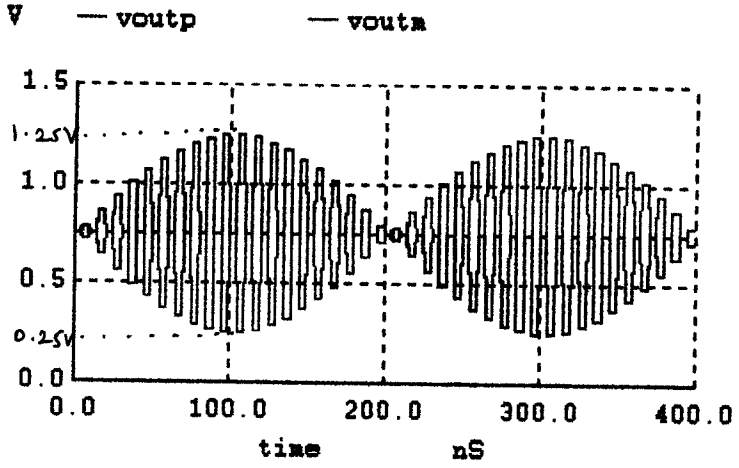
Sample and hold circuit

```
.control
destroy all
run
.endc

*Op-amp using VCVS
E1 Voutp Vcom Vplus Vminus 100MEG
E2 Vcom Voutm Vplus Vminus 100MEG
*Sample and hold capacitors
Cim Vminus Vcomm 1p
Cfm Vminus Vcenm 1p
Cip Vplus Vcomp 1p
Cfp Vplus Vcenp 1p
*switches
S1 Vcenm Vsigp  phis Vswit switmod
S2 Vcomm Vsigp  phis Vswit switmod
S3 Vcomm Vcom   phih Vswit switmod
S4 Vcomp Vcom   phih Vswit switmod
S5 Vcomp Vsigm  phis Vswit switmod
S6 Vcenp Vsigm  phis Vswit switmod
S7 Voutp Vcenm  phih Vswit switmod
S8 Voutp Vminus phis Vswit switmod
S9 Voutm Vplus  phis Vswit switmod
S10 Voutm Vcenp phih Vswit switmod
*supply voltage
VDD VDD 0 DC 1.5
*reference voltages
Vswit Vswit 0 DC 0.75
Vcom Vcom 0 DC 0.75
*Input Signals
Vsigp   Vsigp   0 DC 0 sin 0.75 1.0 2.5MEG
Vsigm   Vsigm   0 DC 0 sin 0.75 0.5 2.5MEG
*Ideal signal
Videal  Videal  0 DC 0 sin  0 1.0 2.5MEG
*Clock Signals
vphis  phis  0 DC 0  Pulse 0 1.5   0    200p  200p  4n 10n
Vphih  phih  0 DC 0  Pulse 0 1.5   5n   200p  200p  4n 10n
Rs phis 0 1MEG
Rh phih 0 1MEG

.tran 2n 400n 0 2n UIC
.model switmod SW RON=1
.end
```

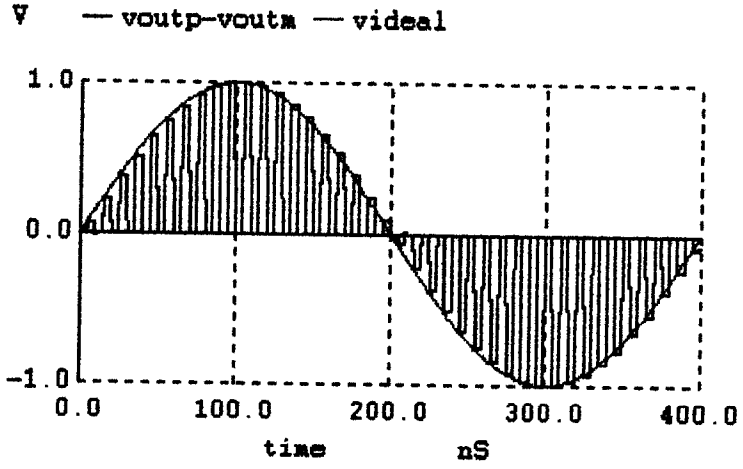
Input Signals



Output signals



Ideal signal and Actual (Voutp-Voutm) Signal



Here the Ideal o/p and Actual (Voutp - Voutm) are same means that the error = Ideal - (Voutp - Voutm) = 0.

EE515 -CMOS Mixed Signal IC Design -- Yantao Ma
-- yantaoma@rocketmail.com

Chapter 34.21. Sketch a circuit to provide the inputs for the four-phase, non-overlapping clock generator shown in Figure. 34.81

[Solution]: Based on state diagram / truth table as following, one of the possible solution circuits can be designed as indicated: (attached simulation results). Note: this circuit can be triggered on both clock rising and falling edges in real design to improve speed. For demo purpose, we only use rising-edge triggering scheme.

Clock Pulse	Q_1	Q_0
Initially	0	0
1	0	1
2	1	0
3	1	1
4 (recycles)	0	0

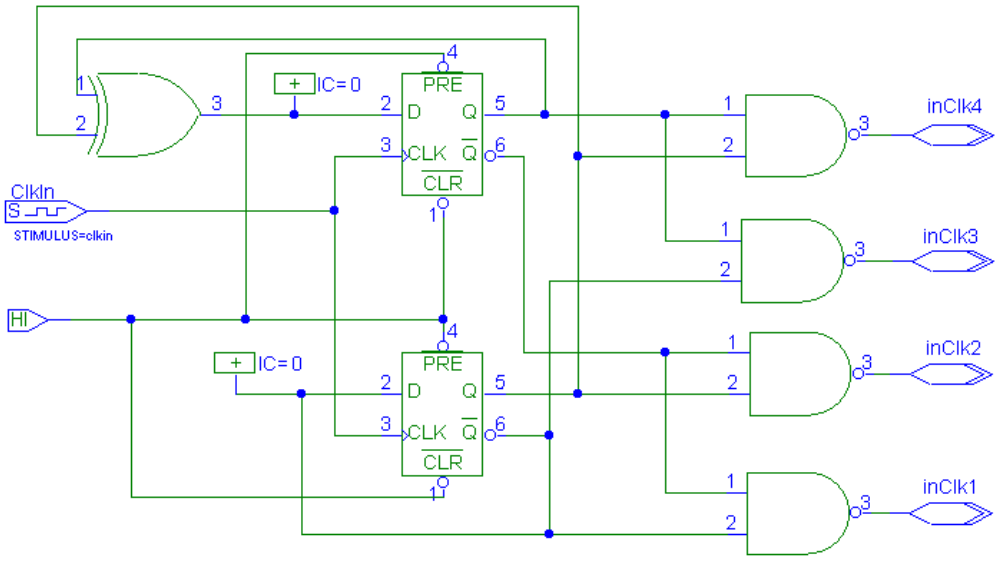
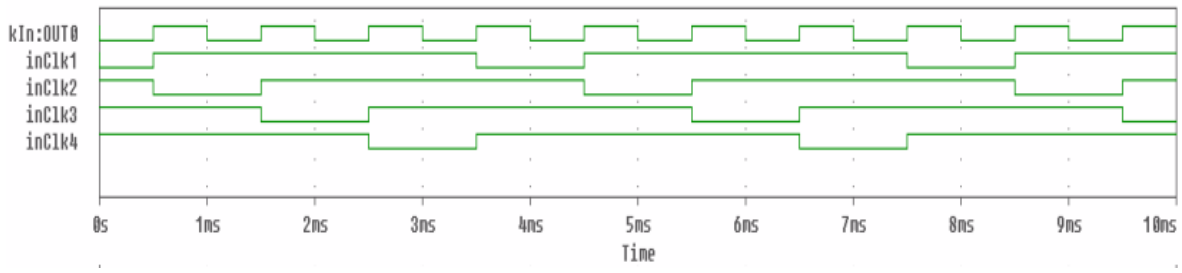


Figure 1: Four-Phase overlapping Clock Generator Circuit Design

Circuit Simulation for Four-Phase, non-overlapping clock Generator Inputs:
(First line: system input clock)



EE515 -CMOS Mixed Signal IC Design -- Yantao Ma
-- yantaoma@rocketmail.com

Chapter 34.22. What is the main advantage of using dynamic CMFB over other CMFB circuits? What is the main disadvantage?

[Answer]: Generally speaking, CMFB circuit is required to precisely balance the outputs of differential amplifier. In the meantime, issues associated with CMFB would be problems if a. CMFB doesn't affect each output the same→ causing a difference mode signal; b. circuit becomes complex, CMFB circuit CMR would impose some limitation on initial Op-Amp design if not careful.

Main advantage of dynamic CMFB: It allows a lower CMFB loop gain thus making it easier to stabilize, without degrading common-mode voltage accuracy theoretically. It does not employ an amplifier. Unlike other CMFB circuits, dynamic CMFB makes it feasible op-amp's outputs not necessarily to settle down to the final accuracy of ADC by the falling edge of all three clock-phases. More exactly, during sampling phase settling time is meaningless since Op-Amp operates in open loop; inputs of Op-Amp are shorted to common-mode voltage, instead.

Main disadvantage of dynamic CMFB:

Dynamic CMFB would require to be compensated depending on the design parameters. It practically limits the gain of first stage otherwise would saturate outputs, causing offset storage mechanism fail.

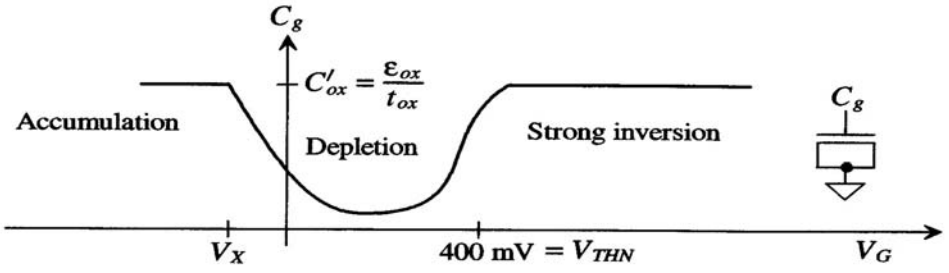
Problem 34.23

Can MOSFETs be used to implement the on-chip decoupling capacitors in Fig 34.77?

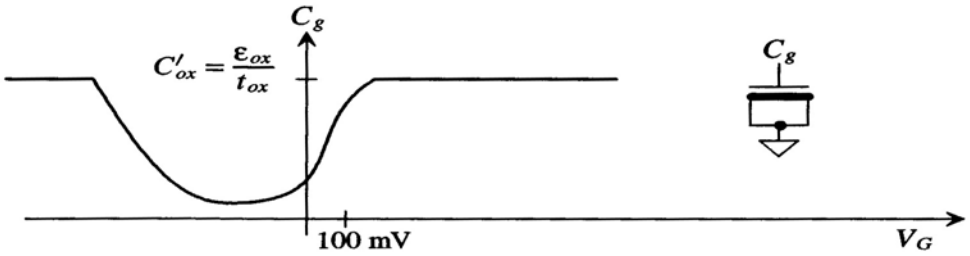
MOSEFTs can be used as the on-chip decoupling capacitors for the power and ground supplies. MOSFETs usually make a very good capacitor when $V_{GS} > V_{THN}$ + a few hundred mV. In Fig 34.77, the gate of decoupling MOSEFT capacitor is connected to the VDD and source/drain connected to the ground. So, V_{GS} (=VDD) is sufficient large to have MOSFET working in the strong inversion region (good cap area).

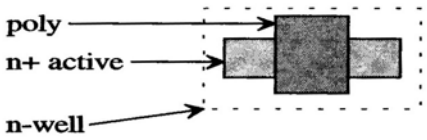
The figure below shows the CV curve for an NMOS transistor with source, drain and body connected to ground. The capacitance between the gate and source/drain is

$$C_{tot} = C_{ox} \cdot W \cdot L$$

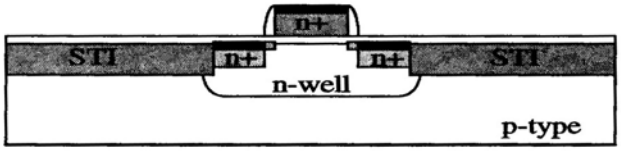


The following figure gives the CV curve for an NMOS with an n-well placed below. This MOSFET capacitor has a very low $V_{THN.}$ To behave as a capacitor, MOSFET required operating in the strong inversion region. If V_{GS} is close to the V_{THN}, then the capacitance can become nonlinear and distortion can happen in the circuit.





(a) Layout view



(b) Cross-sectional view

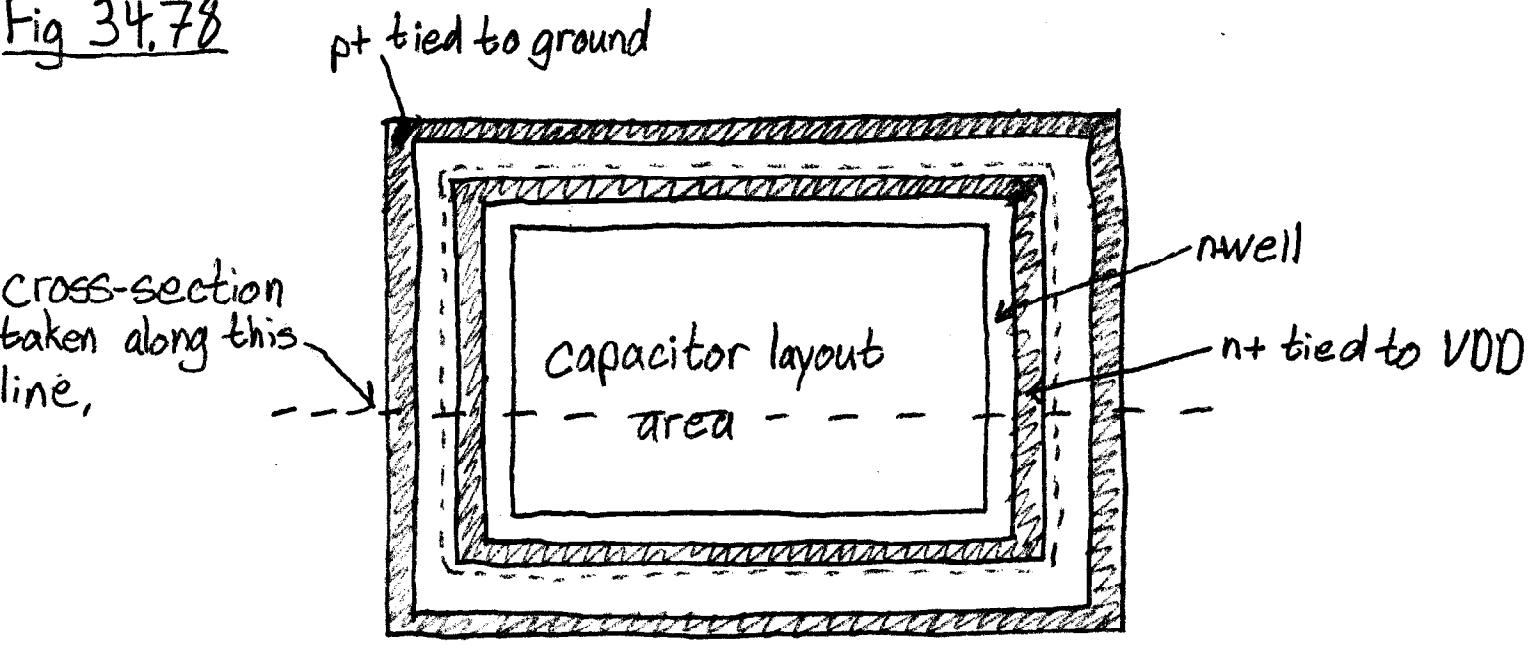
The layout and cross-section of the n-well NMOS capacitor shows above. This type of capacitor is widely used as decoupling capacitor when two layers of poly (like a Flash memory process) are not available in the process.

Curtis Cahoon
curtis_cahoon@ieee.org

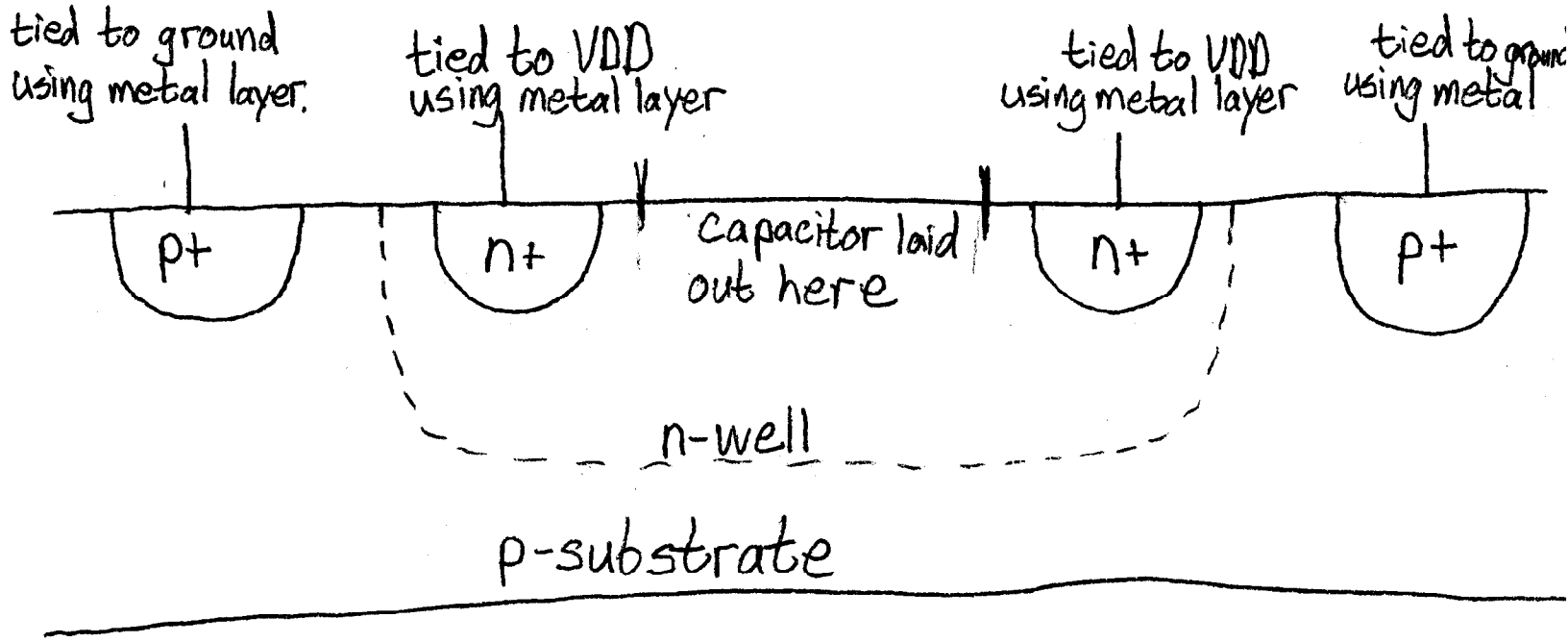
Problem 34.24

Sketch the cross-sectional view of layout in Fig. 34.78,

Fig 34.78



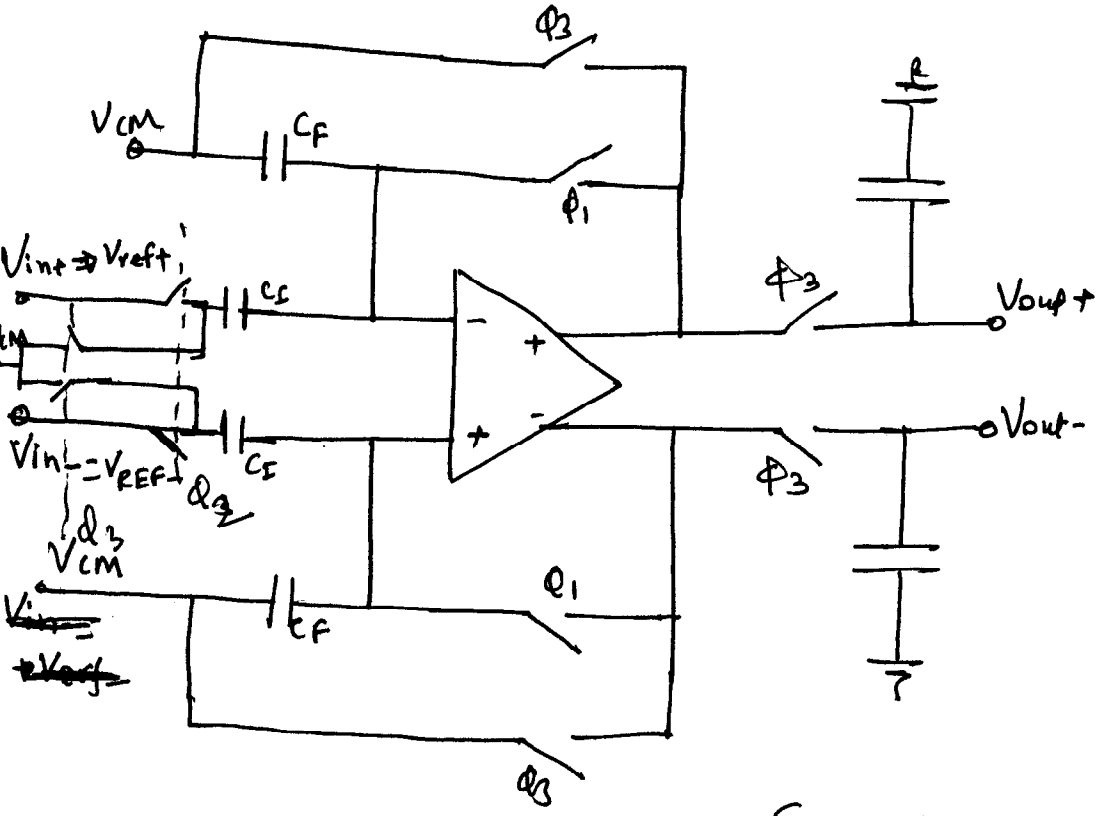
This cross-sectional area will be drawn assuming no metal has been connected on the chip, though I will indicate where metal will be put.



P.K. IRKAR pkirkar@rediffmail.com.

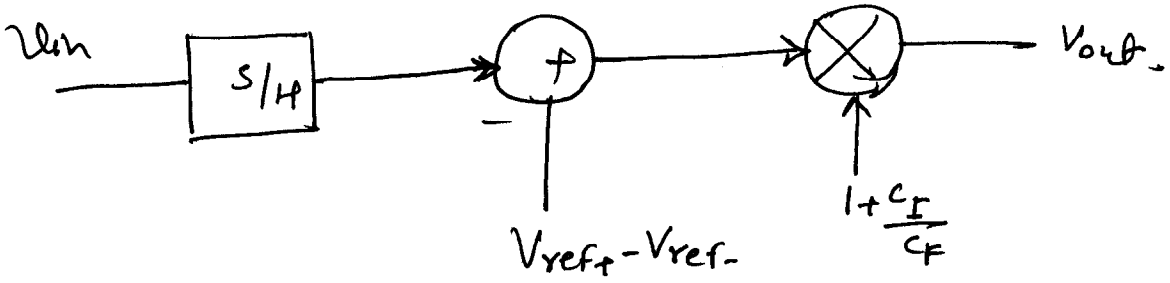
Q.34.25

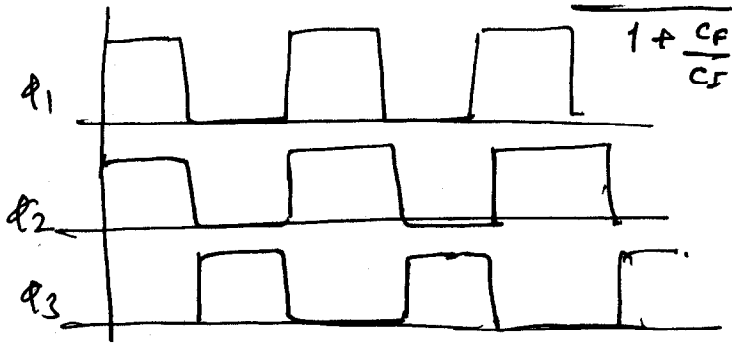
Referring to fig 34.42 with modification to get gain is equal to ½.



$$\frac{C_I}{C_F} = \frac{1}{2}$$

The Block dia. becomes.



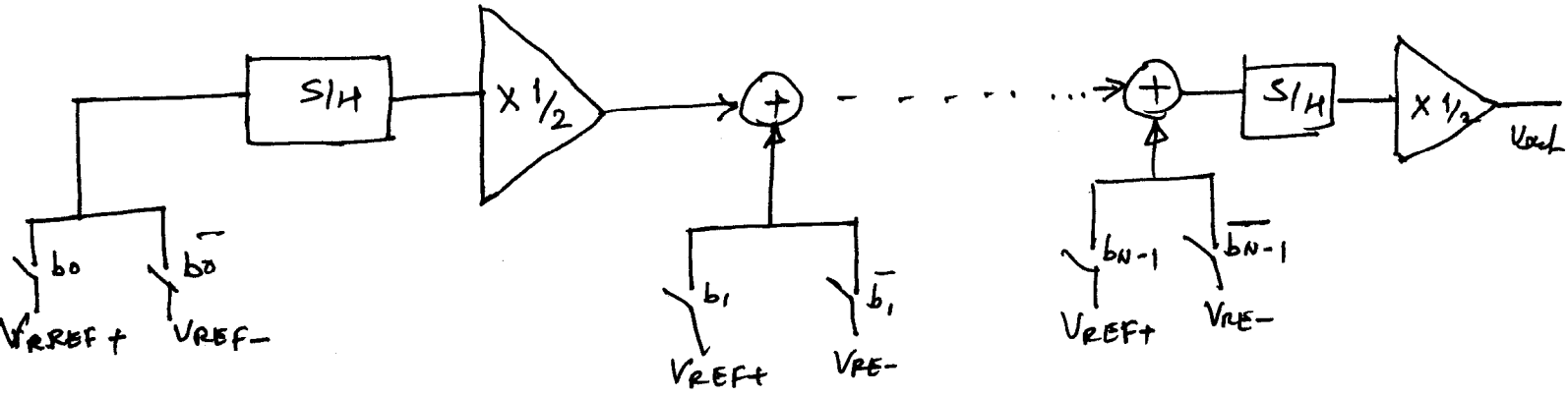


Clock signals.

By setting the $C_I/C_F = 1/2$; we can achieve the gain is equal to $1/2$ which is required DAC pipeline implementation.

Since $C_F = 2C_I$; in ϕ_1/ϕ_2 the vtg across $C_I = V_{in} - V_{cm}$ and the ϕ_3 the output becomes $1/2(V_{in} - V_{cm})$.

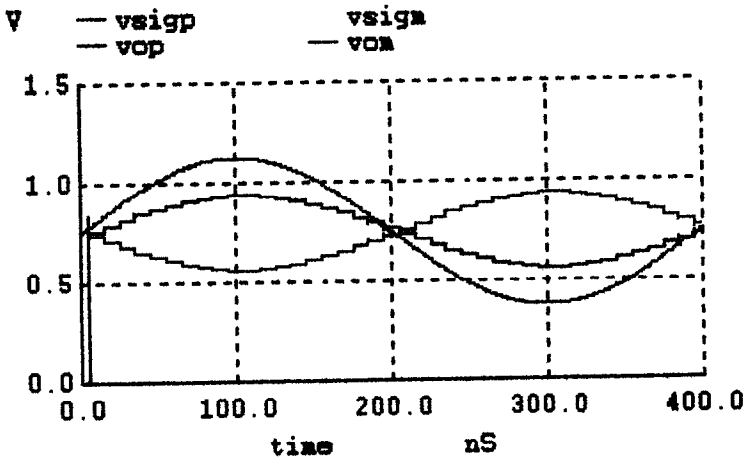
The DAC implementation fig. 34.82



The net list and simulated Results are on the following pages.

Amplifier with gain 1/2

```
.control
destroy all
run
plot vop vom vsigp vsigm
.endc

.options scale=1u ABSTOL=10u VNTOL=10m RELTOL=.01

*Op-amp using VCVS
E1 Voutp Vcom Vplus Vminus 100MEG
E2 Vcom Voutm Vplus Vminus 100MEG
*Sample and hold capacitors
Cim Vminus Vcomm 1p
Cfm Vminus Vcenm 2p
Cip Vplus Vcomp 1p
Cfp Vplus Vcenp 2p
*Switches
S1 Vcenm  Vcom   phi2 Vswit switmod
S2 Vcomm  Vsigp  phi2 Vswit switmod
S3 Vcomm  Vcom   phi3 Vswit switmod
S4 Vcomp  Vcom   phi3 Vswit switmod
S5 Vcomp  Vsigm  phi2 Vswit switmod
S6 Vcenp  Vcom   phi2 Vswit switmod
S7 Voutp  Vcenm  phi3 Vswit switmod
S8 Voutp  Vmimus phi1 Vswit switmod
S9 Voutm  Vplus  phi1 Vswit switmod
S10 Voutm Vcenp  phi3 Vswit switmod
S11 Voutp Vop    phi3 Vswit switmod
S12 Voutm Vom    phi3 Vswit switmod
*Load capacitor
Cop Vop 0 10p
Com Vom 0 10p

*Supply voltage
VDD VDD 0 DC 1.5
*Reference voltages
Vswit Vswit 0 DC 0.75
Vcom  Vcom  0 DC 0.75
*Input Signals
Vsigp  Vsigp  0 DC 0 Sin 0.75 0.375 2.5MEG
Vsigm  Vsigm  0 DC 0 Sin 0.75 -0.375 2.5MEG
*Clock Signals
Vphi1  phi1  0 DC 0  Pulse 0 1.5  0   200p 200p 4n 10n
Vphi2  phi2  0 DC 0  Pulse 0 1.5  0   200p 200p 4n 10n
Vphi3  phi3  0 DC 0  Pulse 0 1.5  5n  200p 200p 4n 10n
R1 phi1 0 1MEG
R2 phi2 0 1MEG
R3 phi3 0 1MEG

.tran 2n 400n 0 2n UIC
.model switmod SW RON=1
.end
-
```



Vsigp =1.25
Vsigm = 0.25

Vcom =0.75

The outputs are as below:

Vop =0.95
Vom =0.5

Hence gain is 1