EE515: CMOS Mixed-Signal IC Design
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Problem 32.1
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Problem 32.1:

Show the details and assumptions leading to Eq. 32.1:

Eq. 32.1: $H(z) = (z^{-1}) / ( 1 - (z^{-1}) )$

Note: Eq. 32.1 is the transfer function of the Discrete Analog Integrator (DAI) in example 32.1.

Answer:

The derivation of the transfer function for a DAI, when the phee_1 switches are closed, is shown in Eq. 31.130 on page 137.

Eq. 31.130: $Vout(z) = CI / CF * ( V1(z) * (z^{-1}) - V2(z) * (z^{-1/2}) ) / ( 1 - (z^{-1}) )$

In Fig. 32.3, all voltages are relevant to ground. In Eq. 31.130, Vout, V1, and V2 are all relevant to VCM. To use Eq 31.130 on Fig 32.3 all the voltages have to be converted from relative to ground to relative to VCM by subtracting VCM from each one in Fig 32.3. So if V2=VCM in Fig 32.3, subtracting VCM from it to convert; it would be used as 0V in Eq 31.130.

If the values C1=1pF, CF=1pF, and V2(z)=0 are plugged into Eq. 31.130 the result is:

$Vout(z) = Vin(z) * ( z^{-1}) / ( 1 - (z^{-1}) )$

Since $H(z) = Vout(z) / Vin(z)$, It can be seen from the above equation that:

$H(z) = (z^{-1}) / ( 1 - (z^{-1}) )$

So the assumptions leading up to Eq. 32.1 are that the phee_1 switches are closed (instead of the phee_2 switches) and that Vout, V1, and V2 are all relevant to VCM in Eq. 31.130.

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**32.2** Would it be possible to operate the DAI of Fig. 32.3 without a 0.75 V supply? Give an example. Show simulations with the output initially at 0.75 V and the same input used to generate Fig. 32.4. Are the DAI outputs the same?

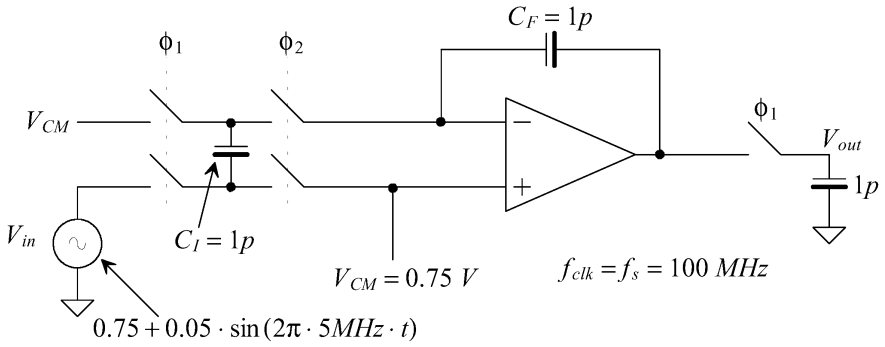



**Figure 32.3** Circuit used in Ex. 32.1.

It is possible to operate the DAI shown in Fig. 32.3 without $V_{CM}$ set to the midpoint between Vcc and Vss. For example, the $V_{CM}$ node may be connected to Vss, with the condition that the input must now swing about Vss (the new $V_{CM}$) in order for an accurate average to be generated. In this case, the op-amp attempts to force the negative terminal to stay at Vss. Fig. 1 shows that the integration remains the same, with the change in the $V_{CM}$ node causing an offset.

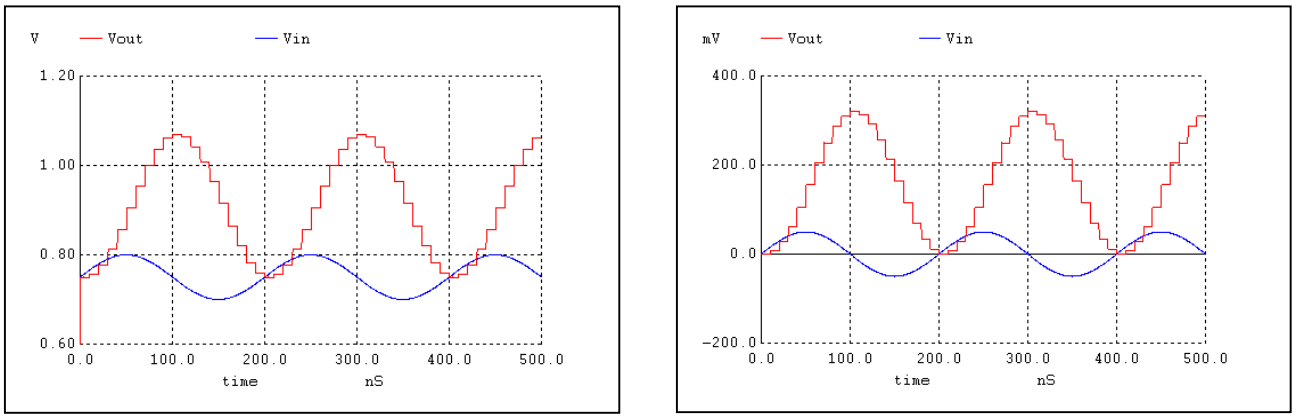



**Figure 1** ADI waveforms with VCM set to 0.75 V (left) and 0 V (right).

To force the op-amp output to 0.75 V, the following line was added before the transient analysis control line

.ic v(Voutop)=0.75

It is important to understand that the initial condition of the output node will create an offset in the output waveform. The reason for this is that, regardless of the initial output condition, the input signal will control the direction of the integration. Fig. 2 shows the output waveform with the initial condition set to zero (the default) and with the output initially set at 0.75 V. Notice that the output has the same shape, but is offset by 0.75 V. Of course, if this circuit were realized using an op-amp with limitations on the output swing, the output would hit the supply rail. The initial output condition must be considered in practical implementations of the ADI.

If the integrator were used in a feedback loop, such as a NS modulator, the initial conditions become irrelevant after a few clock cycles, because the integrator output will drift toward the center of the supply rails.

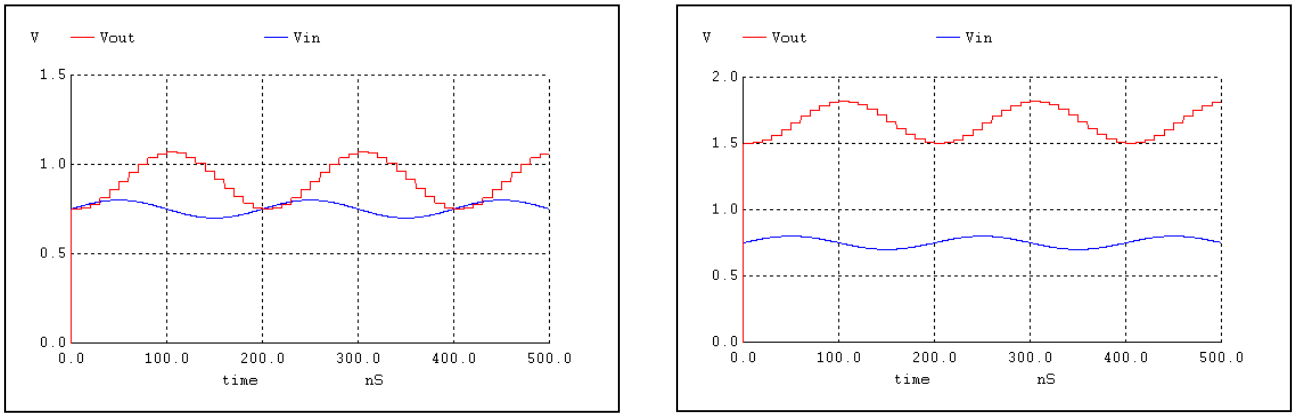


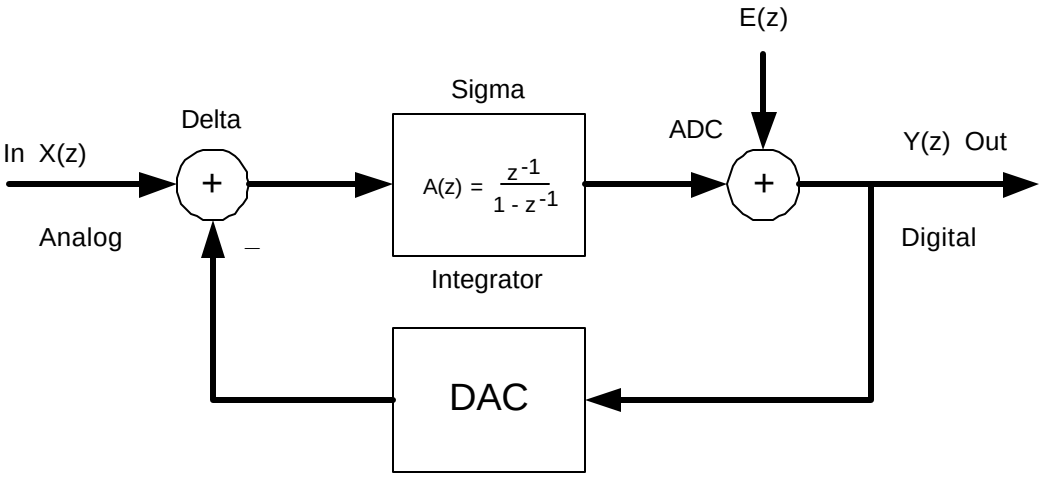

**Figure 2** ADI waveforms with op-amp output initial condition set at 0 V (left) and 0.75 V (right).

# EE515: CMOS Mixed-Signal IC Design

Problem 32.3
Jim Slupe

32.3 Show the derivation of Eq. (32.4) from the block diagram shown in Fig. 32.6.

Answer: Shown below is a re-creation of figure 32.6




Equation 31.138 describes the behavior of this noise shaping modulator and is given here:

$$Y(z)=\frac{A(z)}{1+A(z)*B(z)}*X(z)+\frac{1}{1+A(z)*B(z)}*E(z)$$

In the figure above, B(z) = 1 and A(z) a simple integrator with a delay of $z^{-1}$. Inserting these values into the equation given above yields:

$$Y(z)=\frac{\frac{z^{-1}}{1-z^{-1}}}{1+\frac{z^{-1}}{1-z^{-1}}}*X(z)+\frac{1}{1+\frac{z^{-1}}{1-z^{-1}}}*E(z)$$

This, in turn, simplifies to:

$$Y(z)=\frac{z^{-1}}{1-z^{-1}+z^{-1}}*X(z)+\frac{1-z^{-1}}{1-z^{-1}+z^{-1}}*E(z)$$

Which then becomes equation 32.4:

$$Y(z) = z^{-1} * X(z) + (1 - z^{-1}) * E(z)$$

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32.4 In the basic NS modulator shown in Fig. 32.7 what component serves as the ADC? What component serves as the DAC?

The clocked comparator serves as both the ADC and DAC. This is possible, because the NS modulator implementation uses a 1-bit ADC and a 1-bit DAC as seen in figure 32.6.

In figure 32.7, the comparator compares the output of the integrator to Vcm. The output of the comparator is then either a logic 0 or a logic 1, the ADC stage. This logic 0 is simply 0V, and the logic 1 is VDD. Therefore, no additional data converting is necessary, and the output of the comparator is also used as the output of a 1-bit DAC.

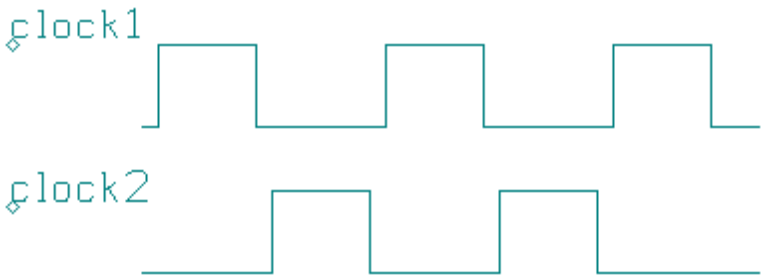
Gexin

Problem for 32.5:
Show, using timing diagrams, how Eq.(32.5) is correct.

Solution for 32.5:

The timing diagram is shown below:

'




In the following discussion, the quantization noise is not taken into consideration, i.e. Here we assume the ADC input is equal to the ADC output.
When $f_1$ is on at $(n-1)\cdot T_s$, the charge on the $C_{in}$ is:
$Q_{in1} = C_{in}\cdot(V_{CM} - V_{in}[(n-1)T_s])$
Since time between $f_1$ going low and $f_2$ going high is small, that is,
Right after $f_1$ is off, $f_2$ is on immediately, during the $f_2$ is on, $C_{in}$ will be charged to:
$Q_{in2} = C_{in}\cdot(V_{CM} - V_{out}[(n-1)T_s])$
The **charge change on the** $C_{in}$ is:
$$\Delta Q_{in} = Q_{in2} - Q_{in1} = C_{in}(V_{in}[(n-1)\cdot T_s] - V_{out}[(n-1)\cdot T_s]) \qquad (1)$$

During the $f_2$ is on, the charge change on $C_f$ is:
$$\Delta Q_f = C_f\cdot(V_{ADCin}[(n-1)\cdot T_s] - V_{ADCin}[(n-2)\cdot T_s]) \qquad (2)$$
The charge change on $C_{in}$ should be equal to the charge change on the $C_f$, that is:
$$\Delta Q_f = \Delta Q_{in} \qquad (3)$$
Since the comparator is clocked by $f_1$, the ADC output is $T_s$ delay than ADC input,
Which means:
$V_{ADCin}[(n-1)\cdot T_s] = V_{ADCout}[n\cdot T_s]$
$V_{ADCin}[(n-2)\cdot T_s] = V_{ADCout}[(n-1)\cdot T_s]$
Thus (2) becomes:
$\Delta Q_f = C_f\cdot(V_{ADCout}(n\cdot T_s) - V_{ADCout}[(n-1)\cdot T_s])$

Thus from (3), we get:

$$C_f \cdot \left(V_{ADCout}\left(n \cdot T_s\right) - V_{ADCout}\left[\left(n-1\right) \cdot T_s\right]\right) = C_{in} \cdot \left(V_{in}\left[\left(n-1\right) \cdot T_s\right] - V_{out}\left[\left(n-1\right) \cdot T_s\right]\right)$$

To represent this equation in the Z domain (Here $C_f = C_{in}$):

Desired ADC output = $\frac{z^{-1}}{1-z^{-1}} \cdot \left(V_{in} - V_{out}\right)$

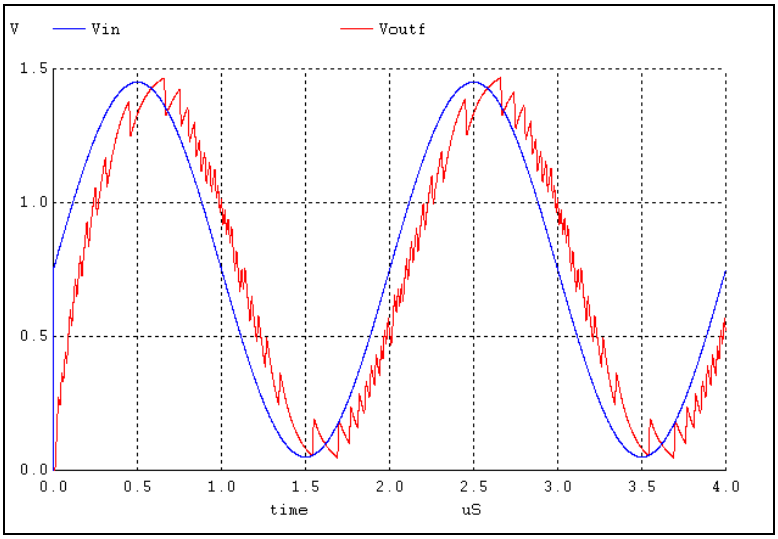
David Goldman

**EE 515 – CMOS Mixed-Signal IC Design**

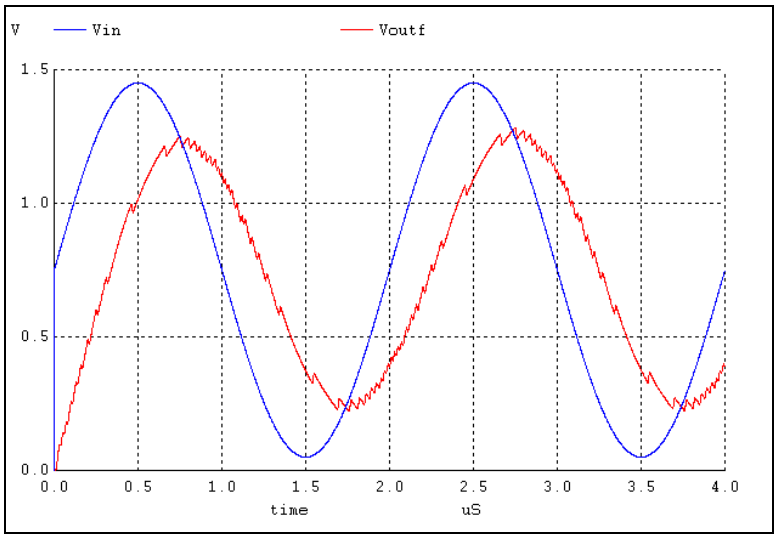
Problem 32.6

Question: Show, using SPICE simulations, how increasing the RC circuit's time constant in Fig. 32.10 will remove additional modulation noise making the output smoother. What happens to the amplitude of the desired signal?

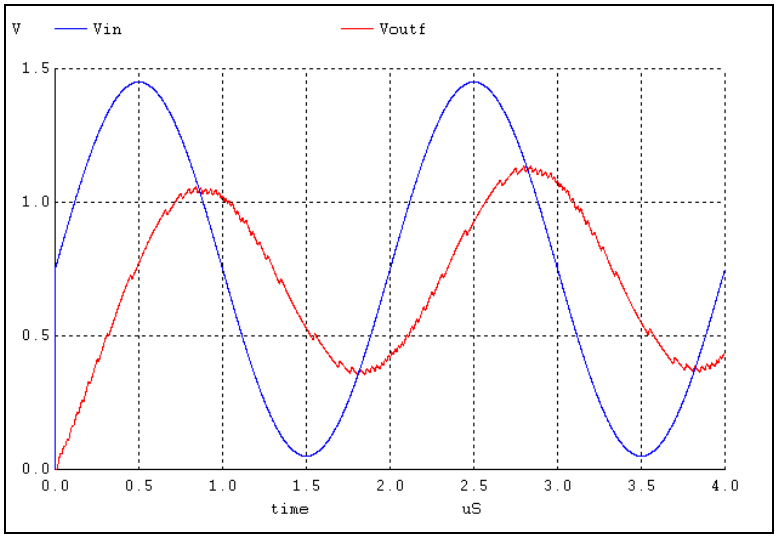
Answer: Fig. 32.10 shows the original waveform with R = 1 kΩ and C = 100 pF, where the time constant equals the product of R and C.




The following plot shows the result of tripling the RC time constant of the previous plot.



The next plot has an RC time constant with a value of five times that of its original value.




Clearly, these plots indicate that as RC increases the plots become smoother, however the peak amplitude simultaneously diminishes.

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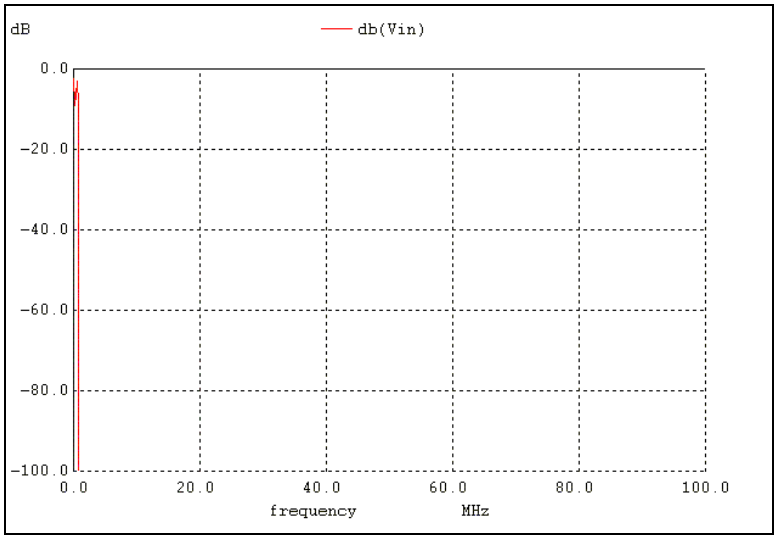
**EE 515 – CMOS Mixed-Signal IC Design**

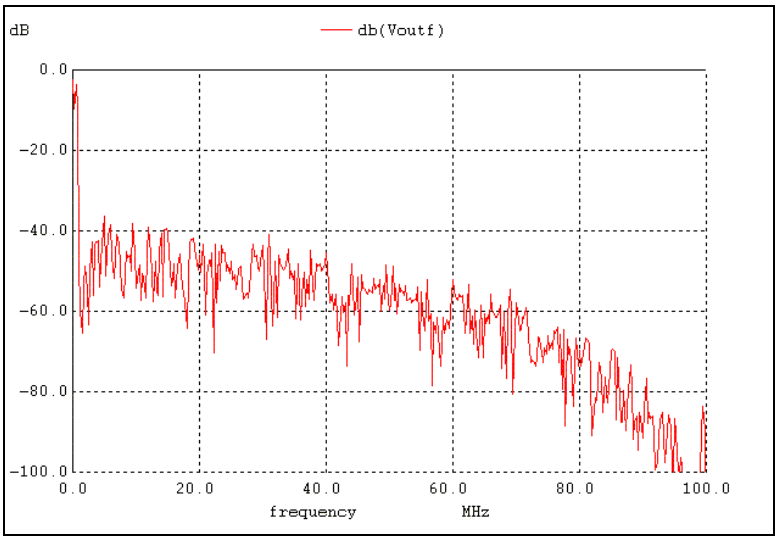
Problem 32.7

Question: Show the spectrums (modulator input, output, and output after filtering) of the signals in question 32.6. Discuss what the spectrums indicate.

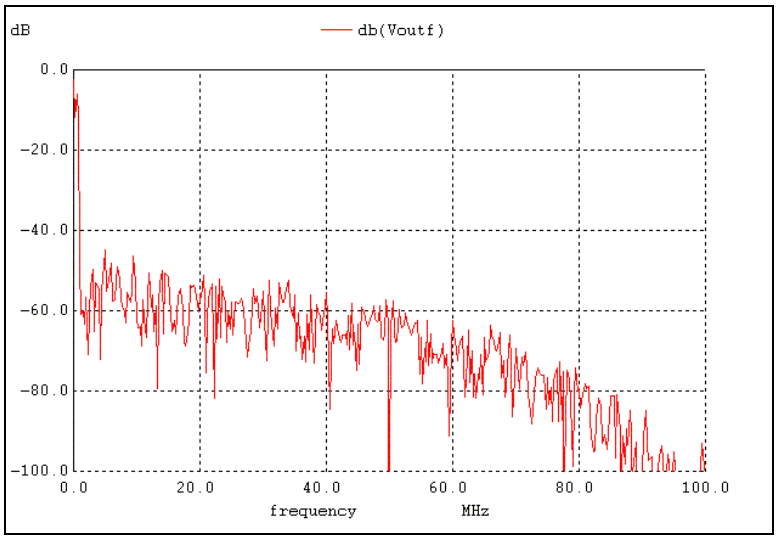
Answer: The spectrum of input is shown below. Note that the spectrum only contains the single, fundamental tone.



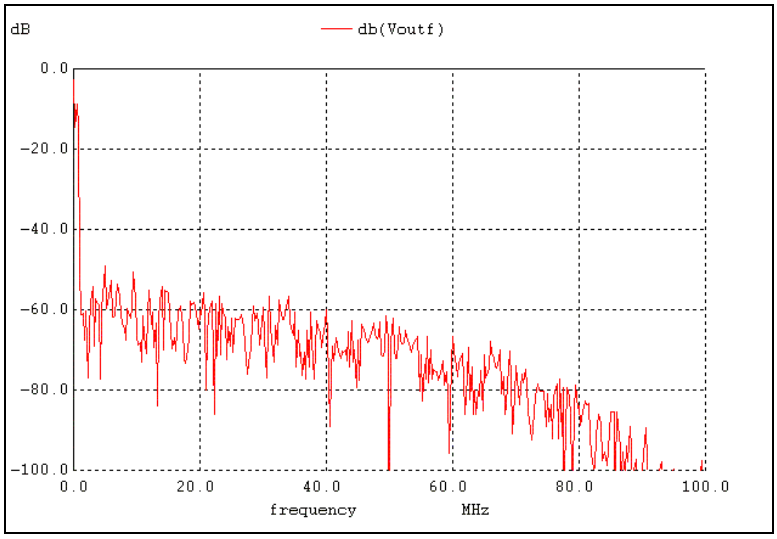

The output spectrum is shown below with the filtering determined by the R and C; namely, R = 1kΩ and C = 100 pF. Note that the noise rolls-off with frequency and the noise peak is greater than -40 dB.



The following plot shows the output when the RC time constant is tripled. Note that the noise peak is less than -40 dB.




The next plot shows that the noise peak decreases further. In this case, the RC time constant is five times that of the original.




The three previous plots illustrate that as the time constant increases the noise peak drops, and the signal-to-noise ratio (SNR) increases. This is expected since the time-domain outputs are smoother (see Problem 32.6.)

Gexin

Problem 32.8: Explain how the quantizer in fig. 32.12 functions.

Solution for 32.8:

The basic idea for this fig.32.12 is that:

(1) The digital word must be represented by 2's complementary format before it can be used as an input to an integrator, which means, in this figure, the input $X(z)$ and the MUX output should be 2's complementary format.

(2) MSB, the select control signal for MUX, is just the MSB of the integrator output represented in Binary offset format. Notice: the integrator feed back signal (not the MUX output), used for integration, is represented by 2's complementary format, that is, the integrator output has been changed to Binary offset format before it's MSB is used in MUX.

Here is the binary offset representation for $V_{ref+}$, $V_{CM}$, and $V_{ref-}$:

$V_{ref+}$ 1111…1

$V_{CM}$ 1000…0

$V_{ref-}$ 0000…0

Here is the 2's complementary representation for $V_{ref+}$, $V_{CM}$, and $V_{ref-}$:

$V_{ref+}$ 0111…1

$V_{CM}$ 0000…0

$V_{ref-}$ 1000…0

The algorithm for quantization is that when the input value of quantizer is greater than $V_{CM}$, then output of the quantizer should be $V_{DD}$, that is, $0111\ldots1$ in 2's complementary. When the input value is less than $V_{CM}$, then output should be ground, that is, $1000\ldots0$ in 2's complementary.

In fig. 32.12, when the accumulator's output is greater than $V_{CM}$, then the MSB for accumulator output is '1' (in Binary offset format), then the MUX output will be $0111\ldots1$. When the accumulator's output is less than $V_{CM}$, then the MSB for accumulator output (in 2's complementary) is '0', then the MUX output will be $1000\ldots0$.

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32.9 What are we assuming about an input signal if the modulation noise follows Eq. 32.7?

$$NTF(z)E(z) = (1 - z^{-1})E(z) = \left(1 - e^{-j2p\frac{f}{f_s}}\right) \cdot \frac{V_{LSB}}{\sqrt{12 f_s}} \qquad (32.7)$$

The assumptions made about the input signal in Equation 32.7 relate to the derivation of the noise spectral density equation,

$$E(z) = V_{Qe}(f) = \frac{V_{LSB}}{\sqrt{12 f_s}}.$$

In the derivation below two assumptions are made. First it is assumed the output of the ADC is filtered through a low-pass filter band limiting the noise power. Worse case the bandwidth is limited to the Nyquist frequency fs/2. Thus integral is evaluated between 0 and fs/2.

Second it is assumed that Bennett's criteria holds and that the voltage spectrum is truly flat. In other words that the noise probability density function for quantization noise is truly random and falls in the range of ±0.5 LSB, defined by Figure 30.47.

$$\frac{V_{LSB}^{\ 2}}{12} = 2\int_0^{f_s/2} V_{Qe}^{\ 2}(f)df \ . \qquad (30.42)$$

$$V_{Qe}(f) = \frac{V_{LSB}}{\sqrt{12 f_s}}.$$

# EE515: CMOS Mixed-Signal IC Design

Problem 32.10
Jim Slupe

32.10 What is the magnitude of Eq. (32.7)?

Answer: Equation 32.7 is shown here:

$$NTF(z)E(z) = (1 - z^{-1})E(z) \rightarrow NTF(f)V_{Qe}(f) = (1 - e^{-j2\pi\frac{f}{f_s}}) * \frac{V_{LSB}}{\sqrt{12 f_s}}$$

$$\left|NTF(z) \mid \bullet \mid E(z)\right| = \frac{V_{LSB}}{\sqrt{12 f_s}}\left(1 - \cos\left(-2\pi\frac{f}{f_s}\right) + \sin\left(2\pi\frac{f}{f_s}\right)\right)$$

For those frequencies less than B where $f << f_s$, $1 - \cos\left(-2\pi\frac{f}{f_s}\right)$ goes to zero.

In addition, where $f << f_s$ the quantity $\sin\left(2\pi\frac{f}{f_s}\right) \approx 2\pi\frac{f}{f_s}$.

So: $\left|NTF(z) \mid \bullet \mid E(z)\right| \approx \frac{V_{LSB}}{\sqrt{12 f_s}} * 2\pi\frac{f}{f_s}$

EE515: CMOS Mixed-Signal IC Design
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Question 32.11:

What is the difference between quantization noise and modulation noise?

Answer:

Modulation noise is the quantization noise after being differentiated by a modulator.

32.12 Show the steps and assumptions leading to equation (32.15).

The frequency response of a differentiator is $\sqrt{2(1-\cos 2\pi \frac{f}{f_s})}$.

The quantization noise of an ADC is $\frac{V_{LSB}}{\sqrt{12 f_s}}$, assuming Bennett's criteria holds.

In a first order noise-shaping feedback modulator, the quantization noise is differentiated. This differentiated quantization noise is called modulation noise.

The modulation noise is therefore $\frac{V_{LSB}}{\sqrt{12 f_s}} . \sqrt{2(1-\cos 2\pi \frac{f}{f_s})}$.

Using the half angle formula $\sin^2 x = \frac{1-\cos 2x}{2}$,

$$\sqrt{2(1-\cos 2\pi \frac{f}{f_s})} = \sqrt{4\left(\frac{1-\cos 2\pi \frac{f}{f_s}}{2}\right)} = \sqrt{4 * \sin^2 \pi \frac{f}{f_s}} = 2 \sin \pi \frac{f}{f_s}.$$

Therefore, the modulation noise is $\frac{V_{LSB}}{\sqrt{12 f_s}} . 2 \sin \pi \frac{f}{f_s}$, assuming $f < f_s$.

The RMS quantization noise, $V_{Q_{e,RMS}}$, present in a bandwidth B is,

$$V_{Q_{e,RMS}}^2 = 2\int_0^B \left( \frac{V_{LSB}}{\sqrt{12 f_s}} . 2 \sin p \frac{f}{f_s} \right)^2 . df$$

Since $B = \frac{f_s}{2K}$, and for small values of x, $\sin x \approx x$,

$$V_{Q_{e,RMS}}^2 = 2 * \frac{V_{LSB}^2}{12 f_s} * 4 * \pi^2 * \int_0^{\frac{f_s}{2K}} \frac{f}{f_s} df$$

$$= \frac{V_{LSB}^2}{12 f_s} * 8 * \pi^2 * \frac{1}{3} * \frac{f_s}{8K^3}$$

So,

$$V_{Q_{e,RMS}} = \frac{V_{LSB}}{\sqrt{12}} * \frac{\pi}{\sqrt{3}} * \frac{1}{K^{3/2}}$$

EE515: CMOS Mixed-Signal IC Design
Question 32.13
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**Question: #32.13**

Is the statement on page 163 that "every doubling in the oversampling ratio results in 1.5 bits increase in resolution" really true if K is small (say 8 or 16)? Explain?

**Solution:**

Ideal SNR for a first order noise shaping data converter is:

$$SNR_{ideal} = 6.02N + 1.76 - 5.17 + 30\log K \quad \text{(in dB)} \qquad (32.17)$$

This results in a 1.5 bit increase, ($N_{inc}$), for every doubling of sampling ratio, K. The equation is accurate for all integer values of K > = 2. It may not be practical or useful to implement a NS Data converter for oversampling ratio's less than 8. The resulting equation to find the increase in the number of bits determined from the oversampling ratio, K, is:

$$N_{inc} = \frac{30 \cdot \log K - 5.17}{6.02} \qquad (32.19)$$

shows that for all integer oversampling values of K>=2, Equation (32.17) is valid. Again, this is not to say that implementing a NS Data Converter is worthwhile for values of K less than 8, but the above equation is still valid for K>=2.

32.14 Does noise-shaping work for DC input signals? If so, how?

Solution: Yes, noise-shaping does work for DC input signals. Noise-shaping techniques can be used to modulate a DC input signal to create a digital representation of that DC input. The corresponding bandwidth of the resulting signal would need to be limited to get rid of the higher frequency modulation noise. Since the input bandwidth is just DC, the output signal should be purposely reduced because the higher frequencies will have more noise associated with it.

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Question 32.15

Show the steps leading up to Eq. (32.25).

Equation 32.25 is the RMS modulation noise error of a first order (M=1) noise shaping converter system with a second order (L=2) sinc averaging filter. It's derivation starts with equation 32.22:

$$V^2_{Qe,RMS} = 2 \int_0^{f_s/2} |NTF(f)|^2 \cdot |V_{Qe}(f)|^2 \cdot |H(f)|^2 \cdot df.$$

This assumes that the noise is bandlimited to $f_s / 2$ and that the integrand represents the square magnitude of the noise in the system. From equation 32.10:

$$|NTF(f)|^2 \cdot |V_{Qe}(f)|^2 = V^2_{LSB} / (12f_s) * 2 * (1 - \cos (2\delta f / f_s)),$$

and using half angle identity:

$$\sin^2 x = \tfrac{1}{2} * (1 - \cos 2x),$$

and using equation 31.93 for a sinc filter with L = 1:

$$|H(f)| = 1/K * \sin (K\delta f / f_s) / \sin (\delta f / f_s),$$

Equation 32.22 can be simplified to equation 32.23:

$$V^2_{Qe,RMS} = V^2_{LSB} / (12f_s) * 8/K^4 * \int_0^{f_s/2} \sin^4 (K\delta f / f_s) / \sin^2 (\delta f / f_s) \cdot df.$$

If we let $\grave{e} = \delta f / f_s$, then $df = d\grave{e} * f_s/\delta$; and if upper limit $f = f_s/2$, upper limit $\grave{e} = \delta(f_s/2) / f_s = \delta/2$. Equation 32.23 can be written as equation 32.24:

$$V^2_{Qe,RMS} = V^2_{LSB} / (12f_s) * 8/K^4 * f_s/\delta \int_0^{\delta/2} \sin^4 K\grave{e} / \sin^2 \grave{e} \cdot d\grave{e}.$$

From using the definite integral formula shown in equation 32.99:

$$\int_0^{\delta/2} \sin^{2(M+1)} (K\grave{e}) / \sin^{2M} \grave{e} \cdot d\grave{e} = K * \delta/2 * \prod_{m=1}^{M} (2m-1)/2m$$

where M = 1, the integral in equation 32.24 evaluates to $K* \delta / 4$. Simplifying and taking the square root, equation 32.24 can be written as equation 32.25:

$$V_{Qe,RMS} = V_{LSB} / SQRT(12) * SQRT(2) / K^{3/2}.$$

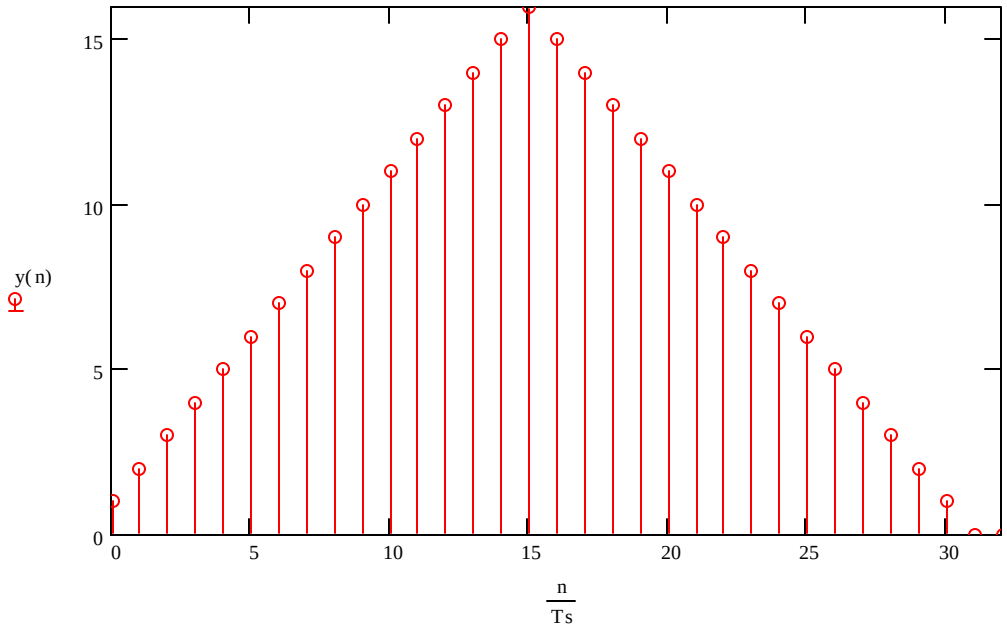
32.16
Jeremy Rice

What is the impulse response of

$$H(z) := \left( \frac{1 - z^{-16}}{1 - z^{-1}} \right)^2$$

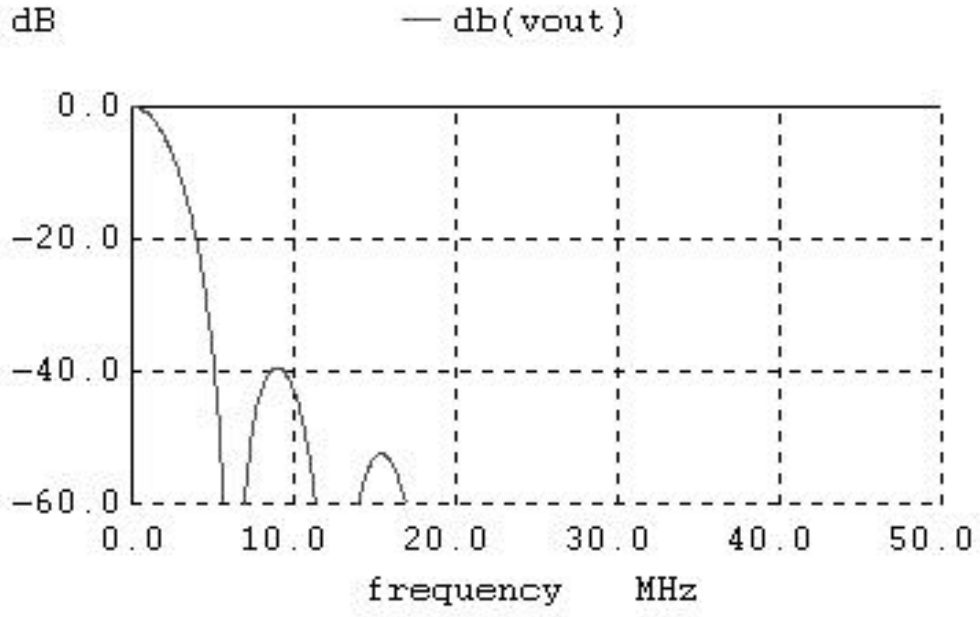
Multiply out and changing to the time domain we have: $n := 0..32$

$$y(n \cdot Ts) = x(n \cdot Ts) + 2 \cdot x[(n-1) \cdot Ts] + 3 \cdot x[(n-2) \cdot Ts] + .... + 2 \cdot x[(n-29) \cdot Ts] + 1 \cdot x[(n-30)Ts]$$



Problem 32.17  Regenerate Fig. 32.23 if L=3.  What is the droop at B?

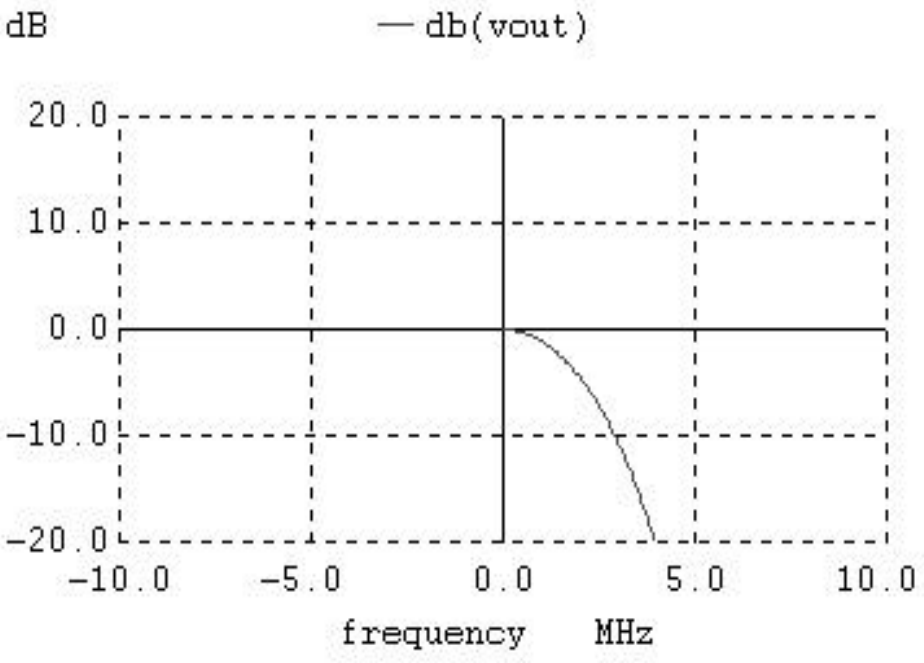
The SPICE listing for the figure below is called prob_32_17.cir.




Using Fig. 31.46 from Chapter 31,

$$\frac{\text{Main lobe}}{\text{First side lobe}} \approx \text{L . 13 dB for K} \geq 8 = 3\text{x}13 = 39 \text{ dB.}$$

The droop at the bandwidth B= 3.125 MHz is L . (-3.9) dB = -11.7 dB as shown below.



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**32.18** Is it possible to eliminate the op-amp in Fig. 32.24 and use the following topology? Comment on the problems associated with this topology.

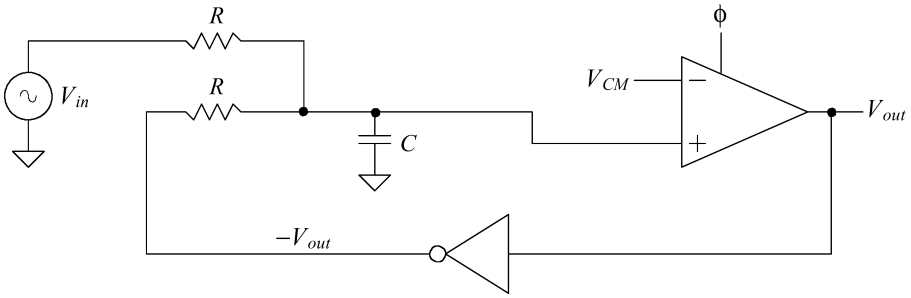


**Figure 32.94** First-order NS modulator for question 32.18.

It is possible to eliminate the op-amp in Fig. 32.24, replacing the active integrating function with a simple passive function. The RC time constant remains the same, but the virtual ground that was created by the op-amp output is no longer present. This reduces the effectiveness of the integrator, as the integration will not be able to reach as high of values. In effect, the virtual ground on the op-amp output allows the charge to be pumped higher and higher, always referencing the current value to the previous integration value. The passive solution will always refer the current integration value to the system ground, eliminating the charge-pumping effect.

With a less effective integration the system's dynamic range is reduced. Also, if the RC time constant were increased to improve the dynamic range, the requirements on the comparator would increase. See the simulation results of Question 32.19 for further details.

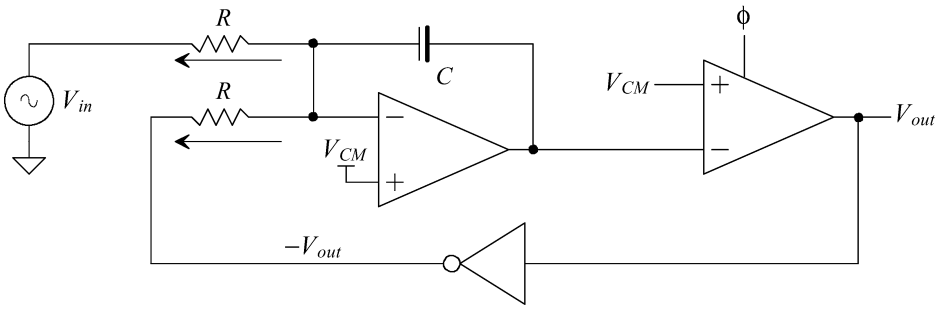


**Figure 32.24** Analog circuit implementation of a first-order NS modulator.

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**32.19** Simulate the operation of the circuit shown in Fig. 32.94.

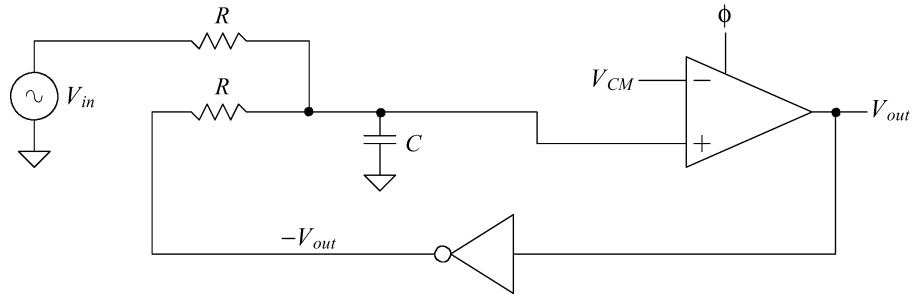



**Figure 32.94** First-order NS modulator for question 32.18.

Before simulating the circuit of Fig. 32.94, it is useful to have simulated results of the analog NS modulator of Fig. 32.24. The SPICE netlist is shown in Fig. 1. Note that the ideal inverter is implemented in the same way as an ideal comparator - with two switches.

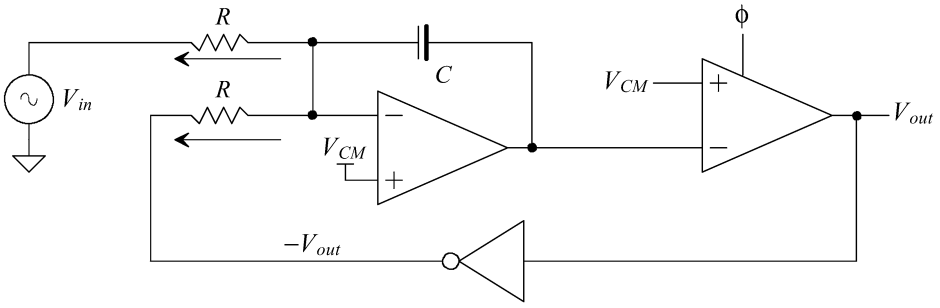



**Figure 32.24** Analog circuit implementation of a first-order NS modulator.

For proper behavior and to ensure that the integrator output does not exceed the supply rails, the RC time constant must adhere to Eq. 32.33. With $f_s$ = 100MHz, and the feedback capacitor set to 1pF, the total R must be

$$R = \frac{1}{f_s \cdot C} = 10K\Omega$$

This is accomplished by setting each resistor to 20K ohms. If the resistor values are set too low, the integrator output will exceed the supply rails (see Fig. 2). With the resistors properly set, the output is comparable to that of the discrete modulator (see Fig. 3 and Fig. 4).

```
* Question 32.19 CMOS: Mixed-Signal Circuit Design *
* Analog NS modulator, using ideal op-amp

.tran 2n 2000n 0 2n UIC

*WinSPICE command scripts
*#destroy all
*#run
*#plot Vout Vin Voutop yl -0.5 2.0

*Input power and references
VDD VDD 0 DC 1.5
Vtrip Vtrip 0 DC 0.75
VCM VCM 0 DC 0.75

*Input Signal
Vin    Vin   0 DC 0 Sin 0.75 0.7 500k

*Clock Signal
Vphi1  phi1  0 DC 0  Pulse 0 1.5   0    200p  200p  4n 10n
R1 phi1 0 1MEG

*Use a VCVS for the op-amp
Eopamp Voutop 0 VCM Vinm 100MEG

*Ideal inverter
S8 VDD Vinvout VTRIP Vout switmod
S9 0 Vinvout Vout VTRIP switmod

*Setup feedback capacitor
CF Voutop Vinm 1p

*Setup summing resistors
R3 Vin Vinm 20k
R4 Vinvout Vinm 20k

*clocked comparator implementation
XSH VDD        VTRIP  Voutop  Outsh   phi1     SAMPHOLD
S6 VDD Vout VCM Outsh switmod
S7 0 Vout Outsh VCM switmod

.model switmod SW RON=0.1

* Ideal Sample and Hold subcircuit
.SUBCKT              SAMPHOLD    VDD    VTRIP  Vin      Vout     CLOCK
Ein      Vinbuf  0        Vin      Vinbuf  100MEG
S1       Vinbuf  VinS     VTRIP    CLOCK   switmod
Cs1      VinS    0        1e-10
S2       VinS    Vout1    CLOCK    VTRIP   switmod
Cout1    Vout1   0        1e-16
Eout     Vout    0        Vout1    0       1
.model switmod SW
.ends
.end
```

**Figure 1** SPICE netlist of analog NS modulator with ideal op-amp shown in Fig. 32.24.

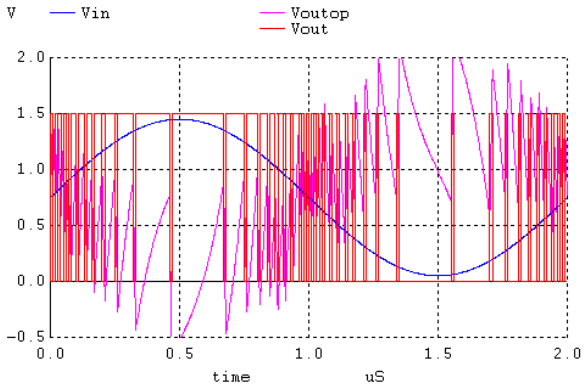



**Figure 2** Simulation results of analog NS modulator of Fig. 32.24 with R values set to 10K each.

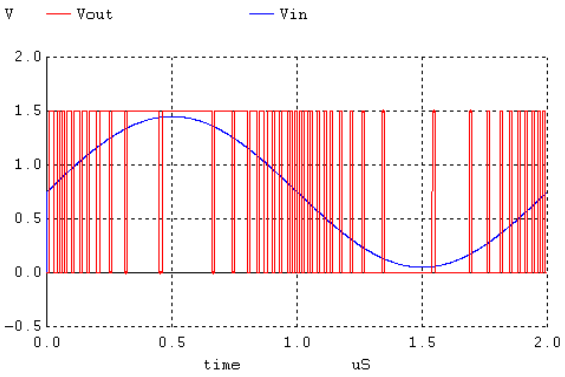



**Figure 3** Simulation results of discrete modulator of Fig. 32.7. (This is the same as Fig. 32.8.)

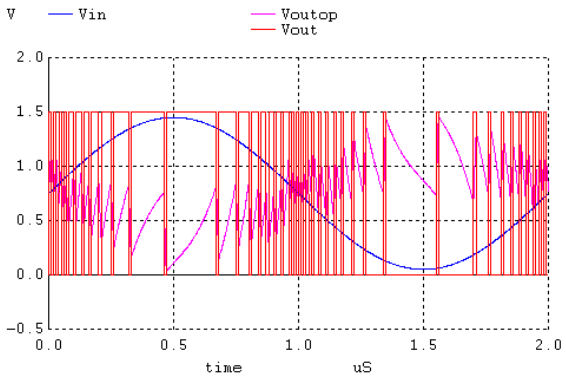



**Figure 4** Simulation results of analog NS modulator of Fig. 32.24 with R values set to 20K each.

To simulate the circuit of Fig. 32.94, the ideal op-amp is removed, the comparator polarity is switched, and the feedback capacitor is tied to ground, providing single-pole low-pass filtering of the sum of the input and the fed-back signal. Note that this eliminates the 'virtual' ground that was provided at the output node of the op-amp.

The netlist of the NS modulator of Fig. 32.94 is shown in Fig. 5. The simulation result with the resistors set to 20K is shown in Fig. 6. Note that the modulator output is oscillating more quickly, showing that the dynamic range has been reduced. In other words, the input swing needs be greater for the modulator to reach its maximum range. This can be attributed to the fact that because the virtual ground is lost, the capacitor charge is always referenced to ground and therefore the sum is not integrated as well as with the op-amp implementation.

```
* Question 32.19 CMOS: Mixed-Signal Circuit Design *
* Analog NS modulator, using RC feedback

.tran 2n 2000n 0 2n UIC

*WinSPICE command scripts
*#destroy all
*#run
*#plot Vout Vin Vrc yl -0.5 2.0

*Input power and references
VDD VDD 0 DC 1.5
Vtrip Vtrip 0 DC 0.75
VCM VCM 0 DC 0.75

*Input Signal
Vin    Vin   0 DC 0 Sin 0.75 0.7 500k

*Clock Signal
Vphi1  phi1  0 DC 0  Pulse 0 1.5   0    200p  200p  4n 10n
R1 phi1 0 1MEG

*Ideal inverter
S8 VDD Vinvout VTRIP Vout switmod
S9 0 Vinvout Vout VTRIP switmod

*Setup load capacitor
CF Vrc 0 1p

*Setup summing resistors
R3 Vin Vrc 20k
R4 Vinvout Vrc 20k

*clocked comparator implementation
XSH VDD        VTRIP  Vrc      Outsh   phi1     SAMPHOLD
S6 VDD Vout Outsh VCM switmod
S7 0 Vout VCM Outsh switmod

.model switmod SW RON=0.1

* Ideal Sample and Hold subcircuit
.SUBCKT                SAMPHOLD     VDD     VTRIP  Vin       Vout      CLOCK
Ein       Vinbuf   0         Vin       Vinbuf   100MEG
S1        Vinbuf   VinS      VTRIP     CLOCK    switmod
Cs1       VinS     0         1e-10
S2        VinS     Vout1     CLOCK     VTRIP    switmod
Cout1     Vout1    0         1e-16
Eout      Vout     0         Vout1     0        1
.model switmod SW
.ends
.end
```

**Figure 5** SPICE netlist of analog NS modulator with RC feedback shown in Fig. 32.94.

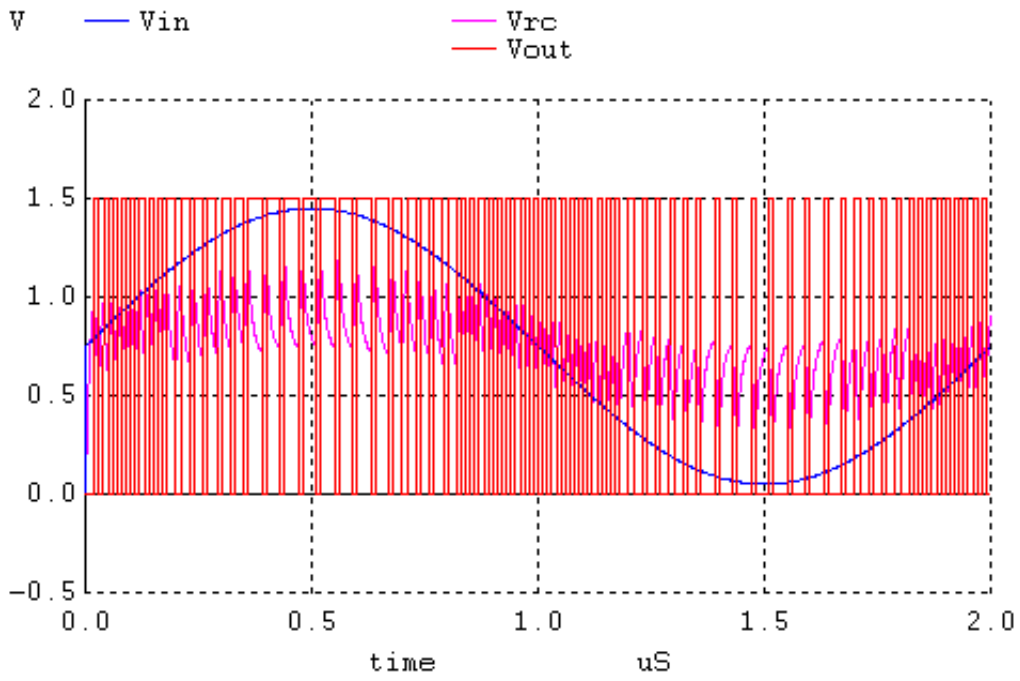



**Figure 6** Simulation results of analog NS modulator of Fig. 32.94 with R values set to 20K each.

Close examination of Fig. 6 shows that the RC time constant is the same as that of Fig. 4, but because the integrated charge is now always referenced to the system ground, rather than the virtual ground with the op-amp, the integration does not reach as high. (Notice that the integration in this circuit is not inverted as it was using the op-amp design.)

In an attempt to increase the dynamic range, the RC time constant may be increased to improve the integration characteristics. Fig. 7 shows the results of using 200K resistors instead of 20K. Notice that the modulator is now oscillating across a wider range, but that the integration values have been reduced. This would require that the comparator be very sensitive to small changes and immune to system noise. This is not practical.

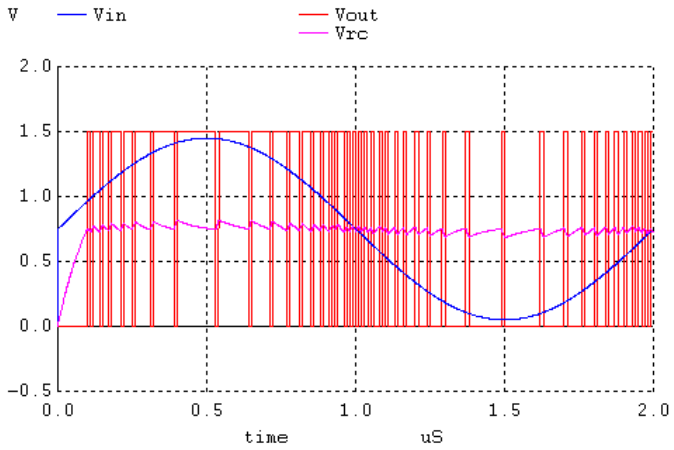
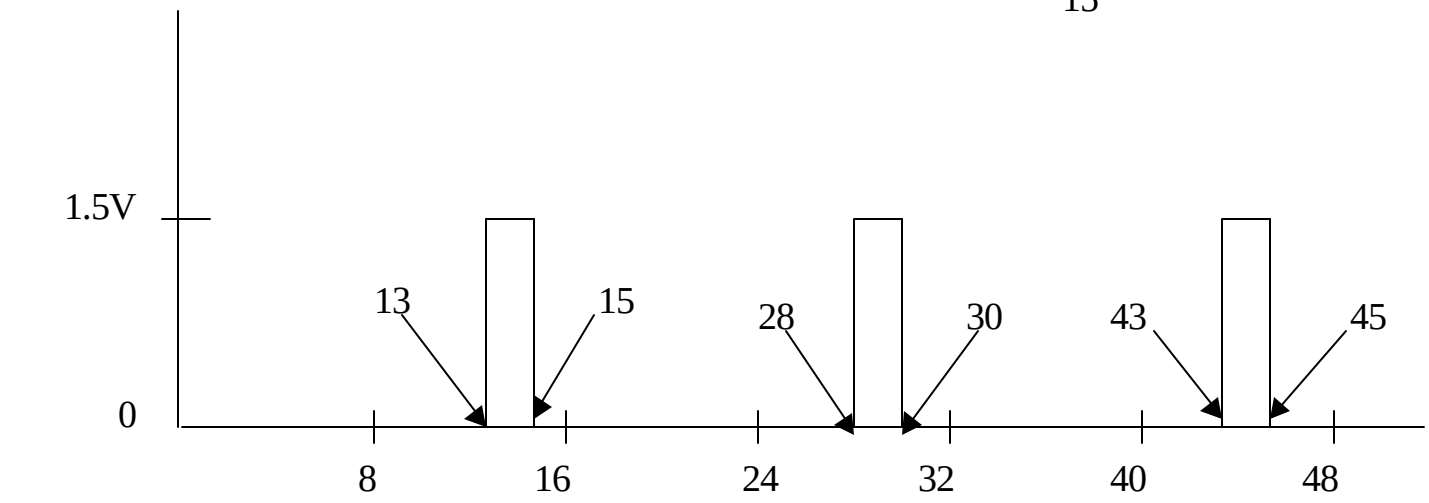



**Figure 7** Simulation results of analog NS modulator of Fig. 32.94 with R values set to 200K each.

Problem 32.20 Sketch a modulator output, similar to Fig. 32.27, if the input is 0.2V.

$$\text{average} = \frac{1.5\text{V} \times 2}{15} = 0.2\text{V}$$



32.21
Jeremy Rice

Ripple on the output of the digital filter in a modulator is the result of not limiting the bandwidth of the filter down low enough. For DC inputs, there will always arise a repetitive sequence on the output of the modulator which will pass through the filter to the output if there is not sufficient decimation( ie, low enough bandwidth) to remove these unwanted tones.

Bob Moehrke EE515 (bmoehrke@amis.com)

Question 32.22

Does adding a dither signal to the input of an NS modulator help reduce the peak-to-peak ripple in the digital filter output? Does it help to break up tones in the filter's output?

For DC signals, adding a noise dither source will cause the period out of the NS to vary. This will keep the noise power from being contained in one frequency and help increase the SFDR. Because with the added noise, one's can be closer together; this can cause the filter output code to be larger. But even though the peak-to-peak ripple can be larger, the average over several periods should be the same as without the dither source.

32.23 Derive Eq.(32.39) .

$$Y(z) = \frac{z^{-1} \cdot G_F}{1+z^{-1}(G_F - 1)} \cdot X(z) + \frac{1-z^{-1}}{1+z^{-1}(G_F - 1)} \cdot E(z)$$

Solution:
This equation was created from the diagram given in Fig. 32.36:

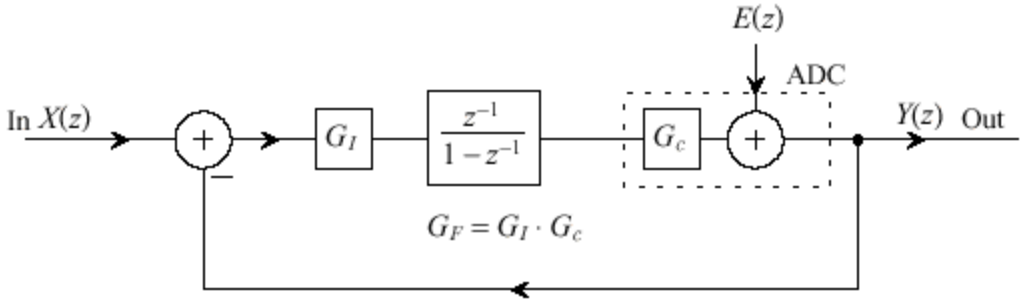



**Figure 32.36** Block diagram of a noise-shaping (NS) modulator showing forward gains.

Examining the point just after the summing point, before the $G_I$ gain block, a couple of relationships are observed by inspection. The signal at that point is the difference of X(z) – Y(z). Applying the forward gains and the noise-shaping up to the addition of the error signal yields: $[X(z) - Y(z)] \frac{z^{-1} \cdot GF}{1-z^{-1}}$ . Adding in the error signal yields:

$$Y(z) = [X(z) - Y(z)] \frac{z^{-1} \cdot GF}{1-z^{-1}} + E(z)$$

Multiply both sides by $(1-z^{-1})$:

$$(1-z^{-1}) \cdot Y(z) = [X(z) - Y(z)]\, z^{-1} \cdot GF + E(z) \cdot (1-z^{-1})$$

Gathering all Y(z) terms:

$$Y(z) - Y(z)\, z^{-1} + Y(z) G_F\, z^{-1} = X(z)\, z^{-1}\, G_F + E(z) \cdot (1-z^{-1})$$

Rearranging twice:

$$Y(z)\,(1 + G_F\,z^{-1} - z^{-1}) = z^{-1}G_F\,X(z) + E(z)\cdot(1-z^{-1})$$

$$Y(z)\,[1 + z^{-1}(G_F - 1)] = z^{-1}G_F\,X(z) + E(z)\cdot(1-z^{-1})$$

And isolating Y(z):

$$Y(z) = \frac{z^{-1}\cdot G_F}{1+z^{-1}(G_F - 1)}\cdot X(z) + \frac{1-z^{-1}}{1+z^{-1}(G_F - 1)}\cdot E(z)$$

QED

EE515: CMOS Mixed-Signal IC Design
Question 32.24
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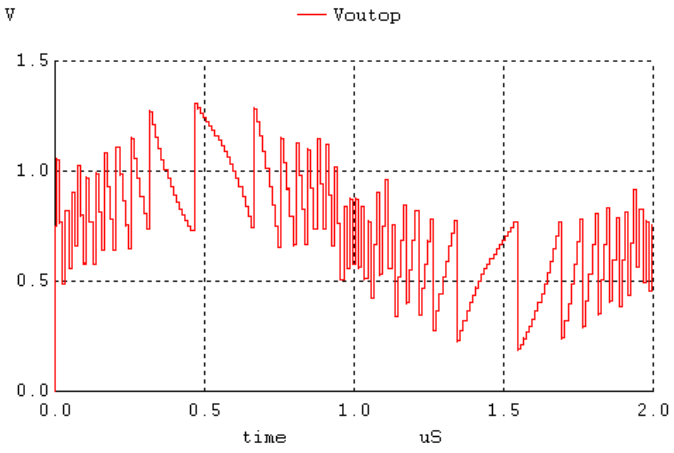
**Question: #32.24**

Repeat Ex 32.11 if the integrator gain is set to 0.5.

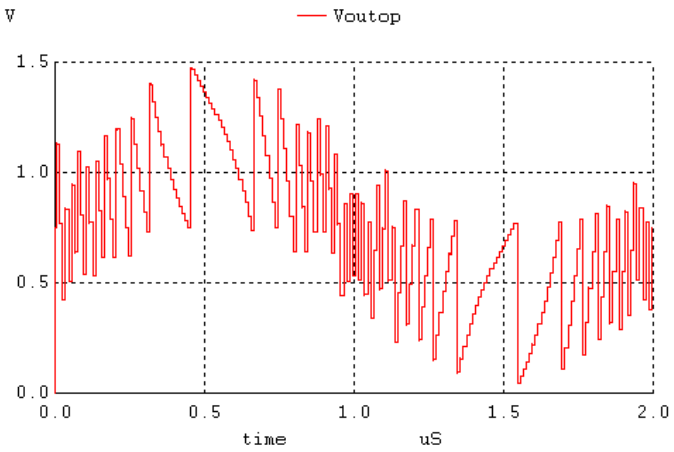
**Solution:**

Example 32.11:

Show using SPICE simulations and the modulator of Fig. 32.7, that an integrator gain of 0.4 will result in an op-amp output range well within the power supply range. The spice simulation result is shown below for a gain=0.4. This shows that the integrator output is well within the voltage supply range of 1.5V.




If the gain of the integrator is set to 0.5, the spice simulation results are shown below:



32.25 Verify equation 32.43 is correct. Use pictures if needed.

Referring to Fig. 31.78, when Vout is connected to the Ö2 switch,

$$Q_2 = C_I(V_{CM} - V_2[nT_s])$$

This is assuming that the op amp is ideal, and therefore the gain is infinite. With a nonideal op amp with finite gain:

$$V_{out}[nT_s] = A_{OL}(f)(V_+[nT_s] - V_-[nT_s])$$

$$\frac{V_{out}[nT_s]}{A_{OL}(f)} = V_{CM} - V_-[nT_s]$$

In the small signal analysis, Vcm = 0 volts AC. Therefore,

$$V_-[nT_s] = -\frac{V_{out}[nT_s]}{A_{OL}(f)}$$

When the Ö2 switch is closed, the voltage at $V_-$ is added to the voltage on the top plate of $C_I$. Therefore,

$$Q_2 = C_I\left(V_{CM} - \frac{V_{out}[nT_s]}{A_{OL}(f)} - V_2[nT_s]\right)$$

EE515: CMOS Mixed-Signal IC Design
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Problem 32.26
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Question 32.26:

Would large parasitic op-amp input capacitance affect the settling time of a DAI?

Answer:

Yes, large parasitic op-amp input capacitance would slow the settling time of a DAI.

The DAI circuit can be seen in Fig. 32.41. The change in the op-amp's output can be written as:

Vout = Voutfinal*(1-exp((-t*2*pi*fu*CF)/(CI+CF))) (see: Eq. 32.53 and Eq. 32.54)

If the op-amp has large parasitic input capacitance (CP) then it is like there is another cap in parallel with CI. You could think of CI and CP as one new cap, CT, that takes the place of CI in Fig, 32.41 (were CT=CI+CP). Then the change in the op-amp's output can be rewritten as:

Vout = Voutfinal*(1-exp((-t*2*pi*fu*CF)/(CT+CF)))

Or as:

Vout = Voutfinal*(1-exp((-t*2*pi*fu*CF)/(CI+CP+CF)))

This clearly shows that the change in the op-amp's output, or settling time, will get slower as CP gets larger.

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**32.27** Determine the transfer function of the DAI shown in Fig. 32.43.

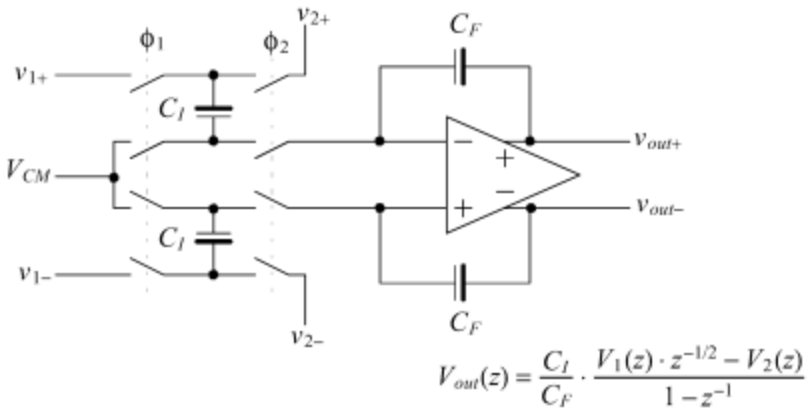



**Figure 32.43** Fully-differential discrete-analog integrator (DAI) implementation.

The transfer function of the fully-differential DAI is determined in a similar fashion to the single-ended DAI, where the charge difference on $C_I$ is transferred to the feedback capacitor, $C_F$. The output only changes state when the $f_2$ switches are closed, so the timing of Fig. 1 is used to determine the capacitor charges when the switch positions are changed.

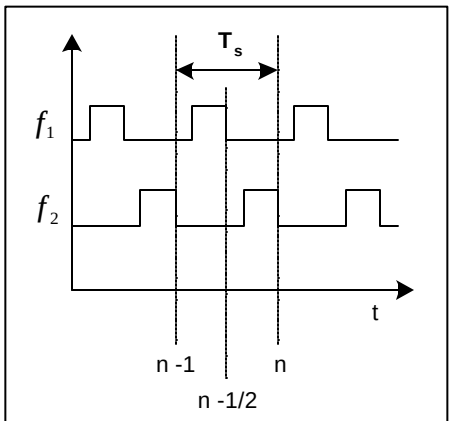



**Figure 1** Clock phase timing.

When the $f_1$ switches are closed at $n-1/2$, the charges stored on the input capacitors are

$$Q_{1(TOP)} = C_I(V_{CM} - v_{1+}[(n-1/2)T_s])$$
$$Q_{1(BOTTOM)} = C_I(V_{CM} - v_{1-}[(n-1/2)T_s])$$

Realizing that the capacitor plates on the op-amp inputs are at $V_{CM}$ when the $f_2$ switches close,

$$Q_{2(TOP)} = C_I(V_{CM} - v_{2+}[nT_s])$$
$$Q_{2(BOTTOM)} = C_I(V_{CM} - v_{2-}[nT_s])$$

The differences in the charges ($Q_1$ – $Q_2$) are transferred to the feedback capacitors, resulting in a change in the output voltages. The changes can be written as

$$C_F(v_{out+}[nT_s] - v_{out+}[(n-1)T_s]) = C_I(v_{1+}[(n-1/2)T_s] - v_{2+}[nT_s])$$
$$C_F(v_{out-}[nT_s] - v_{out-}[(n-1)T_s]) = C_I(v_{1-}[(n-1/2)T_s] - v_{2-}[nT_s])$$

These equations can be written in the $z$ domain as

$$v_{out+}(z) = \frac{C_I}{C_F} \cdot \frac{v_{1+}(z) \cdot z^{-1/2} - v_{2+}(z)}{1 - z^{-1}} \quad \text{and} \quad v_{out-}(z) = \frac{C_I}{C_F} \cdot \frac{v_{1-}(z) \cdot z^{-1/2} - v_{2-}(z)}{1 - z^{-1}}$$

Remembering that $V_{out} = v_{out+} - v_{out-}$, $V_1 = v_{1+} - v_{1-}$, and $V_2 = v_{2+} - v_{2-}$

$$v_{out+}(z) - v_{out-}(z) = \frac{C_I}{C_F} \cdot \frac{1}{1 - z^{-1}} \cdot (v_{1+}(z) \cdot z^{-1/2} - v_{2+}(z) - v_{1-}(z) \cdot z^{-1/2} + v_{2+}(z))$$

$$\Rightarrow \quad V_{out}(z) = \frac{C_I}{C_F} \cdot \frac{V_1(z) \cdot z^{-1/2} - V_2(z)}{1 - z^{-1}}$$

This transfer function is identical to that of the single-ended discrete-analog integrator.

# EE515: CMOS Mixed-Signal IC Design

Problem 32.28
Jim Slupe

32.28 Derive Eq. (32.65).

Answer: Starting with equation 32.64:

$$|NTF(f)| \bullet |V_{Qe}(f)| = \frac{V_{LSB}}{\sqrt{12 \bullet f_s}} \bullet 4 \bullet \sin^2 \pi \frac{f}{f_s} \tag{32.64}$$

$$V_{Qe,RMS}^2 = 2\int_0^B |NTF(f)|^2 \bullet |V_{Qe}(f)|^2 \bullet df = 2 \bullet \frac{V_{LSB}^2}{12 f_s} \bullet 16 \bullet \int_0^B \sin^4 \pi \frac{f}{f_s} \bullet df$$

Substituting $\sin x \approx x$ (equation 32.14):

$$V_{Qe,RMS}^2 \approx 2\int_0^B |NTF(f)|^2 \bullet |V_{Qe}(f)|^2 \bullet df = 2 \bullet \frac{V_{LSB}^2}{12 f_s} \bullet 16 \bullet \int_0^B \left( \pi \frac{f}{f_s} \right)^4 \bullet df$$

Integrating:

$$V_{Qe,RMS}^2 = 32 \bullet \frac{V_{LSB}^2}{12 f_s} \bullet |_0^B \left( \frac{\pi^4}{5} \right) \bullet \left( \frac{f^5}{{f_S}^4} \right)$$

Substituting for B:

$$B = \frac{f_s}{2K} \tag{32.13}$$

$$V_{Qe,RMS}^2 = 32 \bullet \frac{V_{LSB}^2}{12 f_s} \bullet \left( \frac{\pi^4}{5} \right) \bullet \left( \frac{\left( \frac{f_s}{2K} \right)^5}{{f_S}^4} \right) = \frac{V_{LSB}^2}{12 f_s} \bullet 32 \bullet \left( \frac{\pi^4}{5} \right) \bullet \left( \frac{{f_S}^5}{32 \bullet K^5 \bullet {f_S}^4} \right)$$

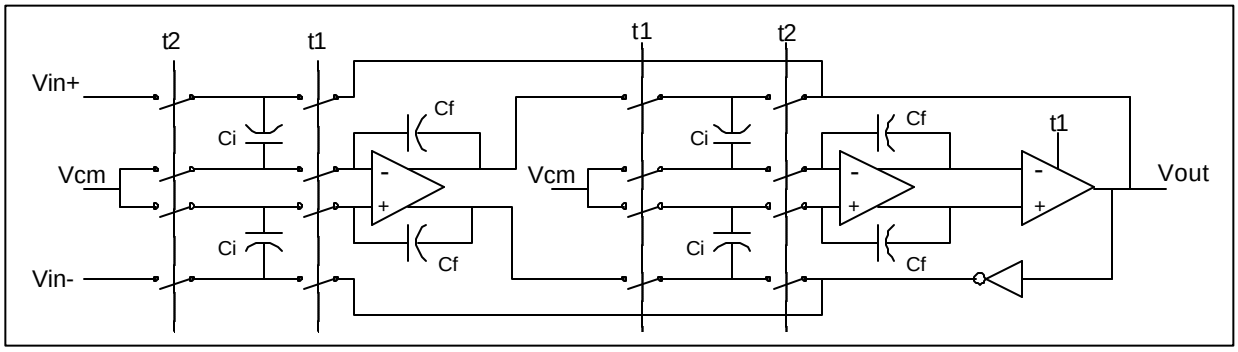
Canceling terms and taking the square root of both sides yields:

$$V_{Qe,RMS} \approx \frac{V_{LSB}}{\sqrt{12}} \bullet \frac{\pi^2}{\sqrt{5}} \bullet \frac{1}{K^{5/2}} \tag{32.65}$$

Brandon Roth
brandonroth@micron.com

32.29 Sketch the implementation of the full-differential second-order NS modulator.

Full-Differential Second-Order NS Modulator

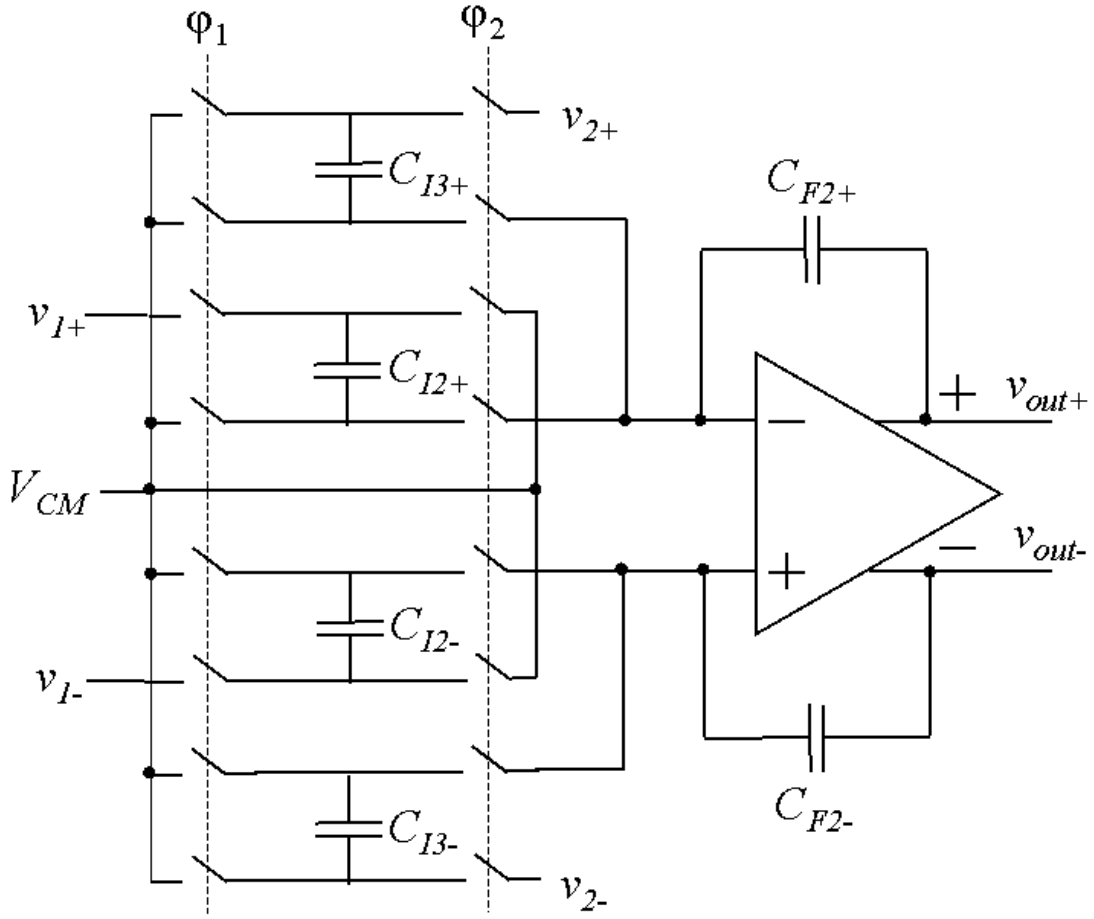


David Goldman

**EE 515 – CMOS Mixed-Signal IC Design**

Problem 32.31
Question: Sketch the fully-differential equivalent of Fig. 32.59.

Answer: In order to change Fig. 32.59 to a fully-differential circuit, $V_{CM}$ is disconnected at the op-amp and all the + components are duplicated for the – components. The fully-differential circuit is shown below.



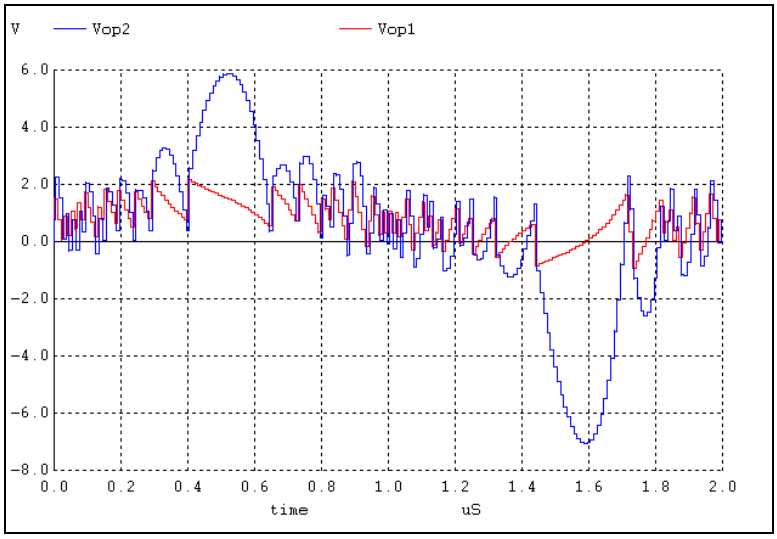
David Goldman

**EE 515 – CMOS Mixed-Signal IC Design**

Problem 32.32

Question: Resimulate the modulator in Ex. 32.13 if the gains are set to one. Comment on the stability of the resulting circuit.

Answer: Ex. 32.13 sets the gains to 0.4 by setting the ratios of the capacitors. In order to set the gains to one, the capacitors must be equal, or $C_{I2} = C_{I3} = C_{F2}$. In this way, the ratio of any two capacitors is one, and all of the gains are one. The figure below shows a resimulation of Fig. 32.62 with all the capacitors changed to a value of 1 pF.




Just as Fig. 32.62 indicates instability of the signal because its magnitude exceeds the power supply, the figure above is also unstable. In fact, since power supply is between 0 and 1.5 V, the figure above is highly unstable.

Gexin

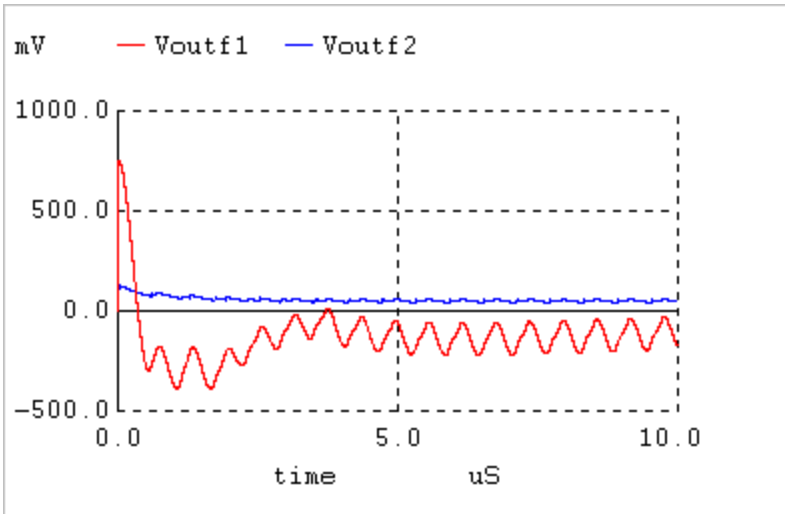
Problem 32.33: Resimulate the modulator in Ex. 32.13 if the input is only 50mV. Comment on the stability of the resulting circuit.

Solution for 32.33:

Use the following statement in the netlist (See fig32_64.cir):

*Input Signal
Vin  Vin  0 DC 0.05

The simulation result is shown below:



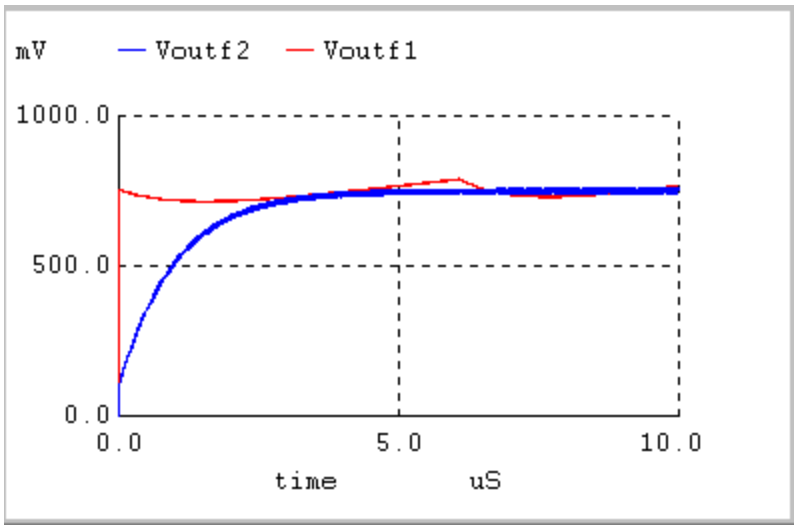

The simulation shows the comparator input and output, after low-pass filtering, for the modulator of Fig. 32.61 when the input signal is 50mV(DC).

The plot shows that the circuit is **unstable**. The average value for comparator output (Voutf2) doesn't match the input signal value.

Increase the input signal amplitude makes the modulator more stable so long as the integrators don't saturate.

To verify this statement, we can increase the input signal amplitude to show how the stability of the modulator will be improved.

When the input signal amplitude is increased to 0.75V,
The simulation is shown as follow:




From the simulation, we can see that the comparator gain is $G_c = 1$. From the equation (32.76), we can get the poles:

$$Z_{p1} = 0.84 + j0.366$$

$$Z_{p2} = 0.84 - j0.366$$

Compare with the Ex.32.12, these poles are more close to origin, which means the circuit is more stable.

Brandon Roth
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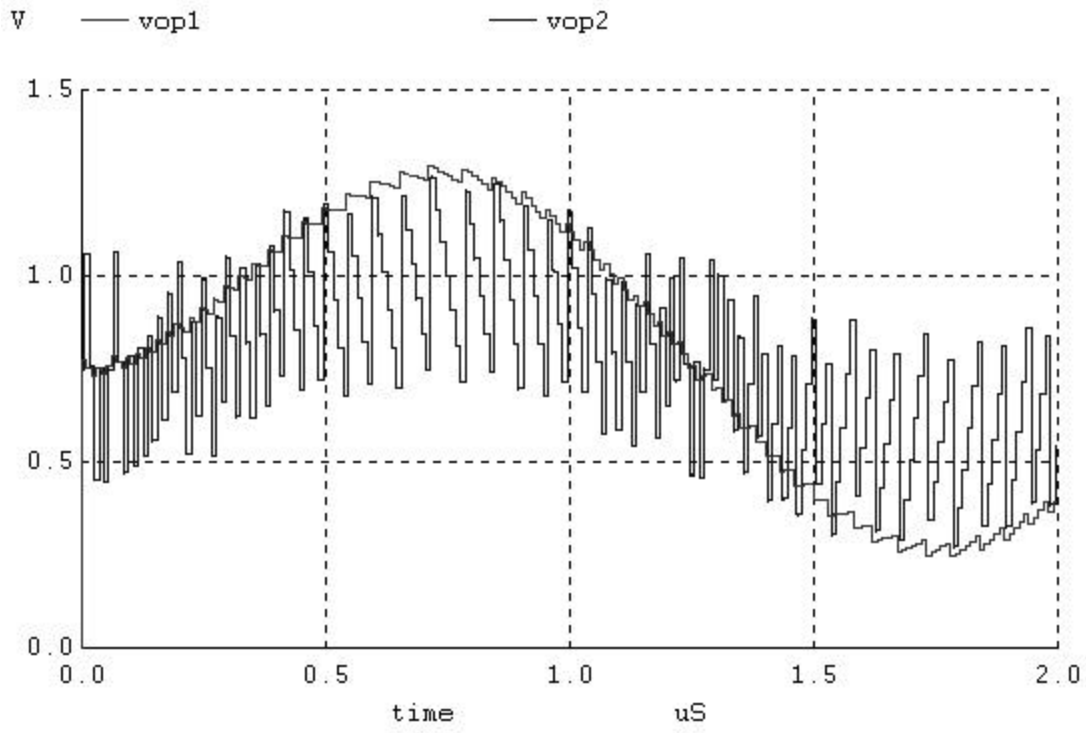
32.34 Regenerate Fig. 32.67 by selecting integrator gains so that the maximum output swing of any op-amp is 1.3V.

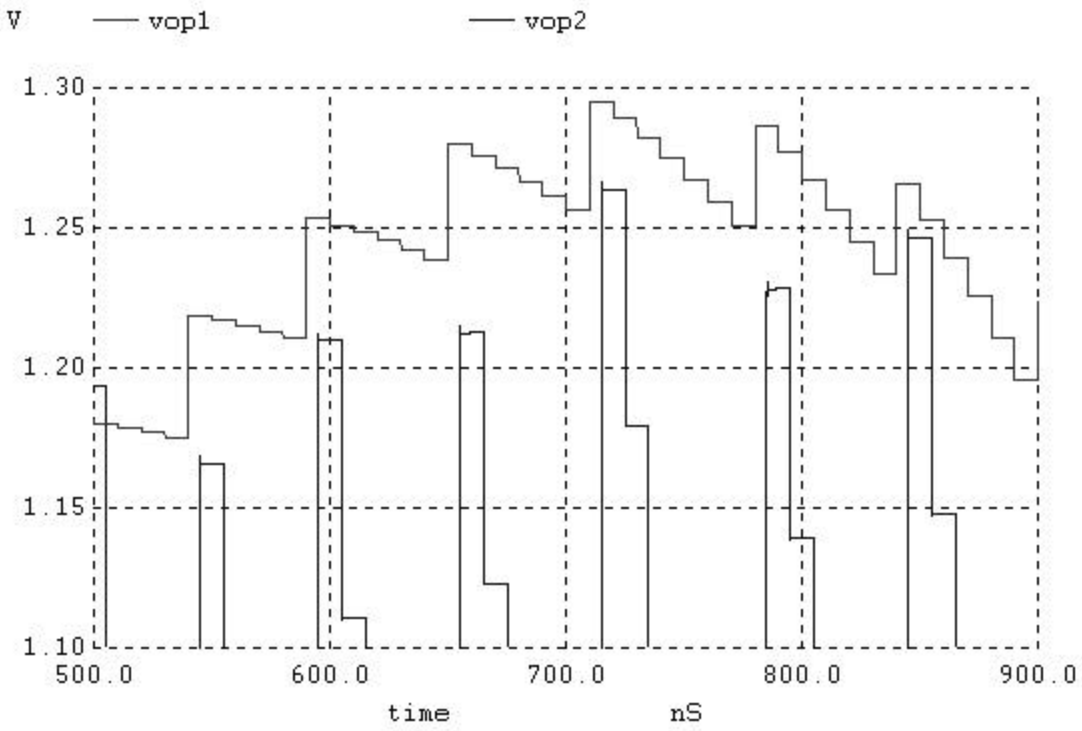
In figure 32.67 the output of the first integrator is well over 1.5V while the output of the second integrator is closer to 1.4V. Since the integrators are in series, lowering the gain of the first integrator will decrease the output swing of both integrators. Therefore, it is only necessary to lower the gain of the first integrator.

Setting $G_1$ equal to 0.03 results in an output swings for both integrators of less than 1.3V. Remember that decreasing gain increases the input-referred noise.

$$G_1 = \frac{C_{I1}}{C_{F1}} = \frac{0.03\,pF}{1pF} = 0.03\,.$$




Simulation results of second order NS Modulator with $G_1$=0.03, $G_2$=0.4, and $G_3$=1.




zoom-in results of previous figure.

# EE515: CMOS Mixed-Signal IC Design

Problem 32.35
Jim Slupe

32.35 Comment, in your own words, why the actual SNR of a NS-based data converter can be worse than the ideal values calculated in the chapter.

Answer: I wish I could comment in my own words, but the reasons were given in lecture 14.

- First, we may not be meeting Bennett's criteria that the input must be busy.
- Second, it was assumed that there were no tones present, there are tones.
- Lastly, it was assumed that the quantization noise was white (the noise power was uniformly spread across the spectrum), this too is incorrect.

32.36
Jeremy Rice

Derive Eq 32.91 with coments

Starting with 32.89:

$$SNR_{ideal} = 6.02 \cdot N + 1.76 - 20 \cdot \log\left(\frac{\pi^{m}}{\sqrt{2 \cdot M + 1}}\right) + (20M + 10) \cdot \log(k)$$

From this equation, we can see the first two terms are the SNR for a standard nyquist converter

From 32.90

$$SNR_{ideal} = 6.02 \cdot \left(N + N_{inc}\right) + 1.76$$

So, Ninc as defined by 32.90 is just the two right hand terms of 32.89 divided by 6.02

$$N_{inc} = \left[(20 \cdot M + 10)\log(k) - 20 \cdot \log\left(\frac{\pi^{M}}{\sqrt{2 \cdot M + 1}}\right)\right] \cdot \frac{1}{6.02}$$

EE515: CMOS Mixed-Signal IC Design
Brian Bergeson
Problem 32.37
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Problem 32.37:

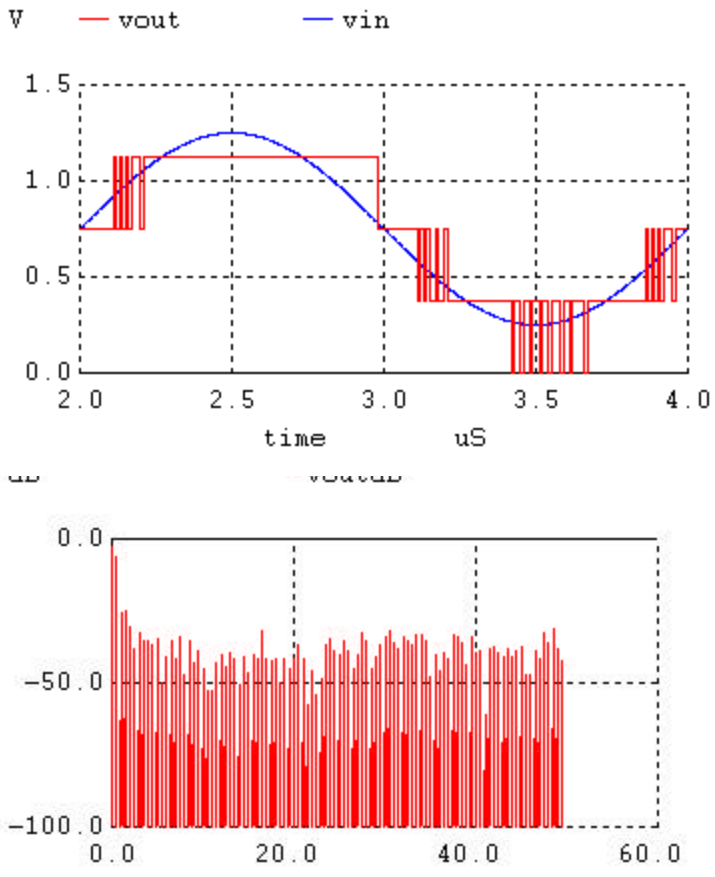
Resimulate Fig. 32.37 using two-bit ADC and DAC.

Results:

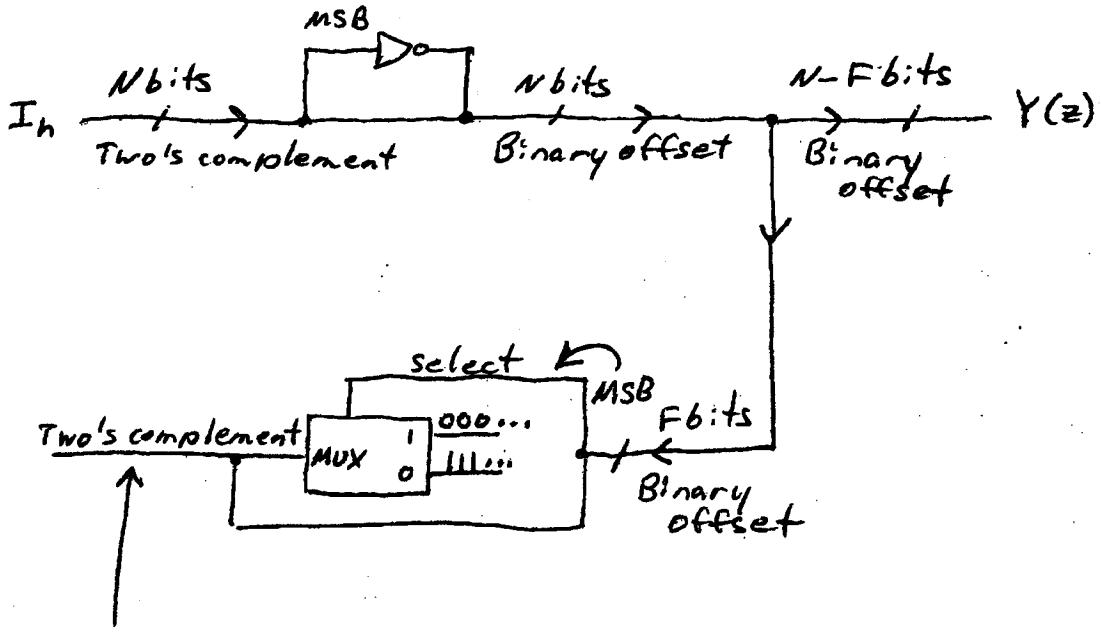
```
* Problem 32.37 CMOS: Mixed-Signal Circuit Design *

.tran 2n 20u 0 2n UIC

*WinSPICE command scripts
*#destroy all
*#run
*#let bout0=b0+1
*#let bout1=b1+3
*#plot bout0 bout1
*#plot vout vin xlimit 2u 4u
*#linearize vout
*#spec 0 50MEG 100k vout
*#let voutdb=db(vout)
*#plot voutdb ylimit -100 0
*don't forget to limit spectral analysis to 3.1MEG (if K=16) when doing spectral analysis
**#let m=mag(vout)
**#let m[0]=0
**#let m[5]=0
**#let qdnoise=0.707*sqrt(mean(m*m)*length(m))
**#print qdnoise
**#let SNRD=db((0.5/sqrt(2))/qdnoise)
**#print SNRD

*Input power and references
VDD VDD 0 DC 1.5
Vtrip Vtrip 0 DC 0.75
VCM VCM 0 DC 0.75

*Input Signal
Vin Vin 0 DC 0 SIN 0.75 0.5 500k

*Clock Signals
Vphi1 phi1 0 DC 0 Pulse 0 1.5 0 200p 200p 4n 10n
Vphi2 phi2 0 DC 0 Pulse 0 1.5 5n 200p 200p 4n 10n
R2 phi1 0 1MEG
R3 phi2 0 1MEG

*Use a VCVS for the op-amp
Eopamp Voutop 0 VCM Vinm 100MEG

*Setup switched capacitors and load
CI Vtop Vbot 0.4p
```

```
CF Voutop Vinm 1p

*Setup switches for the integrator
S1 VCM Vtop phi1 VTRIP switmod
S2 Vin Vbot phi1 VTRIP switmod
S3 Vtop Vinm phi2 VTRIP switmod
S4 Vbot Vout phi2 VTRIP switmod
.model switmod SW RON=0.1

*ADC Implementation
X1 VDD VDD 0 Voutop B1 B0 phi1 ADC2bit

*DAC Implementation
X2 VDD VDD 0 Vout B1 B0 DAC2bit

*** START ADC Subcircuit ***********************************

.subckt ADC2bit VDD VREFP VREFM Vin B1 B0 CLOCK

* Set up common mode voltage
BCM VCM 0 V=(V(VREFP)-V(VREFM))/2

* Set up logic switching point
R3 VDD VTRIP 100MEG
R4 VTRIP 0 100MEG

* Ideal input sample and hold
XSH VDD VTRIP VIN OUTSH CLOCK SAMPHOLD

* Level shift by VREFM and 1/2LSB
BPIP PIPIN 0 V=V(OUTSH)-V(VREFM)+((V(VREFP)-V(VREFM))/2^3)

* 2-bit pipeline ADC
X1 VDD VTRIP VCM PIPIN B1 VOUT1 ADCBIT
X0 VDD VTRIP VCM VOUT1 B0 VOUT0 ADCBIT
.ends

* Ideal Sample and Hold subcircuit
.SUBCKT SAMPHOLD VDD VTRIP Vin Vout CLOCK
Ein Vinbuf 0 Vin Vinbuf 100MEG
S1 Vinbuf VinS VTRIP CLOCK switmod
Cs1 VinS 0 1e-10
S2 VinS Vout1 CLOCK VTRIP switmod
Cout1 Vout1 0 1e-16
Eout Vout 0 Vout1 0 1
.model switmod SW
.ends

* Pipeline stage
.SUBCKT ADCBIT VDD VTRIP VCM VIN BITOUT VOUT
S1 VDD BITOUT VIN VCM switmod
S2 0 BITOUT VCM VIN switmod
Eouth Vinh 0 VIN VCM 2
Eoutl Vinl 0 VIN 0 2
S3 Vinh VOUT BITOUT VTRIP switmod
S4 Vinl VOUT VTRIP BITOUT switmod
```

```
.model switmod SW
.ends
*** END ADC Subcircuit ************************************

*** Start Ideal DAC Subcircuit ******************************

.subckt DAC2bit VDD VREFP VREFM Vout B1 B0

*Generate Logic switching point, or trip, voltage
R1 VDD trip 100MEG
R2 trip 0 100MEG

*Change input logic signals into logic 0s or 1s
X1 trip B1 B1L  Bitlogic
X0 trip B0 B0L  Bitlogic

*Non-linear dependent source, B, for generating the DAC output
Bout Vout 0 V=((v(vrefp)-v(vrefm))/4)*(v(B1L)*2+v(B0L))+v(vrefm)

.ends

.subckt Bitlogic trip BX BXL
Vone one 0 DC 1
SH one BXL BX trip Switmod
SL 0 BXL trip BX Switmod
.model switmod SW
.ends

*** END DAC Subcircuit ************************************
.end
```



32.38 Sketch a possible implementation of a quantizer for the error feedback modulator shown in Fig. 32.78.




Adjust output word size to N-1 just before the shift-left branch of the feedback loop as seen in Fig. 32.78.

EE515: CMOS Mixed-Signal IC Design
Question 32.39
Richard Friel
Rich_Friel@AMIS.COM

**Question: #32.39**

What transfer function is implemented by the diagram in Question 32.39?

**Solution:**

The transfer function diagram in Question 32.39 is implemented by the following function:

$$F(z) = z^{-2} \cdot (2 - z^{-1})$$

32.40 In Fig. 32.84 sketch the block diagram of the circuit in series with the $Y_2(z)$ output.

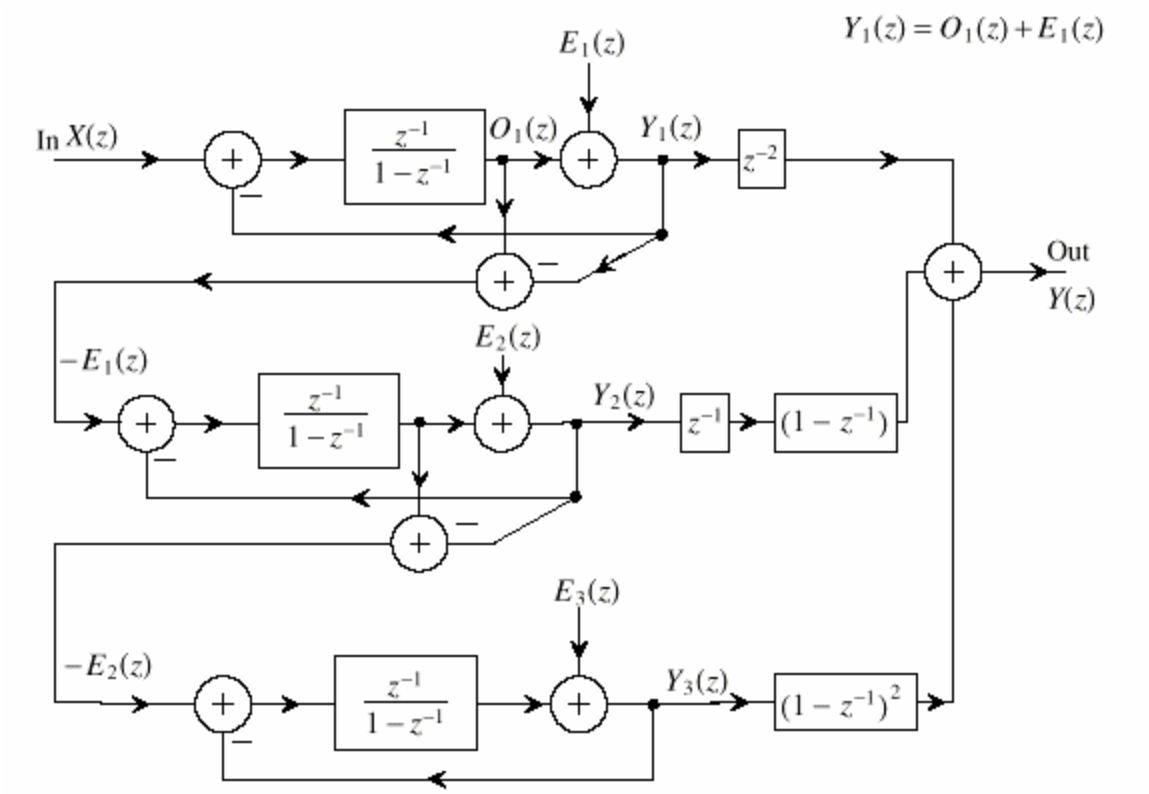
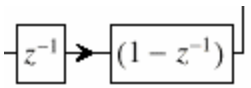
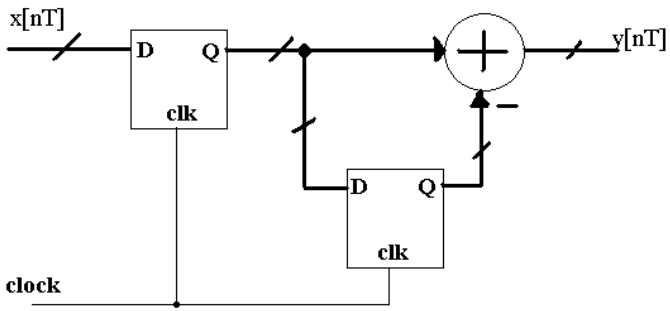



**Figure 32.84** Third-order (1-1-1) cascaded modulator.

Solution:
The portion of the circuit in question is shown below, followed by its block diagram:




x[nT]
D
Q
clk
y[nT]
D
Q
clk
clock

Bob Moehrke EE515 (bmoehrke@amis.com)

Question 32.41

Sketch the block diagram implementation of the transfer function $(1 - z^{-2})^2$. What kind of filter does this transfer function implement?

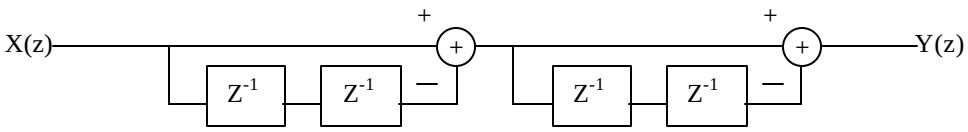
This transfer function represents two cascaded comb filters or differentiators. The magnitude response can be found using the equation right above figure 31.52:

$$|H(f)| = SQRT( 2 * ( 1 - \cos ( 2\delta Kf / f_s )))$$

For this particular case K = 2 and since there is a cascade of two filters, the magnitude response of this transfer function is

$$|H(f)| = 2 * ( 1 - \cos ( 4\delta f / f_s ))$$

The block diagram implementation is



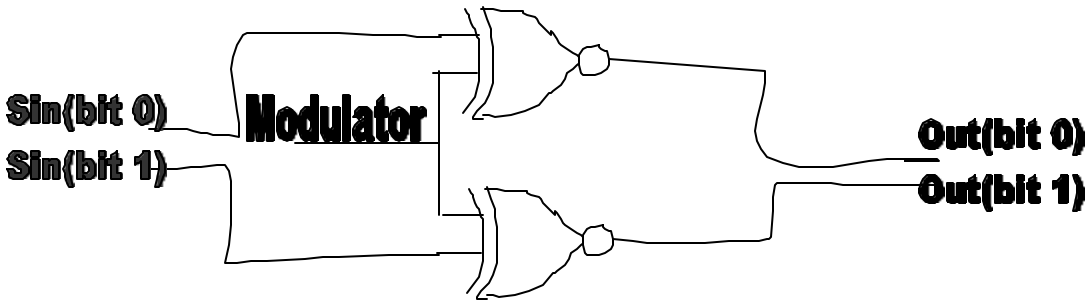
32.42
Jeremy Rice

Sketch the implementation of the multipliers in Fig 32.93.

The multipliers of fig 32.93 take the output of the modulator, and multiply it with either a sin, or cosine wave sampled at Fs/4 which provides only 0, 1, -1 from the sine/cosine waves. To do the multiplication, it is necessary that both the modulator output, and the sine/cosine be converted to 2's compliment. The truth table below shows the possible input/outputs for the system.

| modulator | sine/cosine | output |
|---|---|---|
| 01 | 01 | 01 |
| 01 | 00 | 00 |
| 01 | 10 | 10 |
| 10 | 01 | 10 |
| 10 | 00 | 00 |
| 10 | 10 | 01 |

From this table, it is clear that whenever the output of the modulator is a 1(01), the bits from the sine/cosine are passed directly. And, whenever the output of the modulator is 0(10), the bits from the sine/cosine are inverted. This operation can be accomplished by the circuit below, without converting the modulator output to 2's compliment.



Problem 32.43 Would clock jitter be a concern in a bandpass modulator?

If phase noise due to clock jitter is narrow, then jitter power is concentrated around the frequency of input sinusoid $f_{in}$ as shown in Figure 31.14. So when the input sinusoid $f_{in}$ is applied to a bandpass modulator, the clock jitter power can fall directly in the bandpass's bandwidth of interest around $f_s/4$. The jitter power can add to quantization noise and thermal noise as described in equation (33.29). This will then lower the data converter's SNR. Also, distortion resulting from non-linearities and mismatch in the data converter circuitry can add to the sampling clock error signal. This in turn lowers the data converter's SNDR. Therefore, the clock jitter can be problematic for the bandpass modulator.