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# Chapter 36

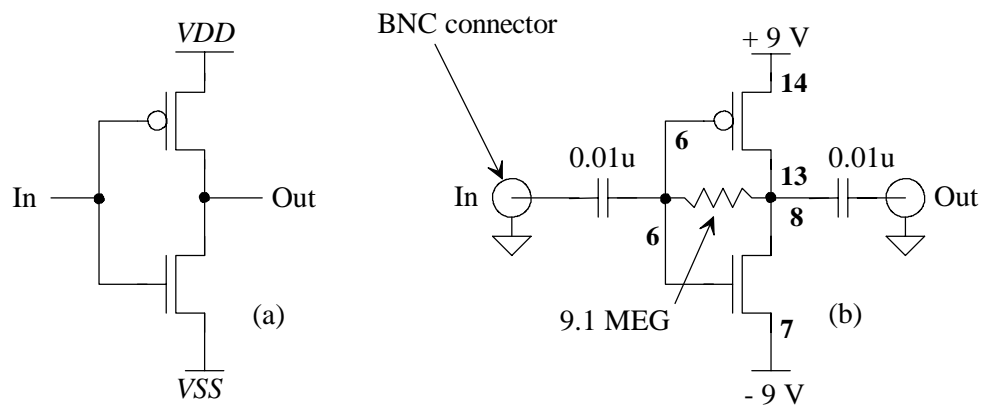
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## At the Bench

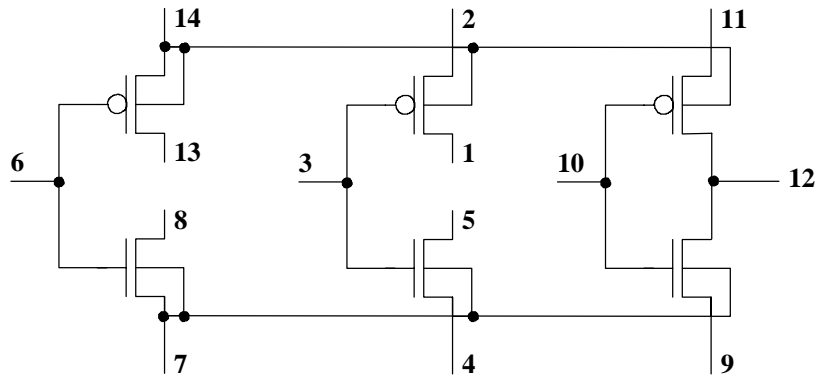
In this chapter we present some practical prototyping techniques to illustrate a few of the concepts discussed in this book. The goal of the chapter is to simply provoke thought and show alternative possibilities (other than hand calculations and simulations) for looking at the performance of a mixed-signal circuit or system.

### 36.1 A Push-Pull Amplifier

The basic CMOS push-pull amplifier (see Ch. 22) is shown in Fig. 36.1a. Figure 36.1b shows the schematic of the implementation used in this section where we have AC coupled the input and output of the amplifier to allow the 9.1 MEG resistor to self-bias the circuit. The bold numbers shown adjacent to the MOSFET terminals correspond to the pin numbers of the 4007, Fig. 36.2, used to prototype the amplifier. Note that by AC coupling our input and output, we can use ground as our input/output reference.



**Figure 36.1** (a) Push-pull amplifier and (b) prototyping the amplifier.



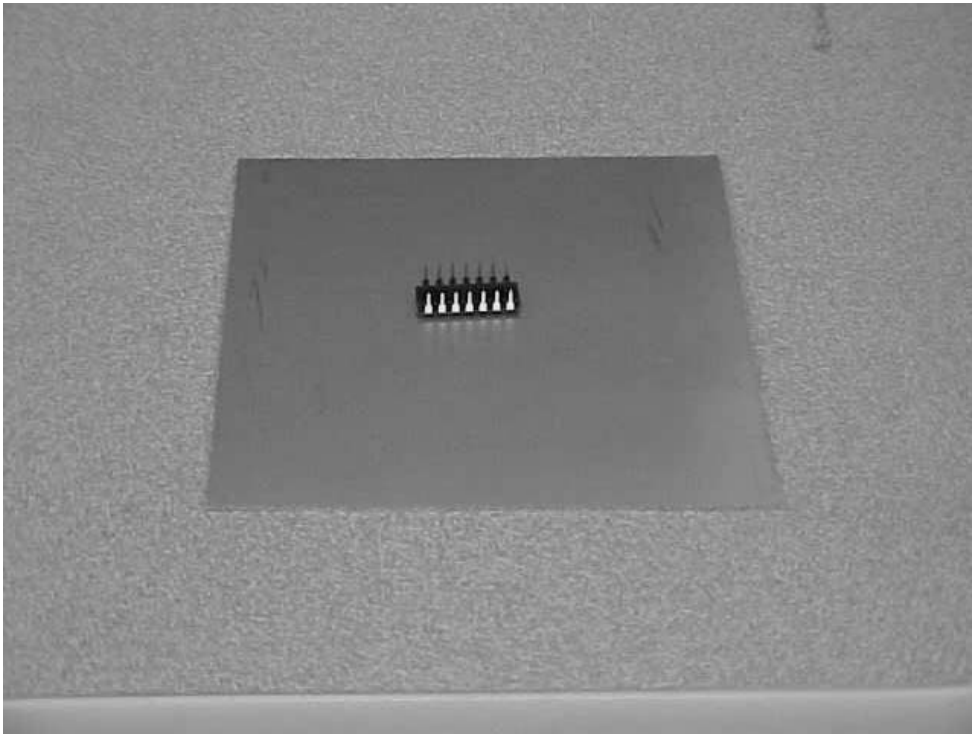
**Figure 36.2** Pin diagram for the 4007. Note how the bodies of all PMOS devices are tied to pin 14, while the bodies of the NMOS devices are tied to pin 7. This means that pin 14 must be tied to the highest potential in the circuit (if the PMOS devices are used), and pin 7 must be tied to the lowest potential.

While the detailed datasheet for the 4007 can be found at the book's website (<http://cmosedu.com>), we will comment that the threshold voltage for these transistors is approximately 2 V and that they can drive around 1 mA or so into a load (this is a serious limitation and will limit the size of the load we can drive). The large threshold voltage and limited drive capability are the reasons we used  $\pm 9$  V power supplies.

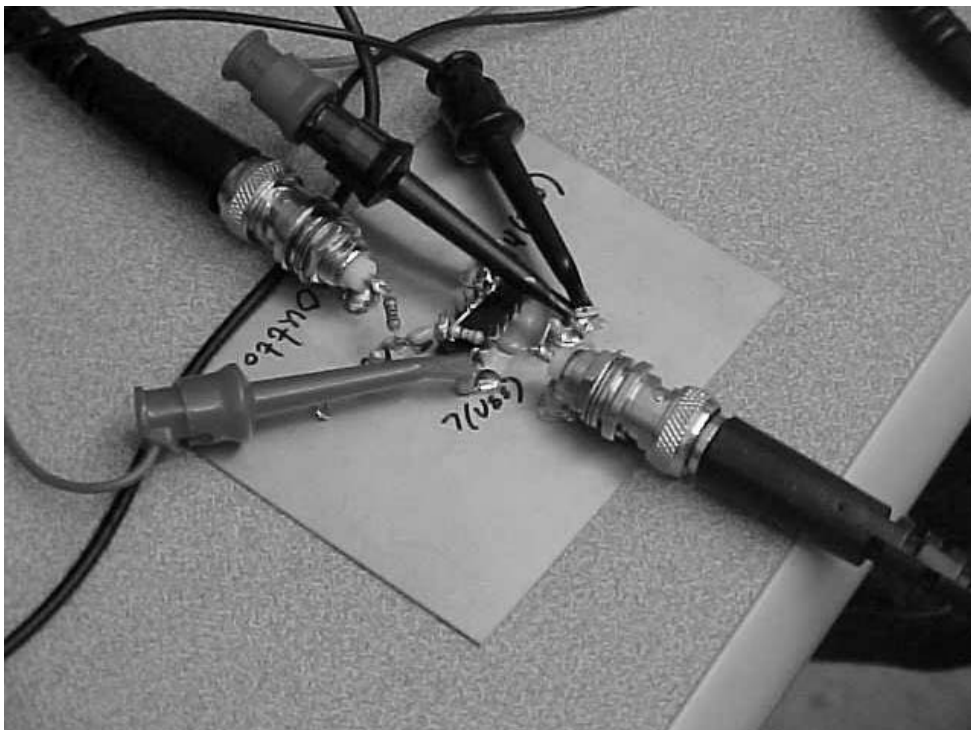
### *Deadbug Prototyping*

Figure 36.3 shows a chip flipped upside down and placed on a copper conductor (a glass epoxy, FR-4 material coated with copper used in printed circuit board manufacturing). The reason this technique is called "deadbug prototyping" should be obvious (unless the reader is so lucky they've never seen a dead cockroach). We use this approach instead of the common white protoboards found in most undergraduate electronics laboratories for prototyping because of the ability to use a good ground plane (the copper conductor). The big drawback is the need to solder all of the components together. A good (meaning equipotential) ground plane is essential to any low-noise, wide-dynamic range, measurement. We'll also use BNC connectors to pipe our signals on-to and off-of the board to avoid long wires, which tend to pick up coupled noise.

Figure 36.4 shows the prototype of the amplifier in Fig. 36.1b implemented using the deadbug technique. The black and red wires coming into the circuit provide power and ground. At the connections of power and ground on the board we add a decoupling capacitor (a capacitor soldered from the power-supply connection to the ground plane). This capacitor provides charge for any fast transients that may occur in the circuit. The capacitor leads can be twisted into small loops and soldered to the ground plane or to a pin on a chip and used as a contact point for the power supply clips. Before looking at some measurement results, we need to discuss probe loading and measurement techniques.



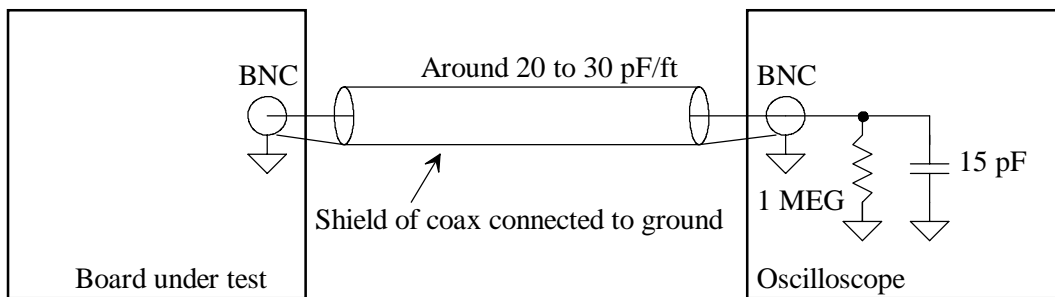
**Figure 36.3** Deadbug prototyping using a copper ground plane.



**Figure 36.4** Deadbug prototype of the amplifier in Fig. 36.1b.

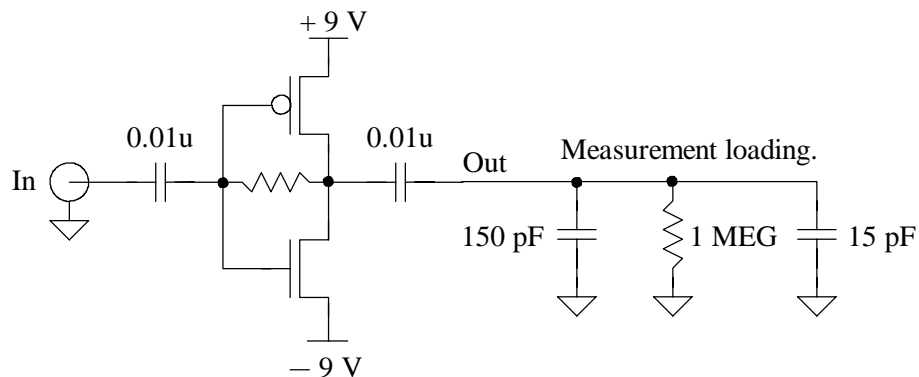
### Probing

If we're not careful, we can load the circuit we are testing with our measuring system. Consider the connection of a piece of coaxial cable to the oscilloscope shown in Fig. 36.5. The scope has an input resistance of  $1\text{ M}\Omega$  and an input capacitance of  $15\text{ pF}$ . When a coax cable is driven by a large impedance and is terminated with a large impedance, we think of it as a capacitor. If a 5-foot piece of coax is used to connect the push-pull amplifier to the oscilloscope, we would get the circuit shown in Fig. 36.6. Clearly, the measuring system will load the amplifier and keep us from accurately measuring the response of the circuit.

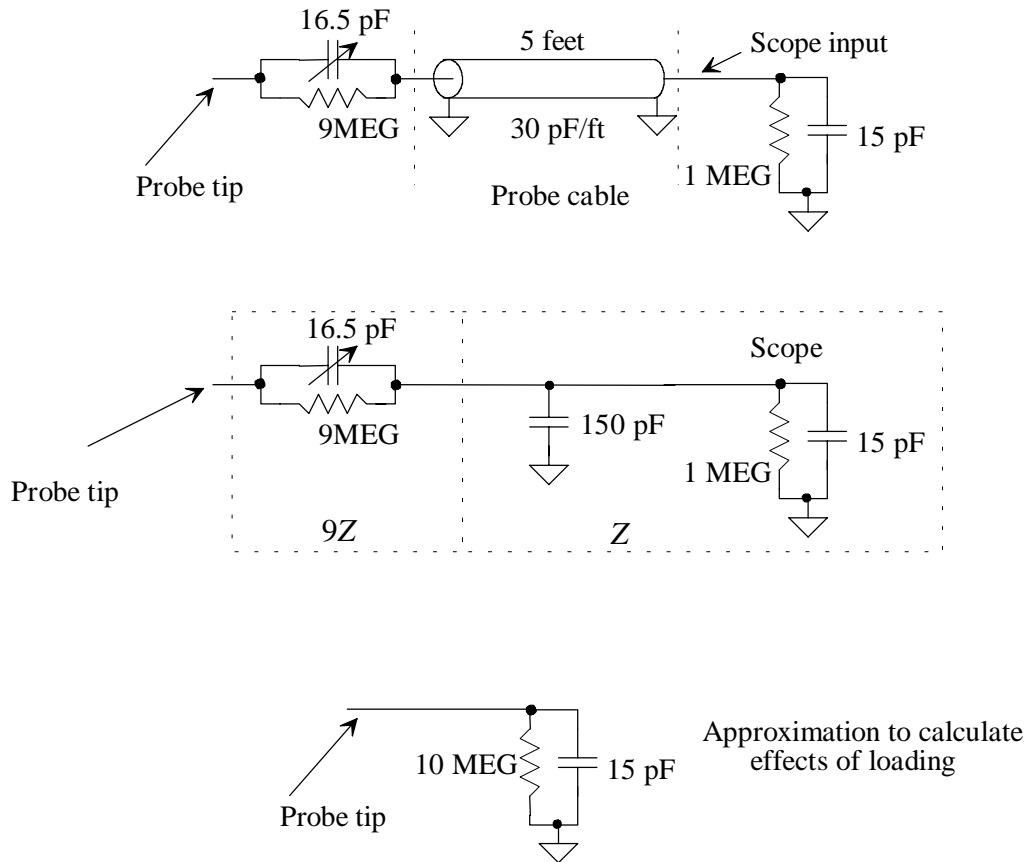


**Figure 36.5** The loading when probing with a piece of coaxial cable.

To reduce the loading by the required coaxial interconnect cable ( $150\text{ pF}$  in Fig. 36.6), a scope probe trades off sensitivity for lighter loading. Figure 36.7 shows a  $10:1$  compensated scope probe. The term  $10:1$  represents the attenuation factor from the probe tip to the input of the scope. One-tenth of the voltage on the tip of the probe actually makes it to the input of the scope. The term "compensated" indicates that the probe is designed to compensate for the large loading of the coaxial cable. If the probe is compensated correctly, the impedance in the probe's tip ( $9Z$ ) is exactly, independent of



**Figure 36.6** How we can mess up a measurement if we're not careful.



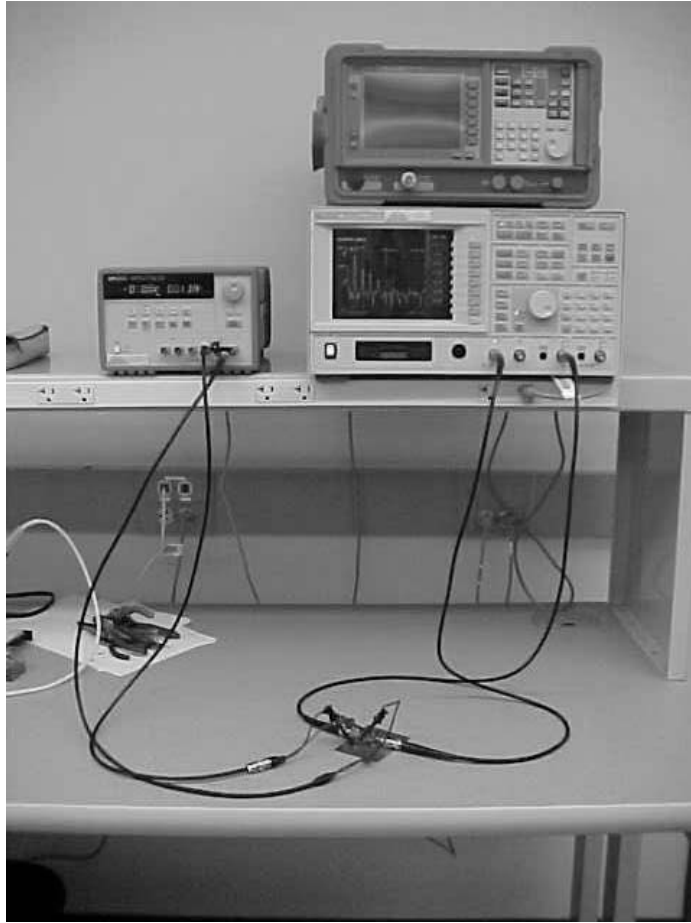
**Figure 36.7** How a compensated probe loads a circuit.

frequency, nine times larger than the impedance of the combination of the coaxial cable and the scope ( $Z$ ). Note how the loading of the probe at DC is 10 MEG while at high frequencies the loading is roughly 15 pF.

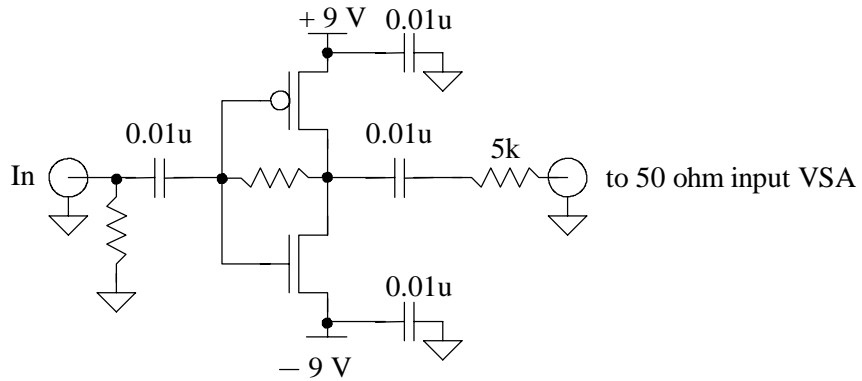
### Testing the Circuit

To test this circuit, we'll use a vector signal analyzer, VSA, (an instrument similar to a spectrum analyzer with the capability to perform an inverse Fourier transform for viewing a signal in the time domain). A test setup is seen in Fig. 36.8. We'll use an input resistance of  $50\ \Omega$  to avoid the need for a compensated probe. Because of the limited drive capability of the amplifier, we'll add a 5k resistor in series with the output. This results in a 100:1 attenuation ( $-40\ \text{dB}$ ) from the amplifier's output to the input of the VSA. The schematic of the amplifier is seen in Fig. 36.9. Note that we also added a resistor to ground on the input of the amplifier to avoid a floating node.

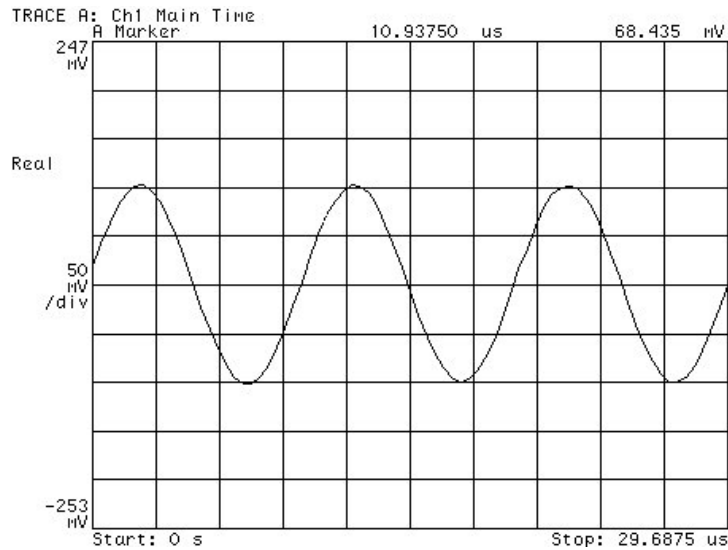
Figure 36.10 shows the input signal to the amplifier in the time domain. It is a 100 mV sinewave with a frequency of 100 kHz. The spectrum of this signal is seen in Fig. 36.11. Note the units on the y-axis are dBm or decibels with respect to 1 mW of power.



**Figure 36.8** A test setup showing a VSA, spectrum analyzer (not in use), and power supply.



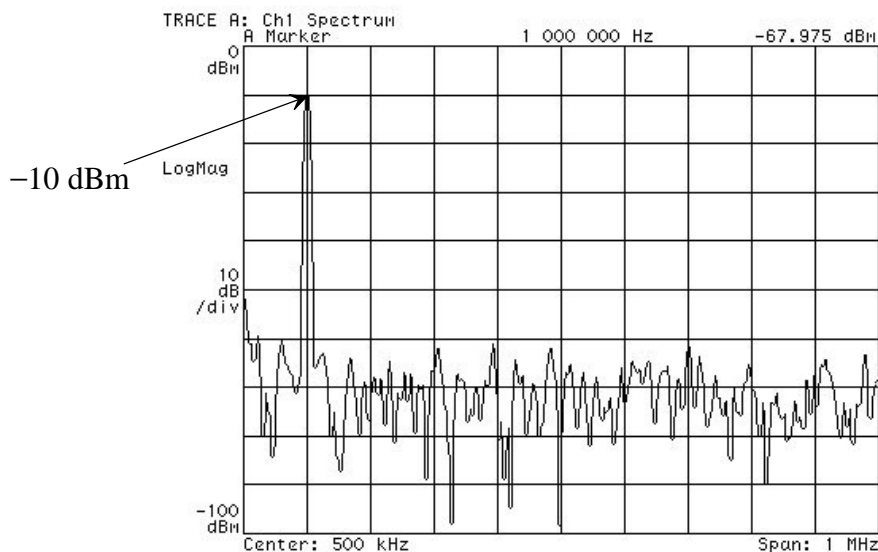
**Figure 36.9** Final schematic of the push-pull amplifier shown in Fig. 36.3.



**Figure 36.10** Input sinewave to the circuit of Fig. 36.9.

Because this is a  $50\ \Omega$  system, we can verify the power in the input sinewave is, as seen in Fig. 36.11,  $-10\ \text{dBm}$  by writing

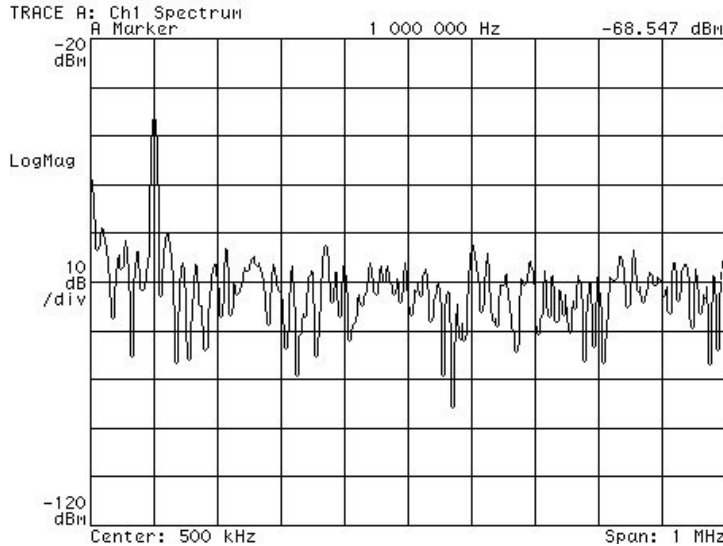
$$\text{dBm} = 10 \cdot \log \frac{\left( \frac{\text{RMS voltage of the input sinewave}}{(\text{Peak voltage amplitude})/\sqrt{2}} \right)^2 / 50\ \Omega}{1\ \text{mW}} = 10 \cdot \log \frac{0.1\ \text{mW}}{1\ \text{mW}} = -10\ \text{dBm} \quad (36.1)$$



**Figure 36.11** Spectrum of the input sinewave.

The spectrum of the amplifier's output is seen in Fig. 36.12. Keeping in mind that we have an attenuation of  $-40$  dB between the amplifier's output and the VSA's input, we can estimate the amplitude of the output as the  $-37$  dBm +  $40$  dB or  $3$  dBm. The gain is then  $13$  dB. This can be converted into a voltage amplitude (of the output sinewave) using

$$3 \text{ dBm} = 10 \cdot \log \frac{V_{outpeak}^2 / (2 \cdot 50)}{1 \text{ mW}} \rightarrow V_{outpeak} = 447 \text{ mV} \quad (36.2)$$



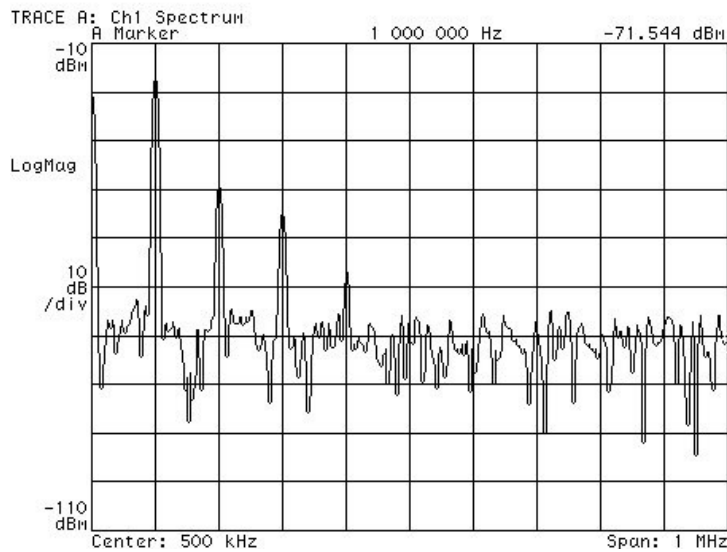
**Figure 36.12** Spectrum of the amplifier's output with the input seen in Fig. 36.11.

Figure 36.13 shows the output spectrum if the amplitude of the input sinewave is increased to  $1$  V. Note the additional tones at multiples of the input frequency. The ideal resulting sinewave peak output amplitude is  $4.47$  V. Clearly this amplitude is well within the bounds of the power supply voltages. However, knowing the MOSFETs in the 4007 can supply only  $1$  to  $2$  mA and that our load is nominally  $5k$  (because of the added attenuating resistor seen in Fig. 36.9), we may run into some loading problems (resulting in the output becoming distorted). Further, we might expect some distortion simply because the amplifier is operating open-loop and, as indicated back in Ch. 22, the large signal gain varies with the input amplitude. Toward characterizing this distortion, we can specify the *total harmonic distortion* (THD), as

$$THD = \sqrt{\frac{a_2^2 + a_3^2 + a_4^2 + \dots + a_n^2}{a_1^2}} \quad (36.3)$$

where  $a_1$  is the amplitude of the fundamental,  $a_2$  is the amplitude of the second harmonic (or the tone at twice the desired frequency),  $a_3$  is the amplitude of the third unwanted tone, etc. The THD is usually specified as a percentage, e.g.,  $0.01\%$ . We can determine the amplitude of the tones from the plot, neglecting the division by  $1$  mW (making the





**Figure 36.13** Output spectrum showing distortion when the input amplitude is increased to 1 V.

actual units dBm) because of the ratio in Eq. (36.3), as  $-18 \text{ dB} = 10 \cdot \log a_1^2$  or  $a_1^2 = 0.0159$ , assuming the second harmonic's amplitude is  $-40 \text{ dB}$   $a_2^2 = 0.0001$ , assuming the third harmonic's amplitude is  $-45 \text{ dB}$ , then  $a_3^2 = 0.0000316$ , and finally the fourth harmonic's amplitude is approximately  $2 \times 10^{-6}$ . The THD can then be calculated as

$$\text{THD} = \sqrt{\frac{0.1 + 0.0316 + 0.002}{15.9}} \rightarrow \text{THD} = 9.1\%$$

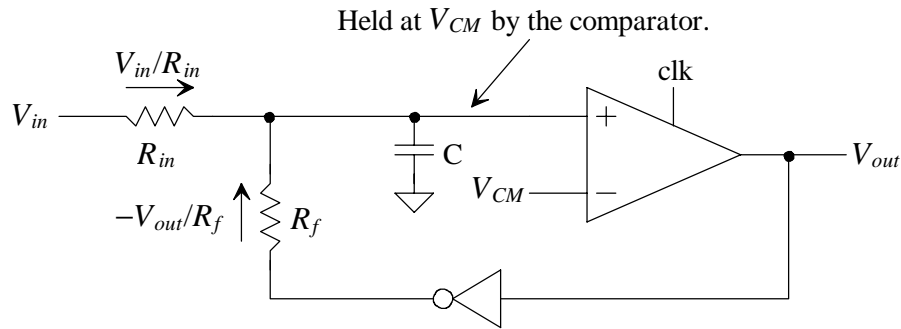
a large value (indicating that this isn't a good, low distortion, amplifier topology by itself).

## 36.2 A First-Order Noise-Shaping Modulator

Let's show how we can implement a simple noise-shaping modulator using a comparator, a capacitor, and a couple of resistors, Fig. 36.14. This type of modulator can be built using discrete components because we can precisely set the values of the resistors and capacitor. This topology may also find use in clever integrated versions of lower SNR NS data converters. When the circuit is operating correctly, the comparator holds its inverting input (the voltage across the integrating capacitor) at ground. Remembering from Ch. 32 that the forward gain of the modulator must be unity, we see that, because the gain of the integrator is much less than one over a significant portion of its operating frequency range, the performance of the comparator becomes very important. In order for the comparator to hold the voltage across the capacitor to a constant value, its gain must be very large. In the following analysis we assume infinite comparator gain, so the voltage across the capacitor is forced to zero by the feedback loop.

The input current (the input signal) can be written as

$$I_{in} = V_{in}/R_{in} \quad (36.4)$$



**Figure 36.14** A passive-integrator NS modulator.

while the feedback current can be written as

$$I_f = V_{out}/R_f \quad (36.5)$$

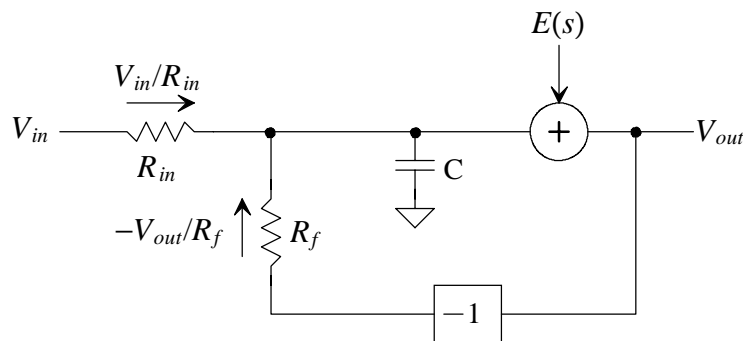
Note that we have not included the common-mode voltage,  $V_{CM}$ , in Eqs. (36.4) and (36.5). If the output of the comparator is 5 V (a logic 1) or 0 V (a logic 0), then the common-mode voltage is 2.5 V. Also note, as we'll show in a moment, the input signal amplitude can be scaled by adjusting the ratio of  $R_{in}/R_f$ .

Consider the block diagram of the modulator of Fig. 36.14 shown in Fig. 36.15. The comparator has been represented, as in Chs. 31 and 32, as a noisy circuit block. For example, assuming the inverting input of the comparator is precisely at 2.5 V and the noninverting input is at 2.6 V, the output of the comparator is 5 V and the quantization noise added to the signal,  $E(s)$  (for this particular input sample), is 2.4 V. We can write

$$\left( \frac{V_{in}}{R_{in}} - \frac{V_{out}}{R_f} \right) \cdot \frac{1}{sC} + E(s) = V_{out} \quad (36.6)$$

After some manipulation, we can write

$$V_{out} = V_{in} \cdot \frac{R_f/R_{in}}{1 + sR_fC} + E(s) \cdot \frac{sR_fC}{1 + sR_fC} \quad (36.7)$$

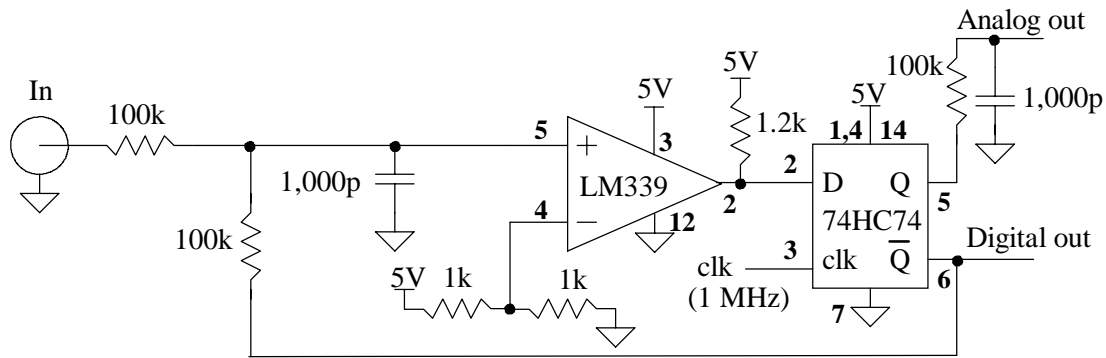


**Figure 36.15** Block diagram of a passive-integrator NS modulator.

The desired signal is lowpass filtered, while the quantization noise is, again, highpass filtered (resulting in the modulation noise). Again, assuming the comparator gain is infinite, passing the output of the modulator through a digital filter with a bandwidth less than  $1/2\pi R_f C$  results in a digital replica of the analog input signal. The practical problems with this topology are the importance of the comparator's gain and the kickback noise injected into the input signal when the comparator switches states.

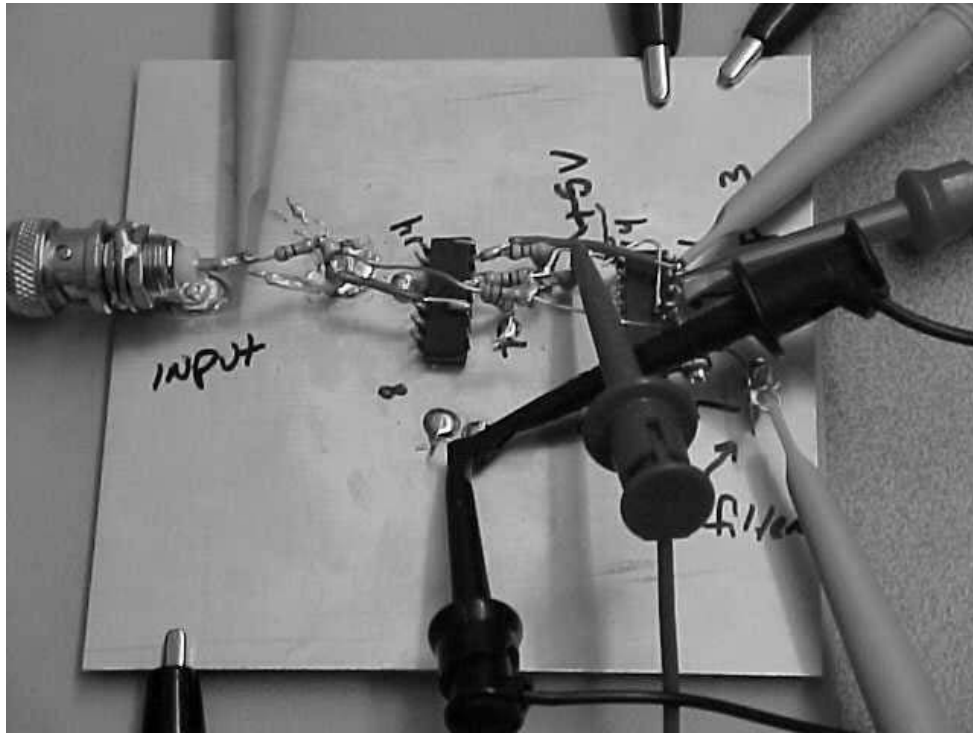
### *Prototyping the Modulator*

Figure 36.16 shows the schematic of the prototype modulator. The D flip-flop was added to make the LM339 comparator appear as though it were a clocked comparator. Also, the 74HC74 is implemented using CMOS and so its outputs swing all the way down to ground and up to +5 V. This is important when we use its output as the fed-back signal in our modulator. The resistors and capacitor on the input of the modulator form a lowpass filter (as seen in Eq. [36.7]) with a time constant of 100  $\mu$ s. The 3 dB frequency associated with this circuit is then 1.59 kHz. Input signal frequencies above this value will experience an attenuation. Figure 36.17 shows the deadbug prototype of the modulator.

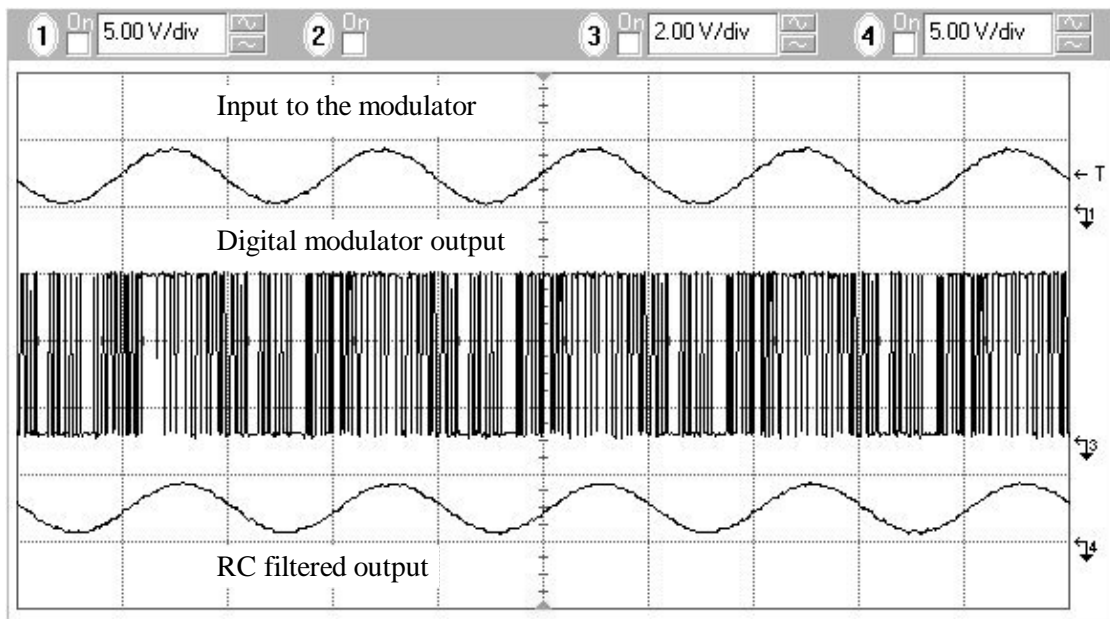


**Figure 36.16** Schematic of the passive-integrator NS modulator.

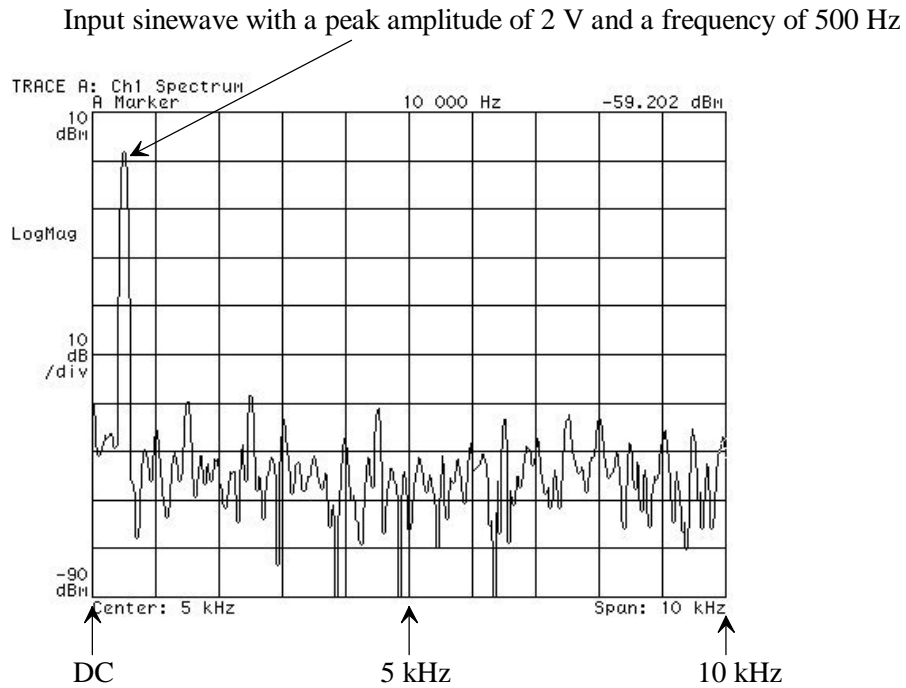
The input to the modulator used to generate some test results, see Fig. 36.18, is a 4 V peak-to-peak sinewave at a frequency of 500 Hz centered around 2.5 V. The digital modulator output is shown in this figure as well. Looking at this digital data alone is somewhat meaningless using the oscilloscope (and so we'll look at the spectrum of this data). Figure 36.19 shows the spectrum of the digital data. A 3-foot coaxial cable is connected between the digital output in Fig. 36.16 and the VSA (with a 1 MEG input resistance so the loading will affect signal frequencies greater than roughly 100 kHz). Figure 36.20 shows the spectrum of the modulator's output up to 200 kHz. Note how, as seen back in Fig. 32.15, the modulation noise increases with increasing frequency. The resolution of the measurement, in Fig. 36.20, is 25 kHz. This causes the desired signal at 500 Hz to appear as though it were occurring at DC. Finally, the bottom trace in Fig. 36.18 shows what happens if we pass the digital data output from the modulator through an RC lowpass filter with a 3-dB frequency of 1.59 kHz. As expected, the resulting analog output is a very close replica of the input signal.



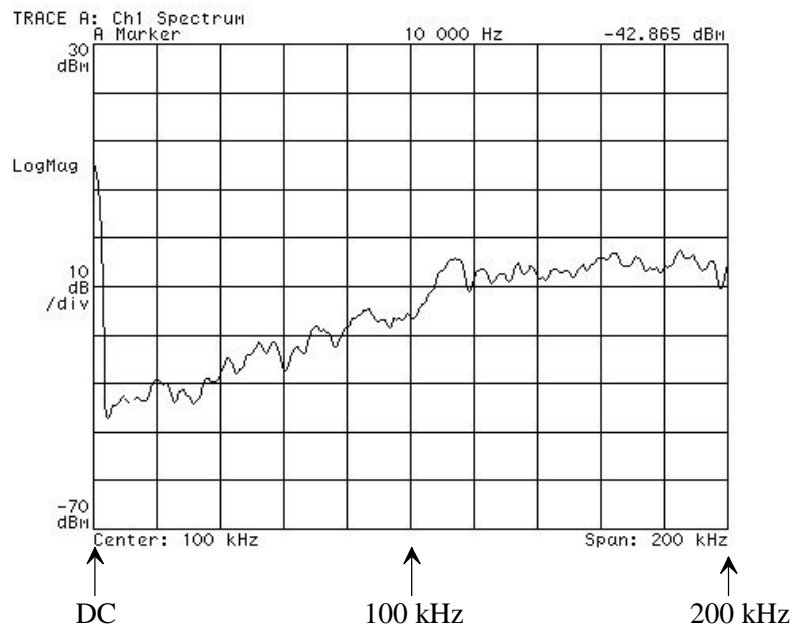
**Figure 36.17** The prototype of the passive noise-shaping modulator of Fig. 36.16.



**Figure 36.18** The outputs of the circuit in Fig. 36.16.



**Figure 36.19** The base spectrum of the modulator's output data.



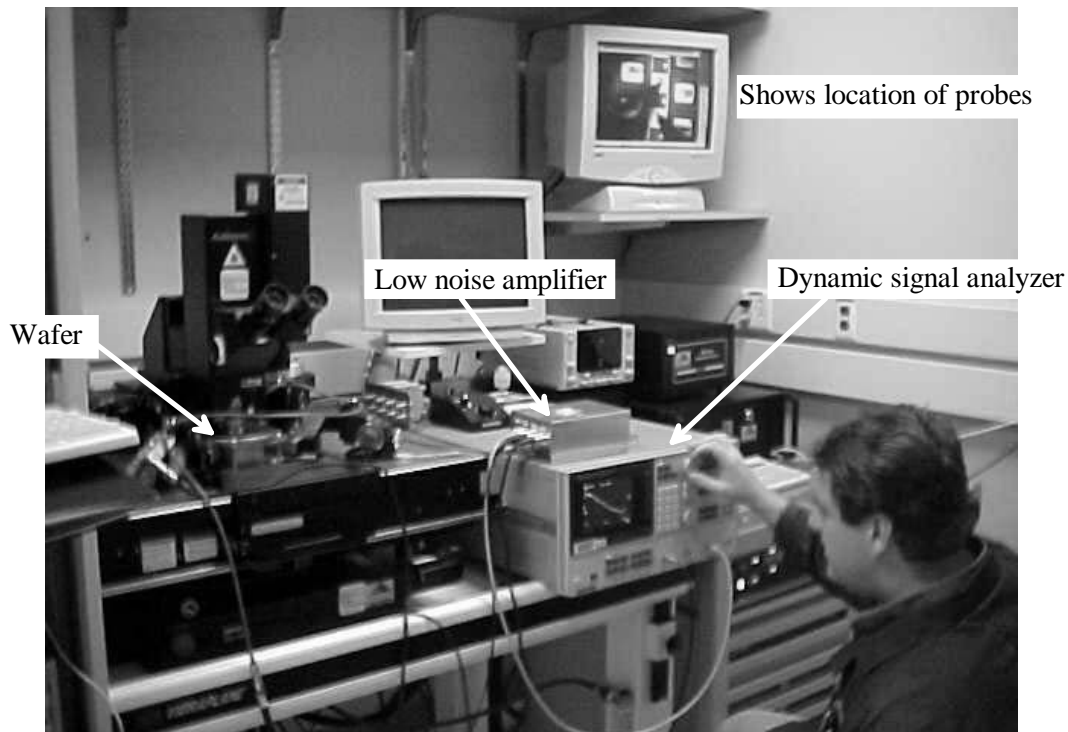
**Figure 36.20** The spectrum of the modulator's output data up to 200 kHz. Resolution bandwidth is 2.5 kHz (and so our input signal is smearing with DC).

### 36.3 Measuring $1/f$ Noise

Circuit noise was reviewed back in Sec. 33.3.3. In that section we showed that averaging thermal noise can be used to increase the SNR. Averaging, as seen in Chs. 30 and 31, can be thought of as lowpass filtering (and thus reducing the bandwidth of the signal and noise). We might wonder if averaging Flicker ( $1/f$ ) noise results in a reduction of the circuit's input-referred RMS noise voltage. We'll show in this section that averaging a wideband signal has little effect on the input-referred contributions from  $1/f$  noise.

Figure 33.85 showed the basic setup to measure  $1/f$  noise. Figure 36.21 shows a lab setup used to measure the  $1/f$  noise present in a submicron MOSFET. Because these devices aren't packaged, we need to use a probe station to pipe the bias signal on to the wafer and the noise signal off of the wafer.

The low-noise amplifier (LNA) shown in Fig. 36.21 is housed in a shielded box to avoid pickup of stray electromagnetic interference. Remembering that the LNA must both amplify the MOSFET's noise and bias the MOSFET to a specific operating point, we can sketch a possible LNA implementation, Fig. 36.22. The circuit is powered with 9 V batteries to avoid the possibility of regular bench power supplies injecting noise into the circuit and thus corrupting the measurement. The low-noise op-amp used, the OP-37, is configured in a gain of 100 configuration. A potentiometer is used to trim out the offset voltage of the op-amp. To see the basic op-amp's noise characteristics (without the



**Figure 36.21** A lab setup used to measure Flicker noise.

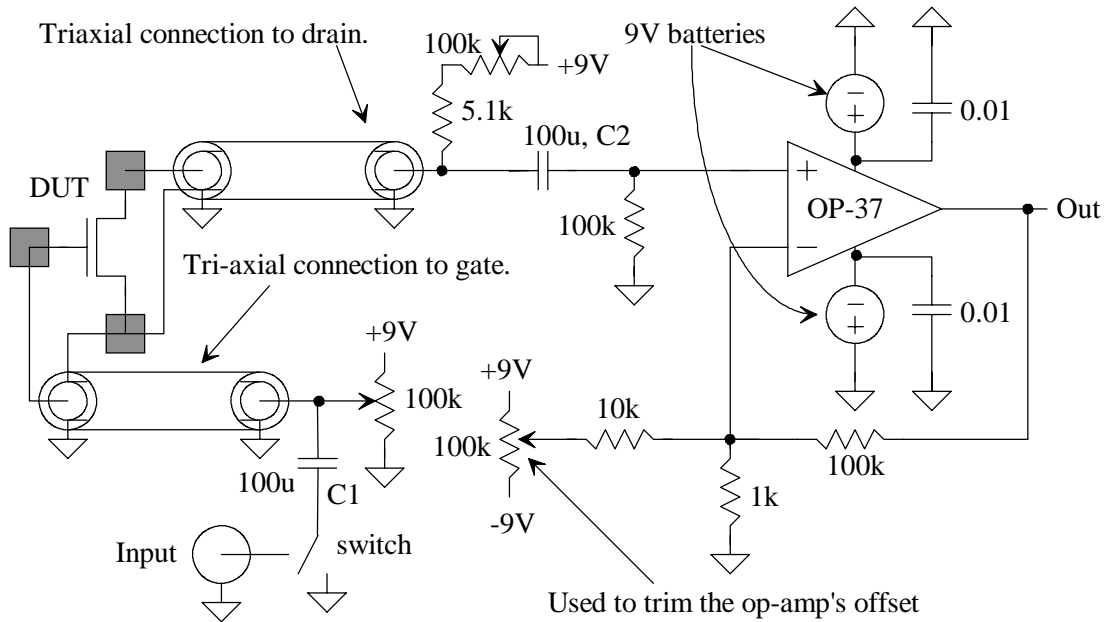


Figure 36.22 Schematic of an LNA.

MOSFETs connected), we simply remove C2 and connect the output to the spectrum analyzer (dynamic signal analyzer). The resulting spectrum is seen in Fig. 36.23. Note that the output spectral noise density of the LNA is roughly  $-80 \text{ dBV}/\sqrt{\text{Hz}}$  ( $100 \mu\text{V}/\sqrt{\text{Hz}}$ ) at 1 Hz (dividing this by the op-amp's gain of 100 results in  $1 \mu\text{V}/\sqrt{\text{Hz}}$  at the MOSFET's drain). In the following, we ignore the LNA's contribution (to simplify the discussion).

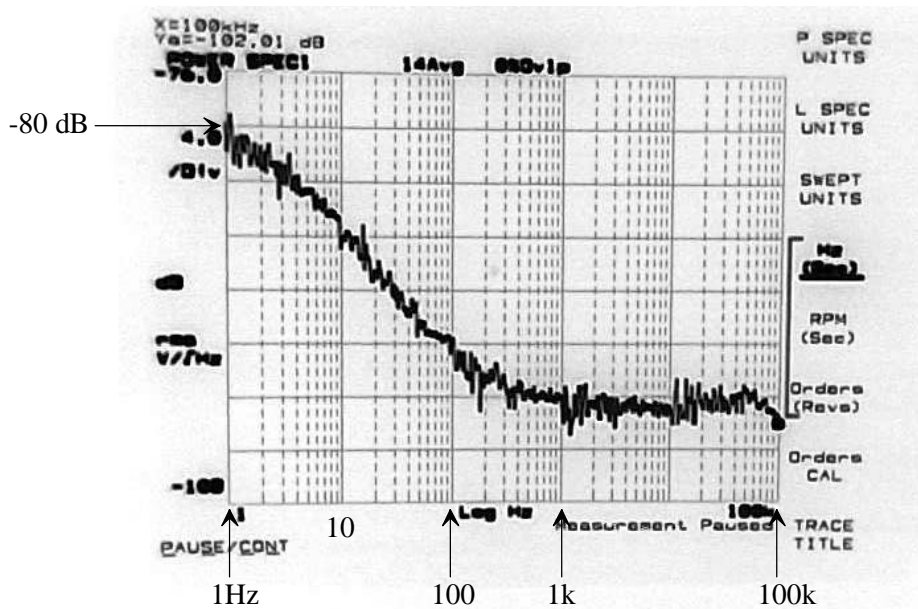


Figure 36.23 Measured noise characteristics of an LNA using the OP-37.

*MOSFET Noise*

Figure 36.24 shows the noise spectrum when we put C2 back in the circuit, bias the MOSFET at a specific operating point, and connect C1 to ground. The spectral density at 1 kHz is roughly  $-70 \text{ dBV}/\sqrt{\text{Hz}}$  or

$$-70 \text{ dBV}/\sqrt{\text{Hz}} = 316 \mu\text{V}/\sqrt{\text{Hz}} \text{ at } 1 \text{ kHz} \quad (36.8)$$

or, calculating the  $1/f$  spectral density (see Ch. 9)

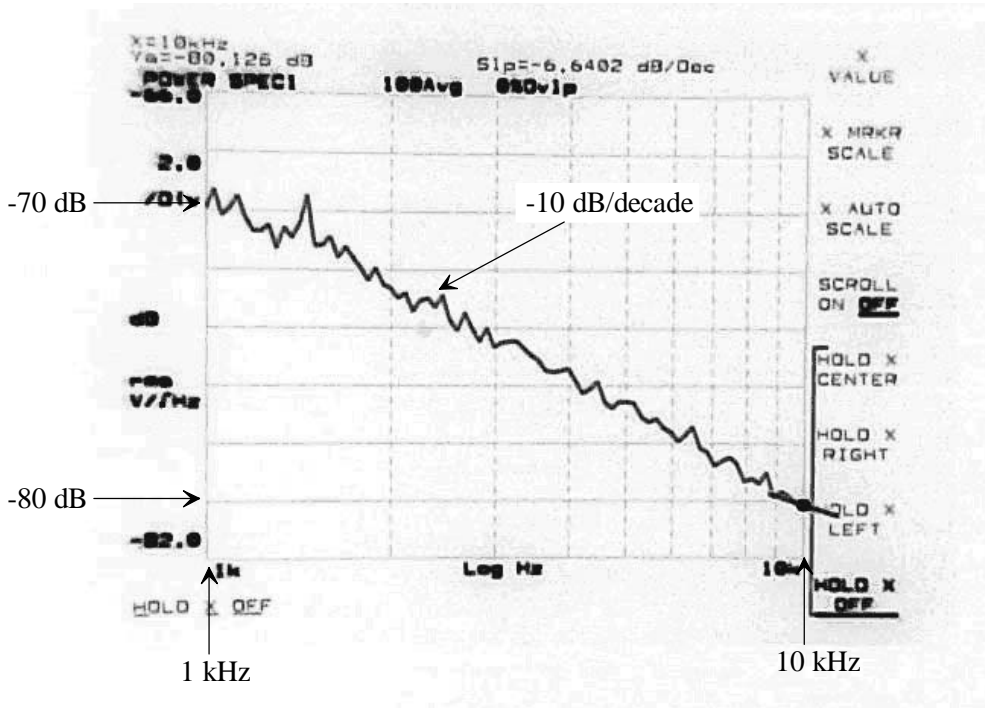
$$\overline{v_{1/f,out}^2} = \left( \frac{316 \mu\text{V}}{\sqrt{\text{Hz}}} \right)^2 = \frac{100 \times 10^{-9} \text{V}^2}{\text{Hz}} = \frac{\text{Flicker noise numerator (FNN)}}{1 \text{ kHz}} = \frac{\overbrace{100 \text{ pV}^2}^{\text{FNN}}}{f} \quad (36.9)$$

As a quick check, the spectral density of the noise at 10 kHz can be calculated as

$$\overline{v_{1/f,out}^2} = \frac{100 \text{ pV}^2}{10 \text{ kHz}} = \frac{10 \text{ nV}^2}{\text{Hz}} \rightarrow \sqrt{\overline{v_{1/f,out}^2}} = \frac{100 \mu\text{V}}{\sqrt{\text{Hz}}} = -80 \text{ dBV}/\sqrt{\text{Hz}} \quad (36.10)$$

which is what we see at 10 kHz in Fig. 36.24. (To determine the MOSFET's output noise spectral density alone we divide the spectral density in Fig. 36.24 by the LNA's gain of 100.) To determine the RMS output noise, we can integrate the  $1/f$  noise spectral density

$$\sqrt{v_{on}^2} = \left[ \int_{f_L}^{f_H} \overline{v_{1/f,out}^2} \cdot df \right]^{1/2} = \left[ \text{FNN} \cdot \ln \frac{f_H}{f_L} \right]^{1/2} \quad (36.11)$$



**Figure 36.24** Measured Flicker noise from the MOSFET/LNA in Fig. 36.22.



This equation is fundamentally important to understand our statement at the beginning of the section, that is, averaging a wideband signal will have little effect on the contributions from  $1/f$  noise to the input-referred or output RMS noise voltages. If we select the largest frequency,  $f_H$ , as 10 GHz ( $10^{10}$  Hz) and the lowest frequency as 1 Hz (once per second), then the natural log term in Eq. (36.11) is 23. However, if we change the lowest frequency of interest to  $10^{-10}$  Hz (roughly once every 320 years), the natural log term increases to only 46! So to get a quick-and-dirty estimate of the contribution of  $1/f$  noise to an output RMS noise voltage, we simply use

$$\text{contributions from } 1/f \text{ noise to RMS output voltage} = 7 \cdot \sqrt{\text{FNN}} \quad (36.12)$$

(knowing, of course, we can only add mean squared noise voltages). So, for the noise spectrum in Fig. 36.24, we can estimate the RMS output noise contributions as

$$\sqrt{v_{on}^2} = 7 \cdot \sqrt{100 \times 10^{-12} \text{ V}^2} = 70 \mu\text{V} \quad (36.13)$$

Again, this approximation is useful for wideband estimates of the RMS noise due to Flicker noise. It's not useful if a narrow bandpass filter is used on the output of a circuit where  $f_H$  and  $f_L$  are well defined.

#### *Input-Referred Noise Voltage*

While knowing the output noise is useful, it is generally more useful to refer this noise back to the input of the circuit so that it can be compared with an input signal. Towards this consider, in Fig. 36.22, connecting C1 to the BNC connector instead of ground. We can inject a signal, say a 1 mV sinewave, into the gate of the MOSFET and then look at the output of the circuit. If the overall gain of the circuit is 1,000 ( $= A$ ), then we would see an output sinewave with an amplitude of 1 V. Knowing the gain of the circuit (MOSFET and op-amp), we can determine the input-referred noise by dividing the noise power spectral density with units of  $\text{V}^2/\text{Hz}$ , by  $A^2$  or the noise voltage spectral density (or RMS output voltage) by  $A$ . Rewriting Eq. (36.12) for the input-referred RMS voltage

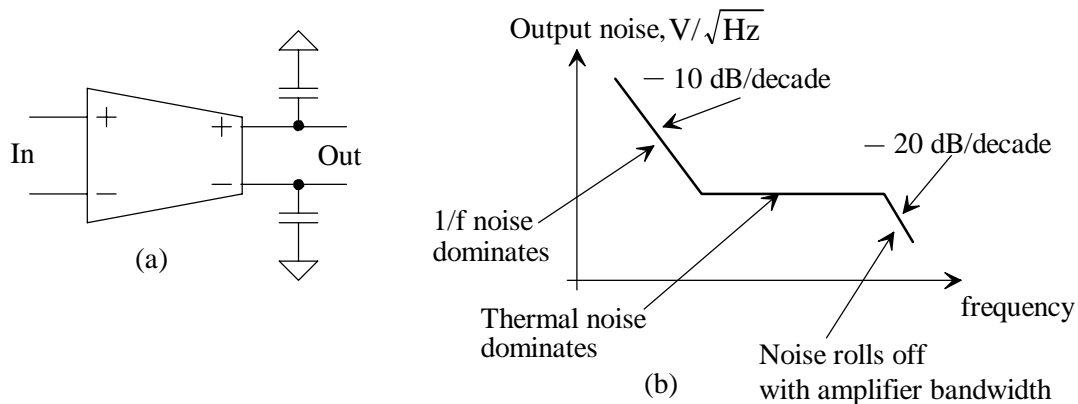
$$\text{Contributions from } 1/f \text{ noise to RMS input-referred voltage} = 7 \cdot \sqrt{\text{FNN}} / A \quad (36.14)$$

An important consideration when measuring the gain of the circuit is the frequency response of the gain. At the high end, the op-amp, in a gain of 100 configuration will have a bandwidth of approximately 10 kHz (assuming a gain bandwidth product of 1 MHz). Also, the MOSFETs have to drive the capacitance of the triax cables, which will result in an upper frequency roll-off in the amplifier's response. At the low end, C1 and C2 must be very large to keep the low-frequency roll-off point from becoming too large. The overall MOSFET/LNA's response has a bandpass shape. The point is that the input sinewave's frequency should be varied in order to find the passband gain of the circuit. Once C1 is grounded, its effect on the low-frequency roll-off is eliminated.

Clearly,  $1/f$  noise can be a significant limiting factor when making sensitive measurements or when trying to attain large SNRs. Because averaging won't provide any help in reducing  $1/f$  noise, let's show one very practical method that will help. While correlated double sampling (CDS) can be used here we discuss chopper stabilization (CHS). See reference [9] in Ch. 33 for additional information.

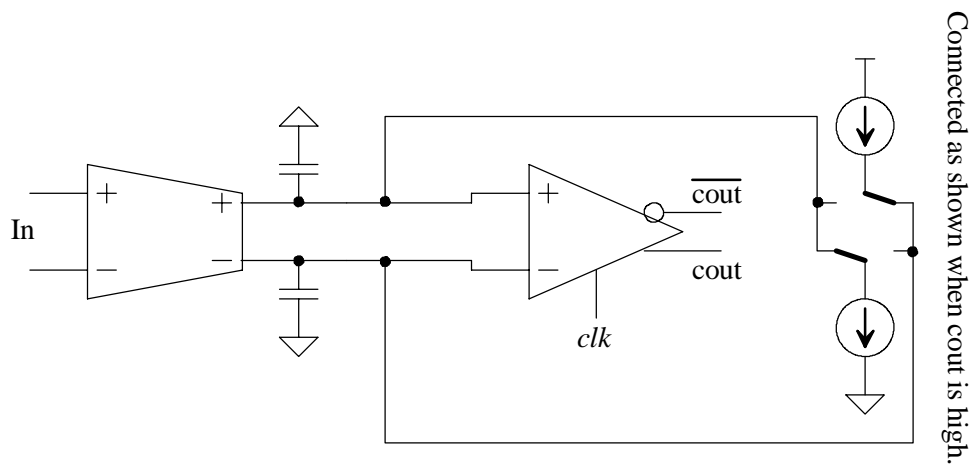
### Chopper Stabilization

Consider the OTA shown in Fig. 36.25a and the associated noise spectral density shown in Fig. 36.25b. This circuit is essentially an integrator. In an ideal integrator, connecting the inputs together and to the common mode voltage would result in the outputs remaining unchanged. However, in a real integrator, the OTA's offset and the  $1/f$  noise results in the outputs of the integrator eventually reaching the supply rails. It would be nice if we didn't have to worry about either the offset or the  $1/f$  noise. What we are going to do in the CHS scheme is modulate the offset and noise to a place in the frequency spectrum where it won't interfere with our desired signal.



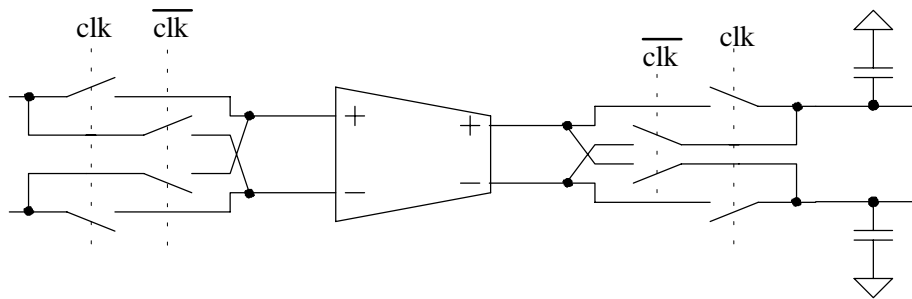
**Figure 36.25** Integrator noise using an OTA.

Toward understanding this last statement consider the first-order noise-shaping modulator shown in Fig. 36.26. This topology is useful when measuring very small signals. It is very power-supply insensitive because of the current sources used. The noise and



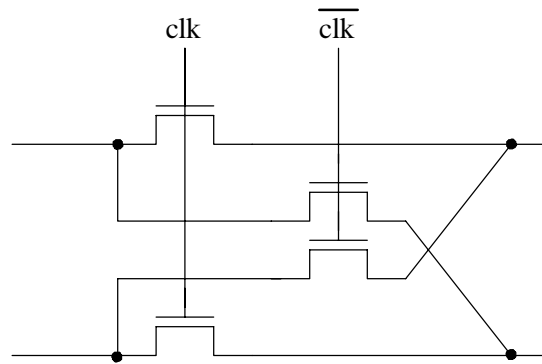
**Figure 36.26** A first-order noise-shaping modulator using an OTA integrator.

offsets contributed by the OTA will directly affect the input sensitivity. Consider what would happen if we chopped (or switched back-and-forth) the input/output terminals of the OTA as seen in Fig. 36.27. When  $clk$  is high, the OTA is connected through switches so that it behaves as seen in Fig. 36.26. The OTA's offset, for example, causes a current to charge/discharge the capacitors. When  $clk$  is low, both the input and output terminals are switched so that the gain of the amplifier remains the same polarity. The offset now causes a current to flow in the capacitors in the opposite direction from the flow when  $clk$  was high. This effectively, if the rate at which we switch back-and-forth is fast, results in net zero current flow into the capacitors. A similar argument can be made for the low-frequency  $1/f$  noise. The chopping, or switching, reduces both the offset and the Flicker noise on the output of the integrator (and so the input-referred noise is decreased as well).



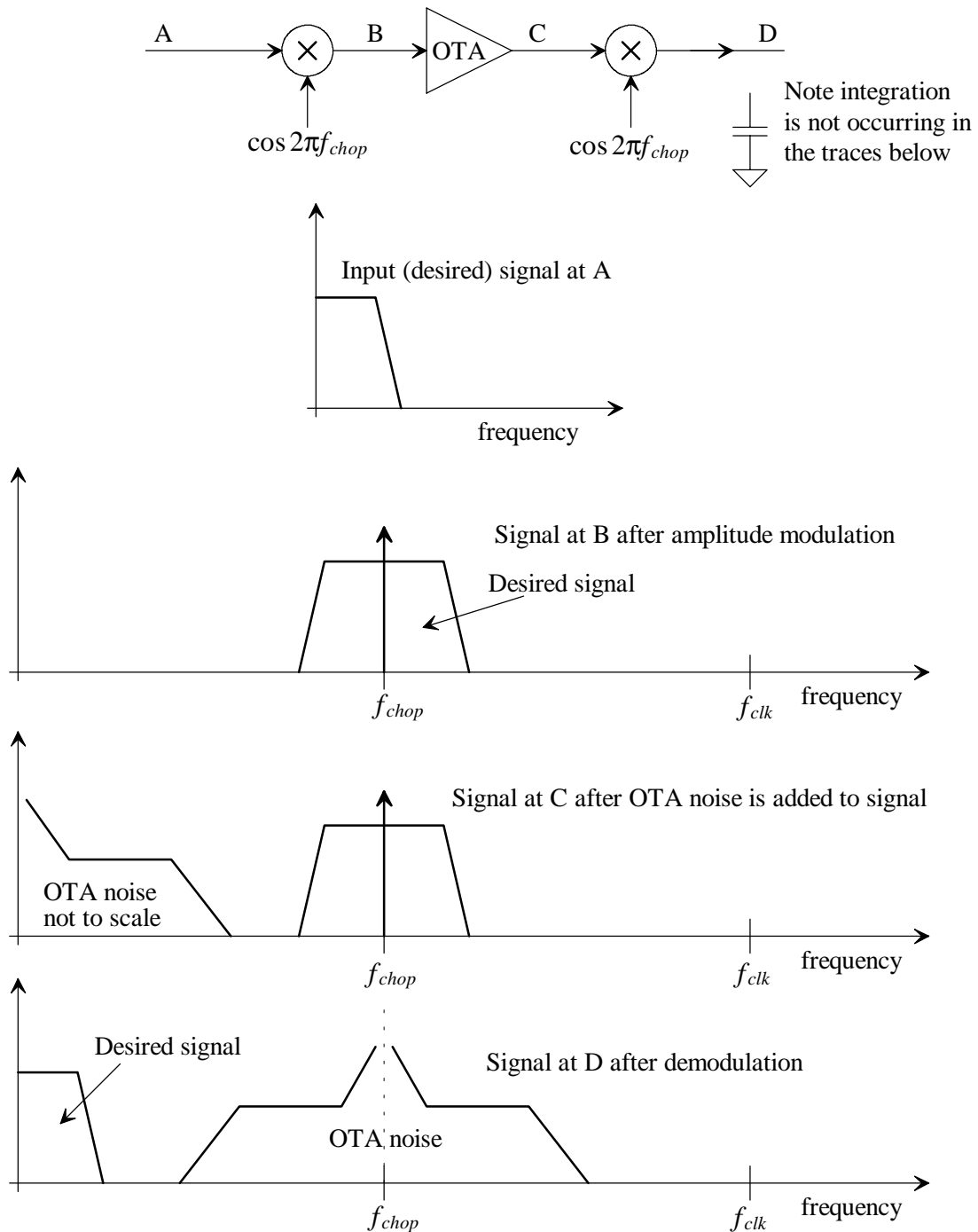
**Figure 36.27** Switching (chopping) the inputs and outputs of the OTA integrator.

Figure 36.28 shows a possible implementation of the chopping switches. This should look familiar from Ch. 26. It was used to implement a multiplier. Here we are also using it for a multiplication. We are multiplying our OTA's input signal by  $+1$  or  $-1$  while doing the same to the OTA's output signal in order to maintain the same gain polarity. If the frequency we chop at is labeled  $f_{chop}$ , then we are multiplying the input by a square wave with this frequency. Looking at only the first harmonic of the waveform, we see this is simply amplitude modulation.



**Figure 36.28** Showing a possible implementation of the chopping switches.

Consider the block diagram of the chopper and OTA of Fig. 36.27 shown in Fig. 36.29. Here we set the chopping frequency to one-half of the clock frequency (the clock used to strobe the comparator in the noise-shaping modulator of Fig. 36.26). We do this so that no aliasing occurs in our signal of interest from sampling the D signal at  $f_{clk}$  (the OTA noise doesn't fold into the signal of interest after sampling). If the settling time, when



**Figure 36.29** How chopping affects the noise and signal in an OTA.

chopping at  $f_{chop}$ , of the amplifier is longer than  $2/f_{chop}$ , then a lower chopping frequency can be used (ultimately set by the integrator's bandwidth). For example, if we are clocking the NS modulator of Fig. 36.26 at 100 MHz, then we might chop the OTA's input/output at a rate of 12.5 MHz (divide the NS modulator's clock by eight using a cascade of three of the circuits in Fig. 33.46).

In a second-order noise-shaping modulator the input-referred noise is mainly due to the first integrator as discussed in Ch. 32. The input-referred  $1/f$  noise is passed directly to the output of the modulator. Modulators that use an autozeroed integrator don't have this problem because the autozeroing operation removes both the offset at DC and attenuates the  $1/f$  noise spectral density. Looking at the power spectral density of  $1/f$  noise on the output of an integrator, when not used in a modulator with feedback, results in a  $1/f^3$  spectral shape. Averaging this noise results in linear growth with averaging time.

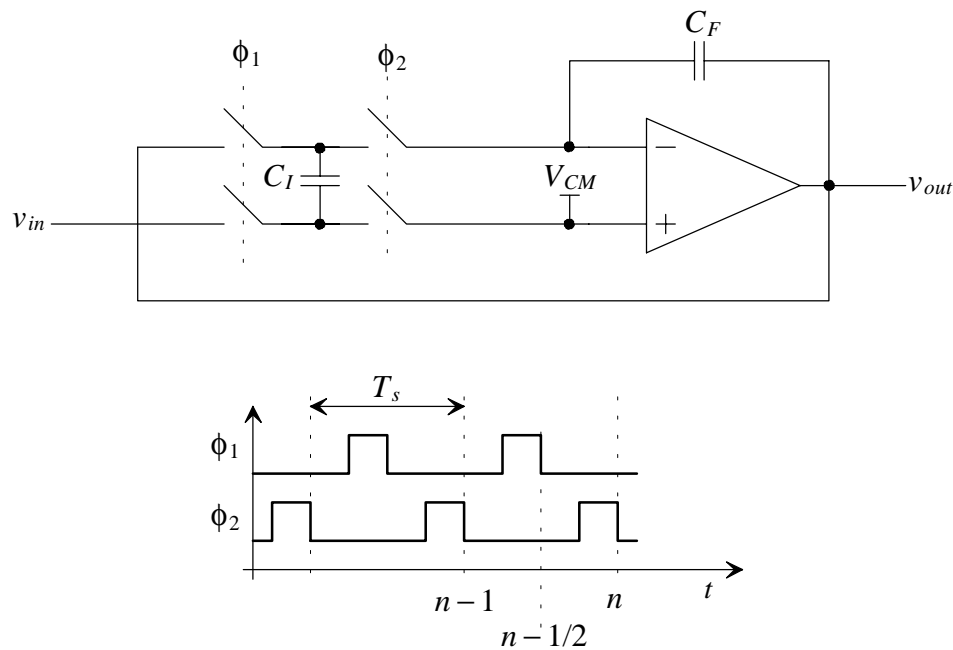
### 36.4 A Discrete Analog Integrator

Let's build a DAI-based first-order lowpass filter. Figure 36.30 shows the circuit (see Fig. 35.22). The charge stored on  $C_I$  when the  $\phi_1$  switches are closed is given by

$$Q_1 = C_I(v_{in}[(n-1/2)T_s] - v_{out}[(n-1)T_s]) \quad (36.15)$$

When the  $\phi_2$  switches close, this charge is transferred to the feedback capacitor,  $C_F$ ,

$$Q_1 = C_F(v_{out}[(n)T_s] - v_{out}[(n-1)T_s]) \quad (36.16)$$



**Figure 36.30** A first-order filter made using a DAI.

Taking the z-transform of this equation results in

$$C_I(V_{in}(z) \cdot z^{-1/2} - V_{out}(z) \cdot z^{-1}) = C_F(V_{out}(z) - V_{out}(z) \cdot z^{-1}) \quad (36.17)$$

$$C_I \cdot V_{in}(z) \cdot z^{-1/2} = V_{out}(z) \cdot (C_F - C_F \cdot z^{-1} + C_I \cdot z^{-1}) \quad (36.18)$$

or

$$\frac{V_{out}(z)}{V_{in}(z)} = \frac{z^{1/2}}{\frac{C_F}{C_I} \cdot z - \frac{C_F}{C_I} + 1} \quad (36.19)$$

noting the  $z^{1/2}$  term in the numerator is simply a phase shift (a time delay), which will be neglected as long as our input frequencies,  $f$ , are much less than the filter's clocking frequency,  $f_s$ . Remembering from Eq. (35.69) that

$$z \approx 1 + \frac{s}{f_s} \text{ when } f \ll f_s \quad (36.20)$$

we can rewrite Eq. (36.19) as

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{1 + sR_{sc}C_F} \quad (36.21)$$

where

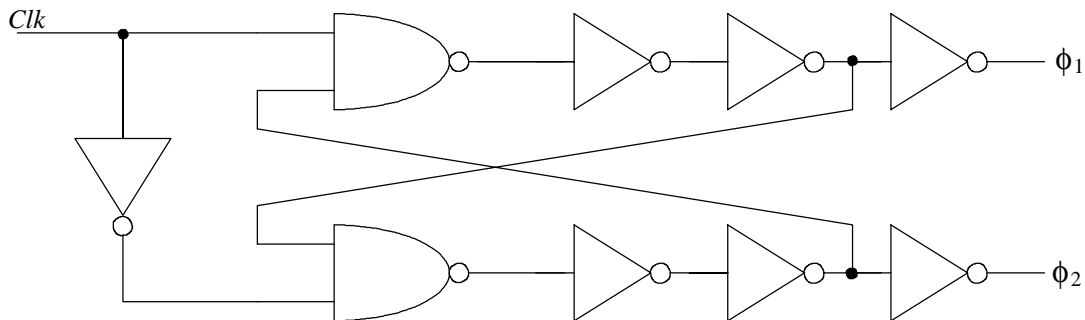
$$R_{sc} = \frac{1}{f_s C_I} \quad (36.22)$$

The filter's 3-dB frequency is located at

$$f_{3dB} = \frac{1}{2\pi R_{sc} C_F} \quad (36.23)$$

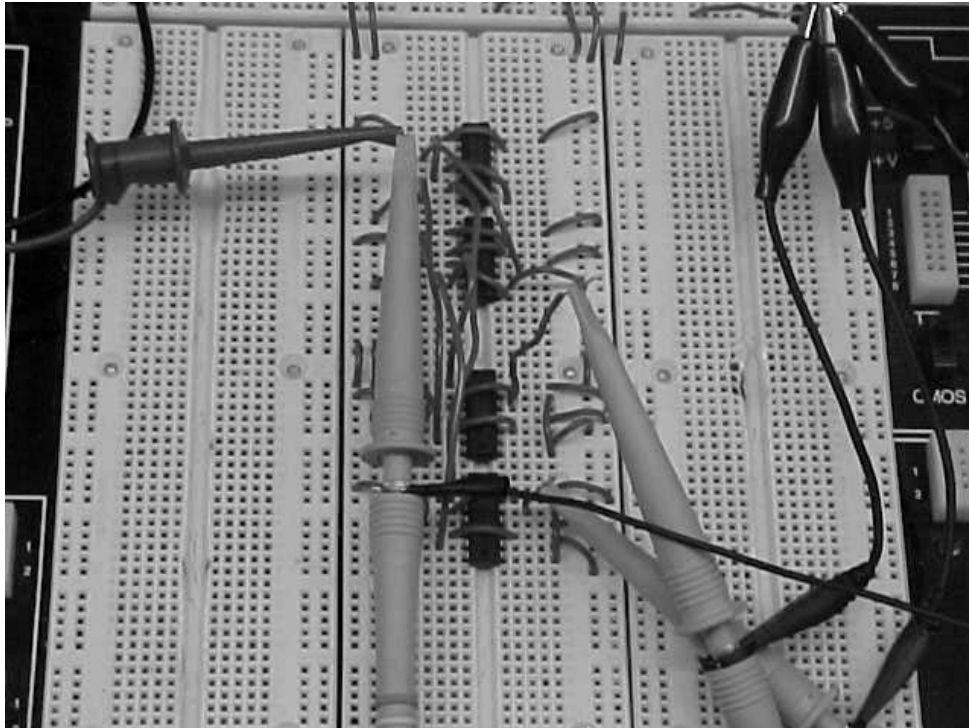
### Clock Generation

The first thing we need to build is the clock generation circuit. Figure 36.31 shows the basic schematic of a nonoverlapping clock generator circuit. We use  $\pm 9$  V supplies. The two phases of the clock should transition between these voltages. We, again, use the 4007



**Figure 36.31** Nonoverlapping clock generation circuit.

CMOS transistors shown in Fig. 36.2 to implement the generator. Further, since this is a purely digital circuit, we breadboard the design (see Fig. 36.32). Figure 36.33 shows the outputs of this generator.



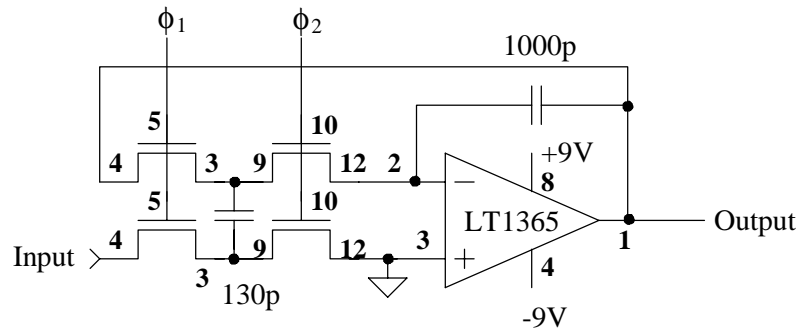
**Figure 36.32** Breadboard of a clock generator.



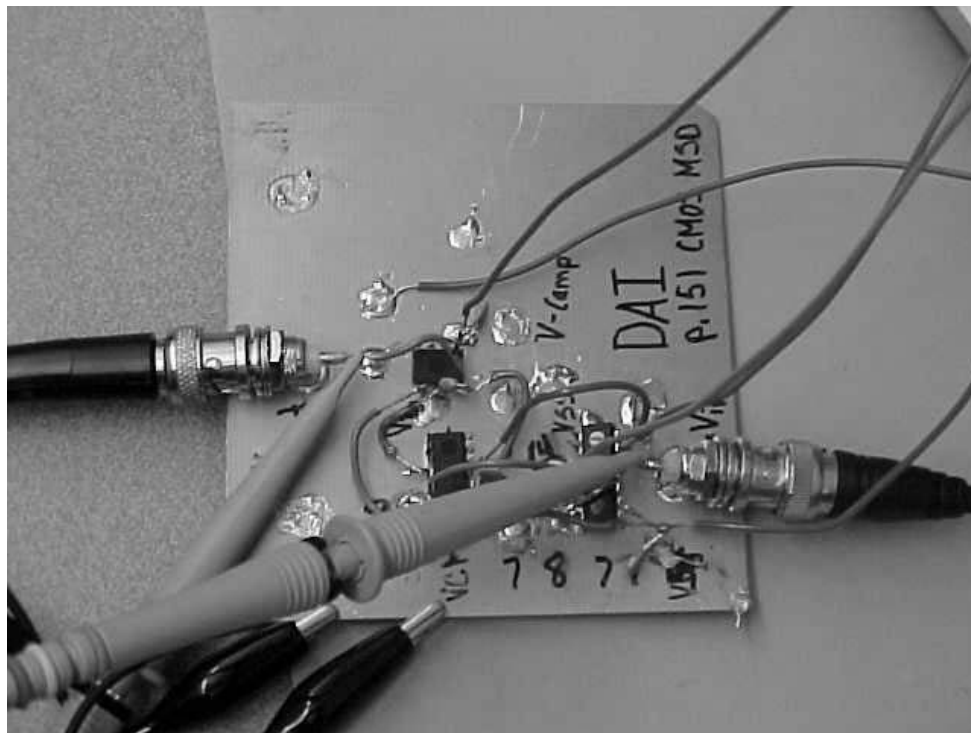
**Figure 36.33** Nonoverlapping clocks.

### Prototyping the Filter

The schematic of our filter is seen in Fig. 36.34. The MOSFET switches are implemented using the 4007. The op-amp is an LT1365. Figure 36.35 shows the deadbug implementation of the filter.



**Figure 36.34** Schematic of the DAI-based filter.

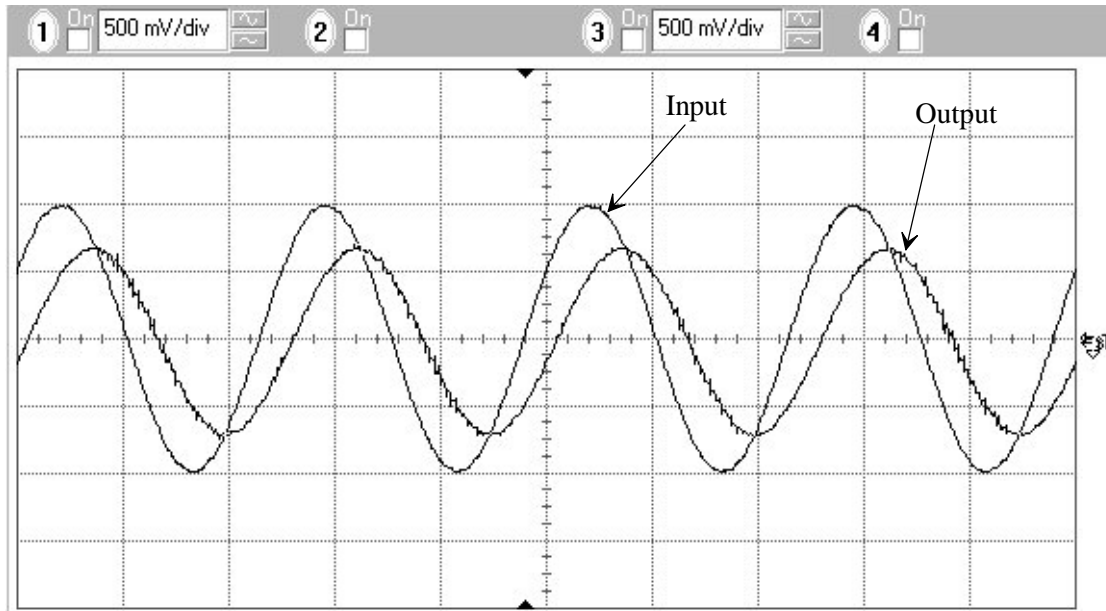


**Figure 36.35** Deadbug prototype of the DAI filter in Fig. 36.34.

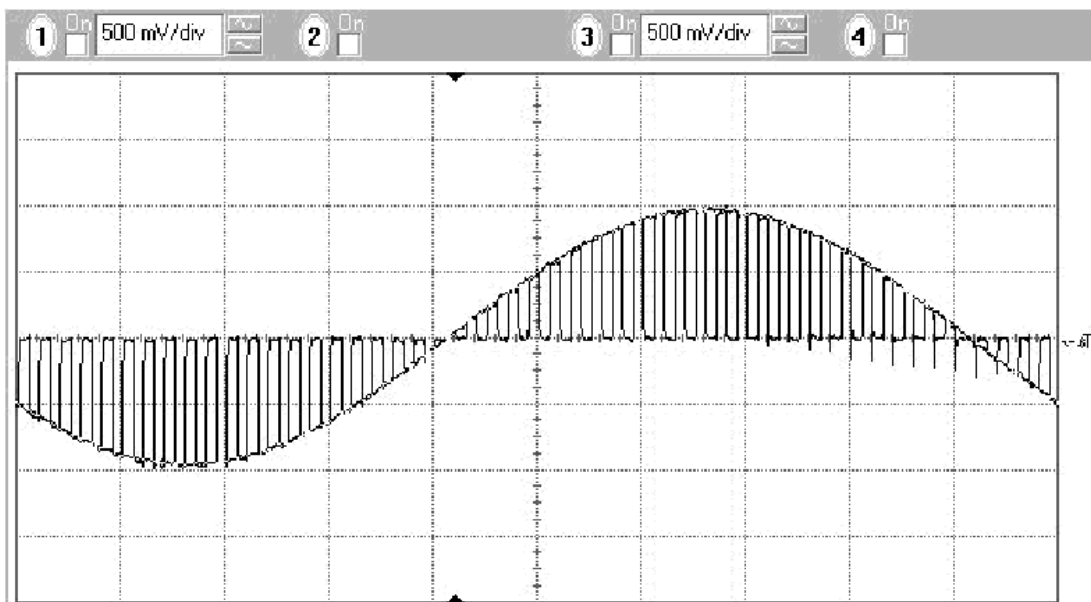
Using Eq. (36.23), we calculate the filter's 3-dB frequency as 2 kHz when the filter is clocked at 100 kHz. Figure 36.36 shows the filter's input and output at this frequency. If



one looks closely at the output signal, the discrete nature is obvious (see the steps in the output waveform shown in the simulation in Fig. 35.23). Figure 36.37 shows how the 130 pF capacitor (the node at the bottom of the schematic) charges to the input signal and then discharges back to ground (making the parasitic capacitance on this node unimportant).

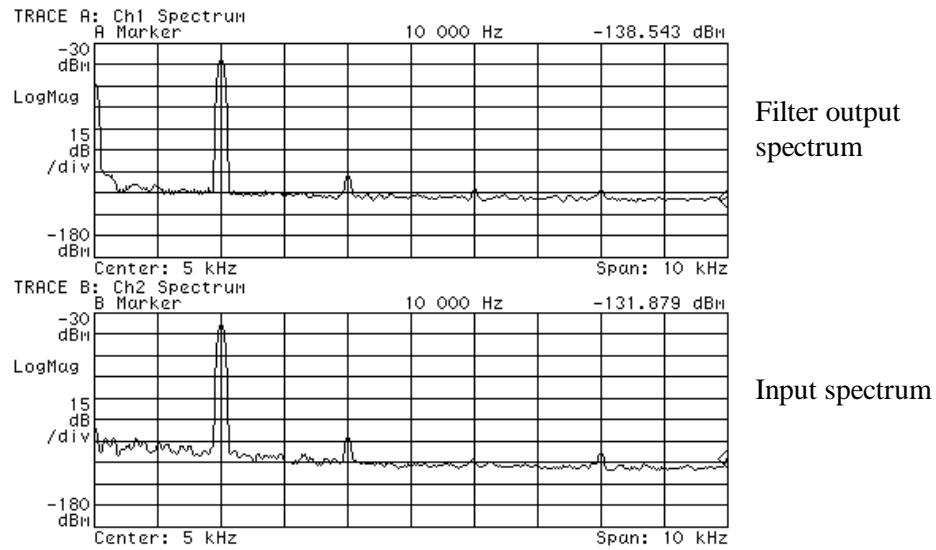


**Figure 36.36** First-order filter's input and output at the 3-dB frequency of 2 kHz.

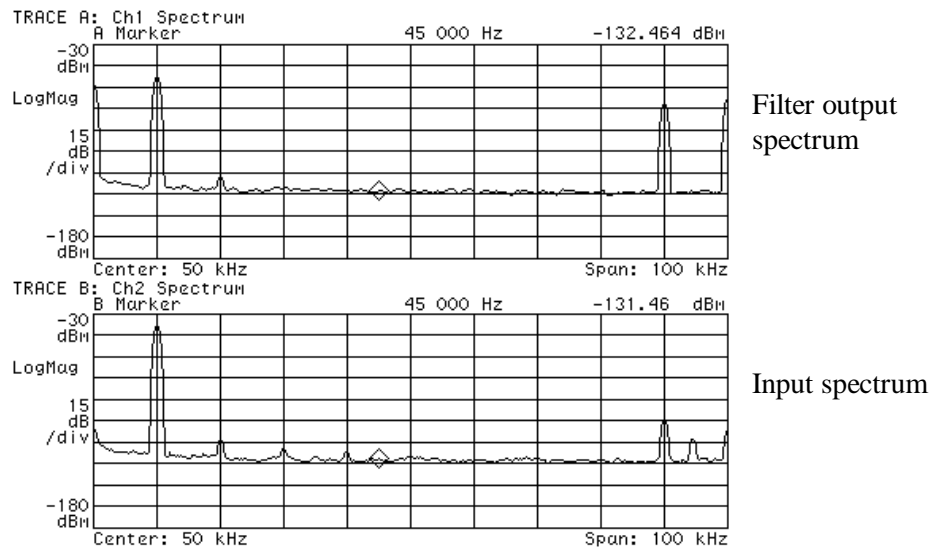


**Figure 36.37** How the 130 pF capacitor charges and discharges.

Before leaving this section, let's show example input/output spectrums for this first-order switched-capacitor filter; Fig. 36.38. The desired signal is at 2 kHz and its peak amplitude has been decreased to 500 mV (to avoid overloading the VSA). The input signal amplitude is then  $10 \cdot \log([(0.5/\sqrt{2})^2/1 \text{ M}\Omega]/1 \text{ mW})$  or  $-39 \text{ dBm}$ . Because we are applying the 3 dB frequency, we expect our output amplitude to be  $-42 \text{ dBm}$  (and it is). Finally, to show that the filter is indeed a sampled circuit, we increase the input frequency to 10 kHz and show the output images around the 100 kHz sampling frequency, Fig. 36.39.



**Figure 36.38** Input and output spectrums for the filter of Fig. 36.34.



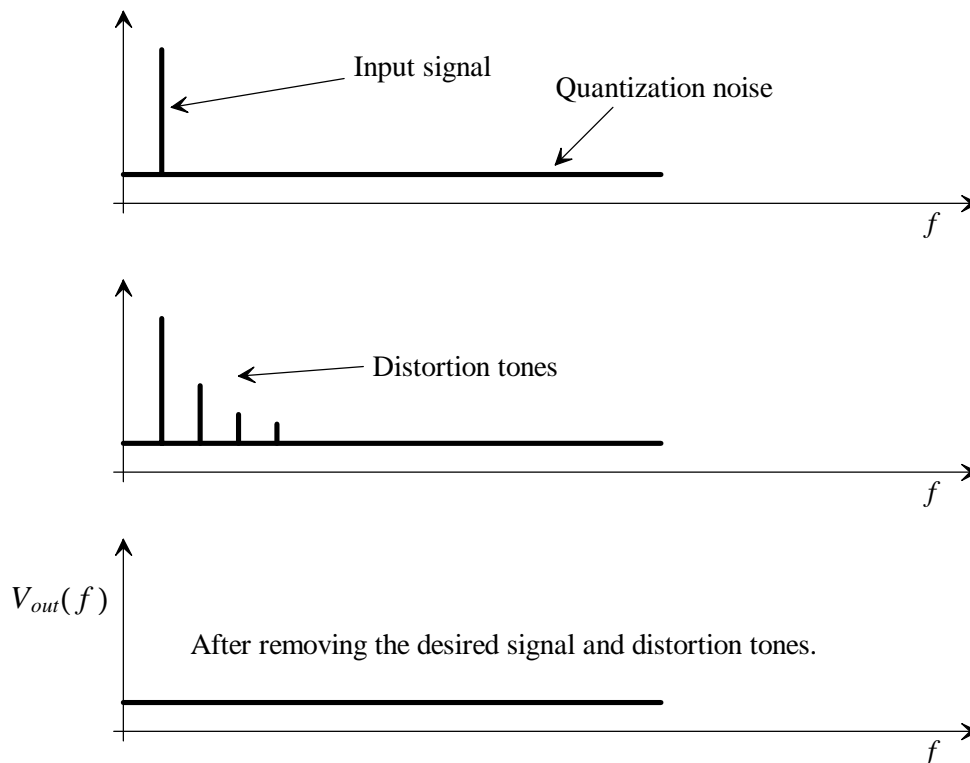
**Figure 36.39** The spectrum up to the clocking frequency (100 kHz).

### 36.5 Quantization Noise

For the last section in this chapter, let's discuss, and show how to calculate, the quantization noise added to a spectrum from a data converter. We showed how to calculate the noise from a simulation spectrum back in Ch. 30; see Eq. (30.33). When presented with a data converter's output spectrum, Fig. 36.40, we can remove the desired signal (and perhaps the distortion if we calculate only the noise in the signal) and calculate the RMS quantization noise (or simply the noise in the spectrum) using

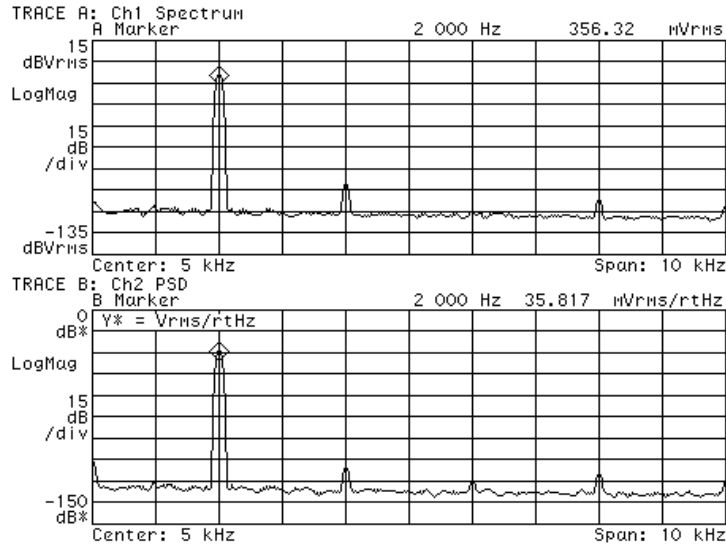
$$V_{Qe,RMS} = \sqrt{\int_{0 \text{ (DC)}}^{f_{\max}} V_{out}^2(f) \cdot df} \quad (36.24)$$

The signal  $V_{out}(f)$  represents the data converter's output spectrum (after removing the desired signal and any distortion spikes) and has units of  $V/\sqrt{\text{Hz}}$ . The maximum frequency we integrate to,  $f_{\max}$ , is generally the Nyquist frequency,  $f_s/2$ . We assume that, when actually using the data converter, a reconstruction filter removes spectral content in the output signal above the Nyquist frequency. In a noise-shaping modulator, a digital filter sets  $f_{\max}$ . Note that we can't accurately calculate the quantization noise added to an input signal unless the input to the data converter is busy. A sinewave of sufficiently large amplitude can be used to exercise the data converter and "whiten" the quantization noise.



**Figure 36.40** The output spectrum of a data converter.

Before going any further, let's show some example spectrums and the corresponding y-axis units. The top waveform in Fig. 36.41 shows the resulting spectrum when the input to the VSA is a 0.5 V (peak) waveform at 2 kHz. The RMS value of this waveform is 354 mV. In dBm (using a 1 M $\Omega$  VSA input resistance) this is  $10 \cdot \log \left[ \left[ (0.354)^2 / 1 \text{ M}\Omega \right] / 1 \text{ mW} \right]$  or  $-39 \text{ dBm}$ ; see the top trace in Fig. 36.42. The units for the top trace in Fig. 36.41 are volts, root-mean-square. Many of the spectrums we used in earlier chapters used peak voltages for the y-axis units.



**Figure 36.41** The relationship between units in spectral plots.

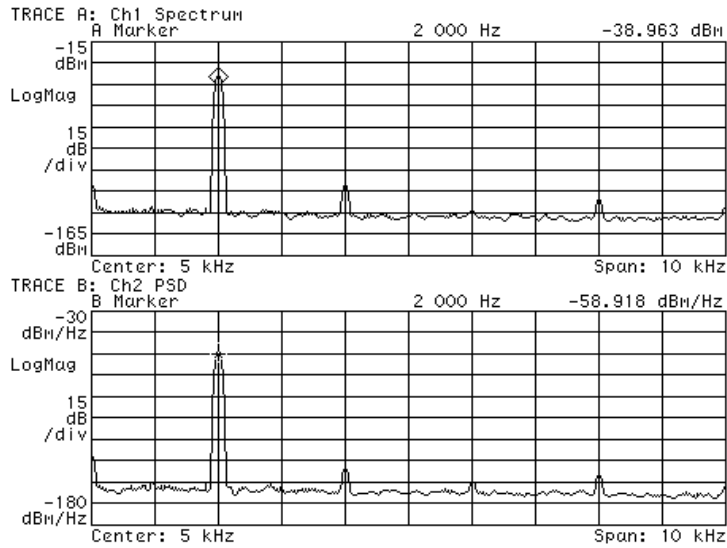
The bottom trace in Fig. 36.41 shows the voltage spectral density of our 0.5 V peak sinewave at 2 kHz. The units of a voltage spectral density are  $\text{V}/\sqrt{\text{Hz}}$  (or more precisely volts RMS per root Hz). Because the same exact waveform is input to the VSA for each spectrum, we can relate the top and bottom waveforms in Fig. 36.41 simply by knowing the resolution bandwidth of the measurement

$$\frac{V_{RMS}}{\sqrt{\text{Hz}}} = \frac{V_{RMS}}{\sqrt{\text{Resolution bandwidth}}} \quad (36.25)$$

The resolution bandwidth used by the VSA, for the waveforms of Fig. 36.41, was 100 Hz. This means the amplitude of the sinewave is now  $354 \text{ mV} / \sqrt{100 \text{ Hz}}$  or  $35.4 \text{ mV} / \sqrt{\text{Hz}}$ . In dB this would be  $20 \cdot \log 0.0354$  or  $-29 \text{ dB}$ . For a power spectral density, see the bottom trace in Fig. 36.42, we can use

$$\frac{\text{V}^2(\text{or Watts})}{\text{Hz}} = \frac{\text{V}^2(\text{or Watts})}{\text{Resolution bandwidth}} \quad (36.26)$$

Because our resolution bandwidth is 100 Hz, we expect the power spectral density to be 20 dB less than the power spectrum (top trace in Fig. 36.42) or  $-59 \text{ dBm/Hz}$ . It should be obvious how to change from  $\text{dBm/Hz}$  to  $\text{V}^2/\text{Hz}$ .



**Figure 36.42** Power spectral density of the spectrums in Fig. 36.41.

Given a spectrum with noise (quantization, thermal, Flicker, or whatever), we can now generate the desired spectrum ( $V_{out}[f]$  in Fig. 36.40) for calculating RMS noise. To illustrate how let's use the modulator output spectrum seen in Fig. 36.19. We begin by removing the desired tone in the spectrum (the sinewave at 500 Hz). Next we assume the noise is white (a flat spectrum) and has a value of  $-60$  dBm. Because the VSA's input resistance is 50 ohms and the resolution bandwidth is 100 Hz, we can estimate the power spectral density of the noise using

$$10^{-60/10} = \frac{V_{RMS}^2/50}{1 \text{ mW}} \rightarrow V_{RMS}^2 = 50 \times 10^{-9} \text{ V}^2$$

and

$$\text{PSD} = V_{out}^2(f) = \frac{50 \times 10^{-9} \text{ V}^2}{100 \text{ Hz}} = 500 \times 10^{-12} \text{ V}^2/\text{Hz}$$

Using Eq. (36.24), we now need to estimate the maximum frequency used in the upper limit of the integration. Looking at the spectrum in Fig. 36.19, we see that the spectrum appears relatively constant over a wide frequency range. However, in any ADC we must use a reconstruction filter (or, for this case where a modulator is used, a digital averaging filter) to bandlimit the noise in the spectrum. For the modulator discussed in Sec. 36.2 a reasonable value of maximum frequency is 2 kHz (again set by a filter). Going above this frequency results, as seen in Eq. (36.7), in an undesired signal reduction (the signal sees the lowpass response of the integrator). The RMS noise in the modulator's output spectrum is then

$$V_{noise,RMS} = \left[ \int_0^{2k} \frac{500 \times 10^{-12} \text{ V}^2}{\text{Hz}} \cdot df \right]^{1/2} = 1 \text{ mV}$$

The RMS value of the desired signal in Fig. 36.19 is 1.41 V. The SNR, for this modulator's output spectrum, is

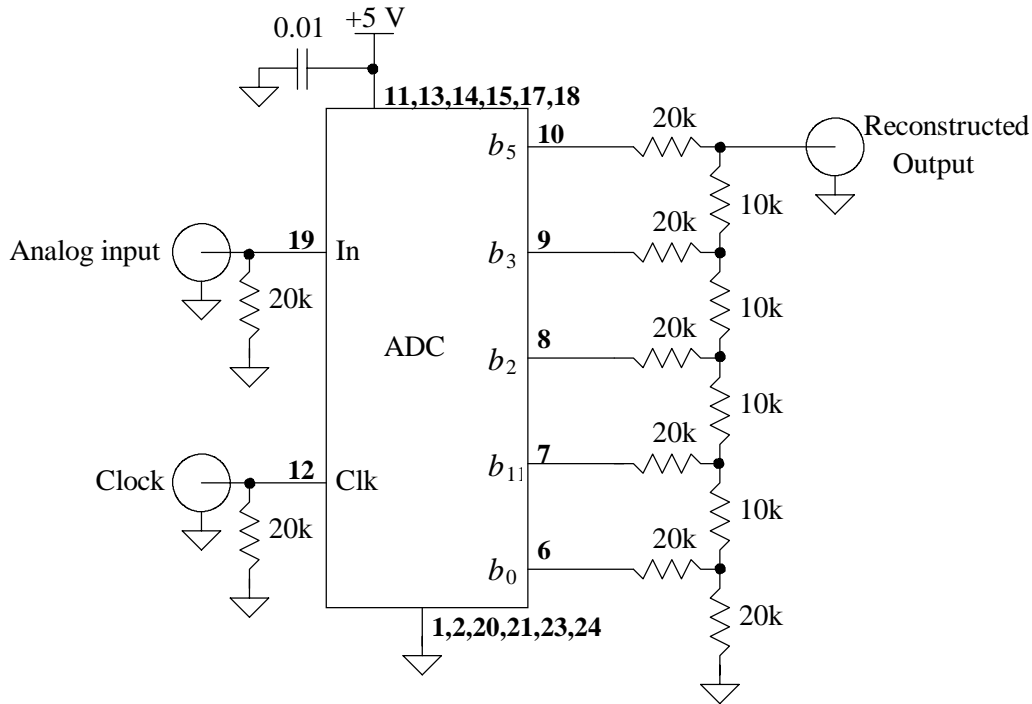
$$\text{SNR} = 20 \cdot \log \frac{1.41 \text{ V}}{1 \text{ mV}} = 63 \text{ dB}$$

Using Eq. (31.5), the effective number of bits is roughly 10.

While these calculations are useful to illustrate how we manipulate data to calculate a SNR, it will be more useful to prototype an actual ADC and compare the quantization noise it adds to a signal to the values calculated theoretically.

### Prototyping the ADC Circuit

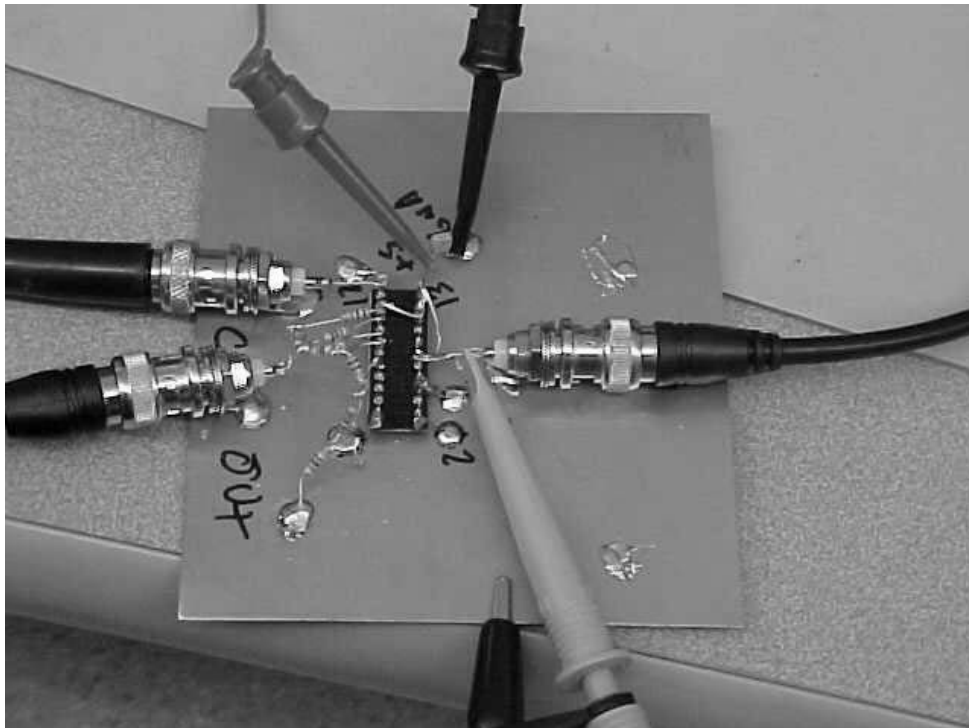
In order to make our measurements practical and simple consider the circuit diagram shown in Fig. 36.43. An ADC and a purely resistive DAC are used to illustrate the noise (from the quantization process) added to an analog signal by the analog-to-digital conversion process. Using such a simple output DAC is useful as long as the ADC outputs swing from rail-to-rail and we use a relatively large resistance (say 10k) so the CMOS outputs can supply a current to the load resistors without a significant output voltage sag.



**Figure 36.43** Schematic of an ADC and resistive DAC.

The ADC we selected is the TLC5540. It is an 8-bit ADC. However, we will only use the upper five bits of the ADC to illustrate the quantization process. The maximum reference voltage,  $V_{REF+}$ , is 5 V, while the minimum reference voltage,  $V_{REF-}$ , is ground. The clock pulse we'll use for our measurements will oscillate between ground and 5 V at 1

MHz. Because we are using five bits we can estimate the weighting of the LSB using Eq. (30.23) as 156 mV. Further, from Eq. (30.30), we can estimate the RMS value of the quantization noise as 45 mV. A picture of the prototyped ADC/DAC is seen in Fig. 36.44. The TLC5540 comes in a plastic small outline package (SOP). This SOP package is difficult to solder by hand in our deadbug prototyping scheme so we soldered it into a dual-in-line package (DIP) carrier. This makes prototyping the circuit much easier.

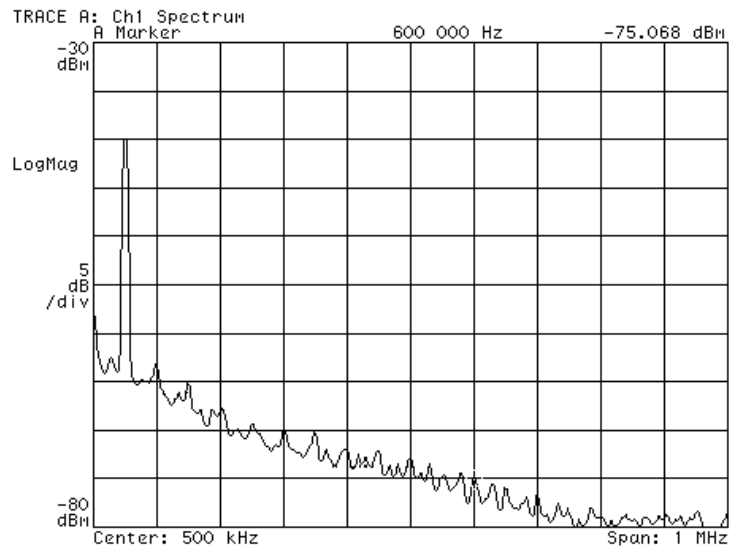


**Figure 36.44** Photograph of the ADC/DAC prototype circuit.

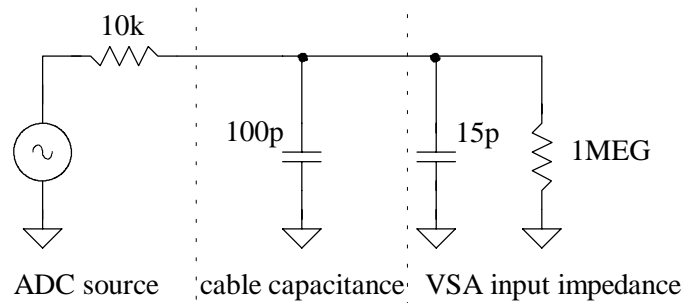
Figure 36.45 shows the output spectrum for the ADC and resistive DAC seen in Fig. 36.43. Again, the clock frequency is 1 MHz. The input signal is a sinewave at 50 kHz with 0.5 V peak and centered around 2 V. The reason we don't see a DC signal in the spectrum is that the VSA's input was AC coupled. Again, the VSA's input resistance is 1 M $\Omega$ . Note how the spectrum rolls off with increasing frequency. We connected the output in Fig. 36.43 to the VSA's input through a piece of coax cable. The coax was 3 feet long and resulted in a capacitance of approximately 100 pF shunting the VSA's input, Fig. 36.46. If we model the ADC/DAC as a voltage source with 10k output resistance, then the frequency response of the measuring circuit is lowpass with a corner frequency of

$$f_{3dB} = \frac{1}{2\pi \cdot 10k \cdot 115 \text{ pF}} = 138 \text{ kHz}$$

Frequencies, in the output spectrum above this frequency will start rolling off at a rate of 20 dB/decade. The point is that instead of seeing a flat quantization spectrum (as in Fig. 30.57, for example), we will see a spectrum that rolls off with increasing frequency.



**Figure 36.45** Output spectrum showing quantization noise for the 5-bit ADC in Fig. 36.43.



**Figure 36.46** How loading affects the ADC's output spectrum.

Looking at Fig. 36.45 and knowing that the spectrum rolls off because of the measuring system, we can get an estimate for the quantization noise power at low frequencies as  $-65$  dBm. Knowing the resolution bandwidth of the measurement was 10-kHz, we can estimate the power spectral density using

$$-65 \text{ dBm} = 10 \cdot \log \frac{V_{RMS}^2 / 1 \text{ M}\Omega}{1 \text{ mW}} \rightarrow V_{RMS}^2 = 316 \times 10^{-6} \text{ V}^2$$

or

$$PSD = V_{out}^2(f) = \frac{316 \times 10^{-6} \text{ V}^2}{10 \text{ kHz}} = 31.6 \times 10^{-9} \text{ V}^2/\text{Hz}$$

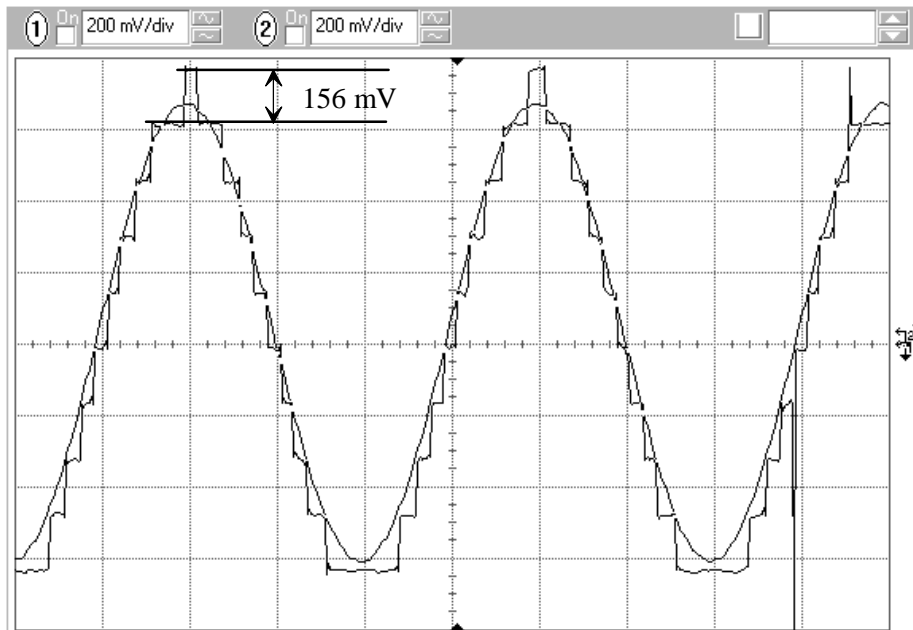
The Nyquist frequency is 500 kHz. If we again assume a filter is used to bandlimit the ADC output to the Nyquist frequency, we can calculate the RMS quantization noise as



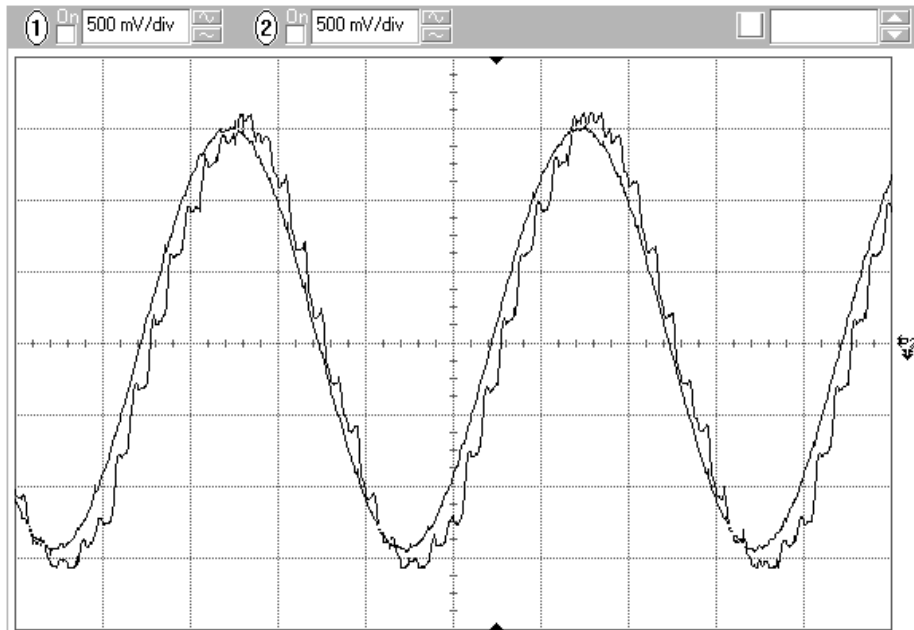
$$V_{Qe,RMS} = \left[ \int_0^{500k} 31.6 \times 10^{-9} \cdot df \right]^{1/2} = 125 \text{ mV}$$

This RMS noise is three times larger than what we calculated earlier (45 mV). We might speculate that the difference is due to not adequately randomizing the noise by using too high of an input frequency, relative to the sampling frequency, or too small an input amplitude (all of which are easy to verify at the bench).

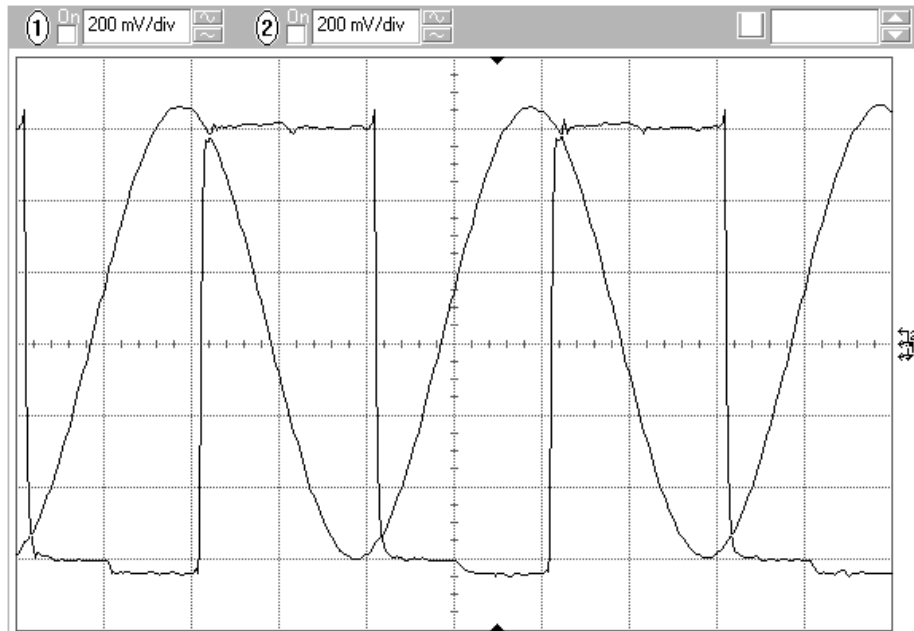
Finally, let's show some time-domain waveforms showing quantization effects. Figure 36.47 shows the input and output waveforms when the input frequency is 5 kHz. Note how, as we calculated earlier, 1 LSB is 156 mV. Figure 36.48 shows the output when the input frequency is increased to 50 kHz, while Fig. 36.49 shows the circuit's inputs and outputs when the Nyquist frequency is applied to the circuit. Note how, as we would expect, the DAC output is simply a square wave at a frequency of 500 kHz. After this output is passed through a reconstruction filter with a frequency of just over 500 kHz we get our exact replica of the input signal simply shifted in time. While the signal in Fig. 36.45 was measured by providing a connection between the circuit and the VSA using a piece of co-ax cable, Fig. 36.46, the signals in Figs. 36.47 - 36.49 were measured using a compensated scope probe, Fig. 36.7. The significantly reduced loading resulting from using the compensated scope probe eliminates the spectrum roll off that was present in Fig. 36.45.



**Figure 36.47** ADC input frequency of 5 kHz and the DAC output.



**Figure 36.48** ADC input frequency of 50 kHz and the DAC output.



**Figure 36.49** ADC input frequency of 500 kHz (the Nyquist frequency) and the DAC output.

While the circuits built in this chapter represent a small number of examples, relative to the material covered in the book, it is hoped that they are representative enough to make the engineer/student want to spend some time at the bench.