Oxide Breakdown

For reliable device operation, the maximum electric field across a device gate oxide should be limited to 10 MV/cm. This translates into 1V / 10 Å of gate oxide. A device with t_{ox} of 20 Å should limit the applied gate voltages to 2 V for reliable long-term operation.

Drain-Induced Barrier Lowering

Drain-induced barrier lowering (DIBL, pronounced "dibble") causes a threshold voltage reduction with the application of a drain-source voltage. The positive potential at the drain terminal helps to attract electrons under the gate oxide and thus increase the surface potential V_s . In other words V_{DS} helps to invert the channel on the drain side of the device, causing a reduction in the threshold voltage. Since V_{THN} decreases with increasing V_{DS} , the result is an increase in drain current and thus a decrease in the MOSFET's output resistance.

Gate-Induced Drain Leakage

Gate-Induced Drain Leakage (GIDL, pronounced "giddle") is a term used to describe a component of the drain to substrate leakage current. When the device is in accumulation (e.g. the gate of an NMOS device is at ground) the surface and substrate potentials are nearly the same. In this situation there can be a dramatic increase in avalanche multiplication or band-to-band tunneling when the drain is at a higher potential. Minority carriers underneath the gate are swept to the substrate creating the leakage current.

Gate Tunnel Current

As the oxide thickness scales downwards, the probability of carriers directly tunneling through the gate oxide increases. For oxide thicknesses less than 15 Å, this gate current can be significant. To reduce the tunnel current, various sandwiches of dielectrics are being explored. Figure 16.67 later in the book presents some results showing values for direct tunnel currents under various operating conditions.

6.5.3 SPICE Models for Our Short-Channel CMOS Process

Section 6.4 presented some SPICE models for the long-channel CMOS process used in this book. In this section we give the BSIM4² models for the 50 nm process we use in the book with VDD = 1 V, see also Table 5.2. The model listing is given below.

BSIM4 Model Listing (NMOS)

```
* 50nm BSIM4 models
* Don't forget the .options scale=50nm if using an Lmin of 1
* 1<Ldrawn<200 10<Wdrawn<10000 Vdd=1V
.model
                              |eve| = 54
          nmos
                     nmos
+binunit = 1
                     paramchk= 1
                                        mobmod = 0
+capmod = 2
                                                           geomod < 0
                     igcmod = 1
                                        iqbmod = 1
+diomod = 1
                     rdsmod = 0
                                        rbodymod= 1
                                                           raatemod= 1
```

² BSIM4 is a fourth generation MOSFET model developed at the University of California, Berkeley. The acronym stands for Berkeley Short-channel IGFET (insulated gate FET) Model. For more information see: http://www-device.eecs.berkeley.edu

+permod = 1	acnqsmod= 0	trnqsmod= 0	
+tnom = 27 +epsrox = 3.9 +II = 0 +Iw = 0 +Iwl = 0	toxe = $1.4e-009$ wint = $5e-009$ wl = 0 www = 0 wwwl = 0	toxp = 7e-010 lint = 1.2e-008 lln = 1 lwn = 1 xpart = 0	toxm = 1.4e-009 wln = 1 wwn = 1 toxref = 1.4e-009
+vth0 = 0.22 +k3b = 0 +dvt2 = -0.032 +dsub = 2 +dvtp1 = 0.05 +ngate = 5e+020 +cdsc = 0.0002 +voff = -0.15 +vfb = -0.55 +uc = -3e-011 +a1 = 0 +keta = 0.04 +pbiblc1 = 0.028 +pvag = 1e-020 +fprout = 0.2 +rsh = 3 +rdswmin = 0 +prwb = 6.8e-011 +beta0 = 30 +egidl = 0.8			$\begin{array}{llllllllllllllllllllllllllllllllllll$
+aigbacc = 0.012 +nigbacc = 1 +eigbinv = 1.1 +cigc = 0.002 +nigc = 1	bigbacc = 0.0028 aigbinv = 0.014 nigbinv = 3 aigsd = 0.017 poxedge = 1	cigbacc = 0.002 bigbinv = 0.004 aigc = 0.017 bigsd = 0.0028 pigcd = 1	cigbinv = 0.004 bigc = 0.0028 cigsd = 0.002 ntox = 1
+xrcrg1 = 12 +cgso = 6.238e-010 +cgsl = 2.495e-10 +moin = 15	xrcrg2 = 5 cgdo = 6.238e-010 ckappas = 0.02 noff = 0.9	cgbo = 2.56e-011 ckappad = 0.02 voffcv = 0.02	cgdl = 2.495e-10 acde = 1
+kt1 = -0.21 +ua1 = 1e-009 +at = 53000	kt1l = 0.0 ub1 = -3.5e-019	kt2 = -0.042 uc1 = 0	ute = -1.5 prt = 0
+fnoimod = 1	tnoimod = 0		
+jss = 0.0001 +ijthsfwd= 0.01 +jsd = 0.0001 +ijthdfwd= 0.01 +pbs = 1 +cjsws = 5e-010 +mjswgd = 5e-010 +cjswgd = 5e-010 +tpbsw = 0.005 +xtis = 3	jsws = 1e-011 ijthsrev= 0.001 jswd = 1e-011 ijthdrev= 0.001 cjs = 0.0005 mjsws = 0.33 pbd = 1 cjswd = 5e-010 mjswgd = 0.33 tcjsw = 0.001 xtid = 3	jswgs = 1e-010 bvs = 10 jswgd = 1e-010 bvd = 10 mjs = 0.5 pbswgs = 1 cjd = 0.0005 mjswd = 0.33 tpb = 0.005 tpbswg = 0.005	njs = 1 xjbvs = 1 njd = 1 xjbvd = 1 pbsws = 1 cjswgs = 56-010 mjd = 0.5 pbswgd = 1 tcj = 0.001 tcjswg = 0.001
+dmcg = 0e-006	dmci = 0e-006	dmdg = 0e-006	dmcgt = 0e-007

+dwj	= 0e-008	xgw = 0e-007	xgl = 0e-008	
+rshg	= 0.4	gbmin = 1e-010	rbpb = 5	rbpd = 15
+rbps	= 15	rbdb = 15	rbsb = 15	ngcon = 1

BSIM4 Model Listing (PMOS)

.model pmos	pmos level = 54		
+binunit = 1 +capmod = 2 +diomod = 1 +permod = 1	paramchk= 1 igcmod = 1 rdsmod = 0 acnqsmod= 0	mobmod = 0 igbmod = 1 rbodymod= 1 trnqsmod= 0	geomod = 0) rgatemod= 1
+tnom = 27 +epsrox = 3.9 +II = 0 +Iw = 0 +Iwl = 0	toxe = $1.4e-009$ wint = $5e-009$ wl = 0 ww = 0 wwl = 0	toxp = 7e-010 lint = 1.2e-008 lln = 1 lwn = 1 xpart = 0	toxm = 1.4e-009 wln = 1 wwn = 1 toxref = 1.4e-009
$\begin{aligned} +vth0 &= -0.22 \\ +k3b &= 0 \\ +dvt2 &= -0.032 \\ +dsub &= 0.7 \\ +dsub &= 0.7 \\ +dvtp1 &= 0.05 \\ +ngate &= 5e+020 \\ +cdsc &= 0.000258 \\ +voff &= -0.15 \\ +vfb &= 0.55 \\ +uc &= 4.6e-013 \\ +a1 &= 0 \\ +keta &= -0.047 \\ +pdiblc1 &= 0.03 \\ +pvag &= 1e-020 \\ +fprout &= 0.2 \\ +rsh &= 3 \\ +rdswmin &= 0 \\ +prwb &= 6.8e-011 \\ +beta0 &= 30 \\ +egidl &= 0.8 \end{aligned}$			$\begin{array}{llllllllllllllllllllllllllllllllllll$
+aigbacc = 0.012 +nigbacc = 1 +eigbinv = 1.1 +cigc = 0.0008 +nigc = 1	bigbacc = 0.0028 aigbinv = 0.014 nigbinv = 3 aigsd = 0.0087 poxedge = 1	cigbacc = 0.002 bigbinv = 0.004 aigc = 0.69 bigsd = 0.0012 pigcd = 1	cigbinv = 0.004 bigc = 0.0012 cigsd = 0.0008 ntox = 1
+xrcrg1 = 12 +cgso = 7.43e-010 +cgsl = 1e-014 +moin = 15	xrcrg2 = 5 cgdo = 7.43e-010 ckappas = 0.5 noff = 0.9	cgbo = 2.56e-011 ckappad = 0.5 voffcv = 0.02	cgdl = 1e-014 acde = 1
+kt1 = -0.19 +ua1 = -1e-009 +at = 33000	kt1l = 0 ub1 = 2e-018	kt2 = -0.052 uc1 = 0	ute = -1.5 prt = 0
+fnoimod = 1	tnoimod = 0		
+jss = 0.0001	jsws = 1e-011	jswgs = 1e-010	njs = 1

	+ijthsfwd= 0.01 +jsd = 0.0001 +ijthdfwd= 0.01 +pbs = 1 +cjsws = 5e-010 +mjswgs = 0.33 +pbswd = 1 +cjswgd = 5e-010 +tpbsw = 0.005 +xtis = 3	ijthsrev= 0.001 jswd = 1e-011 ijthdrev= 0.001 cjs = 0.0005 mjsws = 0.33 pbd = 1 cjswd = 5e-010 mjswgd = 0.33 tcjsw = 0.001 xtid = 3	bvs = 10 jswgd = 1e-010 bvd = 10 mjs = 0.5 pbswgs = 1 cjd = 0.0005 mjswd = 0.33 tpb = 0.005 tpbswg = 0.005	xjbvs = 1 njd = 1 xjbvd = 1 pbsws = 1 cjswgs = 59-010 mjd = 0.5 pbswgd = 1 tcj = 0.001 tcjswg = 0.001
$\left\{ \right.$	+dmcg = 0e-006 +dwj = 0e-008	dmci = 0e-006 xgw = 0e-007	dmdg = 0e-006 xgl = 0e-008	dmcgt = 0e-007
	+rshg = 0.4 +rbps = 15	gbmin = 1e-010 rbdb = 15	rbpb = 5 rbsb = 15	rbpd = 15 ngcon = 1

Simulation Results

Figure 6.19 shows 10/1 PMOS and NMOS device simulation results using the topologies seen in Figs. 6.11–6.13. The actual device sizes are 500 nm (width) by 50 nm (length). From the information in this figure and knowing *VDD* is 1 V, we can estimate the on currents for the MOSFETs. For the NMOS device

$$I_{on,n} \approx 300 \ \mu A/(W \cdot scale) = 600 \ \mu A/\mu m \tag{6.60}$$

For the PMOS device

$$I_{on,p} \approx 150 \ \mu A / (W \cdot scale) = 300 \ \mu A / \mu m \tag{6.61}$$



Figure 6.19 Current-voltage characteristics for 50 nm MOSFETs.