I_D vs V_{GS}. While this is an important concern, and any SPICE model used for simulating submicron circuits should show good agreement, it won't be what we focus on here. Here we focus on the ability of the model to transition continuously from weak to strong inversion. While we might think that looking at the DC curves of a device (e.g., I_D vs. V_{GS}) would show the discontinuities (kinks) between weak and strong inversion, a much better indication is to look at several devices operating under similar, related conditions.

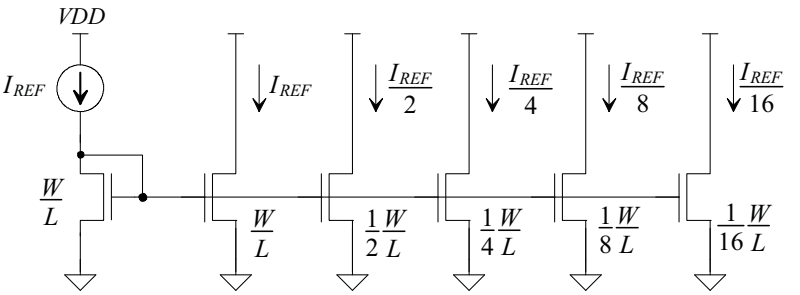

Figure 33.15 Binary weighted current mirror.

Consider the binary weighted current mirror shown in Fig. 33.15. In the following discussion we assume the lengths and widths of the devices are so large that oxide encroachment and lateral diffusion are not an issue. Clearly, in Fig. 33.15, the MOSFETs will all be operating in the same region, for example, strong inversion. What we are going to do, with the binary weighted current mirror, is utilize the fact that MOSFETs in series and parallel can be combined, as seen in Fig. 33.16, to implement a test circuit to evaluate the performance of our submircon SPICE model. Note that our test circuit will have nothing to do, directly, with short-channel behavior, but rather it will evaluate the fundamental implementation of the model.

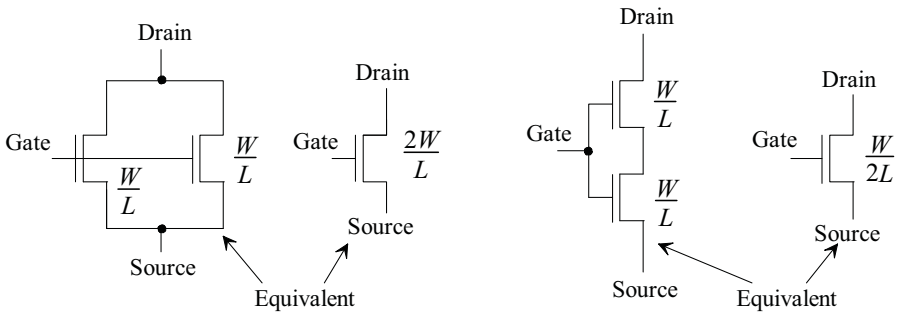

Figure 33.16 Combining parallel and series MOSFETs.

Figure 33.17 shows the implementation of the binary-weighted current mirror using a *W*-2*W* topology (based on the *R*-2*R* divider discussed in the last section). To understand the operation of this circuit first note that currents in M1 and M2 have the same value. Next, notice that the currents flowing in the remaining MOSFETs should sum to I_{REF}. In fact, using the information shown in Fig. 33.16, the remaining MOSFETs can be combined into a MOSFET with the same size as M1 or M2 (and, again, having a drain current of I_{REF}). Each stage we add to this topology essentially divides the reference current by two keeping the overall sum of the currents at I_{REF}.

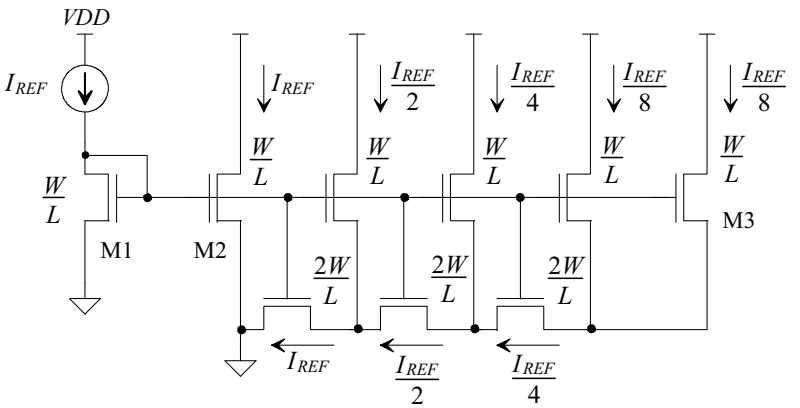

Figure 33.17 W-2W current mirror.

This circuit is useful because it now relates the current flowing in a strongly inverted device, say M1 or M2 in Fig. 33.17, to a weakly inverted device, say M3. If the MOSFET model is operating with a truly continuous change from one region to another the currents will be binary-related and sum to I_{REF}. Figure 33.18 shows the simulation results for an eight-stage *W*-2*W* current mirror modeled with the EKV model. The 1 to 2% error in the binary currents is related to the differing drain-to-source voltages, V_{DS}, of the devices. The minimum length of the device modeled by the EKV model in this simulation is 0.15 μm while the actual length used in the simulation is 5 μm (33 times minimum). The widths of the devices used in the simulation are 20 μm and 40 μm.

Figure 33.19 shows the simulation results using a MOSFET model that doesn't model these transitions well. If one were to use this model where the *W*-2*W* section is used in a DAC, the designer might think the DAC performance is circuit-limited and not matching-limited (keeping in mind that all MOSFETs are perfectly matched in a SPICE simulation). This also points out an important point: *Simulations don't always tell the truth! The good design engineer knows the limitations of the models and the simulator*.

While there are other reasons for using the EKV model (simulation speed, scaling, well-behaved, etc.), the topic of MOSFET modeling is outside the scope of this book [5].

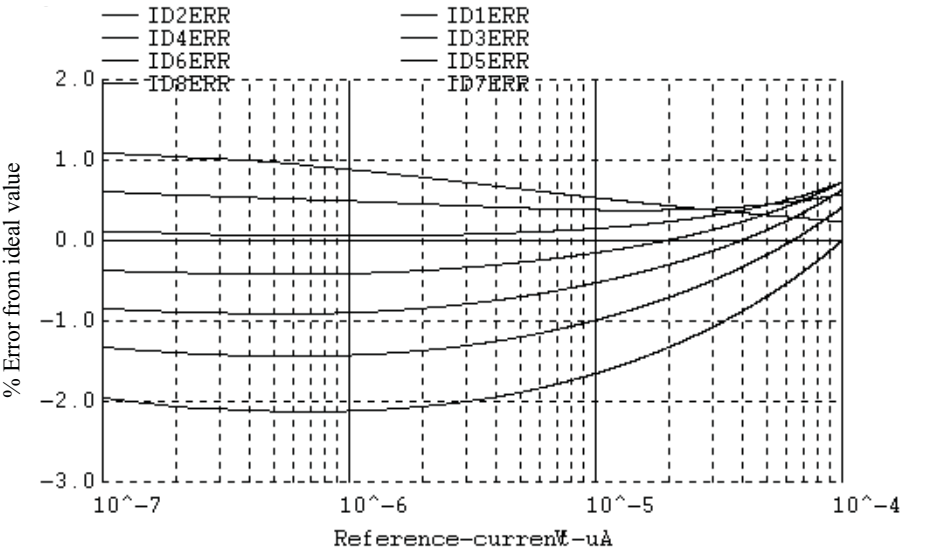

Figure 33.18 Simulated W-2W current mirror using EKV model.

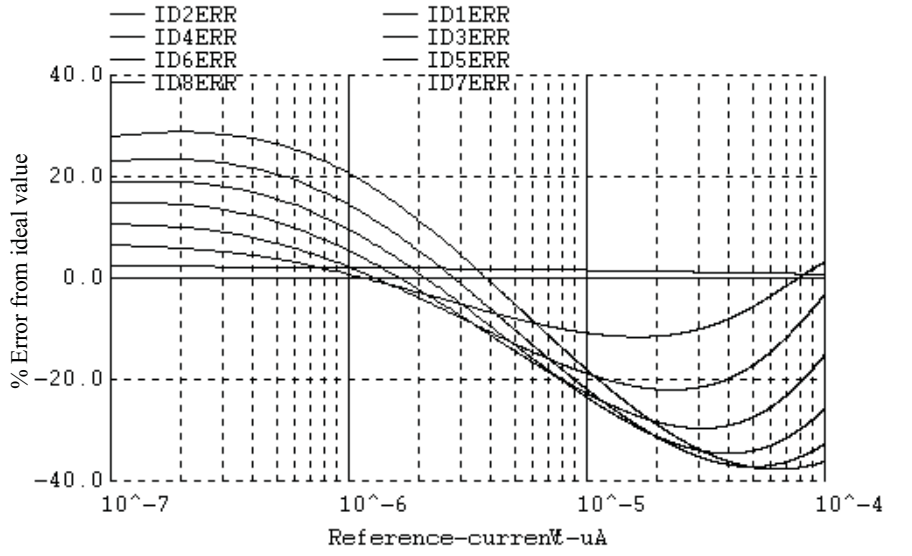

Figure 33.19 Simulated W-2W current mirror showing model problems.

Model Parameters

The EKV model parameters are listed below for both NMOS and PMOS devices. Notice that the minimum length is 0.15 μm and the minimum width is 1.05 μm. Also note that the level used depends on the simulator. For the simulations in this book, again, we will utilize WinSPICE. While some of the model names are discussed in Ch. 5, information concerning the remaining names can be found in [4]. Also note that these models are located in the file models.txt in the zip file chap33_spice.zip located at cmosedu.com.

```
*** SPICE Models

*** Models created by Daniel Foty.
*** (c) 2001, Gilgamesh Associates and EPFL - All rights reserved.
*** These models are provided without warranty or support.
*** These models represent a completely fictitious 0.15um process, and do
***   NOT correspond to any real silicon process.  They are provided expressly for
***   use in the examples provided in this text, and should not be used for any
***   real silicon product design.

*** NMOS EKV MOSFET Model ***************************************************
*** Level=44 in WinSPICE and ELDO, Level=55 in ADM/HSPICE, Level=5 in PSPICE,
*** Level=EKV in Spectre
*** Lmin=0.15u Wmin=1.05u (If Scale=0.15u then Lmin=1 and Wmin=7)
*---------------
.MODEL nmos nmos
+ LEVEL=44

*** Setup Parameters
+ UPDATE=2.6

*** Process Related Model Parameters
+ COX=9.083E-3 XJ=0.15E-6

*** Intrinsic Model Parameters
+ VTO=0.4 GAMMA=0.71 PHI=0.97 KP=453E-6
+ E0=88.0E6 UCRIT=4.0E6
+ DL=-0.05E-6 DW=-0.02E-6
+ LAMBDA = 0.30 LETA=0.28 WETA=0
+ Q0=280E-6 LK=0.5E-6

*** Substrate Current Parameters
+ IBN=1.0 IBA=200E6 IBB=350E6

*** Intrinsic Model Temperature Parameters
+ TNOM=27.0 TCV=1.5E-3 BEX=-1.5 UCEX=1.7 IBBT=0

*** 1/f Noise Model Parameters
+ KF=1E-27 AF=1

*** Series Resistance and Area Calculation Parameters
+ HDIF=0.24e-6 ACM=3 RSH=5.0 RS=1250.526
+ RD=1250.526 LDIF=0.07e-6
```

```
*** Junction Current Parameters
+ JS=1.0E-6 JSW=5.0E-11 XTI=0 N=1.5

*** Junction Capacitances Parameters
+ CJ=1.0E-3 CJSW=2.0E-10 CJGATE=5.0E-10
+ MJ=0.5 MJSW=0.3 PB=0.9 PBSW=0.9 FC=0.5

*** Gate Overlap Capacitances
+ CGSO=3.0E-10 CGDO=3.0E-10 CGBO=3.0E-11


*** PMOS EKV MOSFET Model ********************************************************
*** Level=44 in WinSPICE and ELDO, Level=55 in ADM/HSPICE, Level=5 in PSPICE,
*** Level=EKV in Spectre
*** Lmin=0.15u Wmin=1.05u (If Scale=0.15u then Lmin=1 and Wmin=7)
*---------------
.MODEL pmos pmos
+ LEVEL  = 44

*** Setup Parameters
+ UPDATE = 2.6

*** Process Related Model Parameters
+ COX=9.083E-3 XJ=0.15E-6

*** Intrinsic Model Parameters
+ VTO=-0.4 GAMMA=0.69 PHI=0.87 KP=92.15E-6
+ E0=51.0E6 UCRIT=18.0E6
+ DL=-0.05E-6 DW=-0.03E-6
+ LAMBDA=1.1 LETA=0.45 WETA=0
+ Q0=200E-6 LK=0.6E-6

*** Substrate Current Parameters
+ IBN=1.0 IBA=0.0 IBB=300E6

*** Intrinsic Model Temperature Parameters
+ TNOM=25.0 TCV=-1.4E-3 BEX=-1.4 UCEX=2.0 IBBT=0.0

*** 1/f Noise Model Parameters
+ KF=1.0E-28 AF=1

*** Series Resistance and Area Calculation Parameters
+ HDIF=0.24E-6 ACM=3 RSH=5.0 RS=3145.263
+ RD=3145.263 LDIF=0.07e-6

*** Junction Current Parameters
+ JS=1.0E-7 JSW=5.0E-12 XTI=0 N=1.8

*** Junction Capacitances Parameters
+ CJ=1.3E-3 CJSW=2.5E-10 CJGATE=5.5E-10
+ MJ=0.5 MJSW=0.35 PB=0.9 PBSW=0.9 FC=0.5

*** Gate Overlap Capacitances
+ CGSO=3.2E-10 CGDO=3.2E-10 CGBO=3.0E-11
```