# 12-Bit Pipelined ADC Design Project

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## 1. Introduction

The goal of this project is to design a 12-bit pipeline analog to digital converter (ADC). The pipeline ADC design is to use 1.5 bits/stage and capacitor error averaging. The ADC will operate with a maximum clock frequency of 100MHz, a VDD of 1V, and a maximum $V_{REF}$ range from 0V to 1V. The design will be verified using ideal components in Spice simulation to focus the design effort on the pipeline ADC architecture rather than on the Op-amps and comparators themselves. Using ideal components will also keep the simulation times reasonable.

The purpose of analog to digital converts is to sample and digitize an analog signal. The more precisely the analog signal is converted to digital, the more information can be obtained from it. It is also desirable to convert high bandwidth or high frequency analog signals; thus, ADCs must be capable of a fast sampling rate as well being accurate. The pipeline ADC is the architecture of choice for applications that require both speed and accuracy and where latency is not concern. The basic idea behind the pipeline ADC is that each stage will first sample and hold the input then compare this to $V_{REF}/2$. If the input is greater than $V_{REF}/2$, output a 1 for that stage and pass the input voltage directly to the next stage. If the input is less than $V_{REF}/2$, output a 0 for that stage and multiply the input voltage by 2 before passing it to the next stage. Figure 1 shows the block diagram for this basic operation.

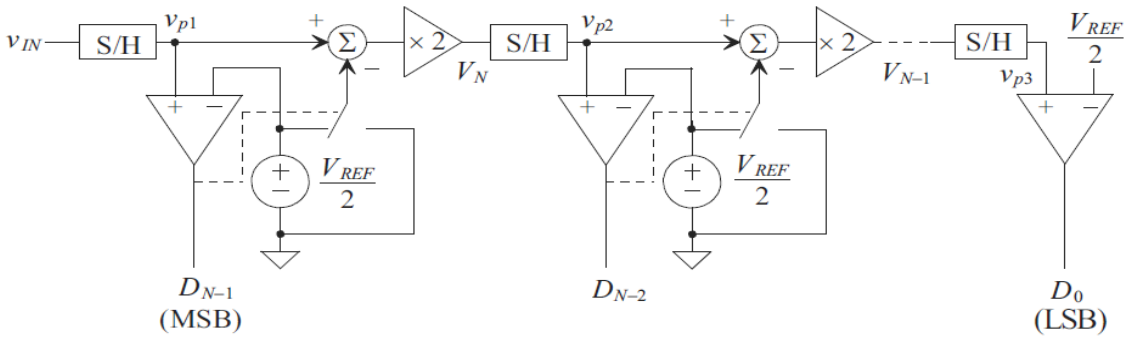



**Figure 1** Pipeline ADC Block Diagram [1]

There are a few challenges with the basic pipeline ADC architecture that this project will attempt to address. Before looking at the sources of error, it is worth noting that an error in the early stages of the pipeline will propagate through the pipeline affectively being amplified by 2 by each successive stage. Errors can be created by the comparators not switching at the correct point. This means that the comparator may have some offset which will result in it making the wrong decision. The sample and hold may also have some offset causing the wrong voltage to be passed to the comparator which will result in the same problem of the comparator making a wrong decision. The other source of error is the multiply by 2 function, because it is difficult to multiply by a gain of exactly 2. These limitations with real op-amps and comparators will result in integral nonlinearity (INL) and differential nonlinearity (DNL) errors.

This design requires 12-bit resolution. This means that there will be $2^{12}$ or 4096 possible output bit combinations. Assuming a $V_{REF}$ of 1V, 1LSB or the level of analog resolution is given by

$$1LSB = \frac{V_{REF}}{2^N} = \frac{1}{4096} = 244\mu V \qquad \text{(Eq. 1)}$$

To correct the errors caused by the offsets in the comparators and the sample and hold op-amps, a technique called 1.5 bits/stage will be used. The name 1.5 bits/stage is based on the fact that each stage has an output with three possible cases consisting of *a* and *b* signals, where *ab* can be 00, 01, or 11. The 1.5 bits/stage algorithm works as follows:

If $v_{in} < \frac{V_{CM}}{2}$, then $ab = 00$ and $v_{out} = 2 \cdot \left(v_{in} + \frac{V_{CM}}{2}\right)$.
If $\frac{V_{CM}}{2} < v_{in} < \frac{3V_{CM}}{2}$, then $ab = 01$ and $v_{out} = 2 \cdot \left(v_{in} - \frac{V_{CM}}{2}\right)$.
If $v_{in} > \frac{3V_{CM}}{2}$, then $ab = 11$ and $v_{out} = 2 \cdot \left(v_{in} - \frac{3V_{CM}}{2}\right)$.

The ideal transfer curve for the 1.5 bits/stage of $v_{in}$ versus $v_{out}$ is shown in Figure 2. And, the relationship between $v_{in}$ and $v_{out}$ can be expressed as

$$v_{out} = 2 \cdot \left(v_{in} + \overline{ab}\frac{V_{CM}}{2} - \bar{a}b\frac{V_{CM}}{2} - ab\frac{3V_{CM}}{2}\right). \quad \text{(Eq. 2)}$$

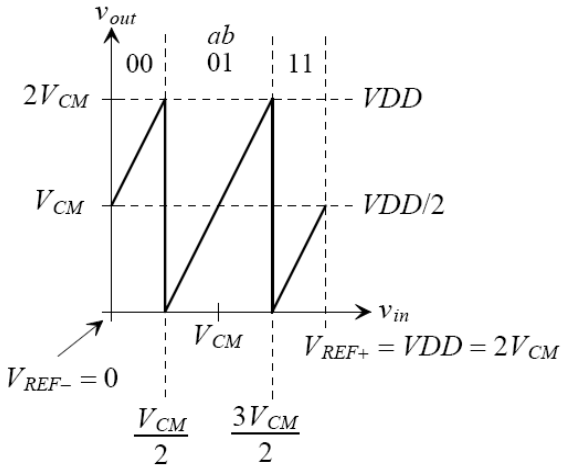



**Figure 2** 1.5 Bits/Stage Transfer Curve (Single-ended) [1]

Using 1.5 bits/stage corrects reasonable comparator offsets by building in error correction with the extra half bit resolution. Only strings of 01 output are valid. For instance, a 00 cannot be followed by another 00 output, and the same is true for 11 output. This is because the subtraction or addition of $V_{CM}$ is done prior to the multiplication by 2. The consequence of this error correction is that extra logic is required to take into account the output of the next stage and get the final digital output code. The logic schematic will be shown in the design considerations section, but it basically does the following logic functions, where $\oplus$ denotes exclusive OR (XOR):

$$b_0 = \overline{a_{1.50}}b_{1.50} \text{ and } c_0 = a_{1.50} \quad \text{(Eq. 3)}$$

$$b_1 = \overline{a_{1.51}}b_{1.51} \oplus c_0 \text{ and } c_1 = \overline{a_{1.51}}b_{1.51}a_0 \quad \text{(Eq. 4)}$$

$$b_{N-1} = \overline{a_{1.5N-1}}b_{1.5N-1} \oplus a_{1.5N-2} \oplus c_{N-2}$$
$$\text{and } c_{N-1} = \overline{a_{1.5N-1}}b_{1.5N-1}a_{1.5N-2} + c_{N-2}(\overline{a_{1.5N-1}}b_{1.5N-1} + a_{1.5N-2}) \quad \text{(Eq. 5)}$$

Also note that the output at this point has a word size of $N+1$ where $b_N$ is given by

$$b_N = a_{1.5N-1} \oplus c_{1.5N-1} \quad \text{(Eq. 6)}$$

Finally, the binary output word needs to have the offset of $V_{CM} - 0.5$ LSB subtracted from it where this offset can be expressed as:

$$V_{CM} - 0.5\,LSB = 001111\ldots \quad \text{(Eq. 7)}$$

The simulation results in the Design Considerations section will show that comparator offset is removed by the error correction of 1.5 bits/stage, but the pipeline ADC still requires a precise multiply by 2. To achieve a more precise multiply by 2, a technique called capacitor error averaging will be used. This technique uses a modified bottom plate sampling switched capacitor op-amp circuit with an ideal gain of 2 as is shown in Figure 3. This circuit works by sampling and holding the input, but instead of sampling again the circuit swaps the positions of the $C$ and $C+\Delta C$ capacitors. The outputs of the amplify and hold phases will then need to be averaged by another bottom plate sample and hold circuit (not shown in Figure 3). The goal is that any mismatch in the capacitance of capacitors will be averaged out by using both capacitors for the multiplication and averaging the result.

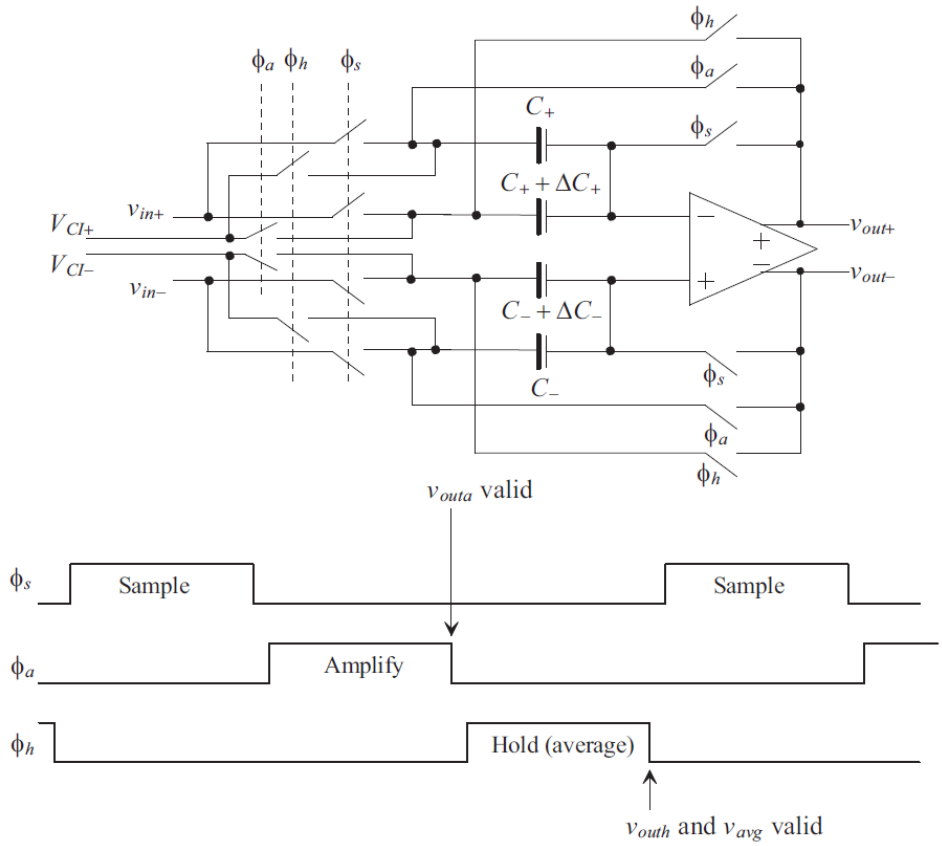


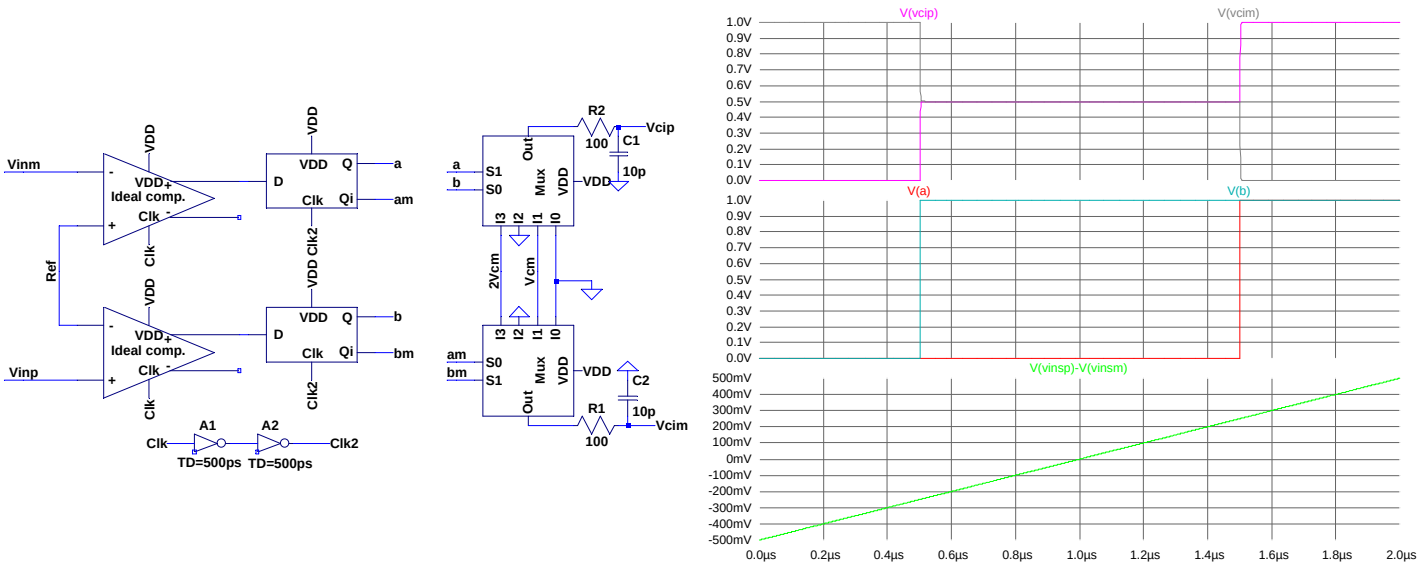

**Figure 3** Capacitor Error Averaging Sample and Hold [1]

The cost of this capacitor error averaging is the added design complexity. There is an extra op-amp and set of switched capacitors for the averaging stage. This will result in more current draw and increase the noise contribution at each stage; although, some of the noise may be canceled out by the averaging action. The other drawback is the need for a three phase non-overlapping clock as shown in the timing diagram at the bottom of Figure 3. This three phase clock must be generated from the input clock which results in a reduction in the sampling rate to less than the input clock rate. Although, the stages can share clocks as will be shown later, there is also a latency penalty for using capacitor error averaging.

An additional goal of this project, beyond the design of the 12-bit ADC, is to investigate whether capacitor error averaging provides any advantage when using op-amps with low open loop gains. The output error with finite gain will be derived based on conservation of charge. Simulations will also be performed looking at the effect of finite gain on the error of the multiply by 2 performed by the sample and hold.

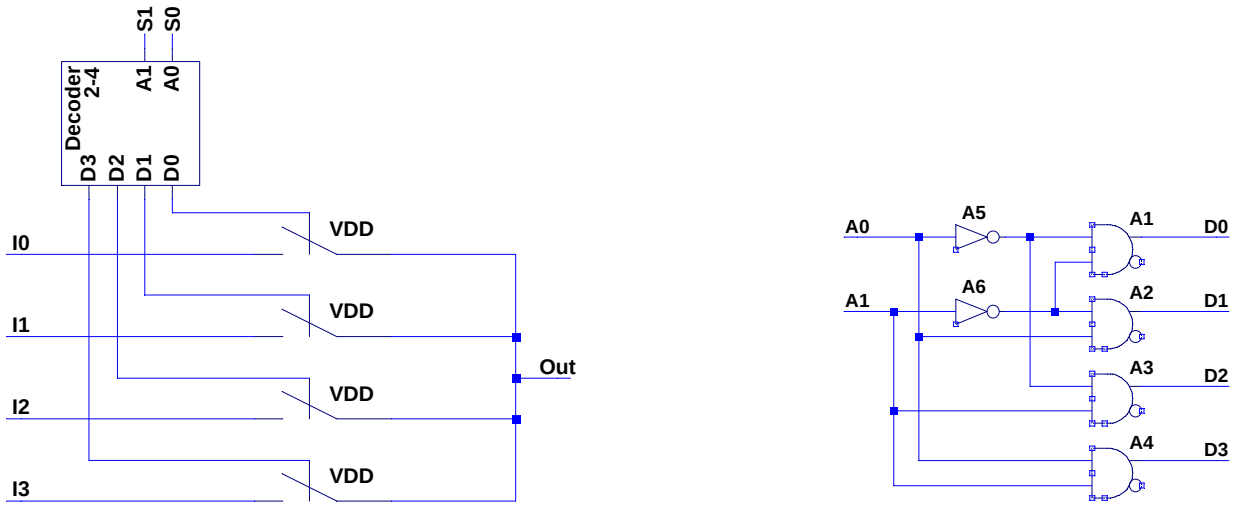
## 2. Design Considerations

The first step in the design is to setup the comparators and multiplexers for the 1.5 bits/stage operation. Figure 4(a) shows the schematic of the block that includes the comparators and multiplexers. The inputs to the cell are the differential sampled analog signal from the previous stage. The outputs of the cell are the *a* and *b* digital codes from the output of the comparators and the $V_{CIP}$ and $V_{CIM}$ voltages that will be added to the input voltage before being multiplied by 2. Note that the outputs of the comparators are connected to a latch with a delayed clock to prevent comparator metastability from resulting in a timing error. Figure 4(b) shows the simulation results for this cell when a differential ramp voltage is applied to the inputs. The simulation results show that at an input differential voltage of -250mV *b* goes to a 1 and $V_{CIP}$ and $V_{CIM}$ both go to $V_{CM}$. At the input differential voltage of 250mV, *a* goes to a 1, $V_{CIP}$ goes to $2V_{CM}$ = 1V and $V_{CIM}$ goes to 0V. Figures 5(a) and (b) show the schematic details of the multiplexer and 2-to-4 decoder which were created for this design.




(a) Comparator and Multiplexer Schematic (b) Transfer Simulation

**Figure 4** 1.5 Bits/Stage Schematic and Simulation




(a) Multiplexer Schematic Detail (b) 2-to-4 Decoder Schematic Detail

**Figure 5** Multiplexer and Decoder Detail

The next major cell to design is the capacitor error averaging sample and hold with a multiplication by two and the addition/subtraction of the $V_{CIP}$ and $V_{CIM}$. Figure 6 shows the schematic of this capacitor error averaging block. The inputs to this cell are the differential analog voltage from the previous stage and the $V_{CIP}$ and $V_{CIM}$ outputs from the multiplexers. The output of this stage is the $v_{out}$ from Eq. 2 and is the differential output of a given stage, which will be the analog input to the next stage. Figure 7(a) shows the simulations results for a $v_{out}$ transfer curve of this single stage where the differential input is a ramp from 0V to 1V as shown in Figure 7(b). Figure 7(b) also shows how $V_{CIP}$ and $V_{CIM}$ are changing in relation to the input and output transfer curve. An important consideration for the design of this cell is the size of the capacitors. The minimum size of the capacitors is determined by $kT/C$ noise which must be less than 0.5 LSB for the maximum operating temperature. Assuming a maximum operating temperature of 100°C, the capacitors must be larger than 0.35pF for the ADC to be 12-bit accurate. Thus, 1pF capacitors should give some margin while not being too large.

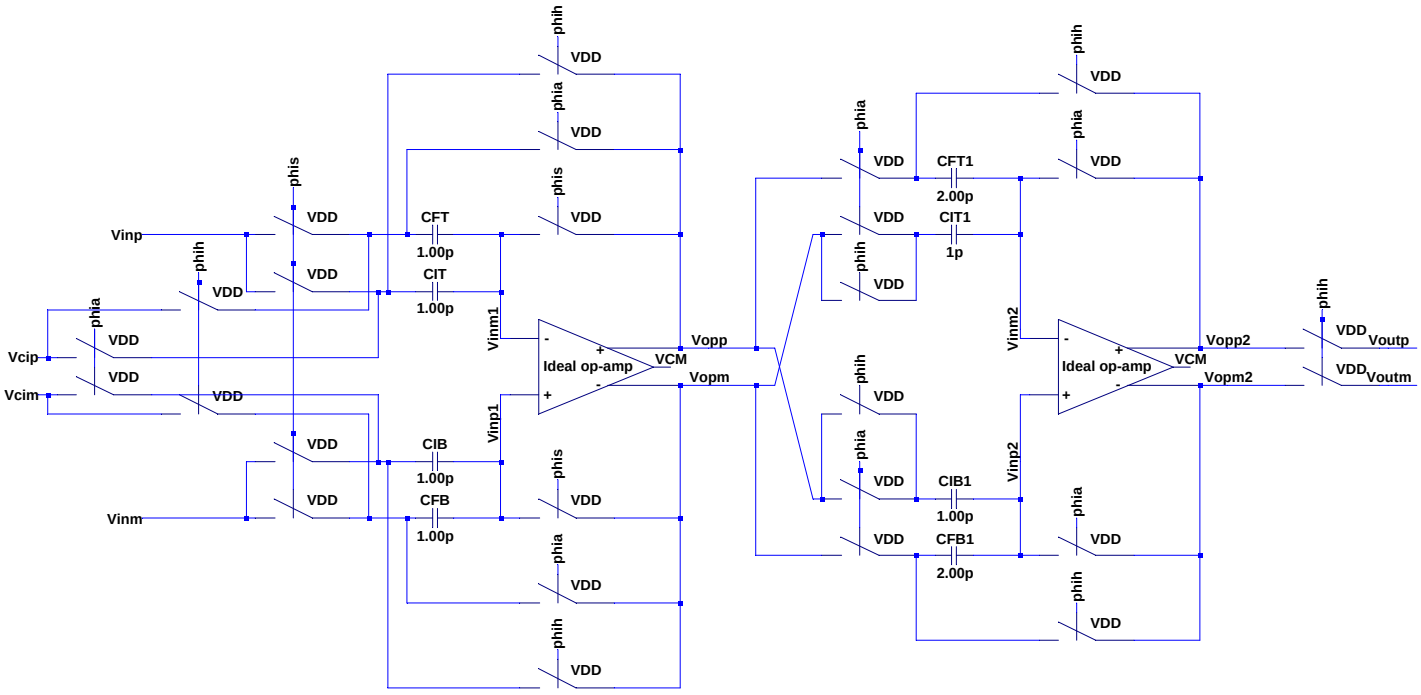
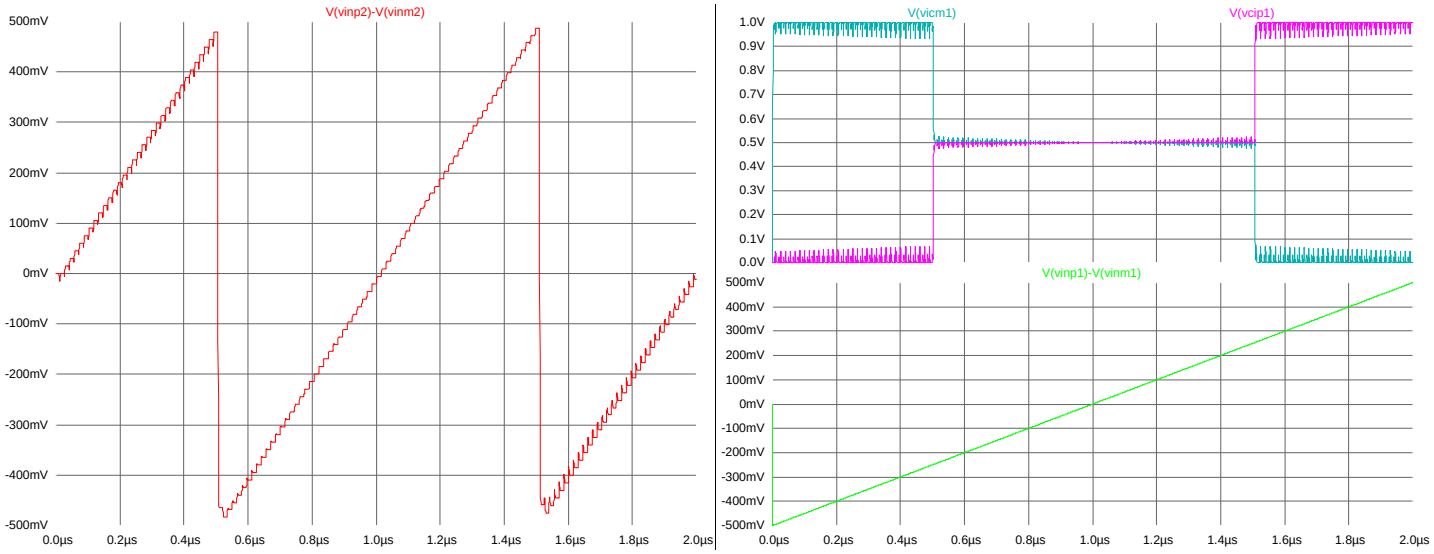


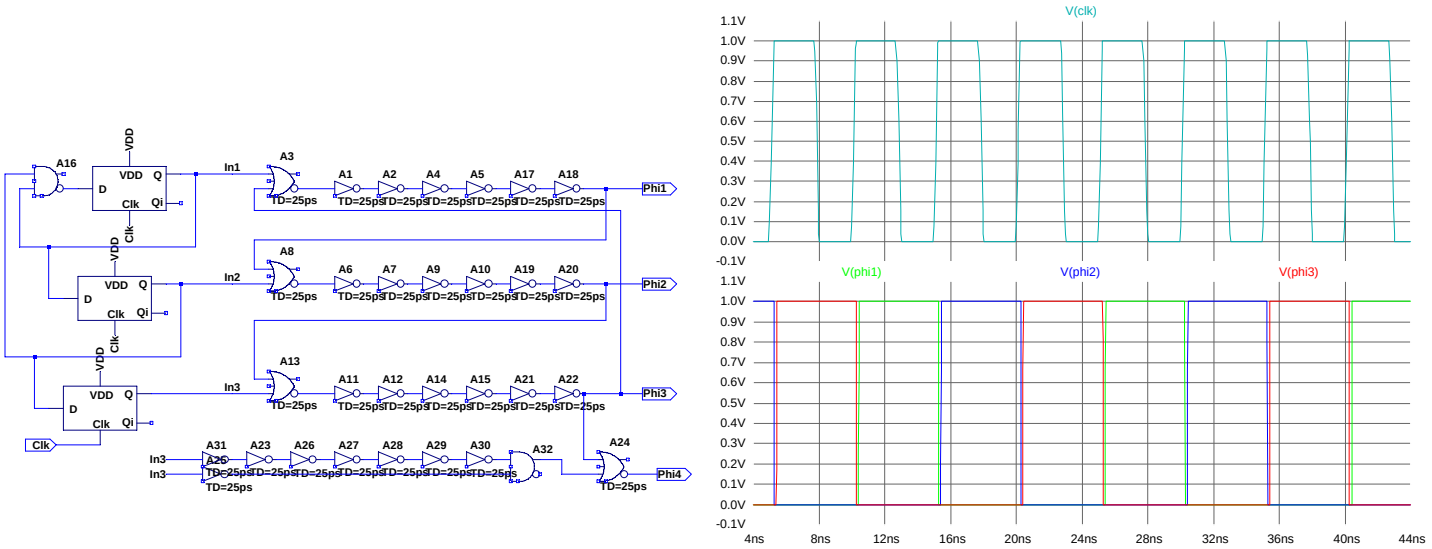

**Figure 6** Capacitor Error Averaging Sample and Hold




(a) 1.5 Bits/Stage S/H Transfer Curve Simulation (b) Transfer Curve Simulation Input Stimulus

**Figure 7** Single Stage Transfer Curve Simulation

The results in Figure 7 use an ideal clock from voltage sources, but the ADC system needs a way to take its 100MHz input clock and convert it to a three phase non-overlapping clock. Figure 8(a) shows the schematic for the three phase non-overlapping clock generation circuit. Figure 8(b) shows the simulation results for the three phase non-overlapping clock generation circuit with a 100MHz input clock signal. Note, that the resulting three phase clock is one third the frequency of the input clock. Thus, the sampling rate of the sample and hold will be one third the clock frequency or 33MS/s for a 100MHz clock. The extra *Phi4* clock in Figure 8(a) will be used for the single-ended to differential conversion.




(a) Schematic (b) Simulation Results

**Figure 8** Three Phase Non-Overlapping Clock Generation

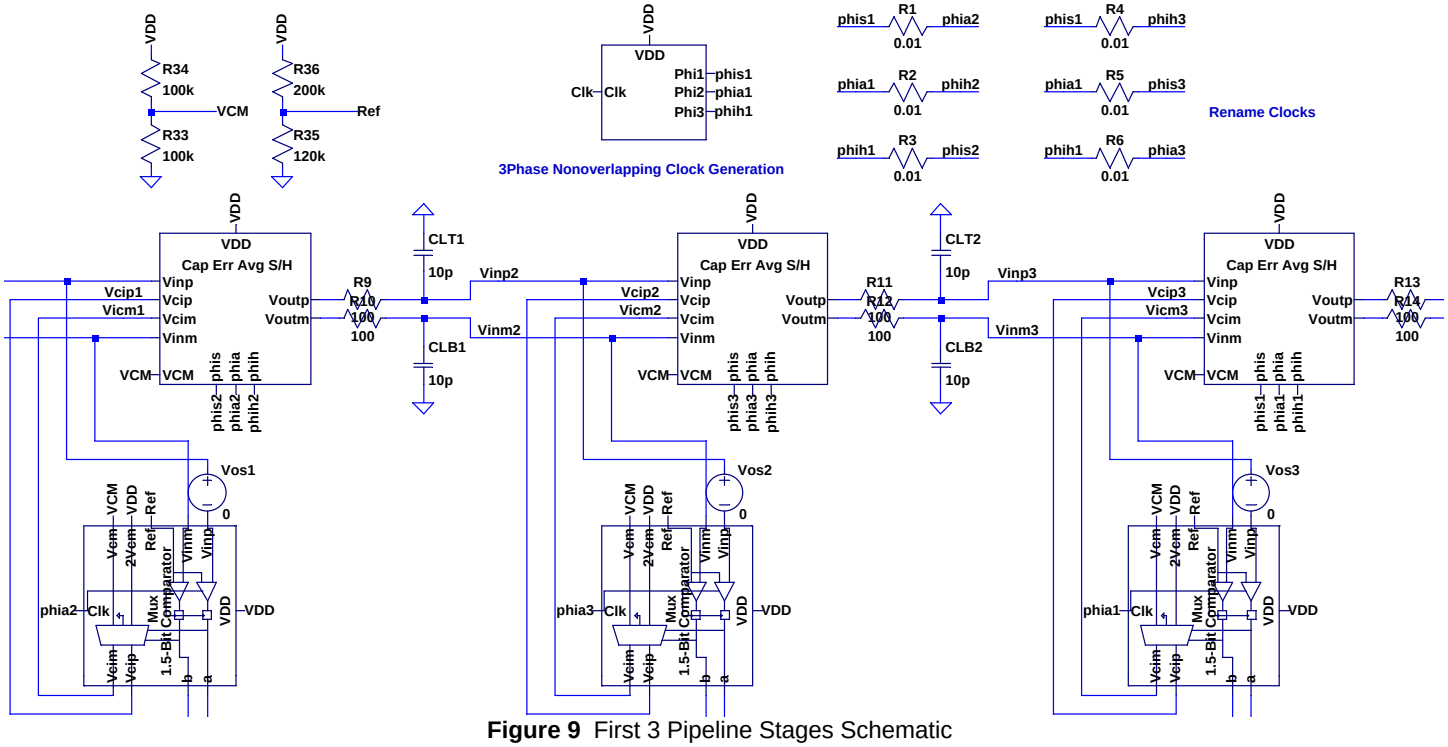



**Figure 9** First 3 Pipeline Stages Schematic

Figure 9 shows the first three stages of the pipeline ADC. The capacitor average error averaging sample and hold cells are the top three blocks, and the comparator and multiplexer cells are the bottom three blocks. This schematic also shows

the $V_{CM}$ and $Ref = 3V_{CM}/4$ generating resistive voltage dividers. The three phase clock generation is also shown. The clock generation is done once to create one set of three phase clock signals, and those signals are renamed for use in the subsequent stages of the pipeline. Figure 10 shows each of the three sets of three phase clock signals. The pattern of clock signals is repeated for the additional stages of the pipeline.

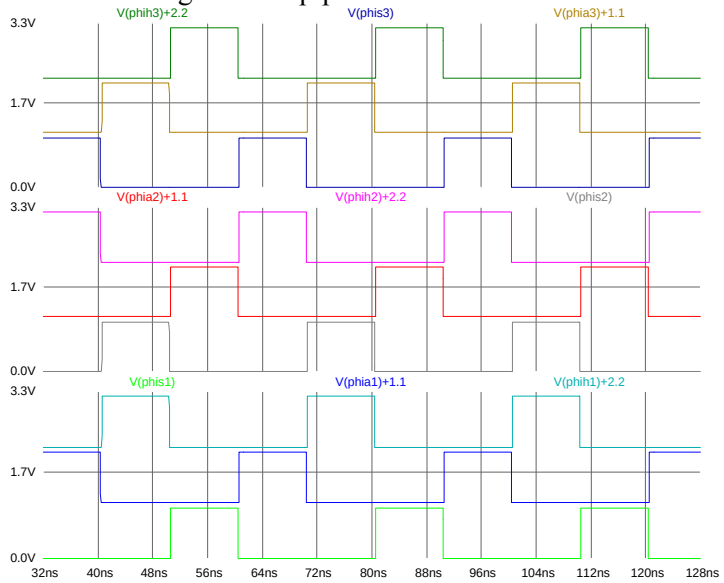
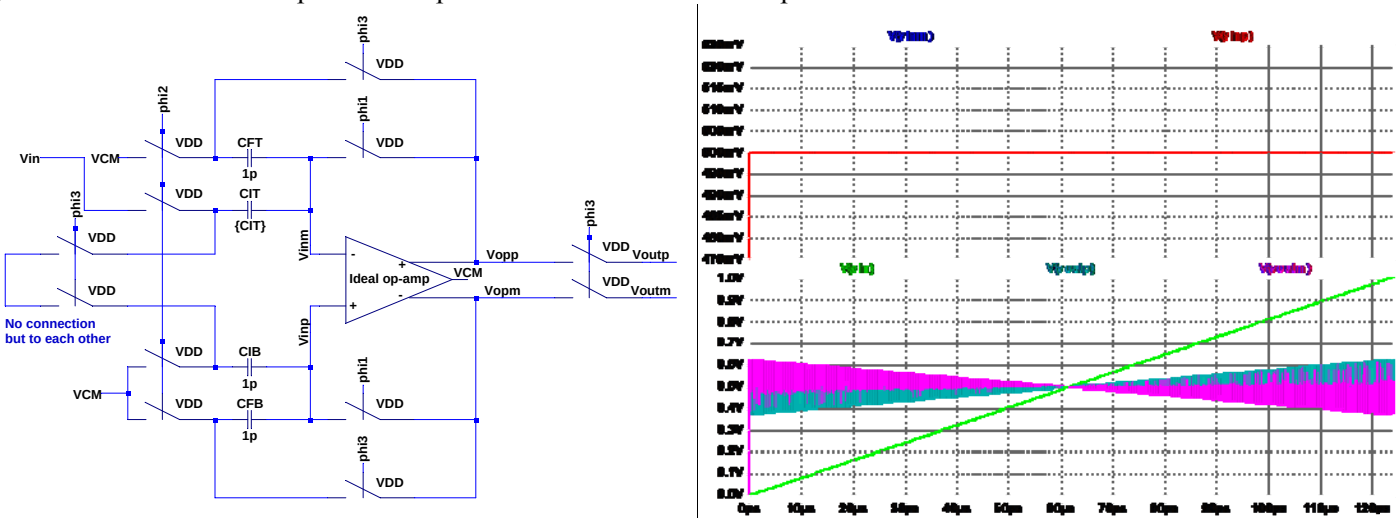



**Figure 10** Single Stage Transfer Curve Simulation

Another important component of the design is a circuit to take the single-ended analog input of ADC and convert it to a differential analog signal with a common mode reference of $V_{CM}$. The circuit shown in Figure 11(a) is one way to convert the single-ended input to differential. The circuit is a basic bottom plate sample and hold that is modified with one of the inputs tied to $V_{CM}$ and the other input broken up between the input and $V_{CM}$. This is to keep the input common mode range of the op-amp at or near $V_{CM}$. Figure 11(b) shows the simulations results for this circuit which demonstrate that for an input ramp of 0V to 1V the common mode voltage on the op-amp does not change. Errors arise with this circuit since it has gain that is determined by $C_I/C_F$ that is set to 1 for this application. Thus, there will be some gain error from this circuit that will show up in the ADC output due to capacitor mismatch. Figure 12 shows the error from the single-ended input to the differential output for three cases of $C_{IT}$ equal to 0.9pF, 1pF, and 1.1pF. This result shows the effect of the gain error that will show up on the output of the ADC due to this capacitor mismatch.




(a) Schematic (b) Simulation Results

**Figure 11** Single-Ended to Differential Sample and Hold

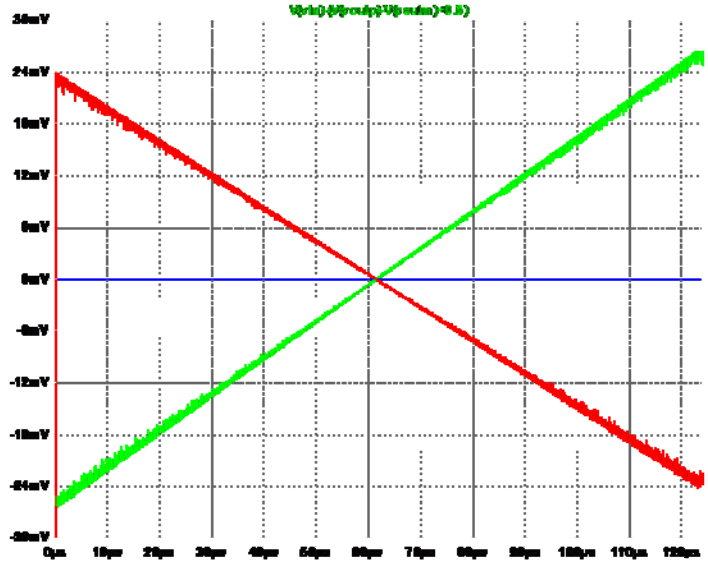


**Figure 12** Single-Ended to Differential Gain Error Simulation Results

Before cascading the stages of the pipeline together, the design needs to implement the logic specified in Equations 3 through 6. Figure 13 shows how the design implements this logic using basic and full adders. Note that both true and complement versions of *a* are required. Figure 13 only shows the first 5 least significant bits of the 13-bit word out of the logic, but the logic is same for all bits except the first two bits and the last bit. The logic for the last 3 most significant bits is shown in Figure 14.

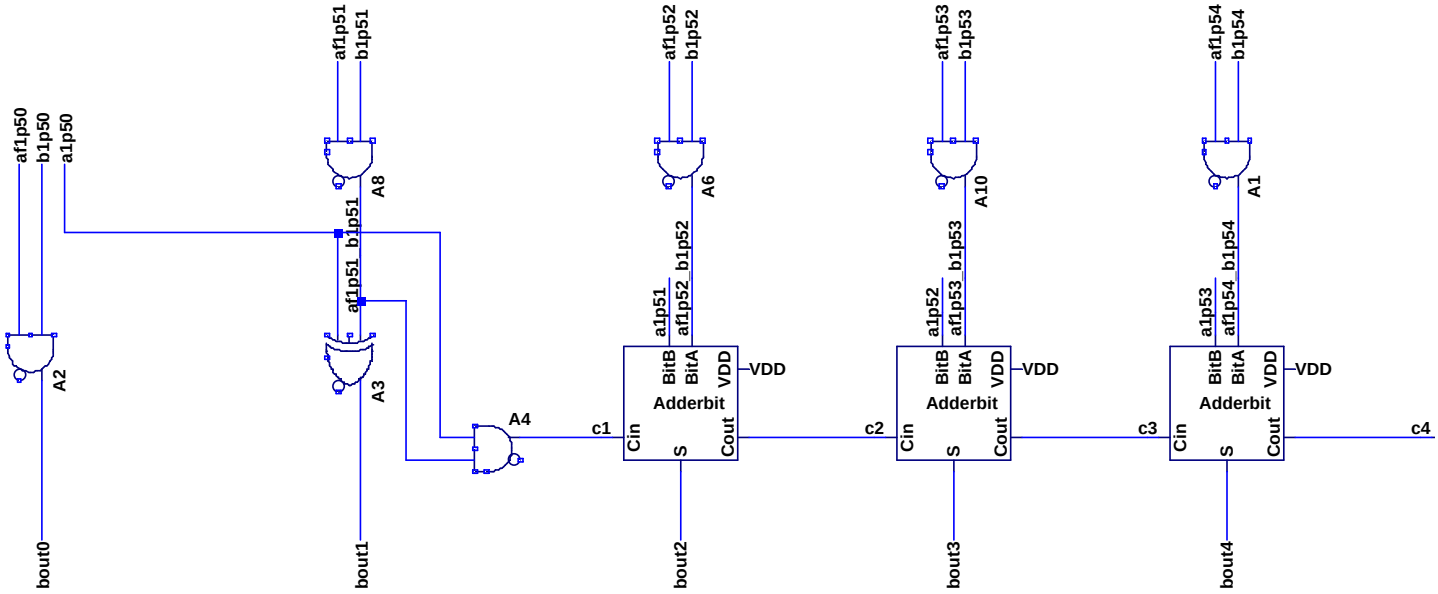



**Figure 13** Logic to Combine the First 1.5 Bit/Stage Outputs

After the *a* and *b* outputs of the 1.5 bits/stage are combined into a binary word, the logic needs to subtract $V_{CM}$ – 0.5 LSB as described in Equation 7 from the digital output code. The equivalent operation is to add the negative value of this to the binary output. This way, the full adders can be used. The 13-bit binary two's complement of $-V_{CM}$ + 0.5 LSB is 1100000000001. The schematic that adds this as a hard coded value to the output word is shown in Figure 15.

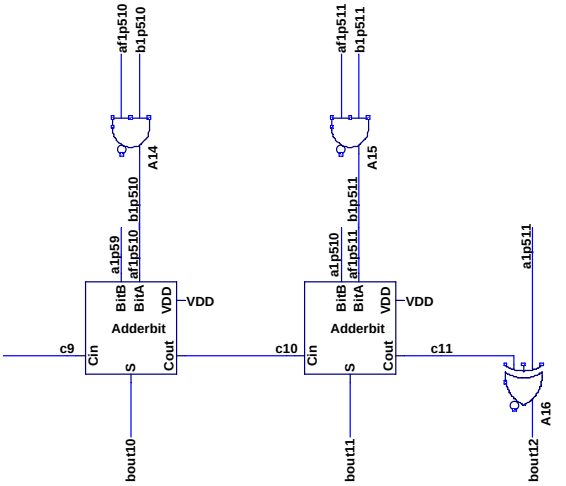



**Figure 14** Logic to Combine the Last 1.5 Bit/Stage Outputs

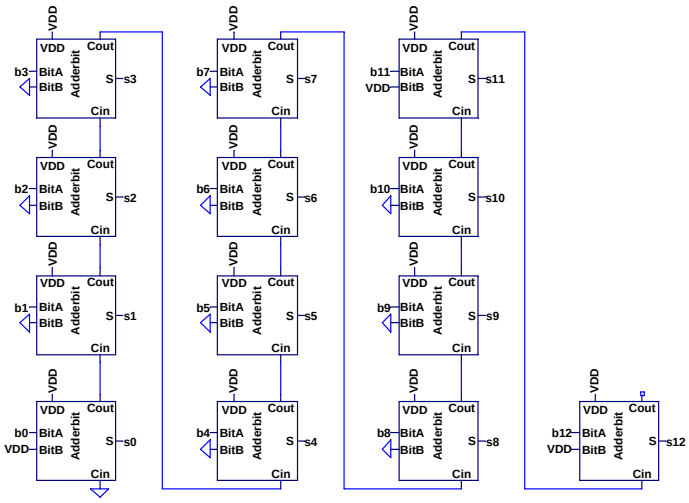



**Figure 15** Subtract $V_{CM}$ Cell Schematic

The design cannot simply take the *a* and *b* outputs of each stage and directly apply them to the logic shown in Figures 13 and 14, because the pipeline processes the analog signal stage by stage each on a different clock cycle. The problem is that the data is available first for the MSB stages and is available many clock cycles later for the LSB stages. The solution is to add latches to delay the data for each stage of the pipeline to match the data coming out of the last stage. This way, the data for each stage is available at the same time for the logic perform is function. Since the stages are sharing the three phase clocks for the capacitor error averaging, the clocking of the data is not 1-to-1. This means that the first stage does need 12 latched clock delays to match the output of the 12$^{th}$ stage. Table 1 shows the number of flip-flops this design used to time align the *a* and *b* data going into the adder logic.

| Significance | Stage | #FF Delays |
|---|---|---|
| MSB | 1 | 8 |
| | 2 | 8 |
| | 3 | 7 |
| | 4 | 6 |
| | 5 | 6 |
| | 6 | 5 |
| | 7 | 4 |
| | 8 | 4 |
| | 9 | 3 |
| | 10 | 2 |
| | 11 | 2 |
| LSB | 12 | 1 |

**Table 1** Logic to Combine the Last 1.5 Bit/Stage Outputs

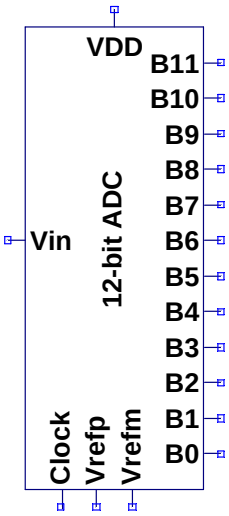



**Figure 16** Subtract $V_{CM}$ Cell Schematic

The top level design symbol is shown in Figure 16, and the top level design schematic is shown in Figure 17. Although the details cannot be seen from the schematic, the Figure does show how the different number of flip-flops are connected to the outputs of each stage. Additionally, it shows how some to the pieces are connected together. The single-ended to differential conversion stage is first followed by 12 stages of the sample and hold and comparators with multiplexer blocks. The complete digital logic for combining the *a* and *b* outputs of the 1.5 bits/stage comparators is at the bottom right. The subtraction cell and a final 12-bit register are directly above the digital logic. The purpose of the final 12-bit register is to synchronize the data to the clock at the final output, which is necessary since real adders will have some delay.

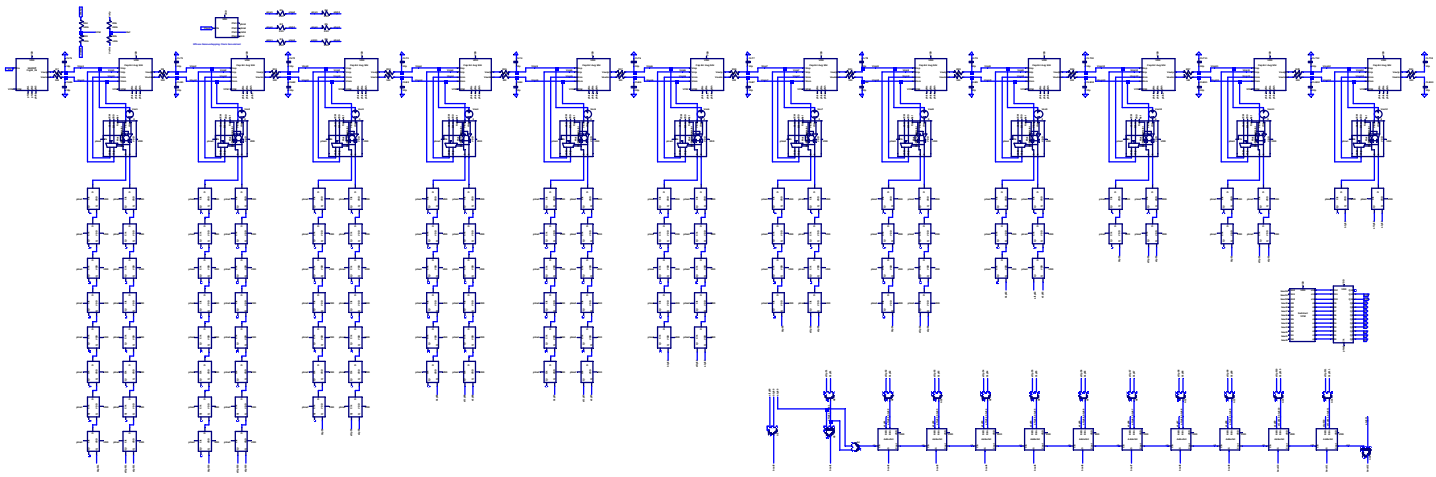
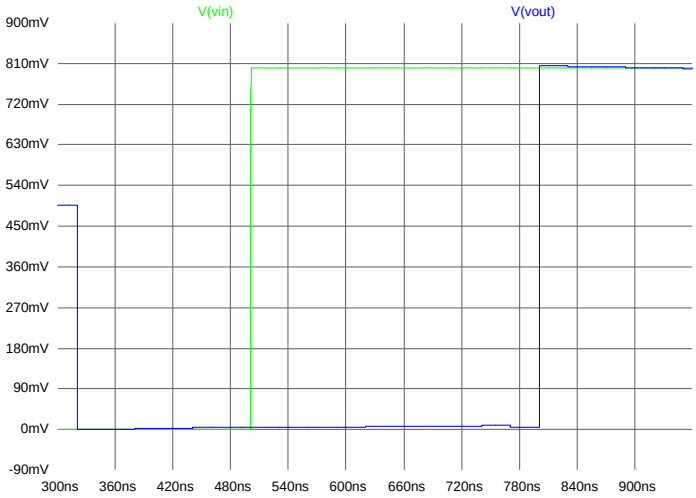


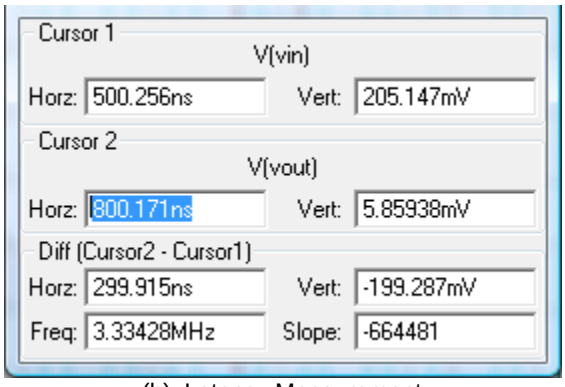
**Figure 17** Logic to Combine the First 1.5 Bit/Stage Outputs

## 3. Characterization Results

Figure 18 characterizes the delay or latency of the pipeline ADC. Figure 18(a) shows the simulation stimulus and output of an ideal digital to analog converter (DAC) that converts the digital output code from the pipeline ADC back to analog voltage. The input voltage is a step from 0V to 0.8V. Figure 18(b) gives the results of measuring from the time the input pulses high to the time when the same pulse is seen on the output. These plots show a 300ns latency with an input clock frequency of 100MHz, which means the latency is 30 clock cycles.




(a) Latency Simulation Waveforms

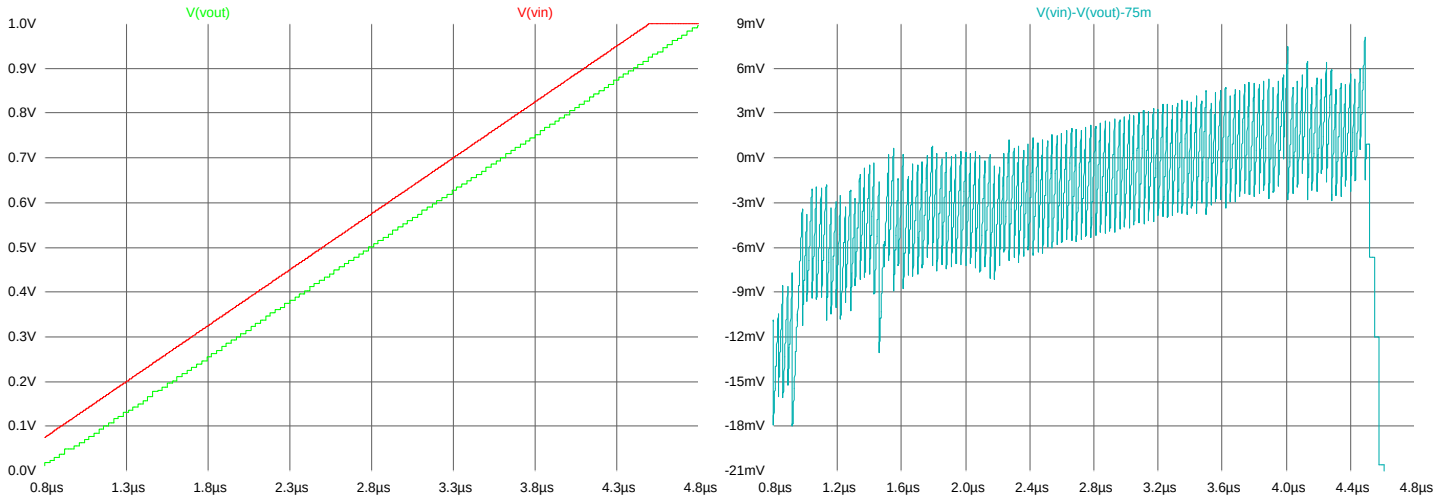



(b) Latency Measurement

**Figure 18** Latency Characterization Simulation Results

Figure 19 shows the simulation results for the ideal pipeline ADC with no comparator offsets, op-amp offsets, or capacitor mismatches. Figure 19(a) shows the analog equivalent output of the pipeline ADC compared to the input ramp. The results show that the output closely matches the input and there are no non-monotonicities. Figure 19(b) gives more detailed perspective of the error between the input and output of the ADC or quantization error. This plot is generated by subtracting the input from the output and also subtracting the static error due to the latency of the pipeline ADC. This factor is based on the latency calculated from Figure 18(b) of 300ns and given the input ramp from 0V to 1V over 4us which translates to about 75mV. Of course, there will always be some quantization error for an ADC since it has a finite

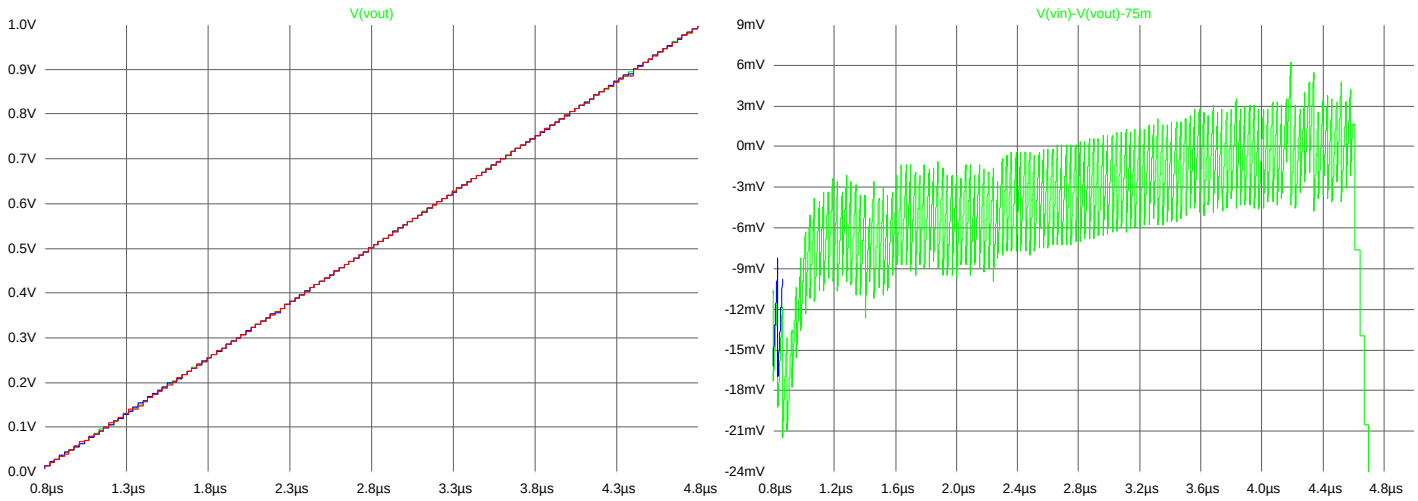
The steeper the input ramp voltage the larger difference between input and output, but ideally the peaks high should be at 0V. The results show that the INL and DNL error are good, but that there may be some gain error which is likely coming from the initial single-end to differential sample and hold. Note that these results cannot be used to determine if the ADC is 12-bit accurate since the ramp is not exercising all 4096 output word combinations.




(a) $V_{out}$ and $V_{in}$ Plot (b) Quantization Error Estimation Plot

**Figure 19** Ideal Ramp Simulation

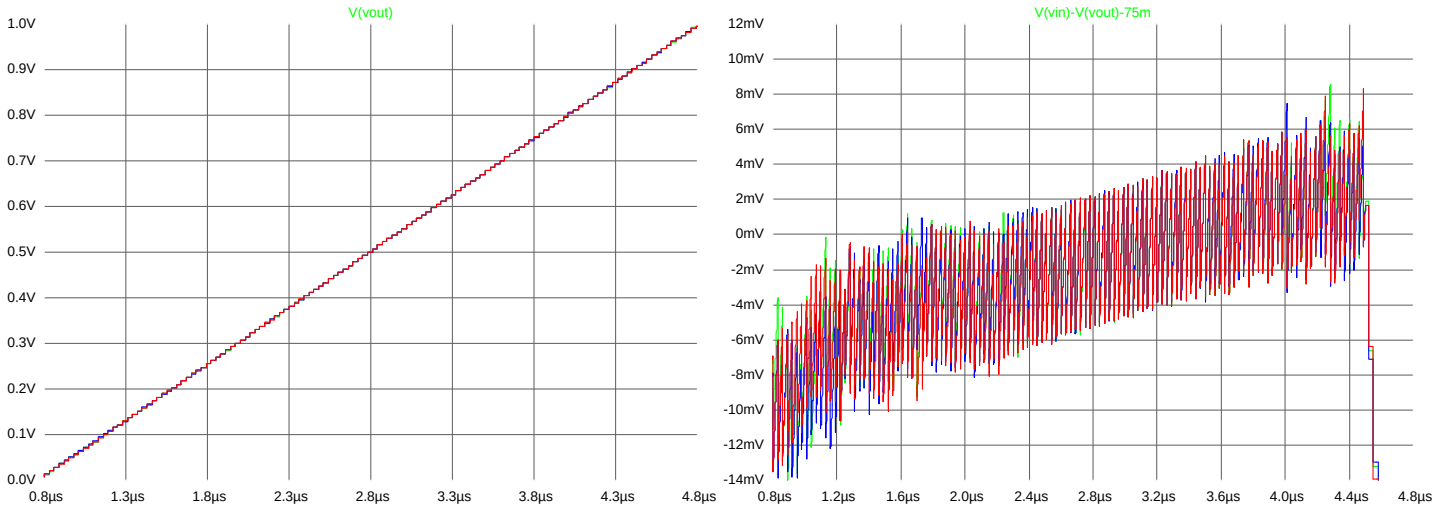
Figure 20 shows the output of the pipeline ADC with all the comparators having an offset on the positive terminal. The green waveform is the baseline and has a comparator offset of 0V. The blue waveform has a comparator offset of 50mV. And, the red waveform has a comparator offset of 75mV. Very little difference can be observed between the ideal case and the offset cases. This proves that the 1.5 bit/stage and error correction logic are able to cancel out these offset levels to a first order.




(a) $V_{out}$ Plot (b) Quantization Error Estimation Plot

**Figure 20** Comparator Offset Simulation

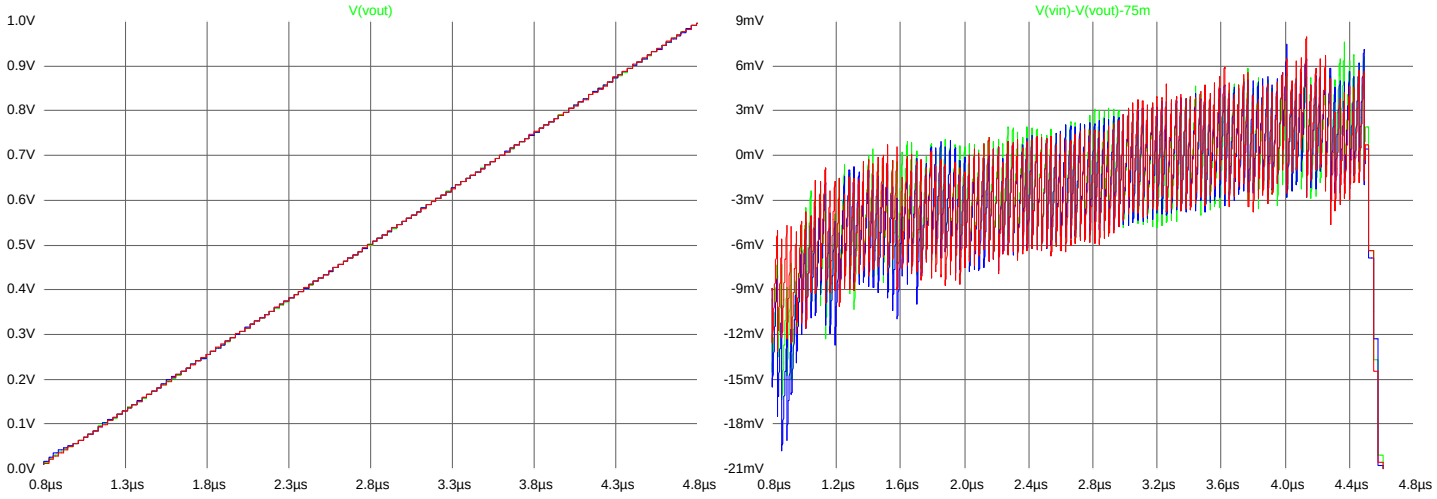
Figure 21 shows the output of the pipeline ADC with all of the op-amps having an offset on the negative terminal. Again, the green waveform is the baseline and has an op-amp offset of 0V. The blue waveform has an op-amp offset of 50mV. And, the red waveform has an op-amp offset of 100mV. There are some small differences in the quantization error with the op-amp offsets, but these are not significant.




(a) $V_{out}$ Plot (b) Quantization Error Estimation Plot

**Figure 21** Op-Amp Offset Simulation

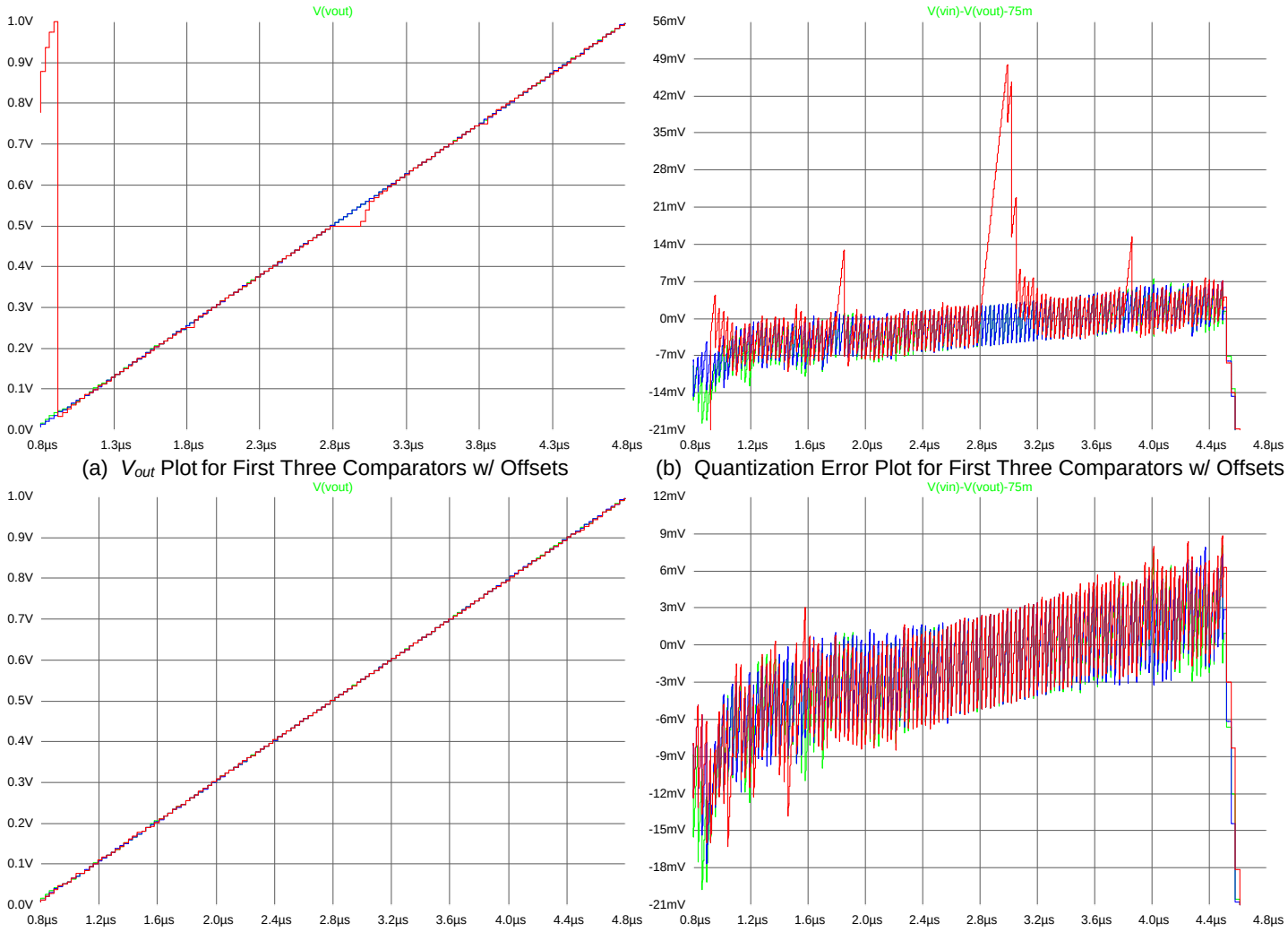
Figures 22(a) and (b) show the output of the ADC and the quantization error with capacitor mismatches in all of the sample and hold cells. Both the $C_{IT}$ and $C_{IT1}$ capacitors in the sample and hold circuit shown in Figure 6 are varied. Both capacitors are set to 1pF (displayed in green), 0.9pF (displayed in blue), and 1.1pF (displayed in red). Again, there are some small differences in the quantization error with the op-amp offsets, but these are not significant.




(a) $V_{out}$ Plot (b) Quantization Error Estimation Plot

**Figure 22** Capacitor Mismatch Simulation

Figures 23(a) and (b) show the output of the ADC and an estimate for the quantization error with comparator offsets in the first three pipeline stages. The comparator offset is set to 0V (displayed in green), 75mV (displayed in blue), and 150mV (displayed in red). The 150mV offset case results in significant DNL errors at and around 0V, 250mV, 500mV and 750mV. These points make sense, because these are the points where the first three comparators make their decisions. The 1.5 bit/stage error correction does help, but cannot completely remove this offset. The 75mV offset makes little difference as is shown in Figure 20(b) where all the comparators have the same offset. Figures 23(c) and (d) show the output of the ADC and the quantization error with comparator offsets in the last three pipeline stages. Interestingly, even the offset of 150mV has little affect on the INL and DNL error when it is present in the last stages only.




(a) $V_{out}$ Plot for First Three Comparators w/ Offsets

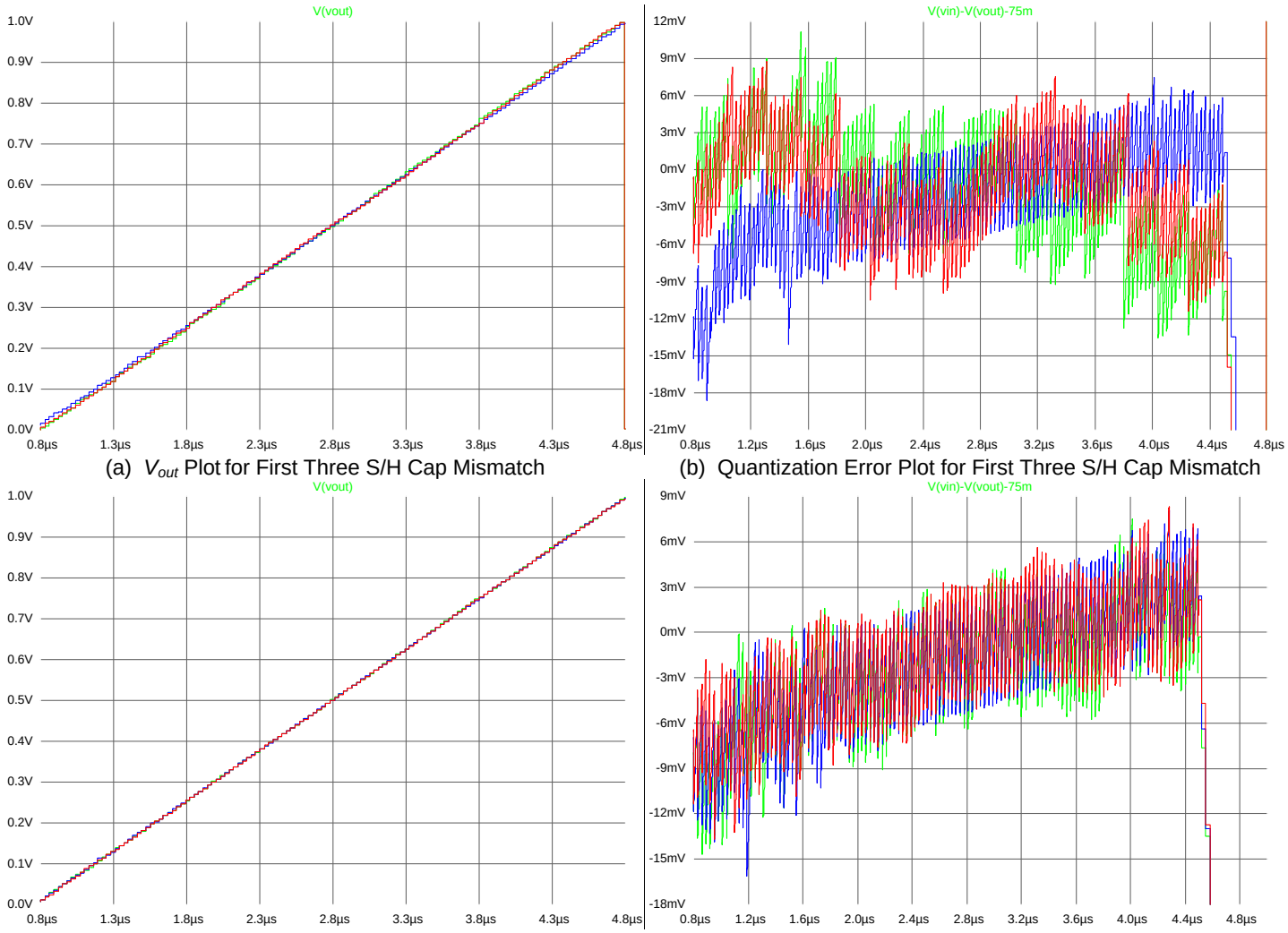
(b) Quantization Error Plot for First Three Comparators w/ Offsets

(c) $V_{out}$ Plot for Last Three Comparators w/ Offsets

(d) Quantization Error Plot for Last Three Comparators w/ Offsets

**Figure 23** Simulation Results with Different Stage Offsets

Figures 24(a) and (b) show the output of the ADC and the quantization error with sample and hold capacitor mismatches in the first three stages of the pipeline. Both the $C_{IT}$ and $C_{IT1}$ capacitors in the sample and hold circuit shown in Figure 6 are varied. They are both set to 1pF (displayed in green), 0.5pF (displayed in blue), and 1.5pF (displayed in red). Both cases of this high capacitor mismatch (±50%) show increases in the INL and DNL error from the ideal case. While, Figures 24(c) and (d) show the output of the ADC and the quantization error with sample and hold capacitor mismatches in the last three stages of the pipeline. Both cases with this amount of capacitor mismatch show some increased INL and DNL error, but both errors are much less significant when the capacitor mismatch is the last few stages.




(a) $V_{out}$ Plot for First Three S/H Cap Mismatch

(b) Quantization Error Plot for First Three S/H Cap Mismatch

(c) $V_{out}$ Plot for Last Three S/H Cap Mismatch

(d) Quantization Error Plot for Last Three S/H Cap Mismatch

**Figure 24** Simulation Results with Different Stage Switched Capacitor Mismatch

## 4. Finite Gain Experiment

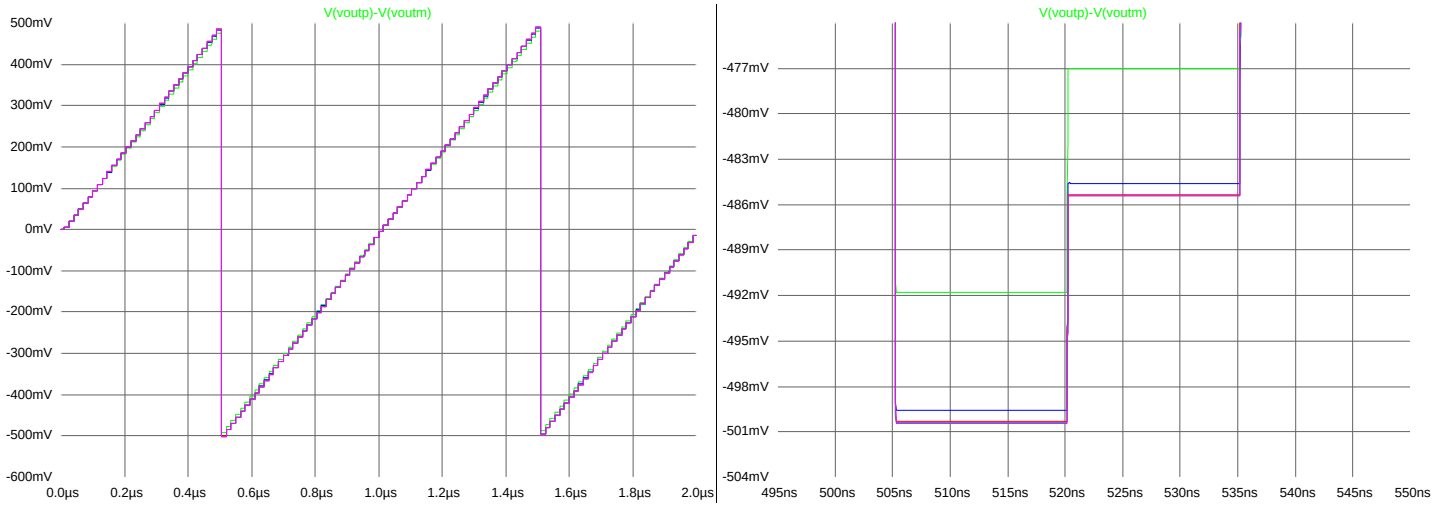
Thus far, the analysis and characterization of the design has assumed that the op-amps in the sample and hold circuit have effectively infinite gain. This section attempts to examine the effects of finite open loop op-amp gain on the performance of the sample and hold cell. Recall from Equation 2 that to get the $v_{out}$ of a pipeline stage, the $v_{in}$ must be multiplied by 2 and some value is subtracted or added based on the $a$ and $b$ outputs of the comparators. This subtraction or addition is done with the $V_{CI}$ inputs to the sample and hold shown in Figure 6. The equation that ideally relates $v_{out}$ to $v_{in}$ in terms of $V_{CI}$ is given by

$$v_{out} = v_{out+} - v_{out-} = 2(v_{in+} - v_{in-}) - (V_{CI+} - V_{CI-}). \quad \text{(Eq. 8)}$$

This equation assumes that there is no offset in the op-amps, the capacitors are exactly the same, and the op-amp gain is sufficiently high. The hand derivations in Appendix A show that there is an error factor when the gain is finite. These derivations assume that the gain of both op-amps is the same value of $A_{OL}$, that there is no offset in the op-amps, and that the capacitors are exactly matched to simplify the equations. The equation for the output of the averaging sample and hold when the op-amps have finite gain is given by

$$v_{out} = v_{out+} - v_{out-} = \left(\frac{A_{OL}^2}{A_{OL}^2+4A_{OL}+4}\right)[2(v_{in+} - v_{in-}) - (V_{CI+} - V_{CI-})]. \quad \text{(Eq. 9)}$$

This equation shows that the output of the sample and hold will be reduced by some factor that depends on the gain of the op-amps. If the open loop gain is 100, the output swing of the sample and hold will be 96.1% of its ideal value. If the open loop gain is 1000, the output swing of the sample and hold will be 99.6% of its ideal value. Figure 25(a) shows the effect on the single stage transfer curve previously shown in Figure 7(a) when the op-amp gain is swept from 100 (plotted in green), 1K (plotted in blue), 10K (plotted in red), and 100K (plotted in pink). Figure 25(b) is a zoomed in plot of Figure 25(a) at the point where the error is at its maximum. These results show the relationship between the open loop gain and the error on the output as Equation 9 predicts.




(a) $V_{out}$ Plot (d) Zoomed $V_{out}$ Plot

**Figure 25** Capacitor Error Averaging Affect of Finite Op-Amp Gain

The characterization results of the 12-bit pipeline ADC have shown that the design is tolerant to op-amp offset and capacitor mismatch in the sample and hold. The tolerance to capacitor mismatch is due to using the capacitor error averaging sample and hold topology shown in Figure 6. The question that also arises is "How does the performance of the capacitor error average compare to a single stage sample and hold when the op-amp gain is low?" Figure 26 shows the topology for the "single stage" bottom plate sample and hold. This topology uses only one op-amp to do the sample, hold, subtract and multiply by 2 operations. There is no swapping of the capacitors and no second stage to average two output values, so this topology will be susceptible to capacitor mismatch error. Although it is not proven in the hand calculations, it is presumed that since this topology has only one op-amp the error will be the square root of the error term from Equation 9. This means that for the topology in Figure 26, the $v_{out}$ can be estimated by

$$v_{out} = v_{out+} - v_{out-} = \left(\frac{A_{OL}}{A_{OL}+2}\right)[2(v_{in+} - v_{in-}) - (V_{CI+} - V_{CI-})]. \quad \text{(Eq. 10)}$$

Figure 27(a) shows the maximum differential error for the single stage sample and hold in Figure 26, while Figure 27(b) shows the maximum differential error for the capacitor error averaging sampled and hold. In these plots, the op-amp gain is swept from 100 (plotted in green), 1K (plotted in blue), 10K (plotted in red), and 100K (plotted in light blue). These results show that the single stage sample and hold topology has less error due to finite op-amp gain. The capacitor averaging sample and hold has slightly less than twice the maximum error compared to the single stage sample and hold. This makes sense based on Equations 9 and 10. If $A_{OL}$ is 100, the "error term" is 96.1% for the capacitor error averaging case and 98.0% for the single stage case. This means that using capacitor error averaging has more of a decrease in performance from finite op-amp gain than the standard single stage bottom plate sample and hold.

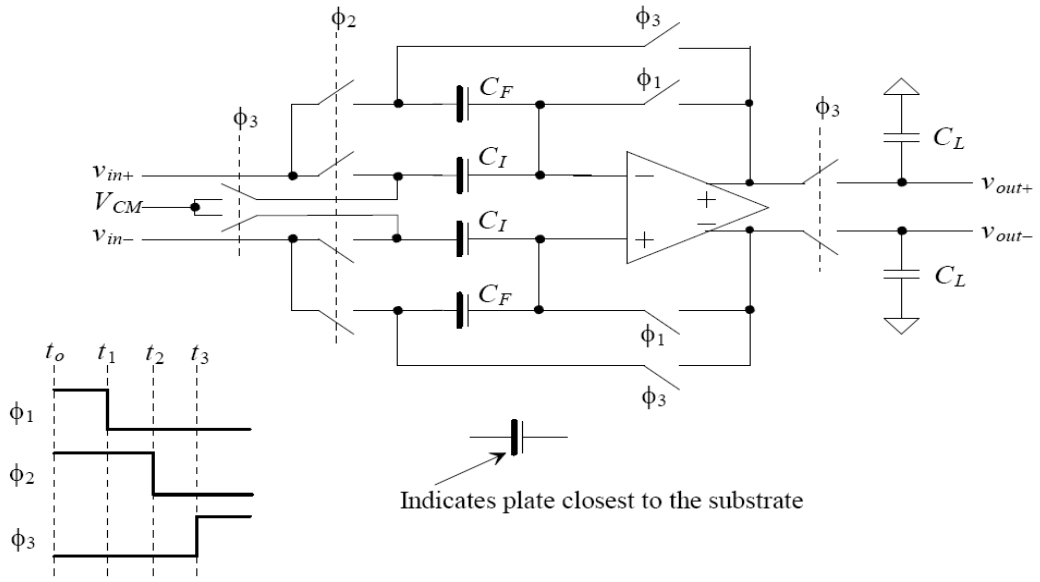
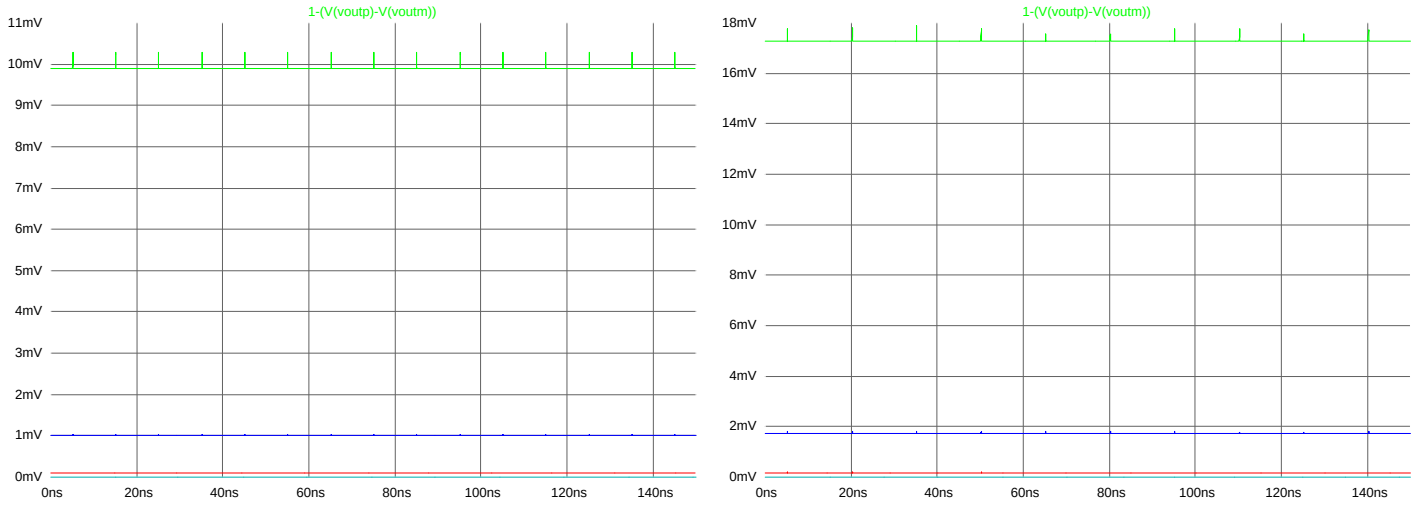



**Figure 26** Single Op-Amp Bottom Plate Sample and Hold [1]




(a) Single Stage Sample and Hold (d) Capacitor Error Averaging Sample and Hold

**Figure 27** Maximum Error for Finite Op-Amp Gain Sample and Hold

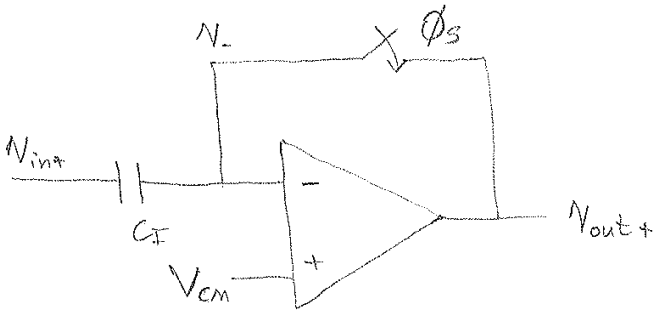
## 5. References

[1] R. J. Baker, *CMOS: Circuit Design, Layout, and Simulation 3rd ed.*, Jon Wiley and Sons Publishers, 2010. ISBN 978-0-0470-88132-3.

## A. Hand Calculations

First, consider the simple sample case:

Simple Sample Case




When the Øs switch closes

$$V_{out+} = V_-$$

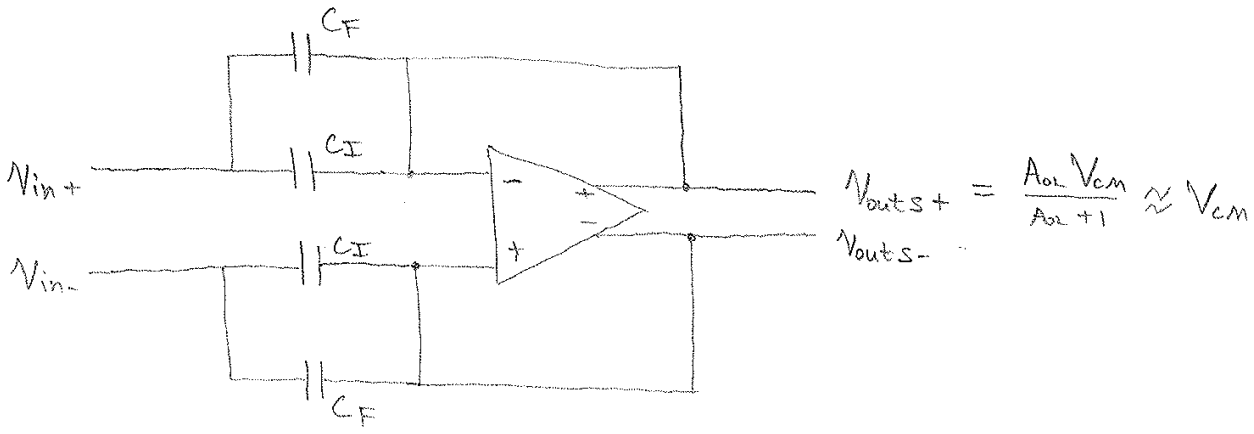
$$V_{out+} = A_{OL}\left(V_+ - V_-\right) = A_{OL}\left(V_{cm} - V_{out+}\right)$$

$$\left(1 + A_{OL}\right) V_{out+} = A_{OL} V_{cm}$$

$$V_{out+} = \frac{A_{OL} V_{cm}}{A_{OL} + 1} \approx V_{cm}$$

Next, consider the first stage of the capacitor error averaging sample and hold shown in Figure 6.

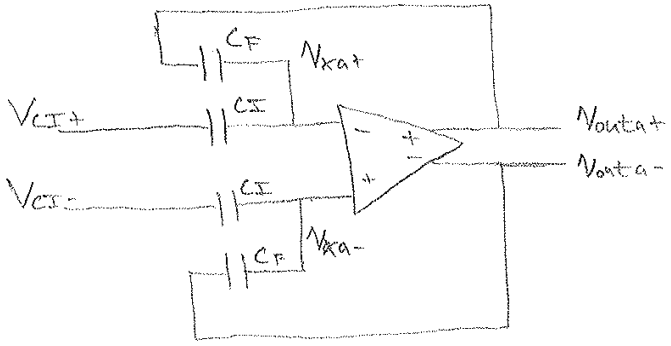
When the $\phi_s$ switch closes




Consider positive (+) signal first. Assume $\pm V_{os} = 0$ and $C_I = C_F$.

$$Q_{I,F}^{\phi_s} = C_{I,F}\left(V_{in+} - V_{CM}\right)$$

When the $\phi_a$ switch closes




$$Q_I^{\phi_a} = C_I\left(V_{CI+} - V_{xa+}\right)$$

For charge to be conserved

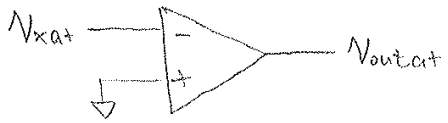
$$Q_F^{\phi_a} = Q_I^{\phi_s} + Q_F^{\phi_s} - Q_I^{\phi_a}$$

$$C_F\left(V_{outa+} - V_{xa+}\right) = C_I\left(V_{in+} - V_{cm}\right) + C_F\left(V_{in+} - V_{cm}\right) - C_I\left(V_{CI+} - V_{xa+}\right)$$

Solve for $V_{outa+}$

$$V_{outa+} = 2V_{in+} - V_{CI+} - 2V_{cm} + 2V_{xa+}$$

Using the following




$$V_{outa+} = A_{OL}\left(0 - V_{xa+}\right) = -A_{OL}V_{xa}$$

$$V_{xa+} = -\frac{V_{outa+}}{A_{OL}}$$

$$V_{outa+} = 2V_{in+} - V_{CI+} - 2V_{cm} - \frac{2V_{outa+}}{A_{OL}}$$

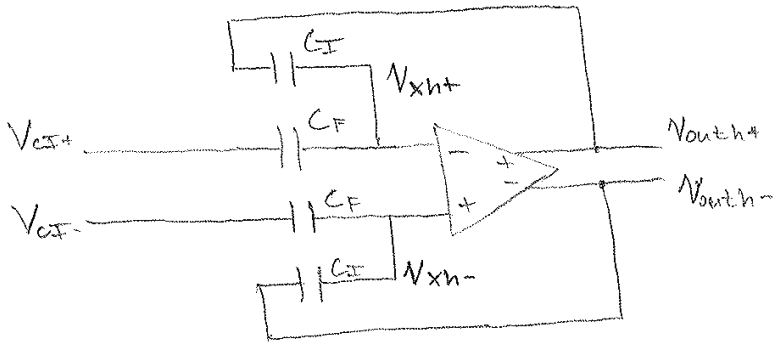
$$\left(1 + \frac{2}{A_{OL}}\right)V_{outa+} = 2V_{in+} - V_{CI+} - 2V_{cm}$$

$$V_{outa+} = \left(\frac{A_{OL}}{A_{OL}+2}\right)\left(2V_{in+} - V_{CI+} - 2V_{cm}\right)$$

Similarly

$$V_{outa-} = \left(\frac{A_{OL}}{A_{OL}+2}\right)\left(2V_{in-} - V_{CI-} - 2V_{cm}\right)$$

When the $\phi_h$ switch closes




From $\phi_a$ phase

$$Q_F^{\phi_a} = C_F\left(V_{outa+} - V_{xa+}\right) \qquad + \qquad Q_I^{\phi_a} = C_I\left(V_{cI+} - V_{xa+}\right)$$

For charge to be conserved

$$Q_I^{\phi_h} = Q_F^{\phi_a} + Q_I^{\phi_a} - Q_F^{\phi_h}$$

$$C_I\left(V_{outh+} - V_{xh+}\right) = C_F\left(V_{outa+} - V_{xa+}\right) + C_I\left(V_{cI+} - V_{xa+}\right) - C_F\left(V_{cI+} - V_{xh+}\right)$$

Solve for $V_{outh+}$

$$V_{outh+} = V_{outa+} - 2V_{xa+} + 2V_{xh+}$$

Using

$$V_{xh+} = -\frac{V_{outh+}}{A_{OL}} \qquad + \qquad V_{xa+} = -\frac{V_{outa+}}{A_{OL}}$$

$$V_{outh+} = V_{outa+} + 2\frac{V_{outa+}}{A_{OL}} - 2\frac{V_{outh+}}{A_{OL}}$$

$$\left(1 + \frac{2}{A_{OL}}\right) V_{outh+} = \left(1 + \frac{2}{A_{OL}}\right) V_{outa+}$$

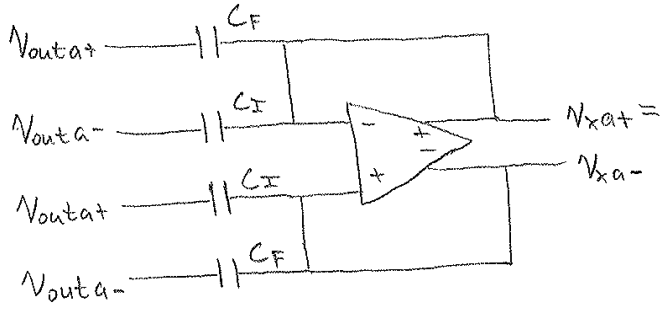
$$V_{outh+} = V_{outa+}$$

Similarly

$$V_{outh-} = V_{outa+}$$

Last, consider the averaging stage of Figure 6.

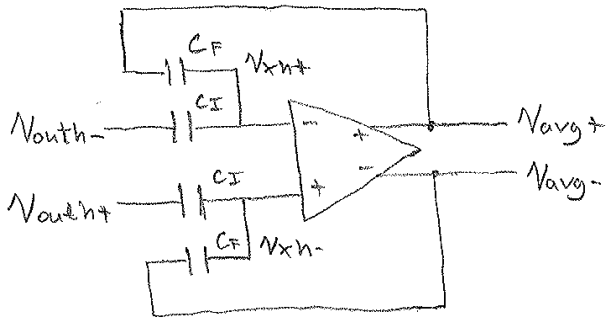
For averging stage, when $\phi a$ switches close,




$$V_{xa+} = \frac{A_{OL} V_{CM}}{A_{OL}+1} \approx V_{CM}$$

$$Q_I^{\phi a} = C_I (V_{outa-} - V_{CM}) \quad \& \quad Q_F^{\phi a} = C_F (V_{outa+} - V_{CM})$$

When the $\phi h$ switches close




$$Q_I^{\phi h} = C_I (V_{outh-} - V_{xh+}) \quad \& \quad Q_F^{\phi h} = C_F (V_{avg+} - V_{xh+})$$

For charge to be conserved

$$Q_F^{\phi h} = Q_I^{\phi a} + Q_F^{\phi a} - Q_I^{\phi h}$$

$$C_F (V_{avg+} - V_{xh+}) = C_I (V_{outa-} - V_{CM}) + C_F (V_{outa+} - V_{cm}) - C_I (V_{outh-} - V_{xh+})$$

Solve for $V_{avg+}$

$$V_{avg+} = V_{outa-} + V_{outa+} - 2V_{cm} - V_{outh-} + 2V_{xh+}$$

Where we know

$$V_{xh+} = -\frac{V_{avg}}{A_{OL}} \quad \& \quad V_{outh-} = V_{outa-}$$

$$v_{avg+} = v_{outa+} - 2v_{cm} - 2\frac{v_{avg+}}{A_{OL}}$$

$$\left(1+\frac{2}{A_{OL}}\right)v_{avg+} = v_{outa+} - 2v_{cm}$$

$$v_{avg+} = \left(\frac{A_{OL}}{A_{OL}+2}\right)\left(v_{outa+} - 2v_{cm}\right)$$

$$v_{avg+} = \left(\frac{A_{OL}}{A_{OL}+2}\right)\left[\left(\frac{A_{OL}}{A_{OL}+2}\right)\left(2v_{in+} - v_{CI+} - 2v_{cm}\right) - 2v_{cm}\right]$$

$$v_{avg+} = \left(\frac{A_{OL}^2}{A_{OL}^2+4A_{OL}+4}\right)\left(2v_{in+} - v_{CI+} - 2v_{cm}\right) - \left(\frac{2A_{OL}}{A_{OL}+2}\right)v_{cm}$$

Similarly

$$v_{avg-} = \left(\frac{A_{OL}^2}{A_{OL}^2+4A_{OL}+4}\right)\left(2v_{in-} - v_{CI-} - 2v_{cm}\right) - \left(\frac{2A_{OL}}{A_{OL}+2}\right)v_{cm}$$

$$v_{avg} = v_{avg+} - v_{avg-} = \left(\frac{A_{OL}^2}{A_{OL}^2+4A_{OL}+4}\right)\left[2\left(v_{in+} - v_{in-}\right) - \left(v_{CI+} - v_{CI-}\right)\right]$$