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From: SAFPAOSP.Workflow@pentagon.af.mil
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Subject: 88 ABW Case Completed: Case Number 88ABW-2012-3988

88 ABW has completed the review process for your case on 17 Jul 2012:

Subject: Integrated Circuit Design CAD Tool Information (Course Description)

Originator Reference Number: AFITENG141
Case Reviewer: William Huntington
Case Number: 88ABW-2012-3988

The material was assigned a clearance of CLEARED on 17 Jul 2012. This email serves as the official notice of the disposition of this case. If you have additional questions, contact the Review Manager for your case, William Huntington, william.huntington@wpafb.af.mil.

88th ABW PUBLIC AFFAIRS SECURITY AND POLICY REVIEW WORKSHEET

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11. OTHER AGENCY COORDINATION REQUIRED *(List contact information)*

12. OTHER INFORMATION

13. NATIONAL SECURITY STATUTES/TECHNOLOGY ISSUES

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☐ 6.1. ☐ 6.3. ☑ N/A
☐ 6.2. ☐ 6.4./HIGHER ☐ OTHER _____

16. EXPLANATION

Reference material for students' personal laptops outside of AFIT; share with other colleagues at civilian schools

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			88ABW20123988

Air Force Institute of Technology
Department of Electrical and Computer Engineering

Integrated Circuit Design CAD Tool Information

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E-mail: helpdesk@afit.edu

This work contains common CAD tool information used for the courses EENG653, EENG695, and EENG795. It has been adapted from similar material used at Tufts, Columbia, University of Virginia, and University of Utah. The Linux material is provided by the University of Surrey (UK) and O'Reilly.

Questions or comments for improvements on this document should be sent to mary.lanzerotti@afit.edu. Cadence is a trademark of Cadence Design Systems, Inc., 2655 Seely Avenue, San Jose, CA 95134

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Kenneth Shepard, Columbia University

Jan Van der Spiegel, University of Pennsylvania

Sameer Sonkusale, Tufts University

Mircea Stan, University of Virginia

Air Force Institute of Technology
Department of Electrical and Computer Engineering

Integrated Circuit Design CAD Tool Information

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Air Force Institute of Technology
Department of Electrical and Computer Engineering

Integrated Circuit Design CAD Tool Information

Integrated Circuit Design CAD Tool Information

1. General Information and Linux Account Information

a. Modern industrial integrated-circuit-design CAD tools will be an integral part of this course. All students in the courses must have access to the CAD tool setup at AFIT. This page contains relevant administrative information for all you need to do to get started with these tools.

b. Read the following:

- **i.** You will use the Linux workstations in the VLSI CAD Lab (Building 640, Room 332)
- **ii.** You need an active login ID

c. Prior to the first class, I will collect a list of student names in the class and send the list to the AFIT Help Desk (helpdesk@afit.edu). I will request that the AFIT Help Desk set up the computer accounts.

d. All students should look for an email messages from either Mr. David Doak or Mr. Donald Bodle with your Linux account information and requesting that you stop by the SC Help Desk ("SC") to set your password.

Following the first lecture, after you receive this email, all students should go to the SC Help Desk and ask for "Unix Help." You will be redirected to another section of SC to Mr. Doak or to Mr. Bodle who will show you how to set your Linux password.

e. As soon as you have your password, you are able to start these labs and can log in to the VLSI Linux machines in the VLSI CAD Lab.

After the first week of class, any problems with login access to the machines should be addressed to Mr. David Doak: helpdesk@afit.edu, the AFIT Systems Administrator.

2. Guidelines for Working in the VLSI CAD Lab

a. The VLSI CAD Lab is maintained by the Electrical and Computer Engineering Department.

b. Do not bring any friends/visitors to the lab and let them use the machines on your account. These are not public machines.

c. Food and drinks are allowed, BUT you must be VERY careful and clean up after yourself.

d. The quota for each student is 20 GB. Please keep only relevant files in your home.

e. Do NOT fire huge printing jobs at the lab printer. Printers are for your convenience and printing anything other than HW or project files is NOT permitted. Also, do not try to print tool documentation. Such files are hundreds of pages.

f. Do NOT reboot the machines. Contact system administrators in case the machine hangs or freezes

g. System Administrator: Mr. David Doak: helpdesk@afit.edu

h. We encourage doing your homework and projects in Building 640, Room 332. This allows the professor and System Administrator to do a walk-through and help you. It also allows you to help each other.

i. All paths for CAD tools should be automatically set.

3. A Beginner's Guide to the Unix and Linux Operating System

a. Linux is a Unix-like operating system.

b. If you are not familiar with Unix and Linux, the following link provides a beginner's guide to the Unix and Linux operating system. Eight tutorials cover the basics of UNIX/Linux commands. These tutorials and summaries below were developed by M.Stonebank@surrey.ac.uk. They are reproduced here for your reference during these tutorials.

c. The link is: http://www.ee.surrey.ac.uk/Teaching/Unix

d. Introduction to the UNIX Operating System

e. Tutorial One Summary

Command	**Meaning**
ls	list files and directories
ls –a	list all files and directories
mkdir	make a directory
cd *directory*	change to named directory
cd	change to home-directory
cd ~	change to home-directory
cd ..	change to parent directory
pwd	display the path of the current directory

f. Tutorial Two Summary

Command	**Meaning**
cp *file1 file2*	copy file1 and call it file2
mv *file1 file2*	move or rename file1 to file2
rm *file*	remove a file
rmdir *directory*	remove a directory
cat *file*	display a file
less *file*	display a file a page at a time
head *file*	display the first few lines of a file
tail *file*	display the last few lines of a file
grep *'keyword' file*	search a file for keywords
wc *file*	count number of lines/words/characters in file

g. Tutorial Three Summary

Command	**Meaning**
command > *file*	redirect standard output to a file
command >> *file*	append standard output to a file
command < *file*	redirect standard input from a file
command1 | command2	pipe the output of command1 to the input of command2
cat *file1 file2* > *file0*	concatenate file1 and file2 to file0
sort	sort data
who	list users currently logged in

h. Tutorial Four Summary

Command	**Meaning**
*	match any number of characters
?	match one character
man *command*	read the online manual page for a command
whatis *command*	brief description of a command
apropos *keyword*	match commands with keyword in their man pages

i. Tutorial Five Summary

Command	**Meaning**
ls –lag	list access rights for all files
chmod [options] file	change access rights for named file
command &	run command in background
^C	kill the job running in the foreground
^Z	suspend the job running in the foreground
bg	background the suspended job
jobs	list current jobs
fg %1	foreground job number 1
kill %1	kill job number 1
ps	list current processes
kill 26152	kill process number 26152

j. Tutorial Six Summary

Other Useful UNIX Commands	**Meaning**
quota	disk space on the file system
df	space left
du	number of kilobytes in each subdirectory
gzip	reduces file size
zcat	reads gzipped file
file	classifies the named files
diff	compares two files and displays the differences
find	searches through directories for files and directories for attribute
History	C shell keeps an ordered list of all entered commands

k. Tutorial Seven Summary

Command	**Meaning**
make	Manage large programs or groups of programs
makefile	Set of compile rules in a text file

l. Tutorial Eight Summary

Variables	**Meaning**
UNIX variables	A way to pass information from the shell to programs
Environment variables	Set by the setenv command
Shell variables	$history, $cwd, $HOME, $PATH, $prompt; % set | less

4. Linux Quick Reference: O'Reilly (www.oreilly.com)

a. Some Useful Commands

Linux Quick Reference

SOME USEFUL COMMANDS

Command	Task
File/Directory Basics	
ls	List files
cp	Copy files
mv	Rename files
rm	Delete files
ln	Link files
cd	Change directory
pwd	Print current directory name
mkdir	Create directory
rmdir	Delete directory
File Viewing	
cat	View files
less	Page through files
head	View file beginning
tail	View file ending
nl	Number lines
od	View binary data
xxd	View binary data
gv	View Postscript/PDF files
xdvi	View TeX DVI files
File Creation and Editing	
emacs	Text editor
vim	Text editor
umask	Set default file protections
soffice	Edit Word/Excel/ PowerPoint docs
abiword	Edit Word documents
gnumeric	Edit Excel documents
File Properties	
stat	Display file attributes
wc	Count bytes/words/lines
du	Measure disk usage
file	Identify file types
touch	Change file timestamps
chown	Change file owner
chgrp	Change file group
chmod	Change file protections
chattr	Change advanced file attributes
lsattr	List advanced file attributes

Command	Task
File Location	
find	Locate files
slocate	Locate files via index
which	Locate commands
whereis	Locate standard files
File Text Manipulation	
grep	Search text for matching lines
cut	Extract columns
paste	Append columns
tr	Translate characters
sort	Sort lines
uniq	Locate identical lines
tee	Copy stdin to a file and to stdout simultaneously
File Compression	
gzip	Compress files (GNU Zip)
compress	Compress files (Unix)
bzip2	Compress files (BZip2)
zip	Compress files (Windows Zip)
File Comparison	
diff	Compare files line by line
comm	Compare sorted files
cmp	Compare files byte by byte
md5sum	Compute checksums
Disks and Filesystems	
df	Show free disk space
mount	Make a disk accessible
fsck	Check a disk for errors
sync	Flush disk caches
Backups and Remote Storage	
mt	Control a tape drive
dump	Back up a disk
restore	Restore a dump
tar	Read/write tape archives
cdrecord	Burn a CD
rsync	Mirror a set of files

O'REILLY
www.oreilly.com

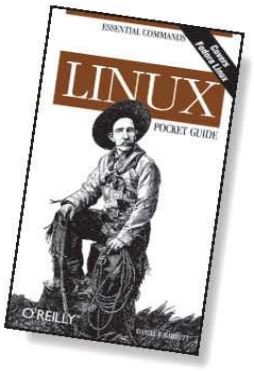
b. Some Useful Commands

Linux Quick Reference

SOME USEFUL COMMANDS

Command	Task
Printing	
lpr	Print files
lpq	View print queue
lprm	Remove print jobs
Spelling Operations	
look	Look up spelling
aspell	Check spelling interactively
spell	Check spelling in batch
Processes	
ps	List all processes
w	List users' processes
uptime	View the system load
top	Monitor processes
xload	Monitor system load
free	Display free memory
kill	Terminate processes
nice	Set process priorities
renice	Change process priorities
Scheduling Jobs	
sleep	Wait for some time
watch	Run programs at set intervals
at	Schedule a job
crontab	Schedule repeated jobs
Hosts	
uname	Print system information
hostname	Print the system's hostname
ifconfig	Set/display network information
host	Look up DNS
whois	Look up domain registrants
ping	Check if host is reachable
traceroute	View network path to a host

Command	Task
Networking	
ssh	Securely log into remote hosts
telnet	Log into remote hosts
scp	Securely copy files between hosts
sftp	Securely copy files between hosts
ftp	Copy files between hosts
evolution	GUI email client
mutt	Text-based email client
mail	Minimal email client
mozilla	Web browser
lynx	Text-only web browser
wget	Retrieve web pages to disk
slrn	Read Usenet news
gaim	Instant messaging/IRC
talk	Linux/Unix chat
write	Send messages to a terminal
mesg	Prohibit talk/write
Audio and Video	
grip	Play CDs and rip MP3s
xmms	Play audio files
cdparanoia	Rip audio
audacity	Edit audio
xcdroast	Burn CDs



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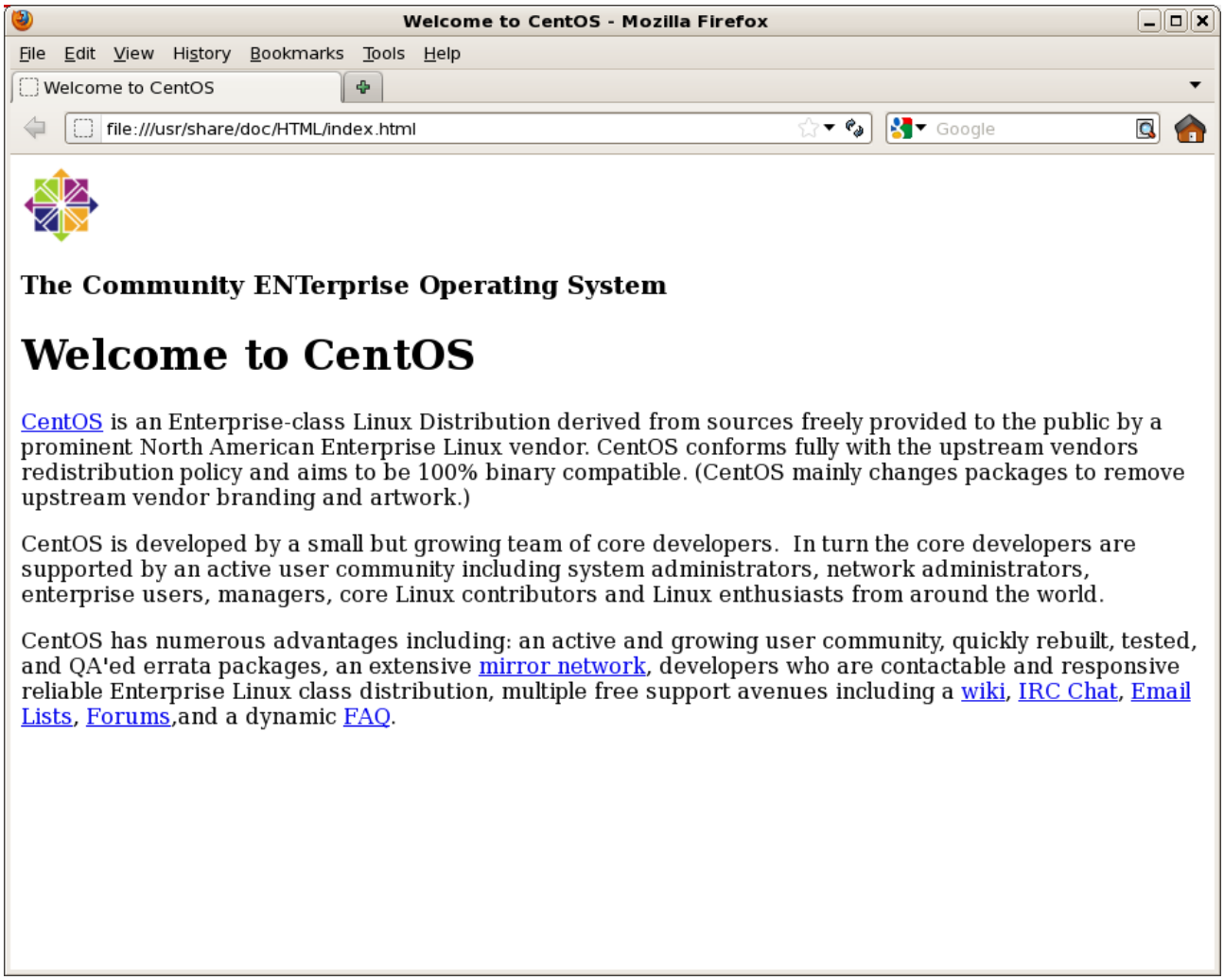
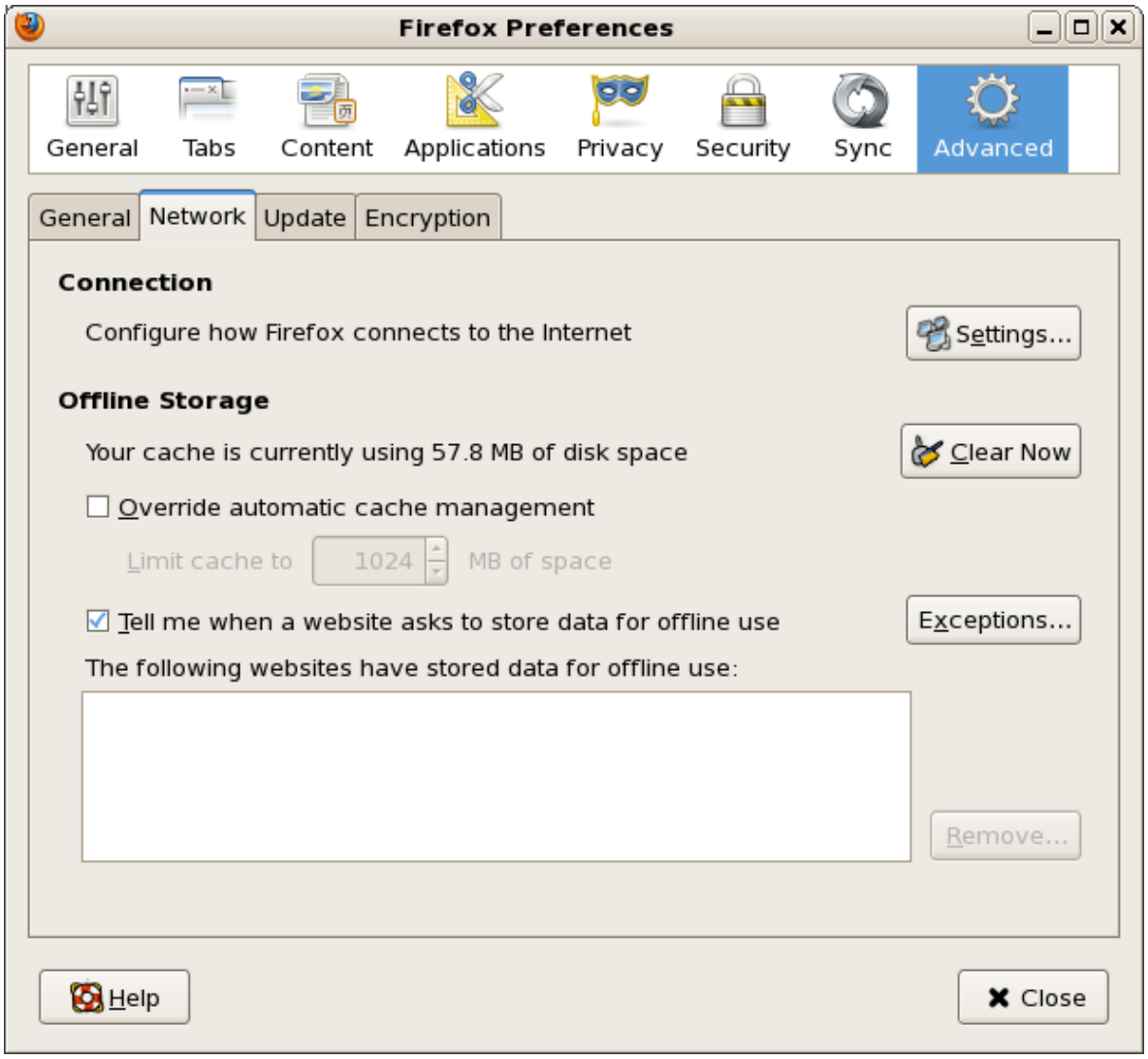
Excerpted from Linux Pocket Reference

5. Setting up Firefox

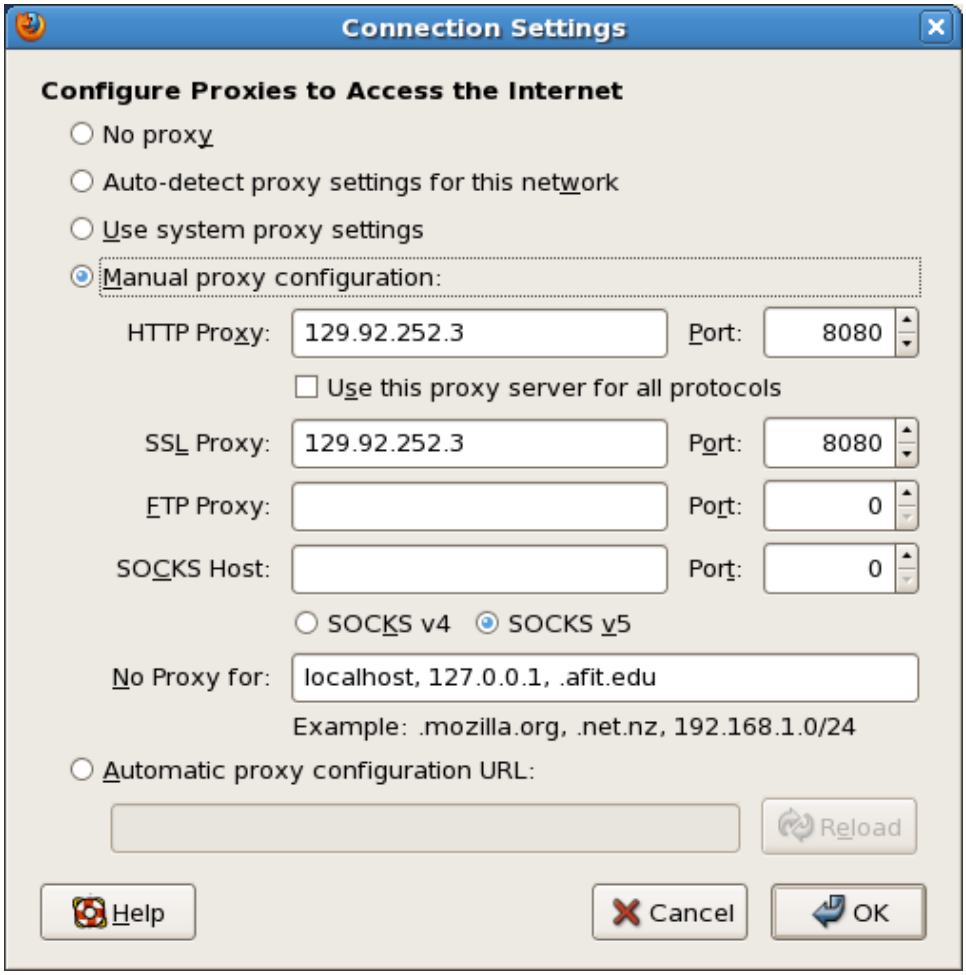
a. In this step you will set up the Proxies for Firefox. Open a Firefox window as shown below.



b. In the banner at the top of the Firefox window, select 'Edit → Preferences" and click on the 'Advanced' button and then the 'Network' tab. The 'Firefox Preferences' window will appear as shown in the image below.



c. In the 'Firefox Preferences' window, select 'Settings.' The 'Connection Settings' window will appear. Select 'Manual proxy configurations" button as shown, with HTTP Proxy: 129.92.252.3 Port: 8080; SSL Proxy: 129.92.252.3 Port: 8080; No Proxy for: localhost, 127.0.0.1, .afit.edu. Then click OK in this window and close the Firefox preferences window.



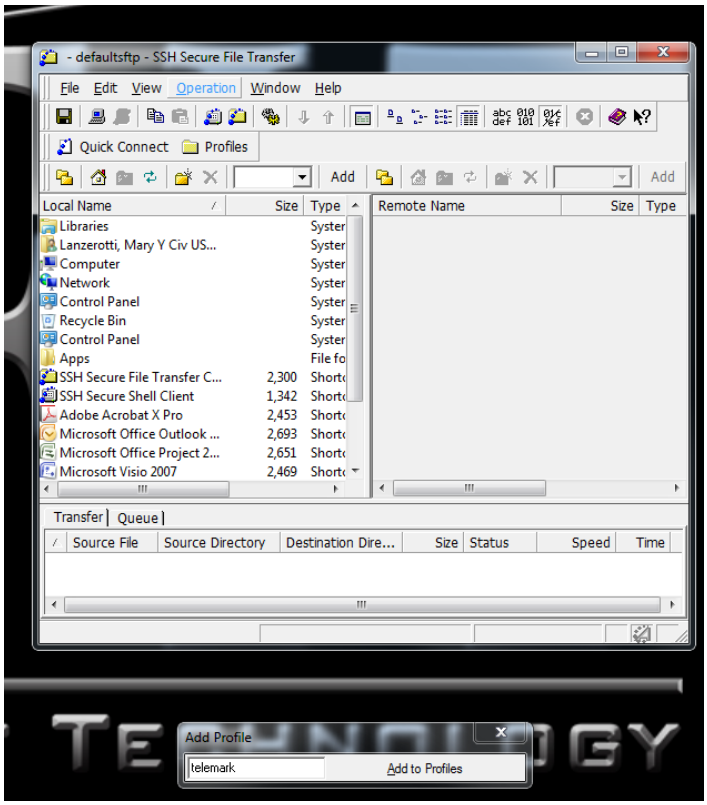
d. You should now be able to access the internet.

6. Setting up Secure Shell (SSH)

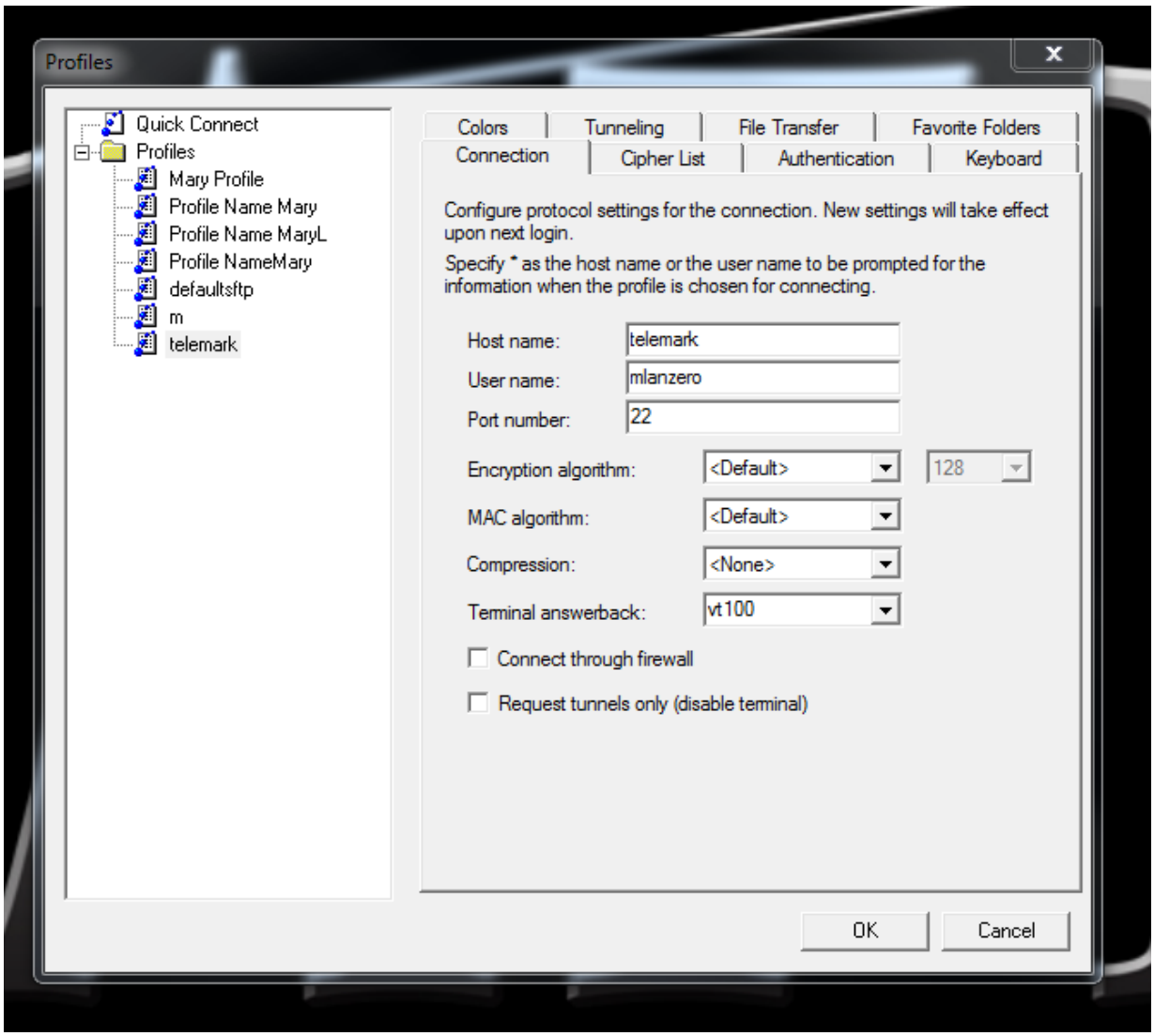
a. On your Windows machine, go to the Start menu and click on "All Programs." Move the cursor to the "SSH Secure Shell" folder, open it, right click on the "Secure File Transfer Client" and then Pin to Taskbar.

b. Open the SSH Secure File Transfer Client (now pinned on your taskbar).

c. In the "SSH Secure File Transfer Client," click on the "Profiles" button (it looks like a yellow folder) and press "Add Profile." The "Add Profile" window will open, and enter "telemark" in the profile name field as shown below. Then click "Add to Profiles."



d. Then click on "Profiles" again and click "Edit Profiles." The Profiles window will appear. In this window, under the "Connection" tab, set "Host name:" to "telemark" and "User name:" to your Linux username (e.g. your first initial followed by your last name). The Port number should already be set to "22" as shown in the image below.



e. Press OK on the "Profiles" window.

f. Now in the "SSH Secure File Transfer" window, click on "Profiles" again and select 'telemark.' Select 'yes' and then click 'OK' on the two windows that appear. Then enter your Linux password in the "Enter Password" window that appears. Click OK after entering your password.

g. In the "SSH Secure File Transfer" window, the left side is your Windows information (click on the pulldown to find the various drives, such as the I: drive). Click on "Computer" and your home directory is located with your Windows username. On the right side is your Linux information. You can navigate to where you have saved the files you want to transfer.

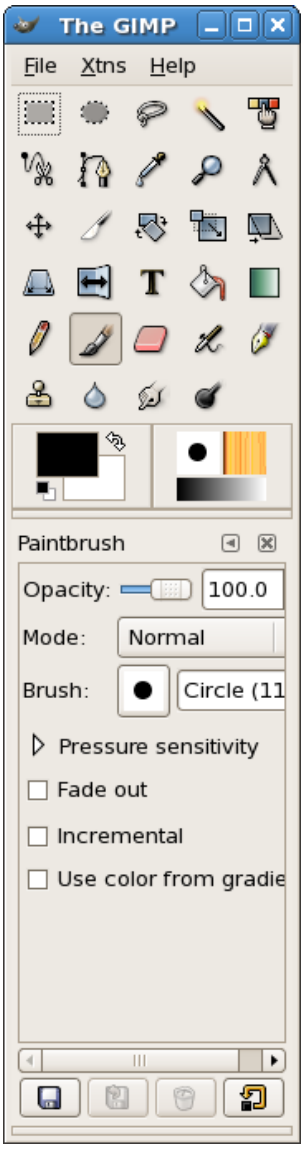
h. When you find the files on the Linux (right) side that you want to transfer to Windows, you will click on the files using 'SHIFT and CNTL" to select multiple files. Then drag the selected files to the Windows side and drop into your desired directory.

i. You can keep this "SSH Secure File Transfer" window open.

j. Use the 'Refresh' (circular arrows) button if you save a new file on Linux.

7. Screen Capture of Images with The GIMP

a. To launch Gimp, move your cursor to the upper-left hand corner of the screen (Linux). Select "Applications → Graphics → The GIMP". The GIMP graphical user interface will appear as shown in the figure below.



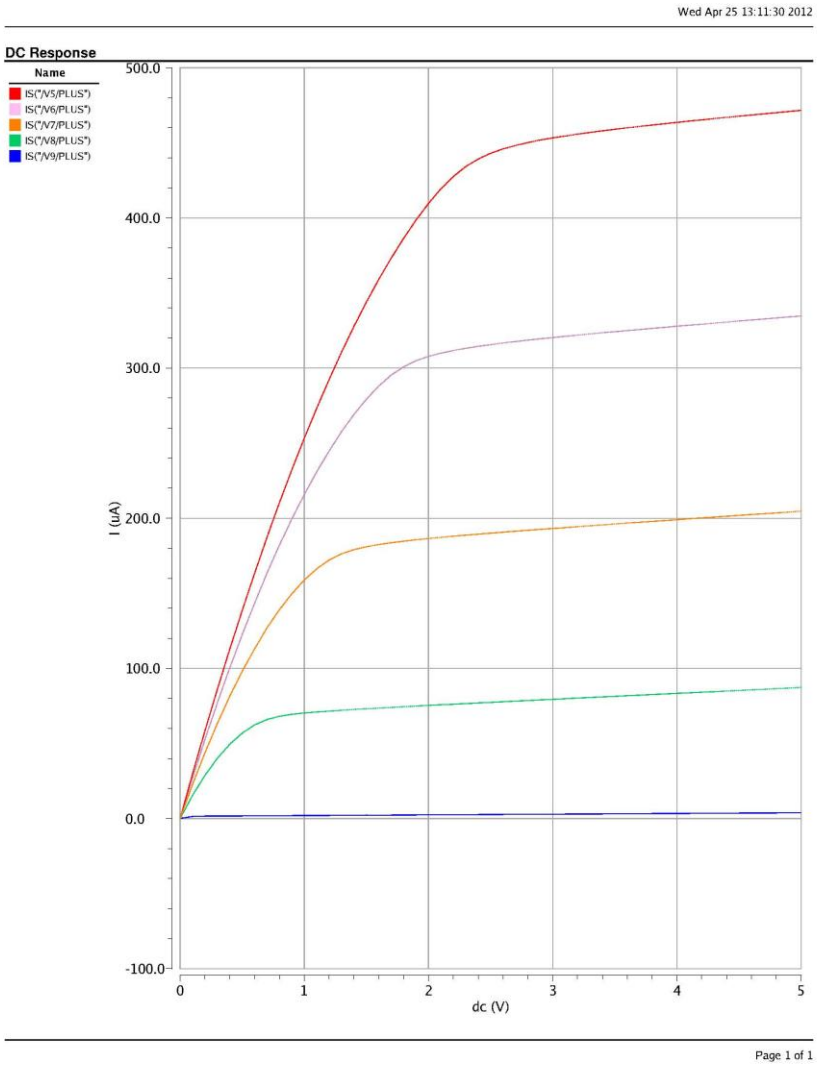
b. On The GIMP GUI, select "File → Acquire → Screen shot." In the Screen Shot window, select "a Single Window" and "1 second delay." Then click Grab.

c. Then click on the window that you wish to save. A Gimp.tif window will appear.

d. Save your window in .tif format with your desired filename in one of your directories. You may also save in other file formats (.tif is preferred; .ps and .eps formats are preferred in LaTex documents; in this document, .tif files are used for the screenshots of Cadence windows).

8. Printing and Plotting

a. To print a Virtuoso ® Visualization & Analysis window, select "File → Print → Print to File (postscript)". A "Print" window will appear. Enter the name of your desired output file in the window. GIMP is able to read ps files generated from a print from the Visualization & Analysis window as shown below.

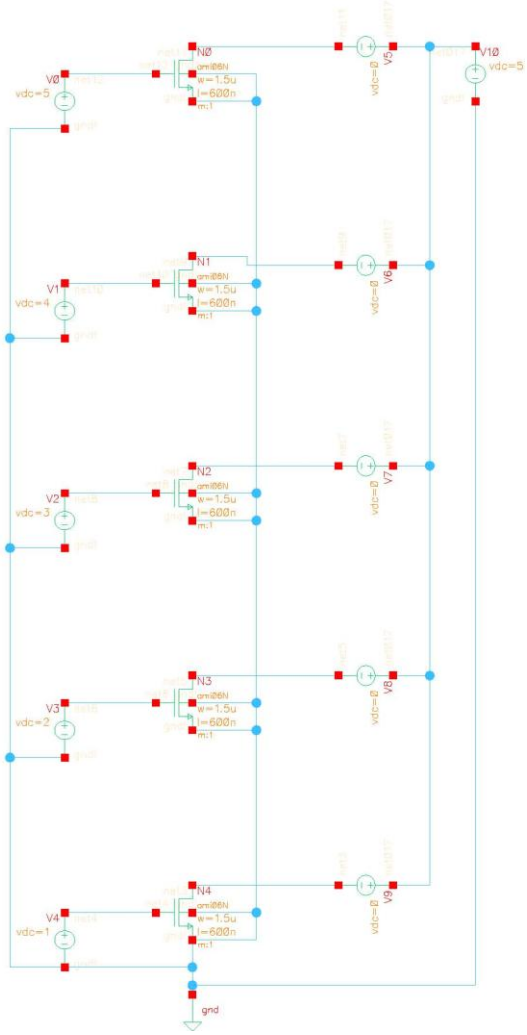


b. To print an entire schematic in a Virtuoso window (Schematic, Layout, Extracted view), select "File → Print → Plot Options" and fill in the print window. You may send the output to your AFIT email account: mary.lanzerotti@afit.edu and the file to <filename.ps> which will be written in your working directory, such as $HOME/cadence/ncsu-cdk-1.6.0.utah folder. Kghostview is able to read multi-page postscript files generated from a Virtuoso Schematic winder. To start Kghostview, in the Linux screen, click on the menu bar: "Applications → Graphics → KGhostView → File → Open." Then point the window to your printed file, which should be in your home directory. Printing with the header information selected will produce a document such as the schematic shown below (two pages).

c. To print a portion of a schematic, select "File → Print → Plot Options" and fill in the print window using the appropriate coordinates of your plot (lower left and upper right coordinates) in the "Area to Plot" field. Be sure to add extra space if you would like to see extra space around the boundary of your plot.


USER: mlanzero
DATE: Thu Apr 26 11:46:47 2012
PLOT SIZE: 5.12 x 9.64 Inches
Library: EENG653Tutorial
Cell: IVcurves
View: schematic
Plot Area: ((-1.7125 -5.25) (2.275 2.2625))

Integrated Circuit Design CAD Tool Information

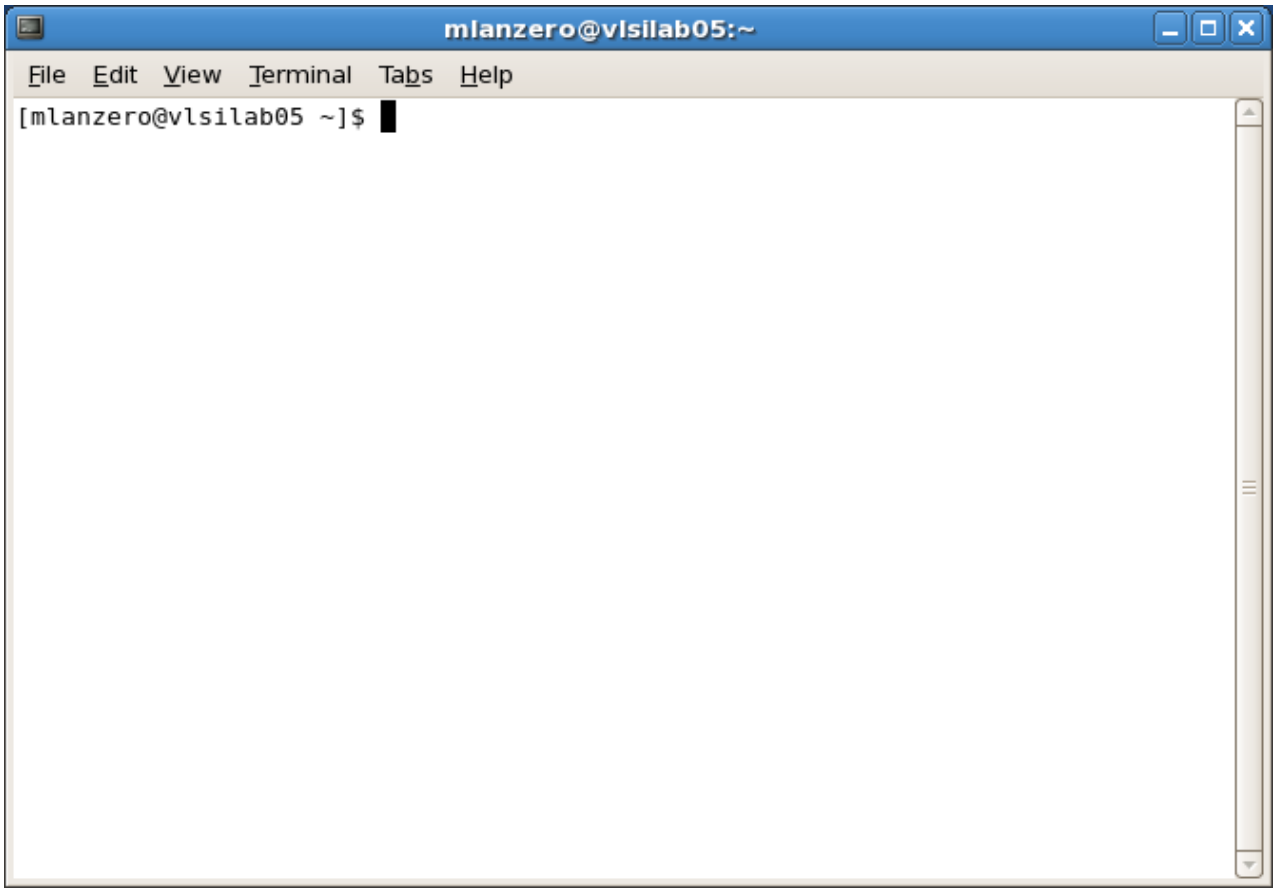


9. Setting up the Linux Environment and Getting Started with Cadence 6.1.5.

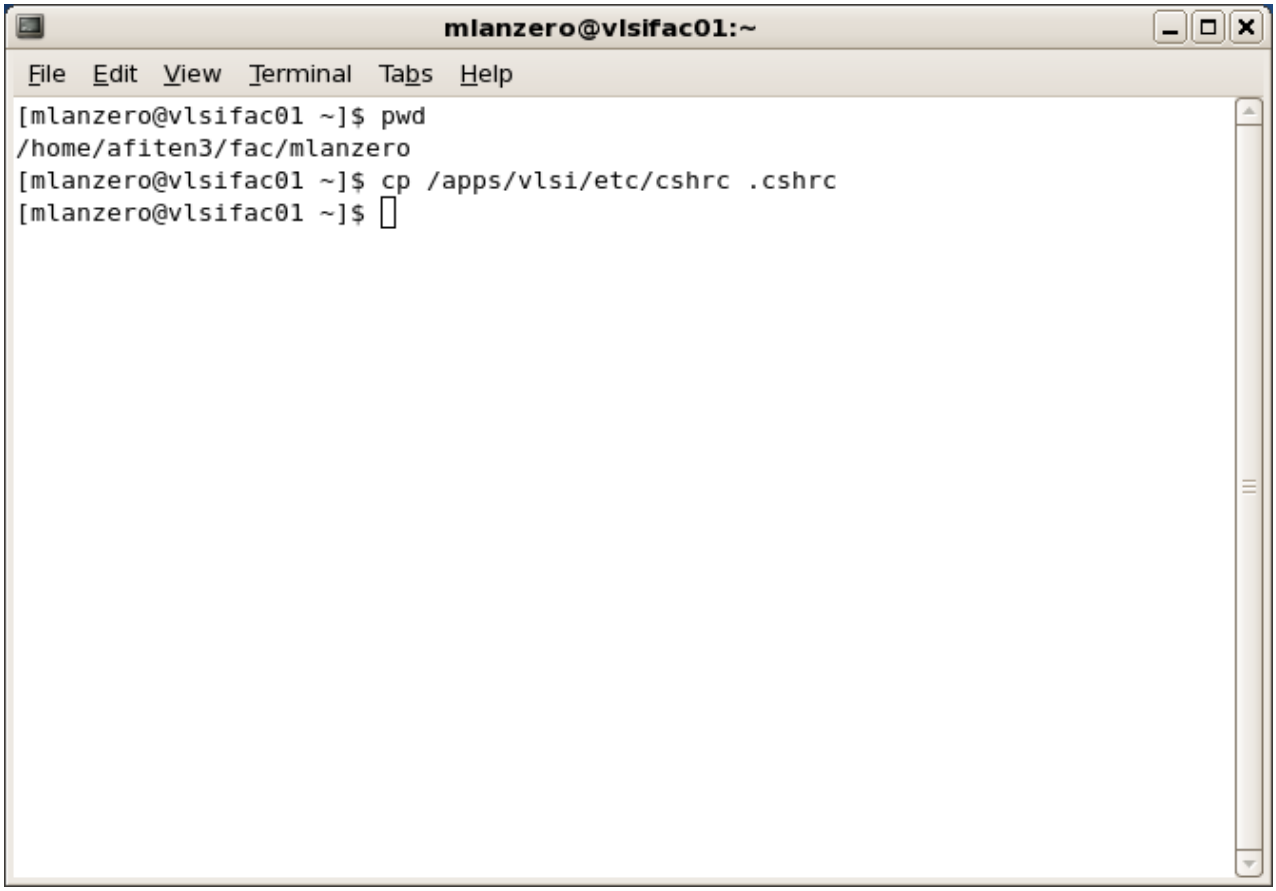
a. You should already have contacted Mr. David Doak (david.doak@afit.edu) and have a Linux email userid and Linux password

b. Log in to a Linux machine

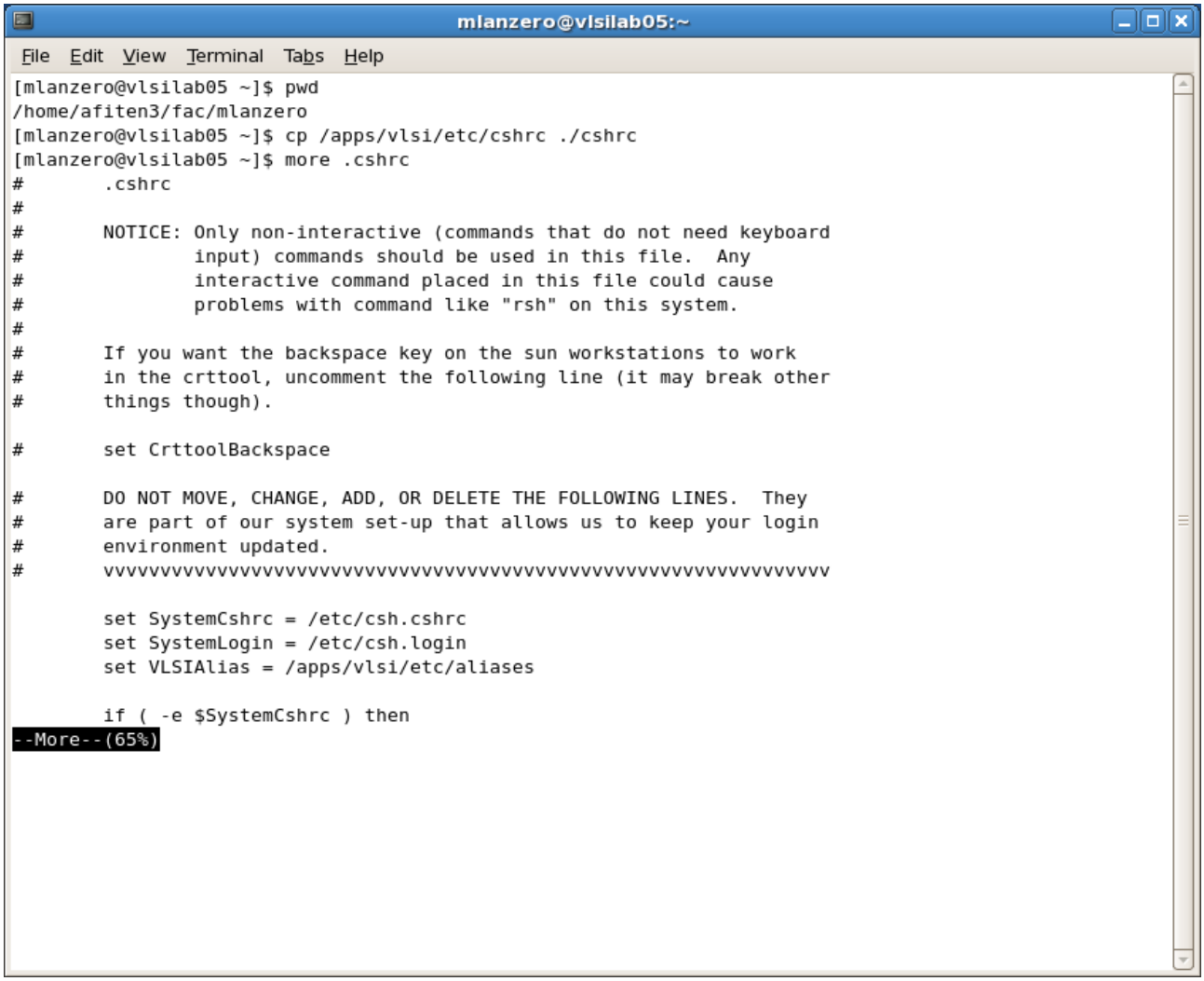
c. Open a terminal window (right click with the mouse)



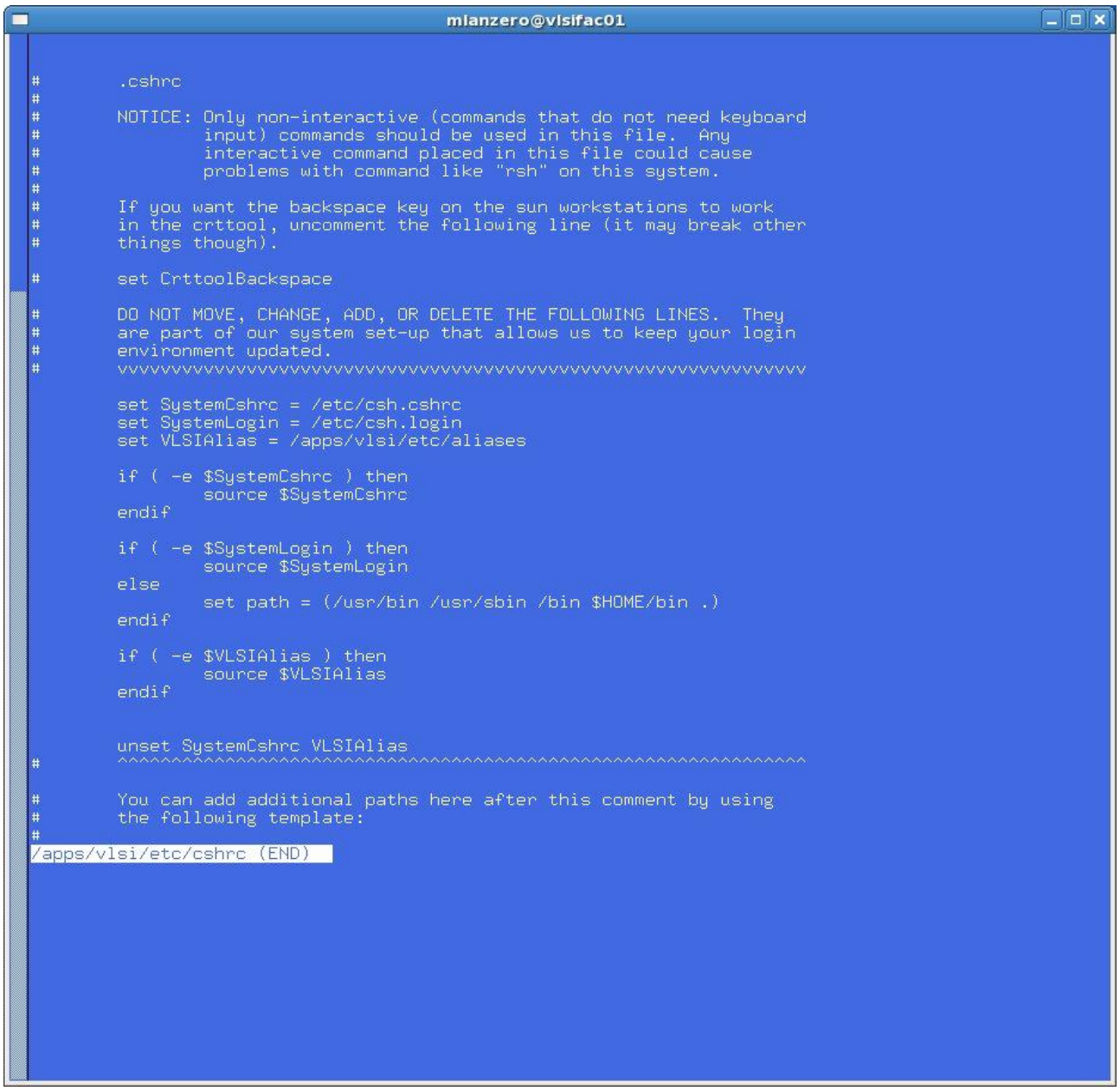
d. At the command line in this window, type:
cp /apps/vlsi/etc/cshrc .cshrc



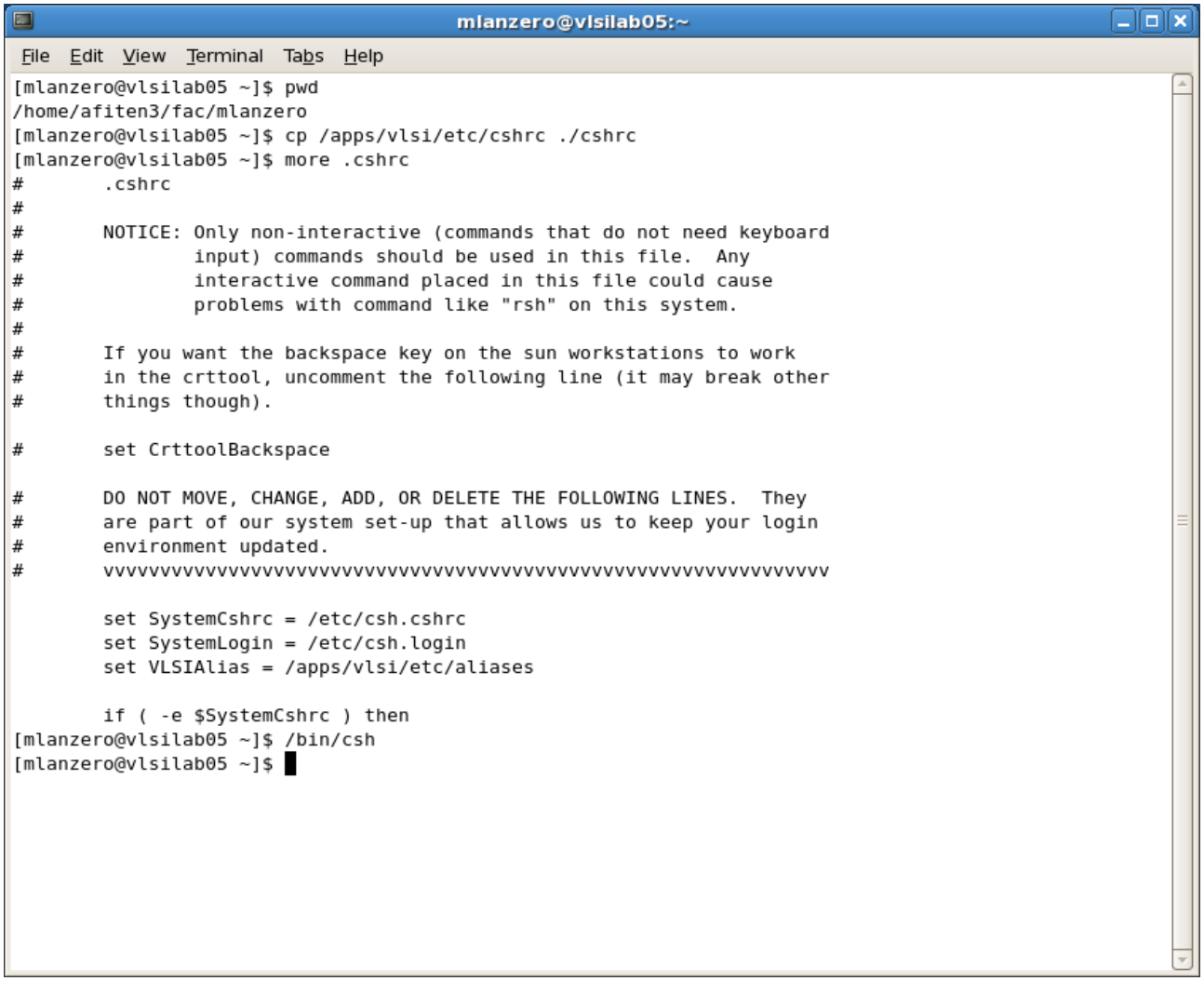
e. To verify the copy command, type
more .cshrc



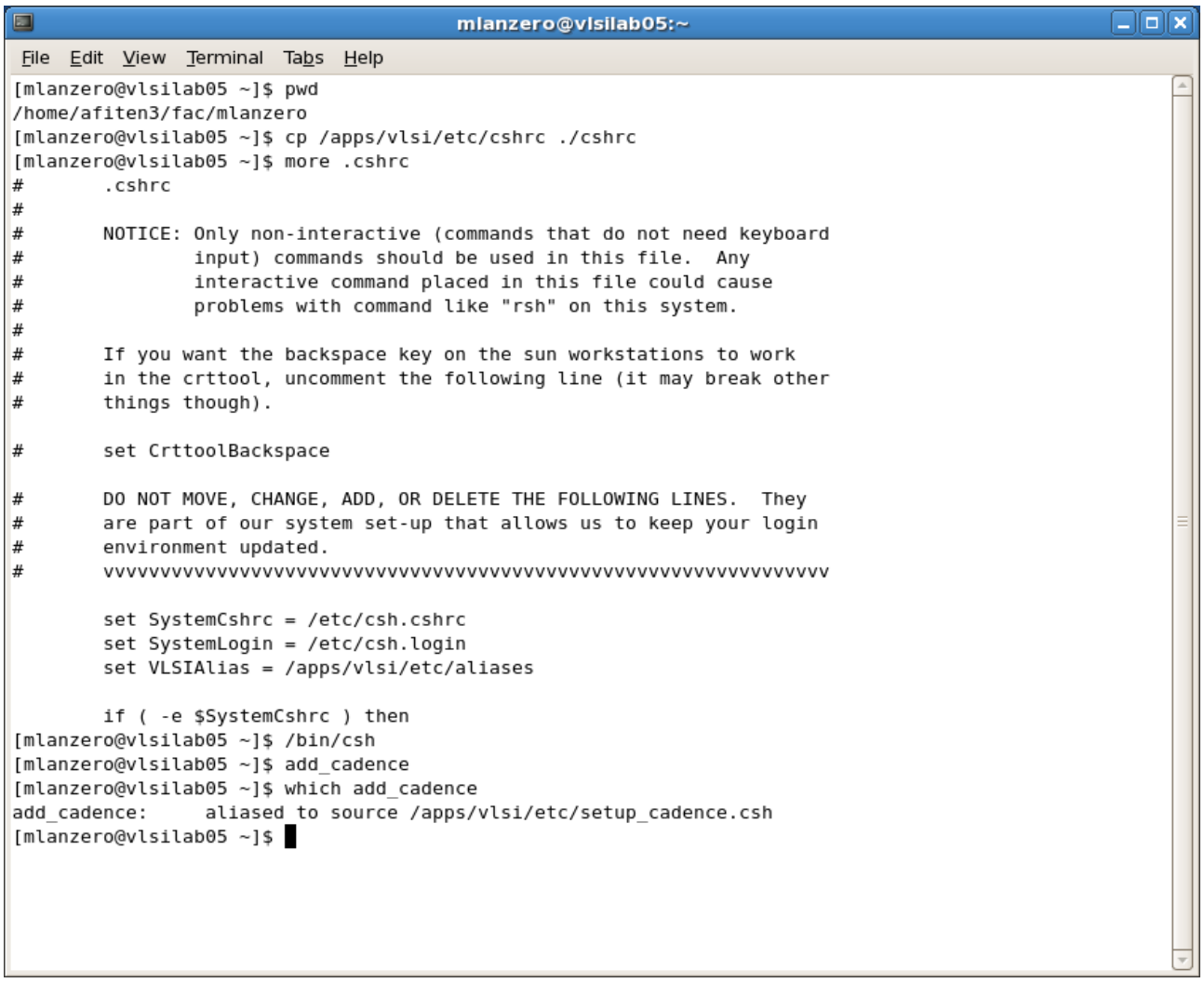
Integrated Circuit Design CAD Tool Information



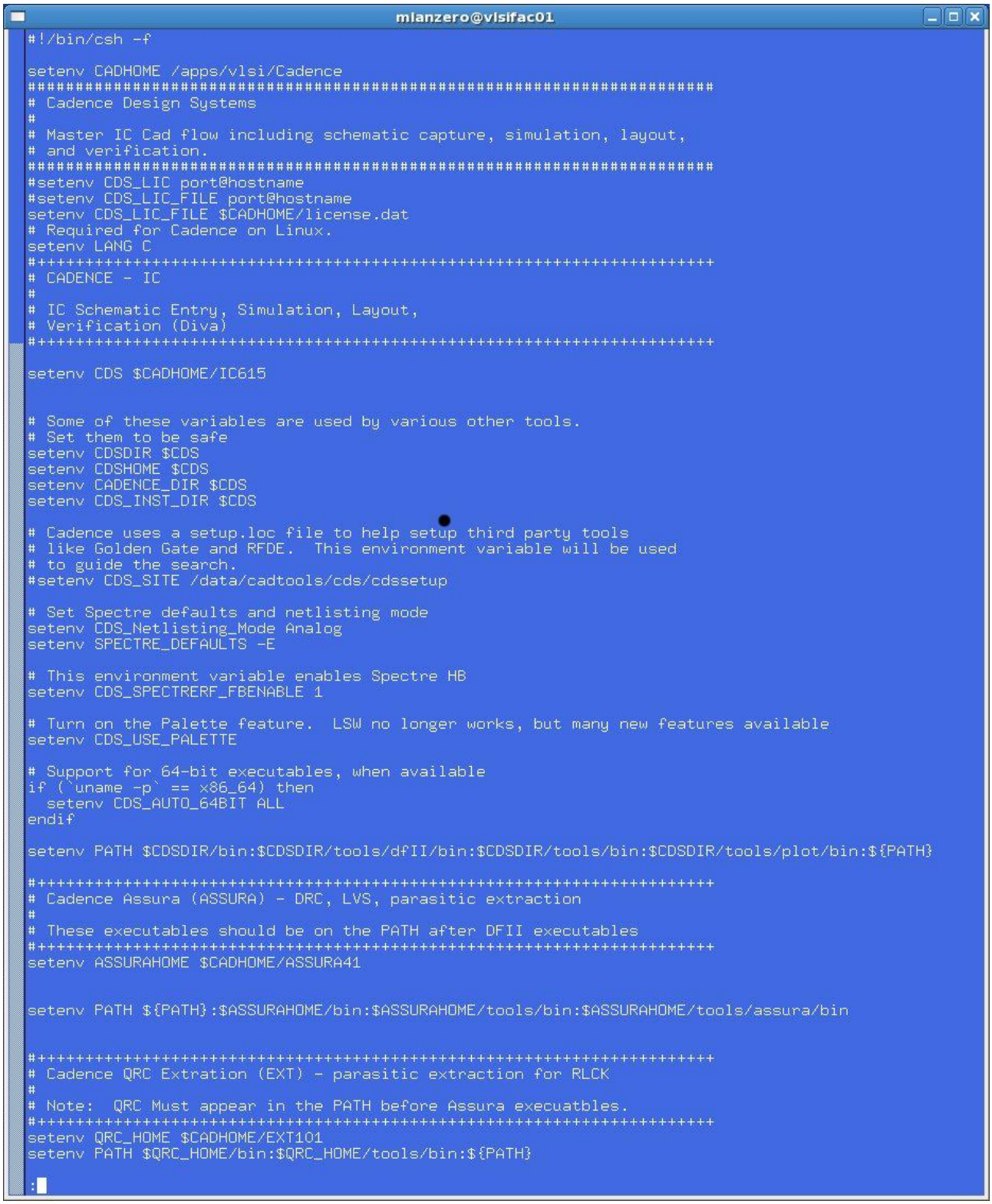
f. At the command line in the same window, type:
/bin/csh



g. At the command line in the same window, type:
add_cadence



Integrated Circuit Design CAD Tool Information



Integrated Circuit Design CAD Tool Information

mlanzero@visifac01

```
# Set Spectre defaults and netlisting mode
setenv CDS_Netlisting_Mode Analog
setenv SPECTRE_DEFAULTS -E

# This environment variable enables Spectre HB
setenv CDS_SPECTRERF_FBENABLE 1

# Turn on the Palette feature.  LSW no longer works, but many new features available
setenv CDS_USE_PALETTE

# Support for 64-bit executables, when available
if (`uname -p` == x86_64) then
  setenv CDS_AUTO_64BIT ALL
endif

setenv PATH $CDSDIR/bin:$CDSDIR/tools/dfII/bin:$CDSDIR/tools/bin:$CDSDIR/tools/plot/bin:${PATH}

#++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
# Cadence Assura (ASSURA) - DRC, LVS, parasitic extraction
#
# These executables should be on the PATH after DFII executables
#++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
setenv ASSURAHOME $CADHOME/ASSURA41


setenv PATH ${PATH}:$ASSURAHOME/bin:$ASSURAHOME/tools/bin:$ASSURAHOME/tools/assura/bin


#++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
# Cadence QRC Extration (EXT) - parasitic extraction for RLCK
#
# Note:  QRC Must appear in the PATH before Assura execuatbles.
#++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
setenv QRC_HOME $CADHOME/EXT101
setenv PATH $QRC_HOME/bin:$QRC_HOME/tools/bin:${PATH}

#++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
# Cadence Analog Simulators (MMSIM) - Spectre, SpectreRF
#
#++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
setenv MMSIMHOME ${CADHOME}/MMSIM101
setenv PATH $MMSIMHOME/bin:$MMSIMHOME/tools/bin:${PATH}

#++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
# Cadence Digital Flow
#
#++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
############
# 10.1 Flow
############
# Encounter Digital Implementation (EDI) - Synthesis and P&R
setenv PATH $CADHOME/EDI101/bin:$CADHOME/EDI101/tools/bin:${PATH}

# Conformal (CONFRML) - Verification (LVR) for digital flow
setenv PATH $CADHOME/CONFRML101/bin:$CADHOME/CONFRML101/tools/bin:${PATH}

# Conformal Constraint designer (CCD)
setenv PATH $CADHOME/CCD101/bin:$CADHOME/CCD101/tools/bin:${PATH}

# Encounter Timing System (ETS)
setenv PATH $CADHOME/ETS101/bin:$CADHOME/ETS101/tools/bin:${PATH}

# Encounter Test (ET)
setenv PATH $CADHOME/ET101/bin:$CADHOME/ET101/tools/bin:${PATH}



#++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
# Cadence Incisive Unified Simulator (IUS) - Digital HDL simulators.
#++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
setenv PATH $CADHOME/INCISIV102/bin:$CADHOME/INCISIV102/tools/bin:${PATH}
(END)
```

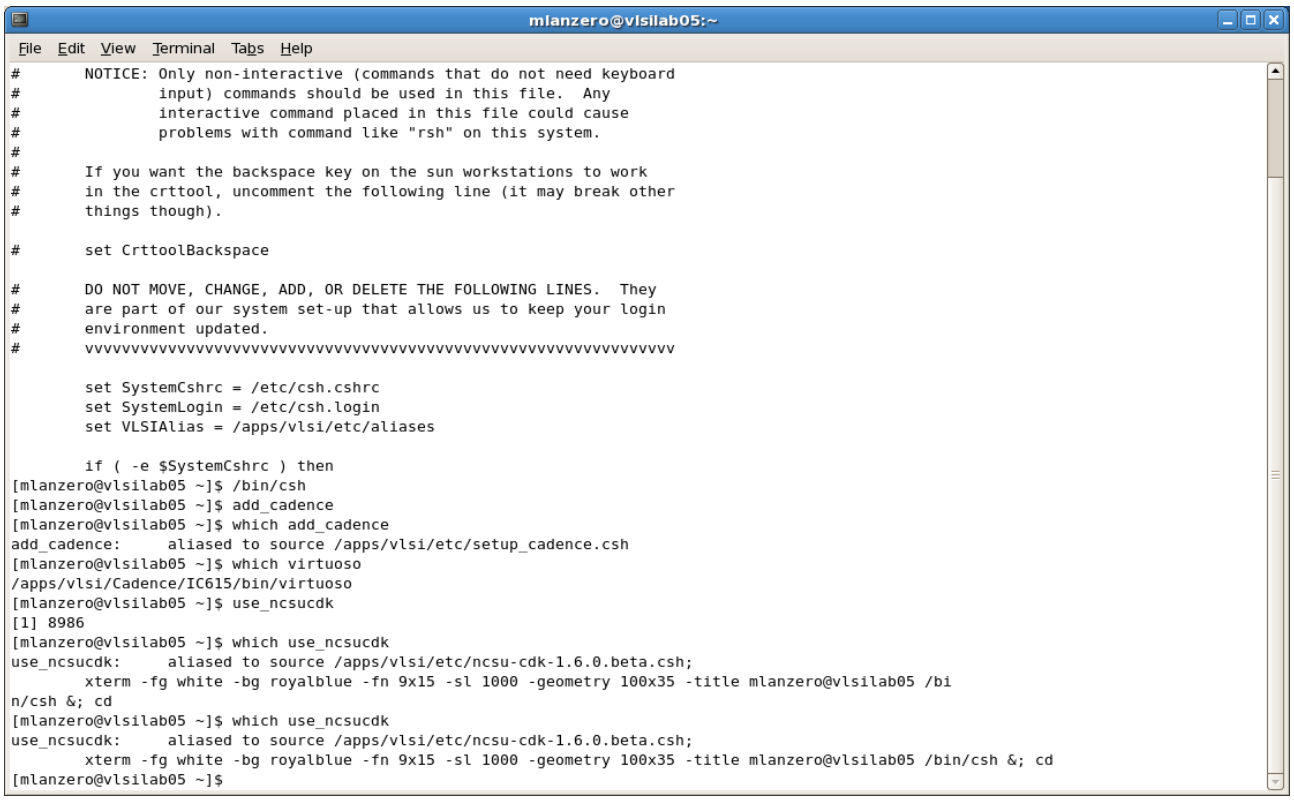
h. To verify that the executable is in the path, type:
which virtuoso

```
mlanzero@vlsilab05:~
File  Edit  View  Terminal  Tabs  Help
[mlanzero@vlsilab05 ~]$ pwd
/home/afiten3/fac/mlanzero
[mlanzero@vlsilab05 ~]$ cp /apps/vlsi/etc/cshrc ./cshrc
[mlanzero@vlsilab05 ~]$ more .cshrc
#       .cshrc
#
#       NOTICE: Only non-interactive (commands that do not need keyboard
#               input) commands should be used in this file.  Any
#               interactive command placed in this file could cause
#               problems with command like "rsh" on this system.
#
#       If you want the backspace key on the sun workstations to work
#       in the crttool, uncomment the following line (it may break other
#       things though).

#       set CrttoolBackspace

#       DO NOT MOVE, CHANGE, ADD, OR DELETE THE FOLLOWING LINES.  They
#       are part of our system set-up that allows us to keep your login
#       environment updated.
#       vvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvv

        set SystemCshrc = /etc/csh.cshrc
        set SystemLogin = /etc/csh.login
        set VLSIAlias = /apps/vlsi/etc/aliases

        if ( -e $SystemCshrc ) then
[mlanzero@vlsilab05 ~]$ /bin/csh
[mlanzero@vlsilab05 ~]$ add_cadence
[mlanzero@vlsilab05 ~]$ which add_cadence
add_cadence:     aliased to source /apps/vlsi/etc/setup_cadence.csh
[mlanzero@vlsilab05 ~]$ which virtuoso
/apps/vlsi/Cadence/IC615/bin/virtuoso
[mlanzero@vlsilab05 ~]$
```

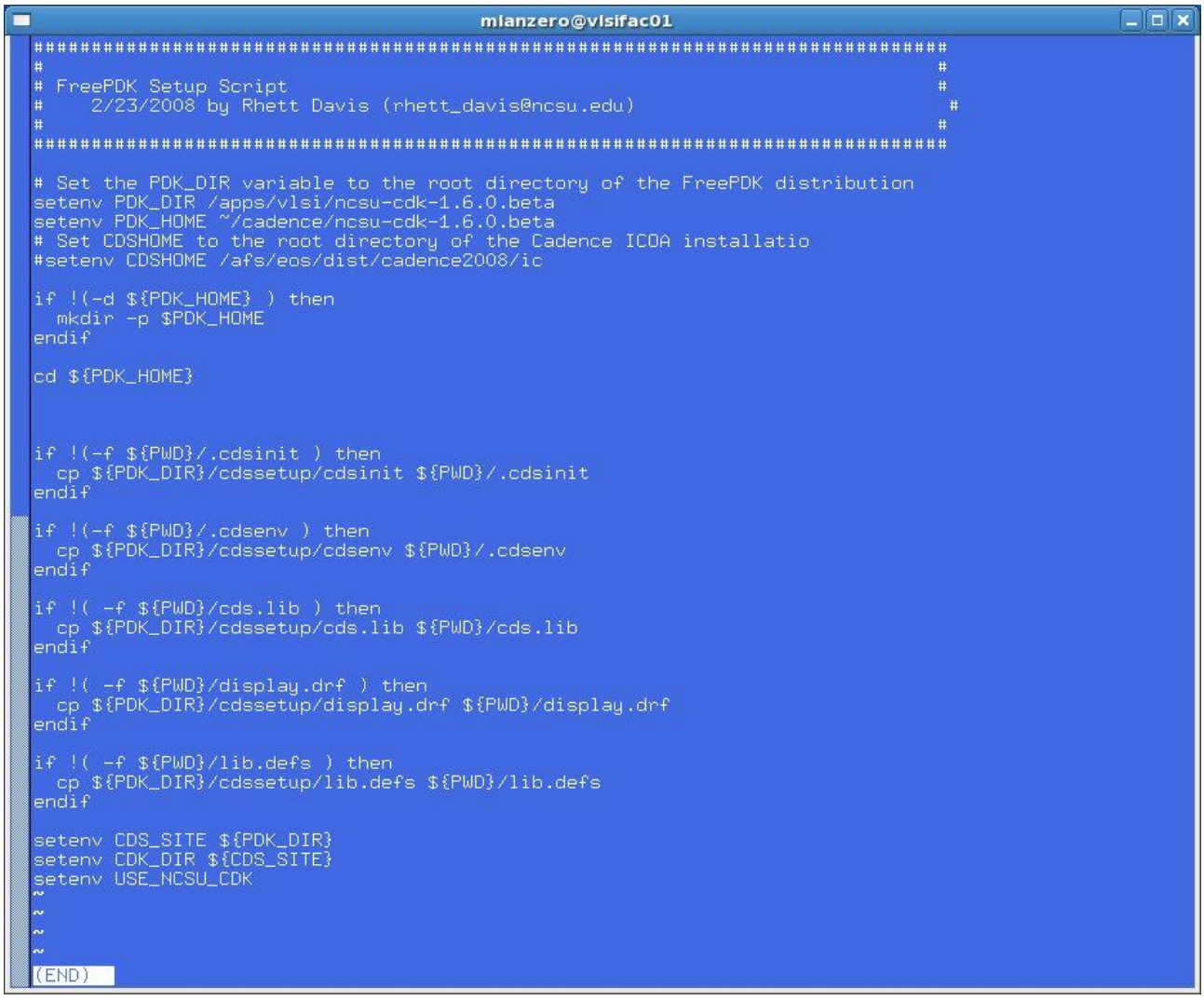
Integrated Circuit Design CAD Tool Information

i. Type:

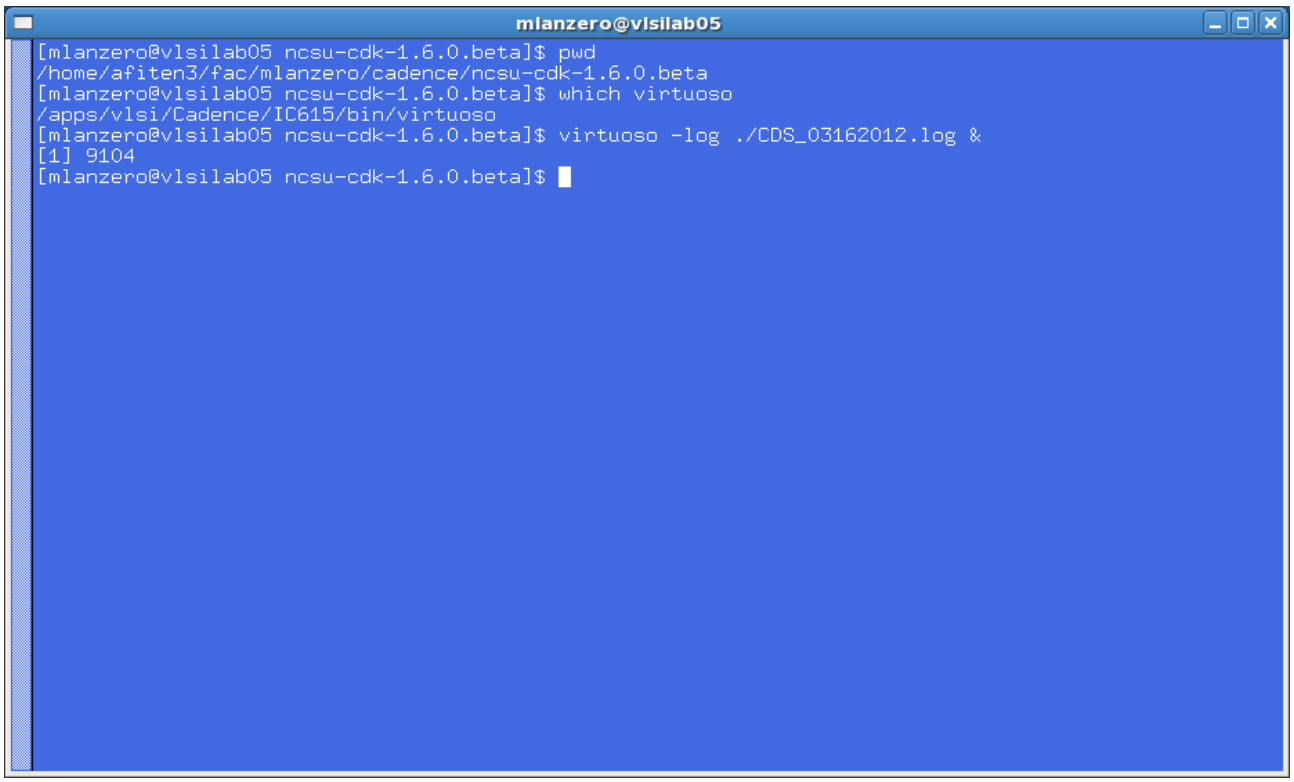
use_ncsucdk



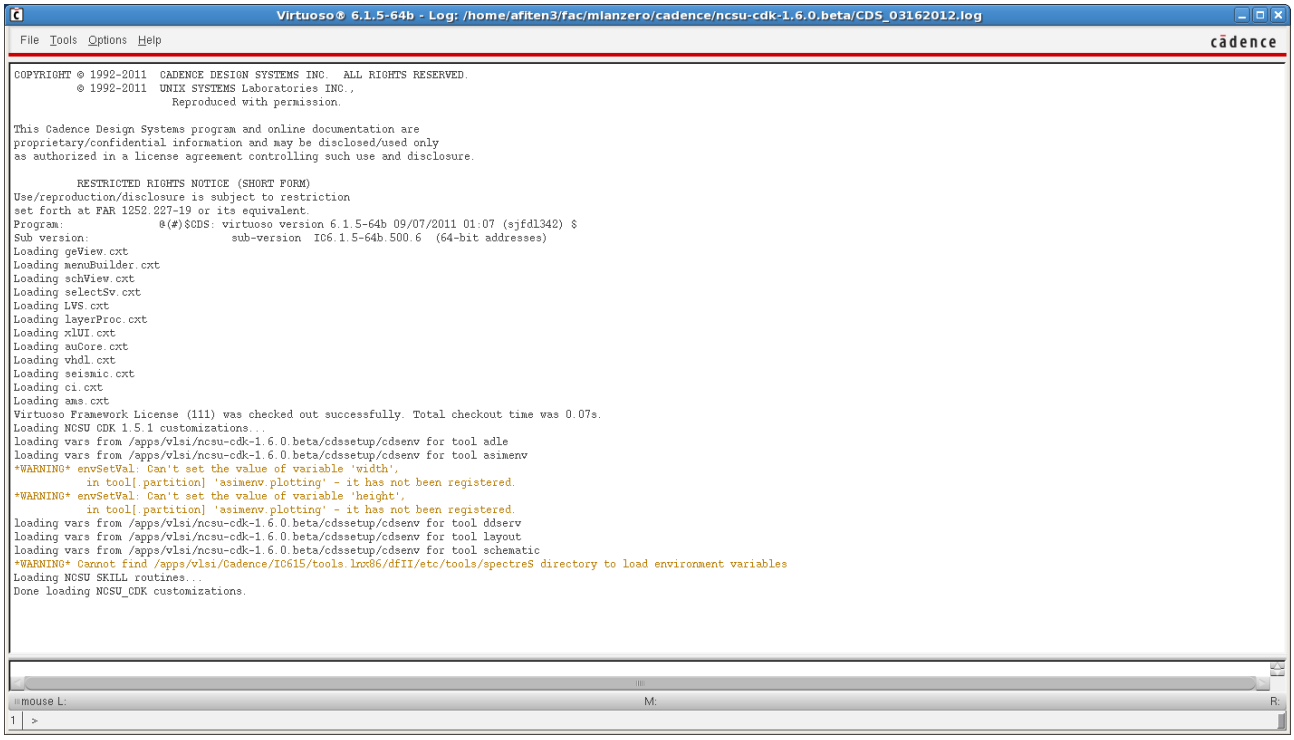
Integrated Circuit Design CAD Tool Information



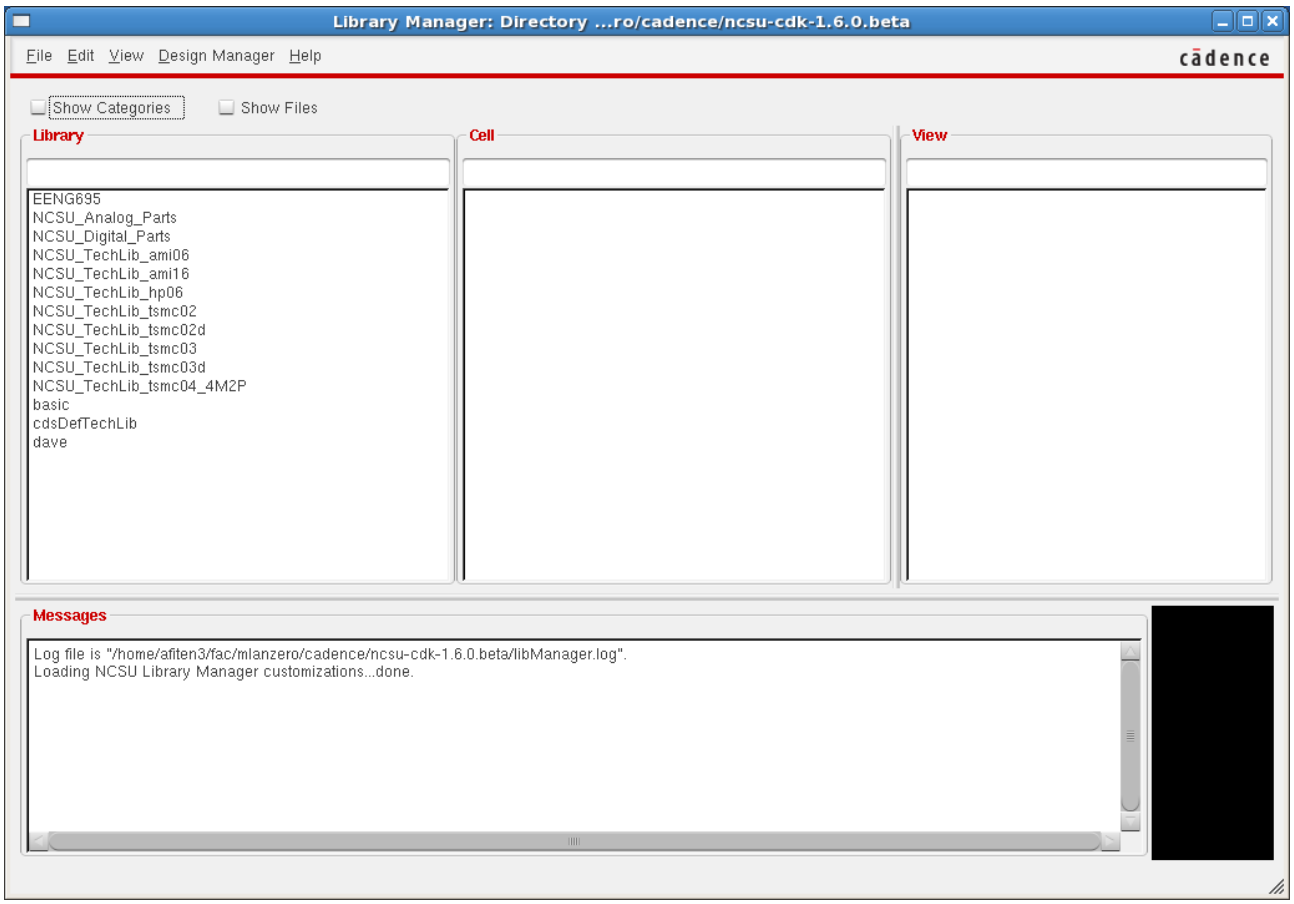
j. In the blue window that appears, type:
virtuoso –log ./CDS_lab.log &



k. The CIW for Virtuoso ® 6.1.5-64b will appear with the log file indicated in the banner at the top of the window.



l. The Library Manager will also appear indicating the run directory in the banner at the top of the window.



10. Sending Email from Linux

a. Step 1

i. Open a blue Linux terminal by typing the following command in a white terminal (Right click in the Linux desktop and select 'open terminal').

ii. Type 'use_ncsucdk'.

b. Step 2

i. Type mail <user_email address> in the blue window that appears, and then hit 'Enter'.

ii. Example: mail mary.lanzerotti@afit.edu and hit 'Enter.'

c. Step 3

i. Copy and paste your link or other ascii information into the message space.

d. Step 4

i. Hit Return and on the blank line at the bottom of your note, type '.'

e. Step 5

i. Add any other email addresses in the cc: line

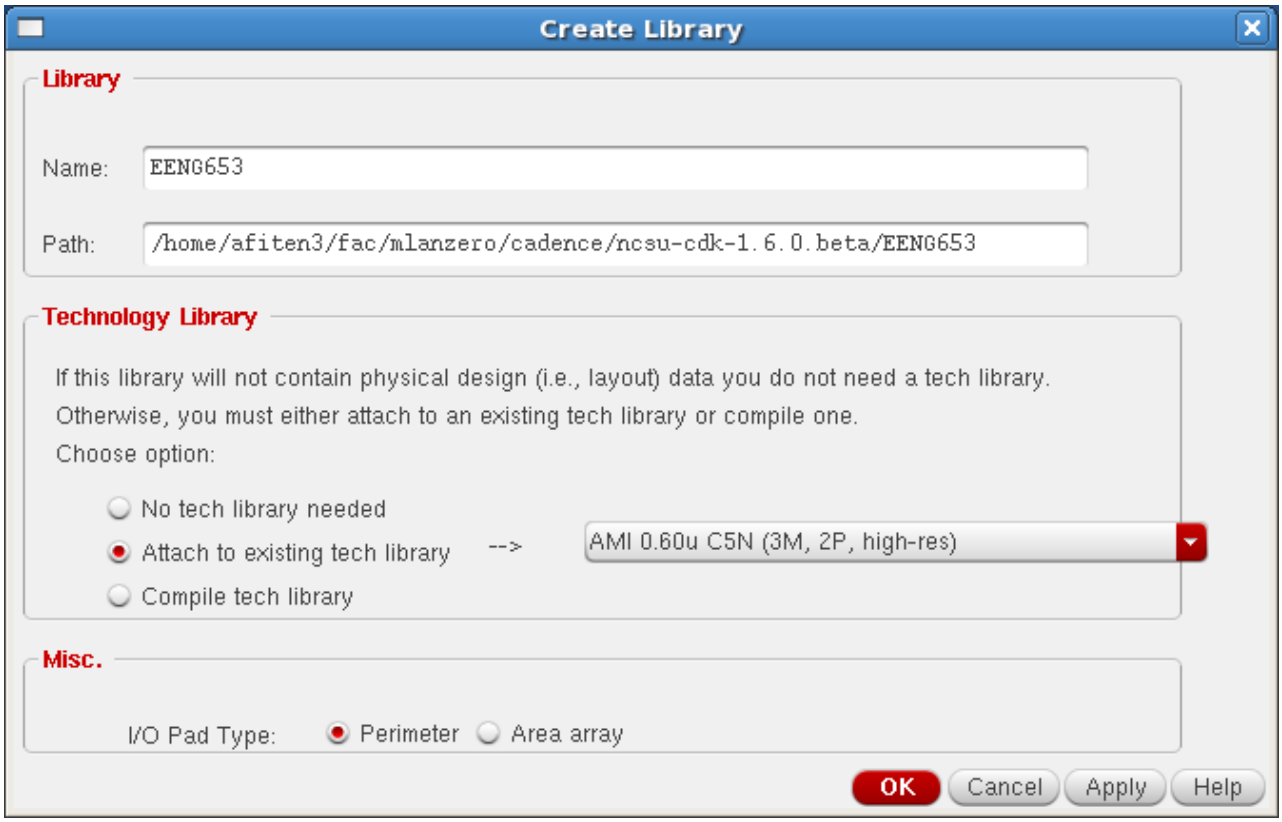
ii. Otherwise hit 'Return.'

f. The email is sent.

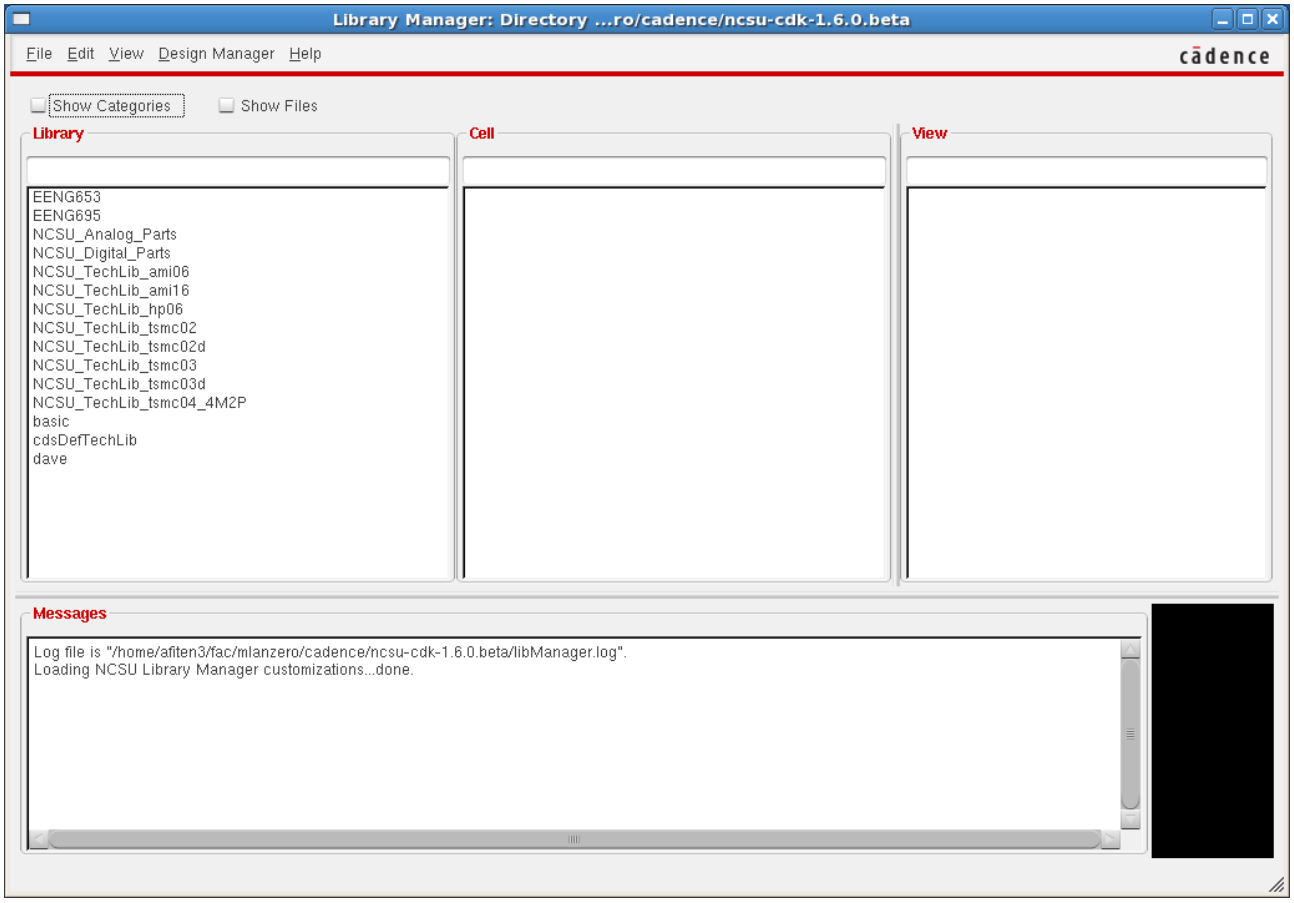
11. Inverter: Creating a Library

a. Now you will create a library to store your circuit designs. Every library will be associated with a foundry-supplied technology file. For this laboratory, the technology file is supplied in the NCSU Design Kit.

b. In the CIW or Library Manager window, click with the mouse on File → New → Library to obtain the following window. Complete the two fields for Name: and Path. The Name of your Library is 'LibName'. Your Path should be <Your Working Directory/LibName>. In the example shown below for the course EENG653, 'Name' is set to 'EENG653.' The working directory is '/home/afiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta.'



c. Now you will see EENG653 appear in the Library Manager Window in the list of libraries on the left-hand side.

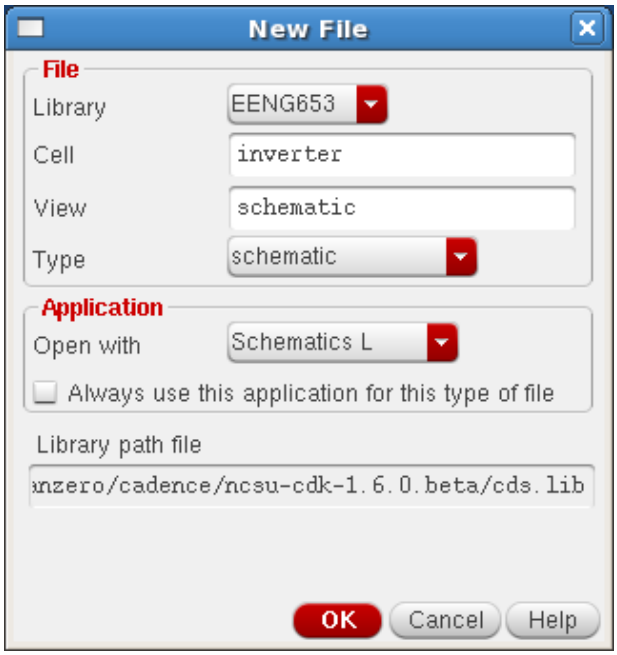


d. Now you have completed the task of creating a new empty Library.

12. Inverter: Creating a Schematic

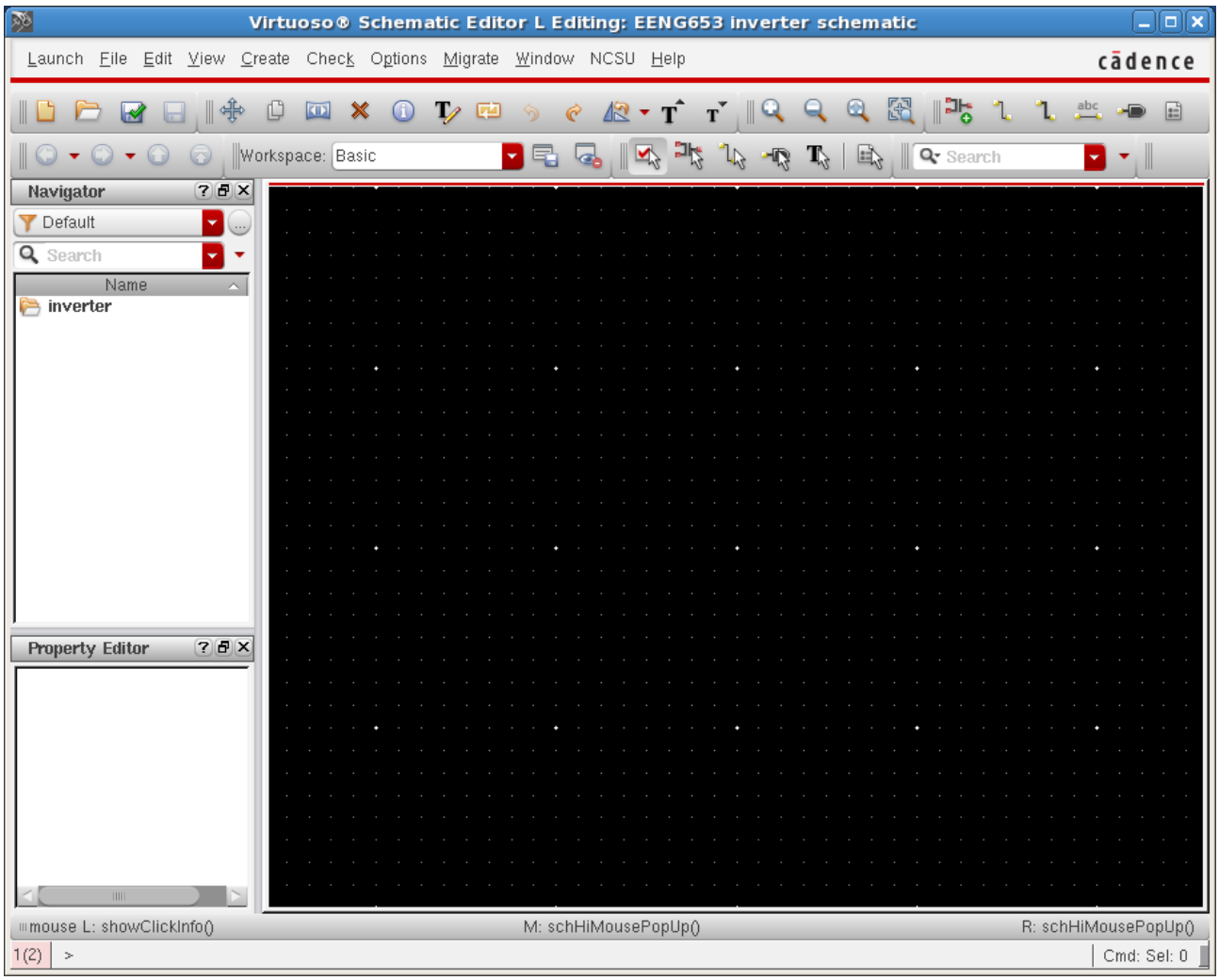
a. Now you can create a Schematic in the library. To create a schematic, highlight the library EENG653 in the Library Manager.

b. Click in the Library Manager Window with the mouse on the File → New → Cell View. Another window will appear as shown below with "New File" in the banner at the top of the window. Fill in the fields for Cell as 'inverter' and View as 'schematic.'

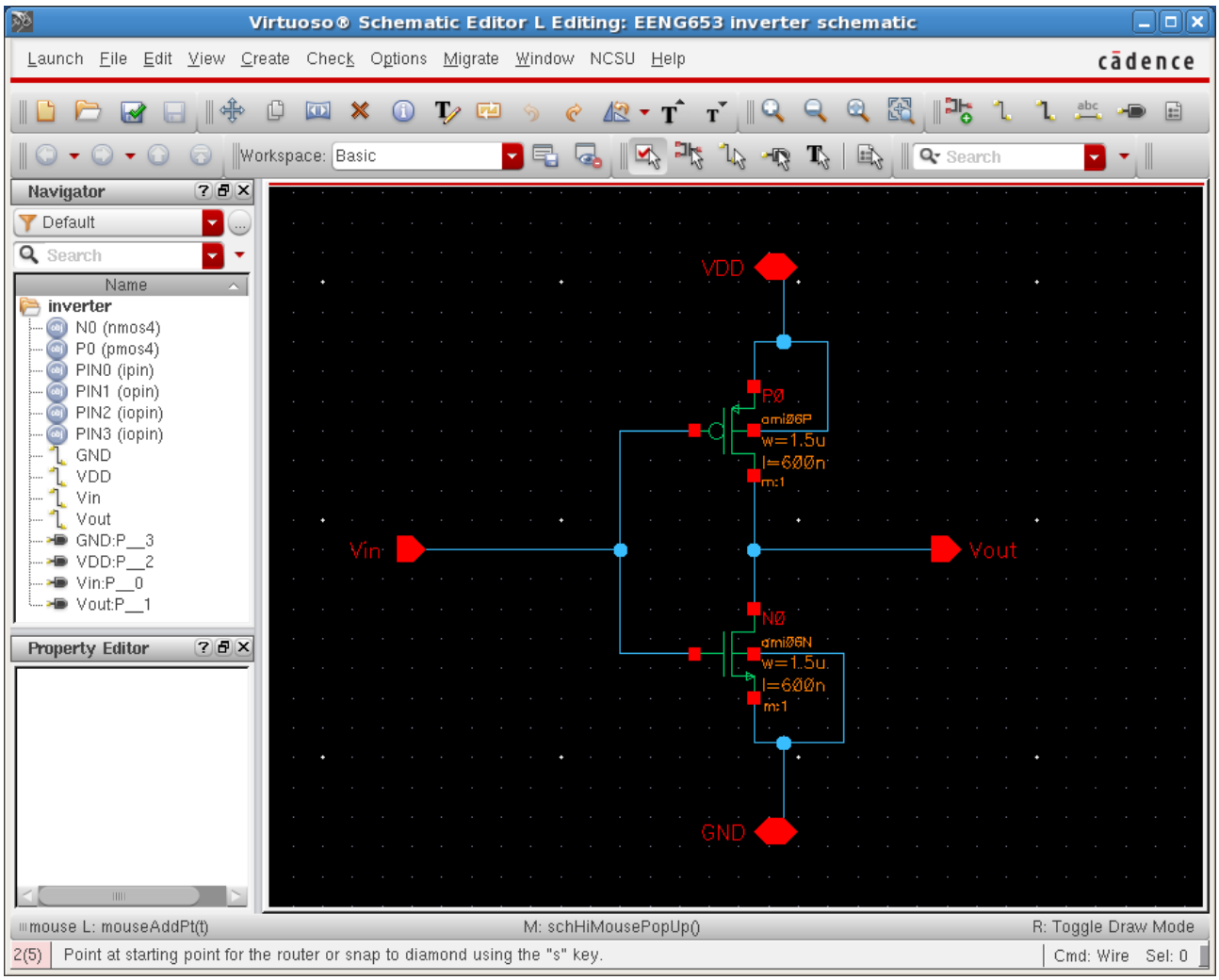


c. Click OK in the "New File" form.

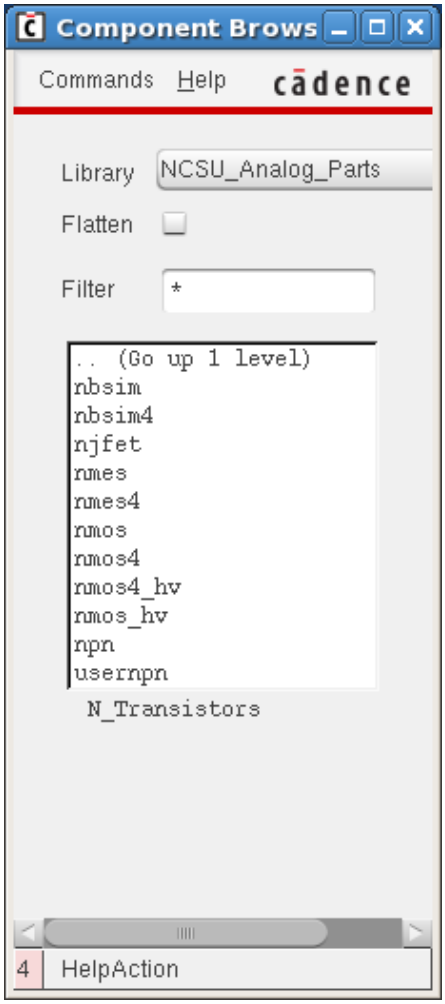
d. A new Schematic window will appear with the title "Virtuoso Schematic Editor L Editing: EENG 653 inverter schematic" in the banner at the top of the window.



e. Now you are going to insert instances of devices into this Schematic Window in order to create an inverter shown below.



f. The first instance you will insert is an nfet. Click on the Schematic Window and type 'i' in the window. Two new Windows will appear. The Component Browser window and Add Instance browser are shown below:



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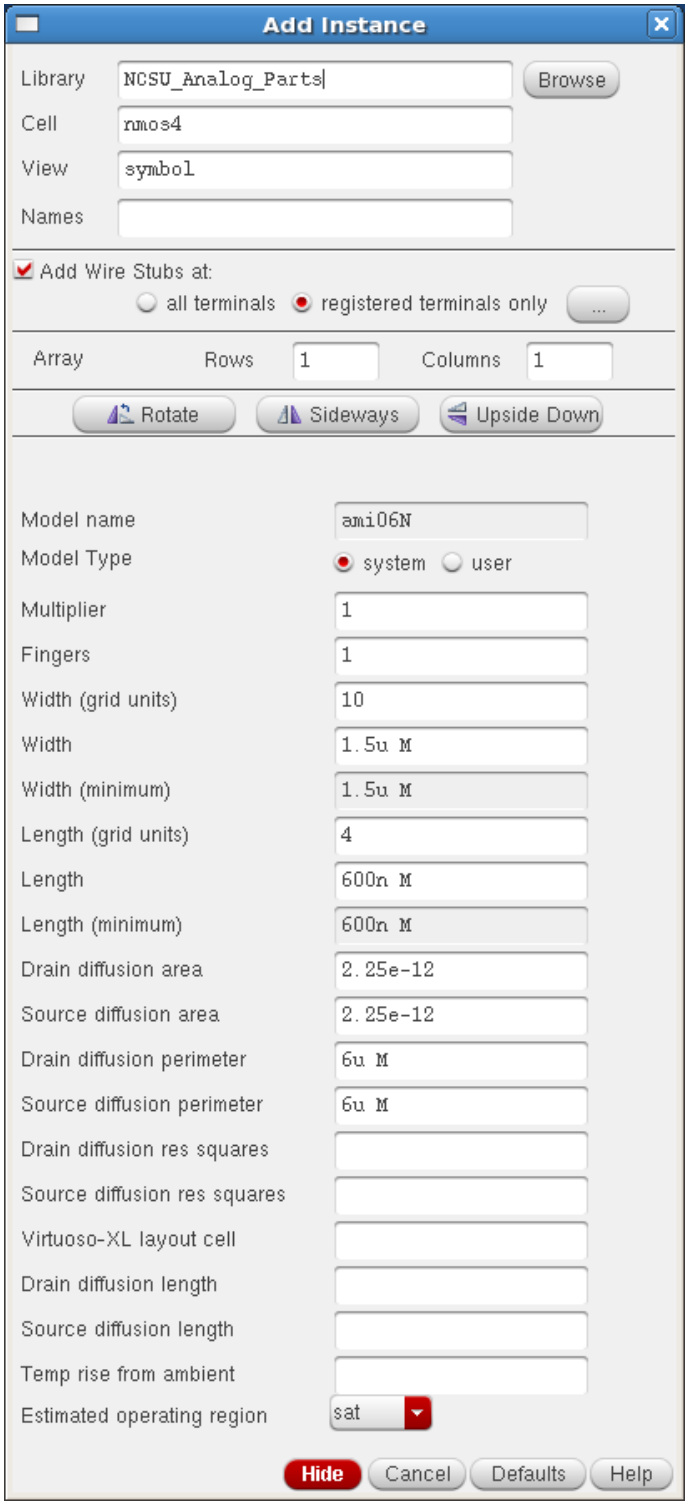


g. In the Component Browser Window, select NCSU_Analog_Parts → N_Transistors → nmos4, which will select a four-terminal nfet in the Add Instance Window. Fill in the fields in the Add Instance Window as shown in the Window above. Note that you have the ability to change the values of the channel width ('Width'), channel length ('Length'), and number of fingers ('Fingers') in the Add Instance Window.

h. Click with the left mouse button in the Schematic Window in order to place one instance of the nfet in the Schematic Window.

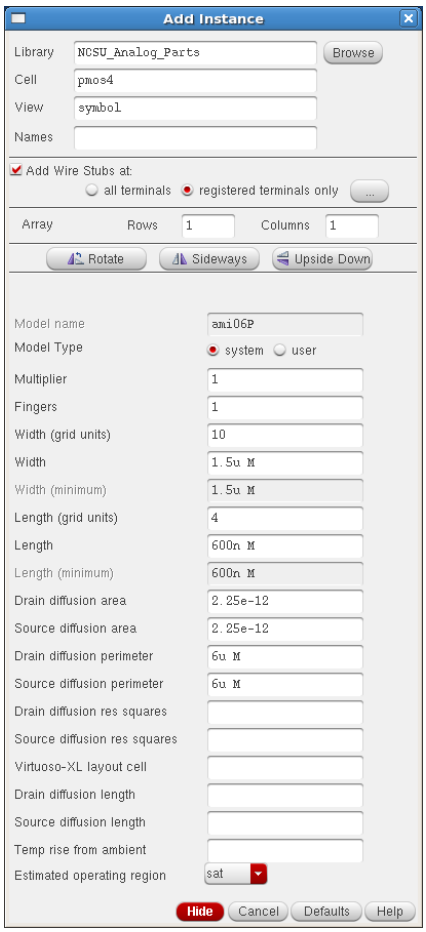
i. Press 'ESC' to cancel the placement of any additional nfets.

j. If you wish to go back and change the properties ('Width', 'Length', 'Fingers') of the nfet that you just placed, click with the mouse on the instance to highlight it. Then type 'q'. Another form will appear to allow you to edit the object properties.

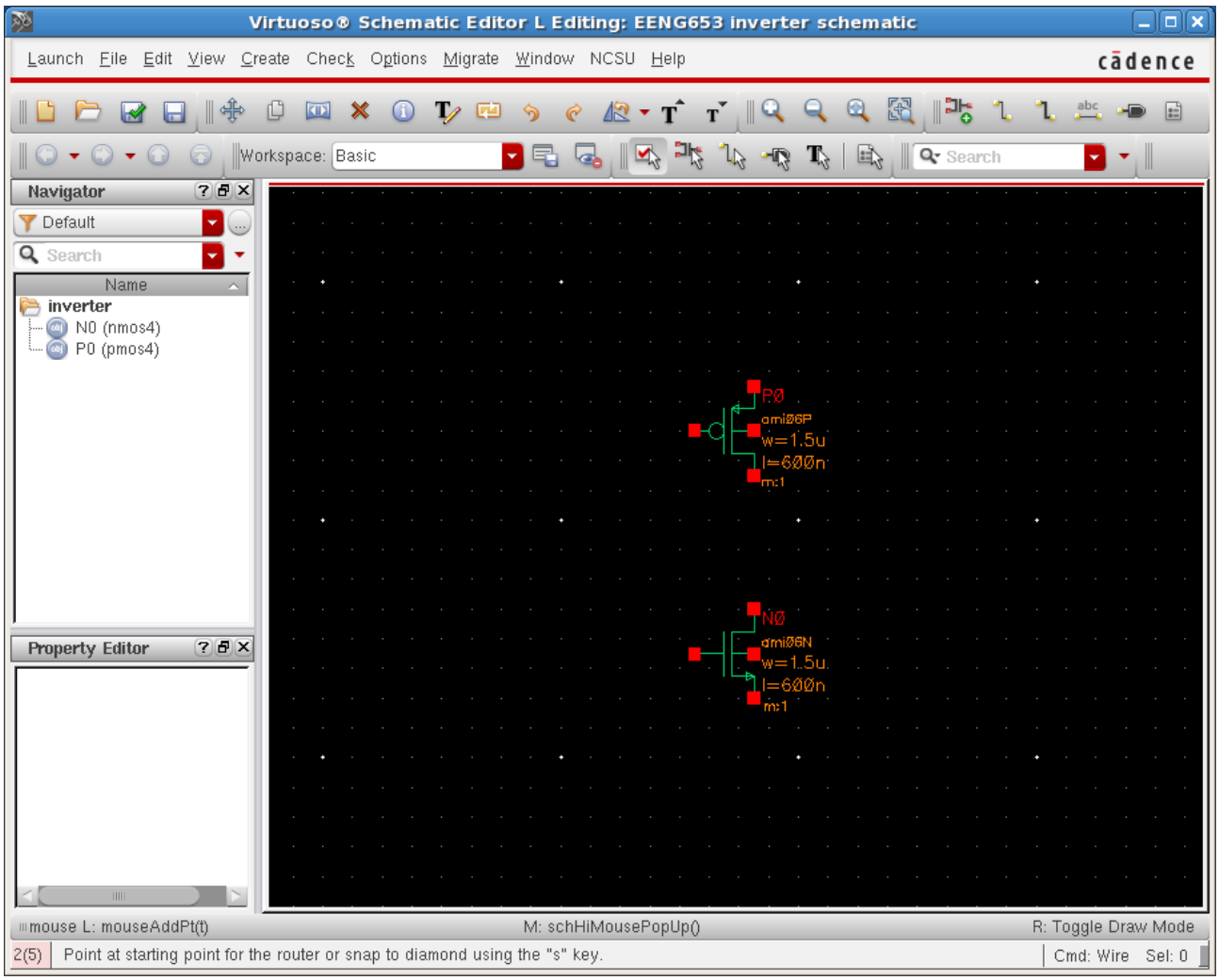
k. The next instance you will insert is a pfet. Click on the Schematic Window and type 'i' in the window. Two Windows will appear.

Integrated Circuit Design CAD Tool Information

l. In the Component Browser Window, select NCSU_Analog_Parts → p_Transistors → pmos4, which will select a four-terminal pfet in the Add Instance Window. Fill in the fields in the Add Instance Window as shown in the Window above. Note that you have the ability to change the values of the channel width ('Width'), channel length ('Length'), and number of fingers ('Fingers') in the Add Instance Window.



m. Click with the left mouse button in the Schematic Window in order to place one instance of the pfet in the Schematic Window. Place the pfet above the nfet as shown in the inverter schematic.

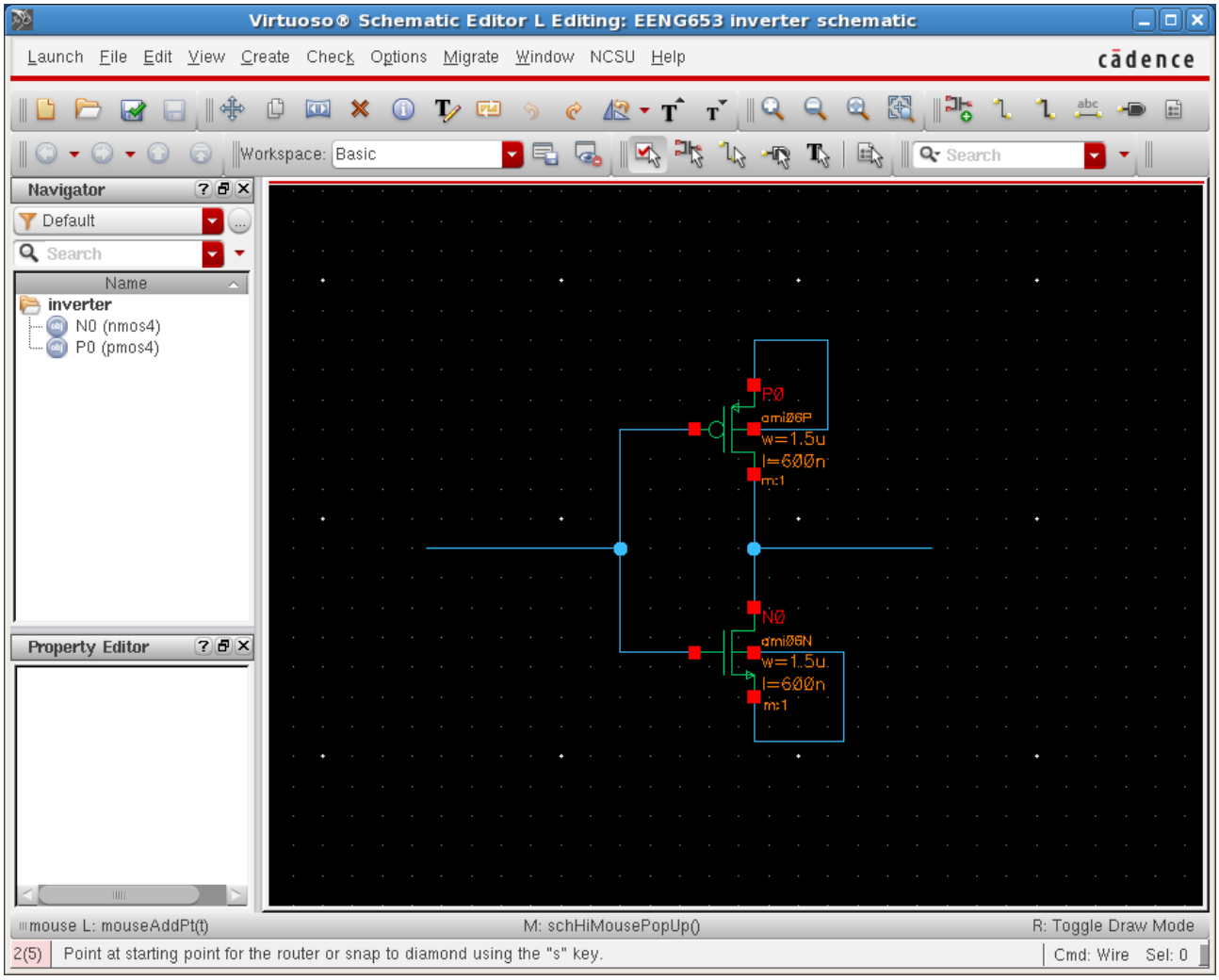


n. Press 'ESC' to cancel the placement of any additional pfets.

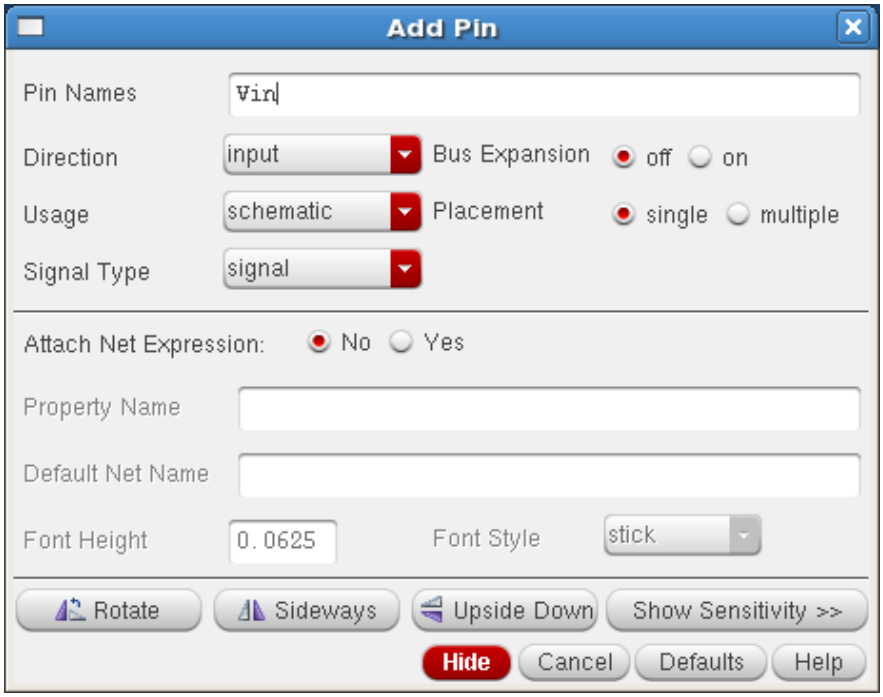
o. If you wish to go back and change the properties ('Width', 'Length', 'Fingers') of the pfet that you just placed, click with the mouse on the instance to highlight it. Then type 'q'. Another form will appear to allow you to edit the object properties.

p. Now you will create wires to connect the two devices. Click on the Schematic window. In the Schematic window, type 'w' and click with the left mouse button at the location you wish to add the wire. The wire will be blue. Move the mouse to the final location of the wire. Double-click with the mouse at the final location to finish adding the wire. Press 'ESC' to stop adding the wire.

q. Add wires to the Schematic window so that the design looks like the image shown below.



r. Now you will add pins to the schematic. Click on the Schematic Editor window. In the Schematic Editor window, type 'p', and an Add Pin window will appear as shown in the image below.



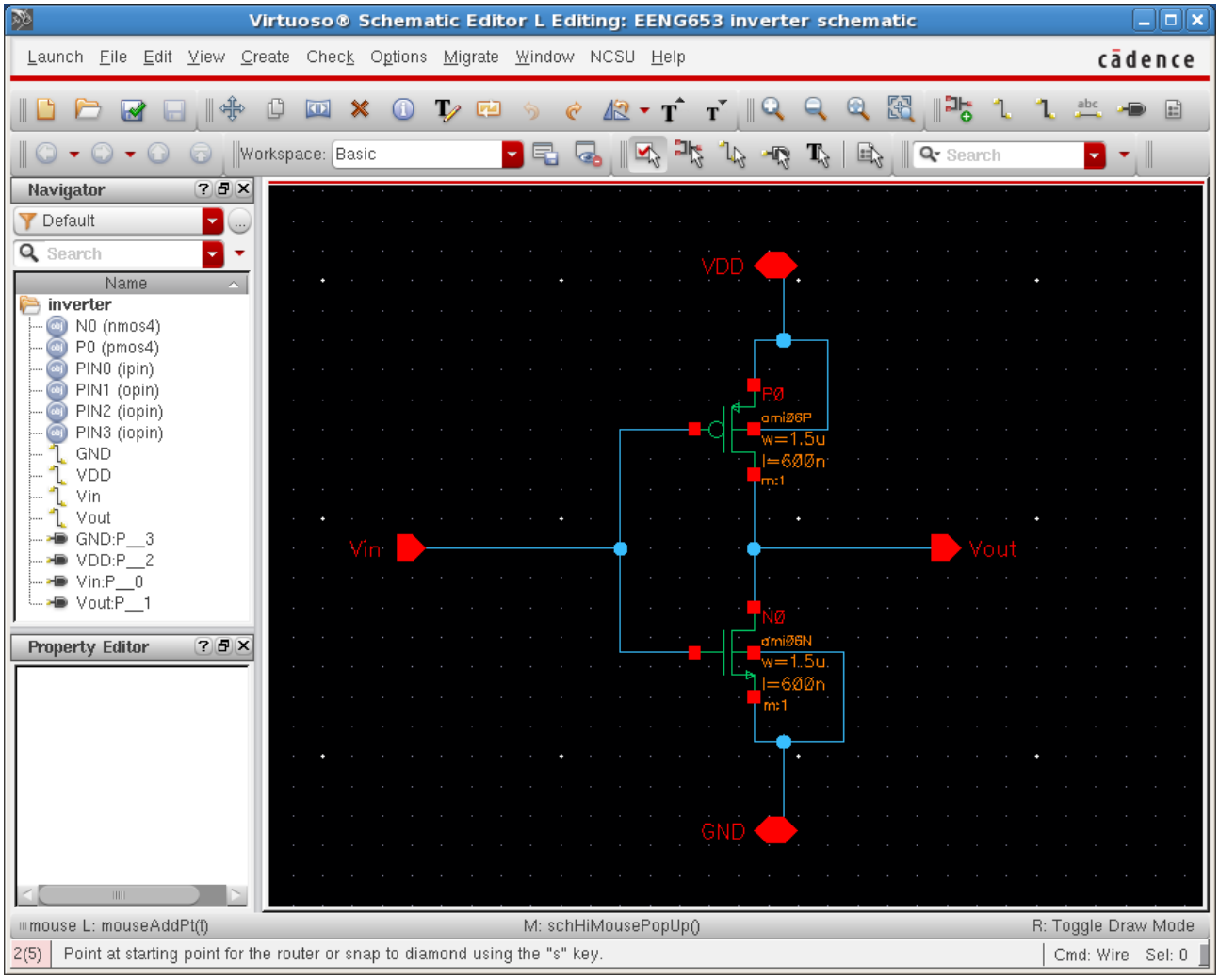
s. In the Add Pin window, fill in the field "Pin Names" with 'Vin' and for the "Direction" pulldown, select 'input'. Move the mouse to the location on the wire where you will add the pin, and click with the left mouse button to place the pin. Make sure you click the mouse button on the wire so that the pin is connected to the wire.

t. In the Add Pin window, fill in the field "Pin Names" with 'Vout' and for the "Direction" pulldown, select 'output'. Move the mouse to the location on the wire where you will add the pin, and click with the left mouse button to place the pin. Make sure you click the mouse button on the wire so that the pin is connected to the wire.

u. In the Add Pin window, fill in the field "Pin Names" with 'VDD' and for the "Direction" pulldown, select 'inputoutput'. Move the mouse to the location on the wire where you will add the pin, and click with the left mouse button to place the pin. Make sure you click the mouse button on the wire so that the pin is connected to the wire.

v. In the Add Pin window, fill in the field "Pin Names" with 'GND' and for the "Direction" pulldown, select 'inputoutput'. Move the mouse to the location on the wire where you will add the pin, and click with the left mouse button to place the pin. Make sure you click the mouse button on the wire so that the pin is connected to the wire.

w. The inverter in the Schematic window will look like the image below.



x. Now you have finished the task of creating an inverter schematic.

y. Here is a Quick Reference of commands.

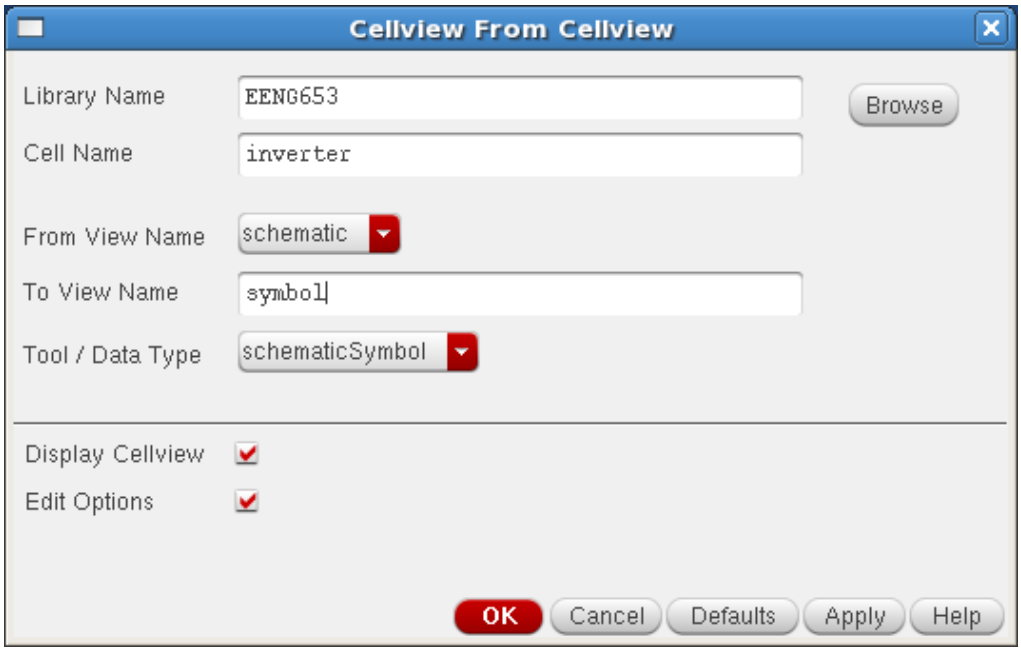
Command Quick Reference	
Command	**Function**
i	Add instance
p	Add pin
q	Edit properties
w	Add wire
f	Fit schematic within your schematic window
l	Label a wire
m	Move an object
DEL	Delete an object
ESC	Terminate any of the operations in the schematic window
Up	Up arrow moves up in a schematic window
Down	Down arrow moves down in a schematic window

13. Inverter: Creating a Symbol

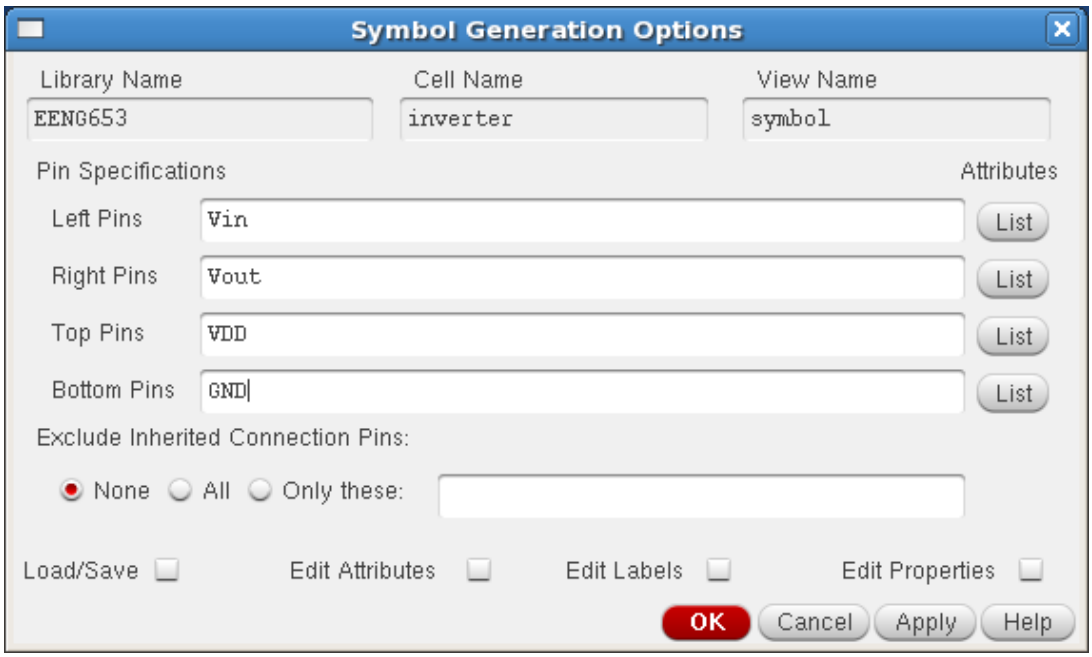
a. A symbol is a representation of a schematic. Symbols are instantiated in higher-level schematics in order to create hierarchical schematics that represent more complex designs.

b. You will now create a symbol of the inverter that you designed in the previous section.

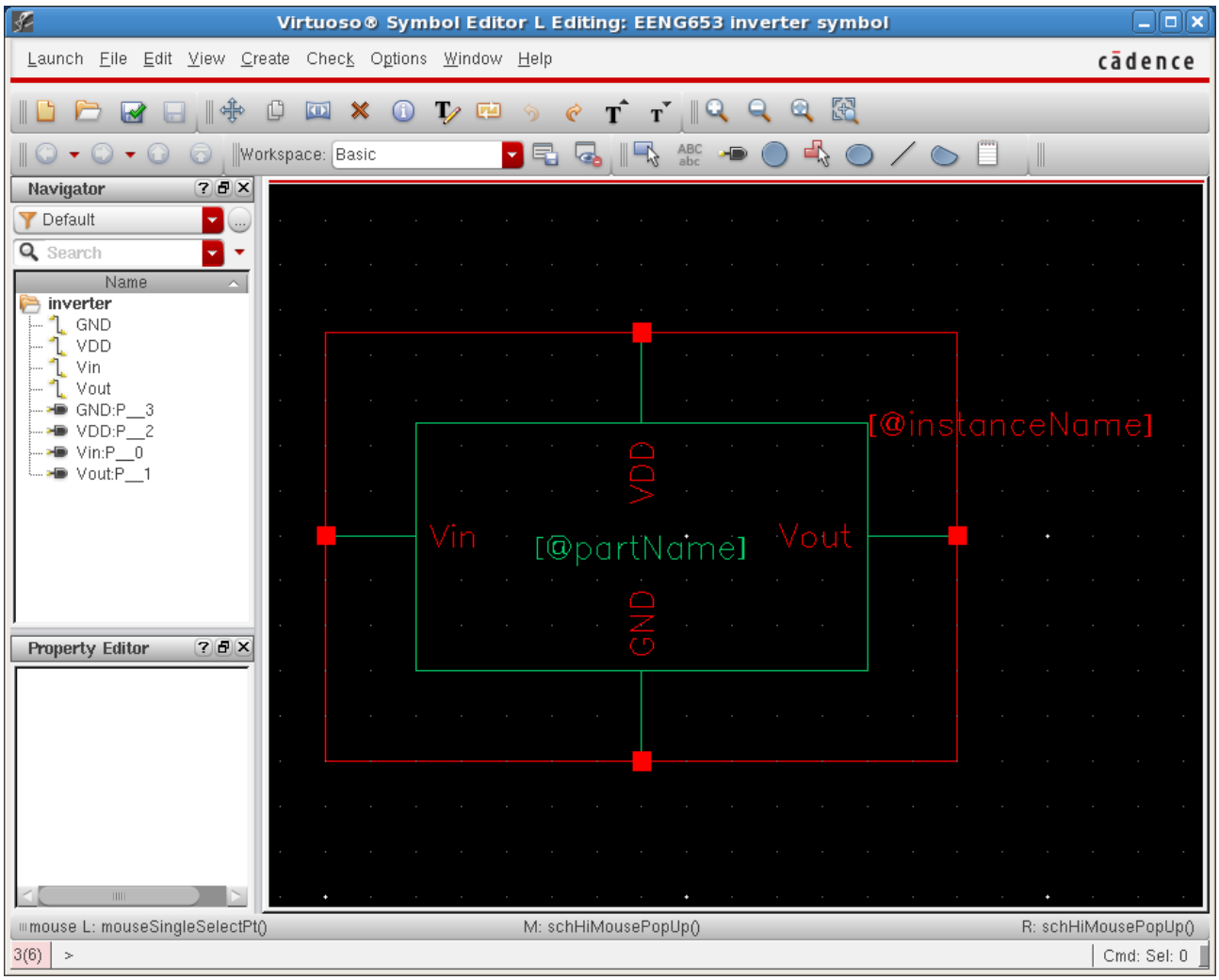
c. Click on the Schematic Window. In the Schematic Window, click 'Create → Cellview → From Cellview'. Fill in the Fields for 'Library Name' as "EENG653" and 'Cell Name' as 'inverter' as shown in the image.



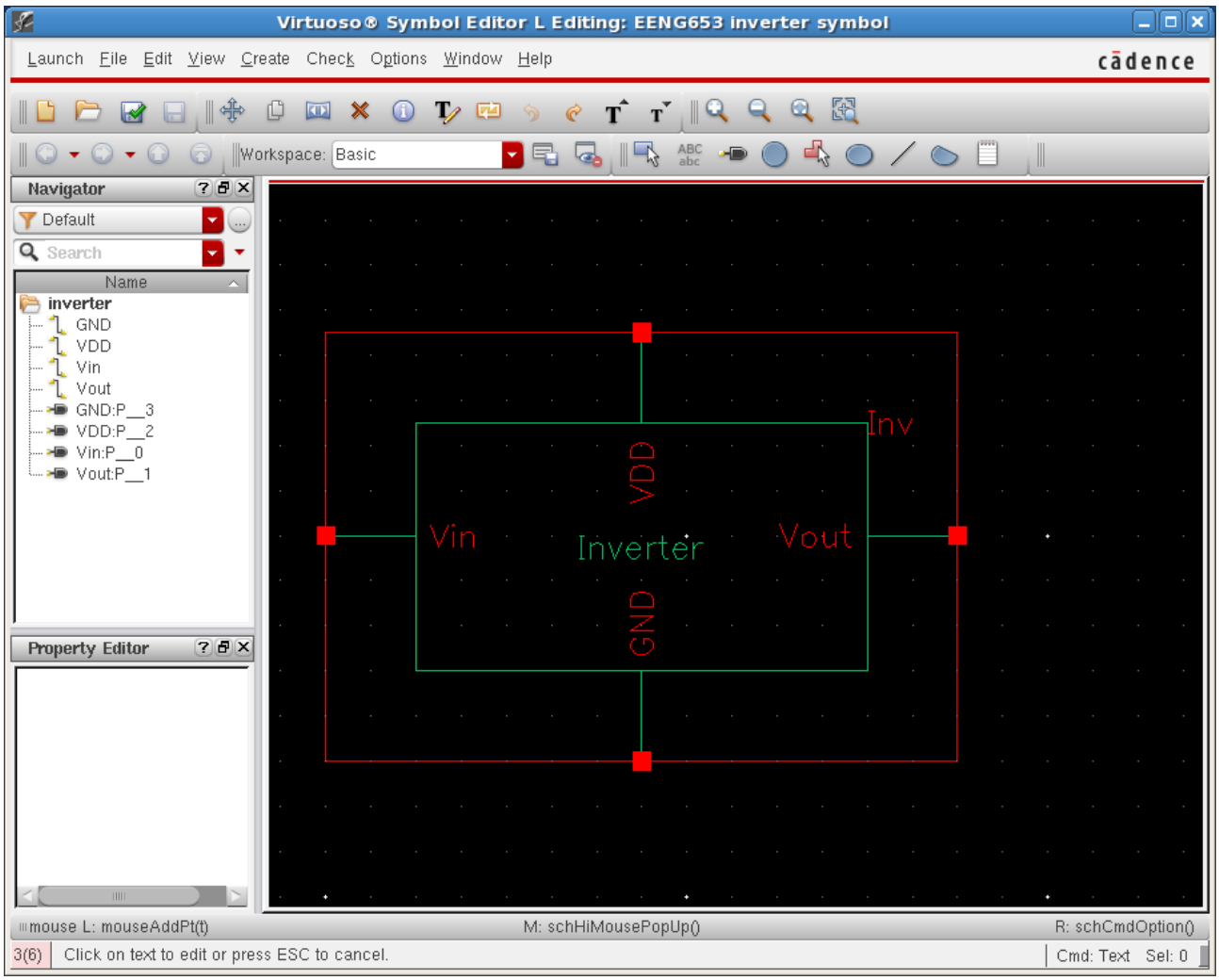
d. In the Symbol Generation Options Window, select the location of the pins as shown in the schematic, as represented in the image shown below.



e. After selecting the pins, click the 'OK' button on the Symbol Generation Options window. A Symbol Editor window will appear as shown in this figure.



f. Click in the Symbol Editor window and make the changes to the partName to 'Inverter' and instanceName to 'Inv' to match the image shown below.



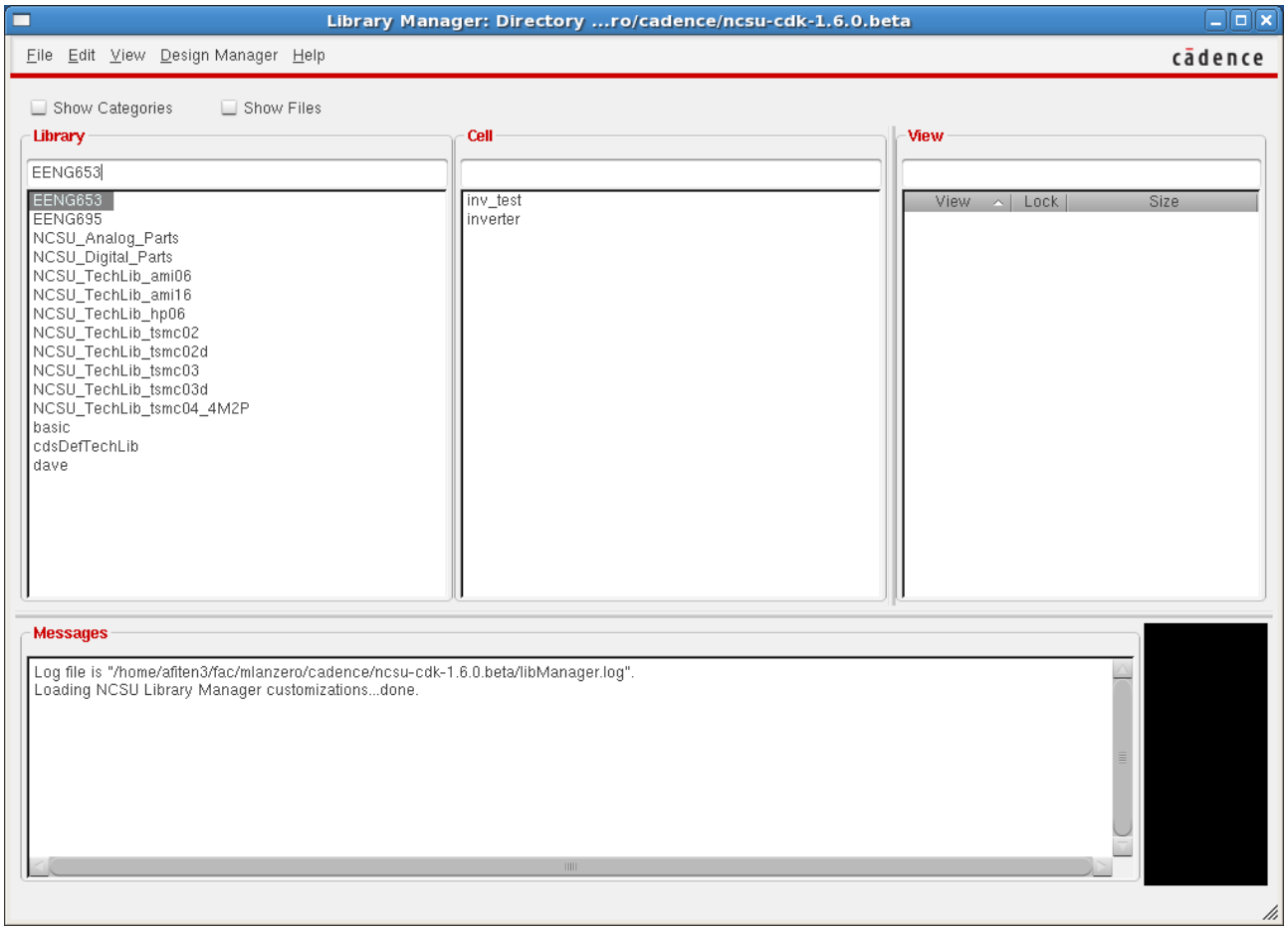
g. If you have extra time, you can manipulate the Symbol view to turn the rectangle into a triangle to represent the inverter. Use the menu (with the arrow pointing to the red back-wards L-shape) at the top of the Symbol Editor window to manipulate the geometry of your symbol. It is considered good design practice to create symbols of standard cells with the same size.

h. Now you have completed the task of creating a Symbol from a Schematic.

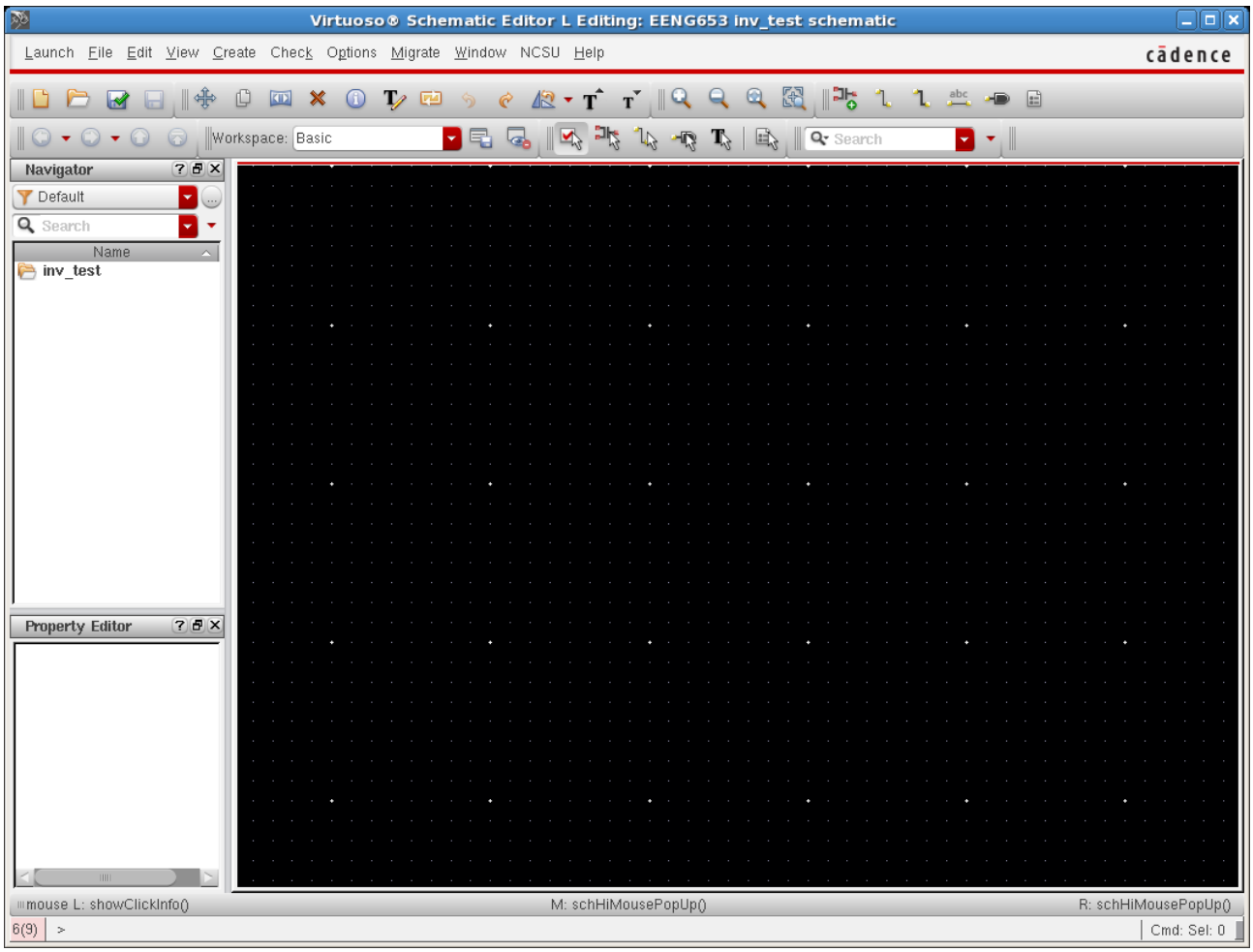
14. Inverter: Performing a Spectre Simulation on a Schematic

a. You are now going to create another Cell View to test the inverter that you created in the previous section. You are going to perform DC and transient (time-dependent) simulations on the inverter. In this laboratory, you are going to use Cadence spectre to perform the simulations.

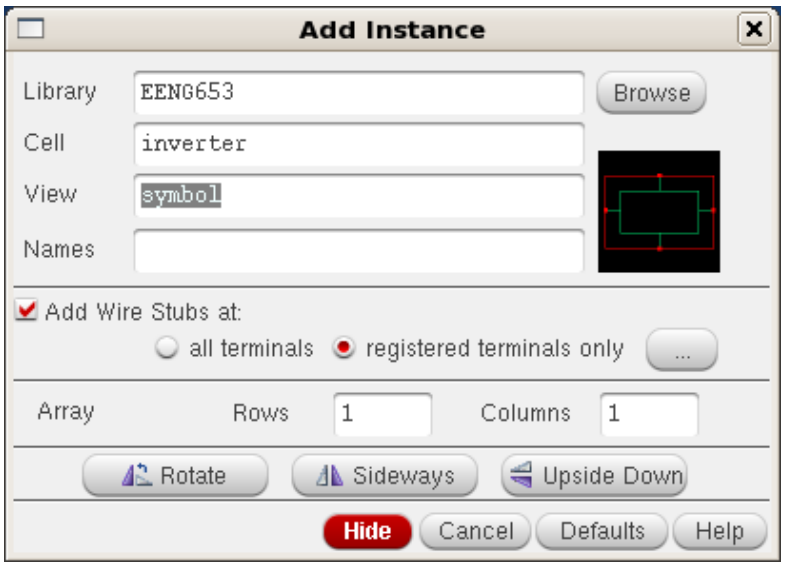
b. Create a new schematic Cell View called 'inv_test' in your EENG653 library, as shown in the figure below.



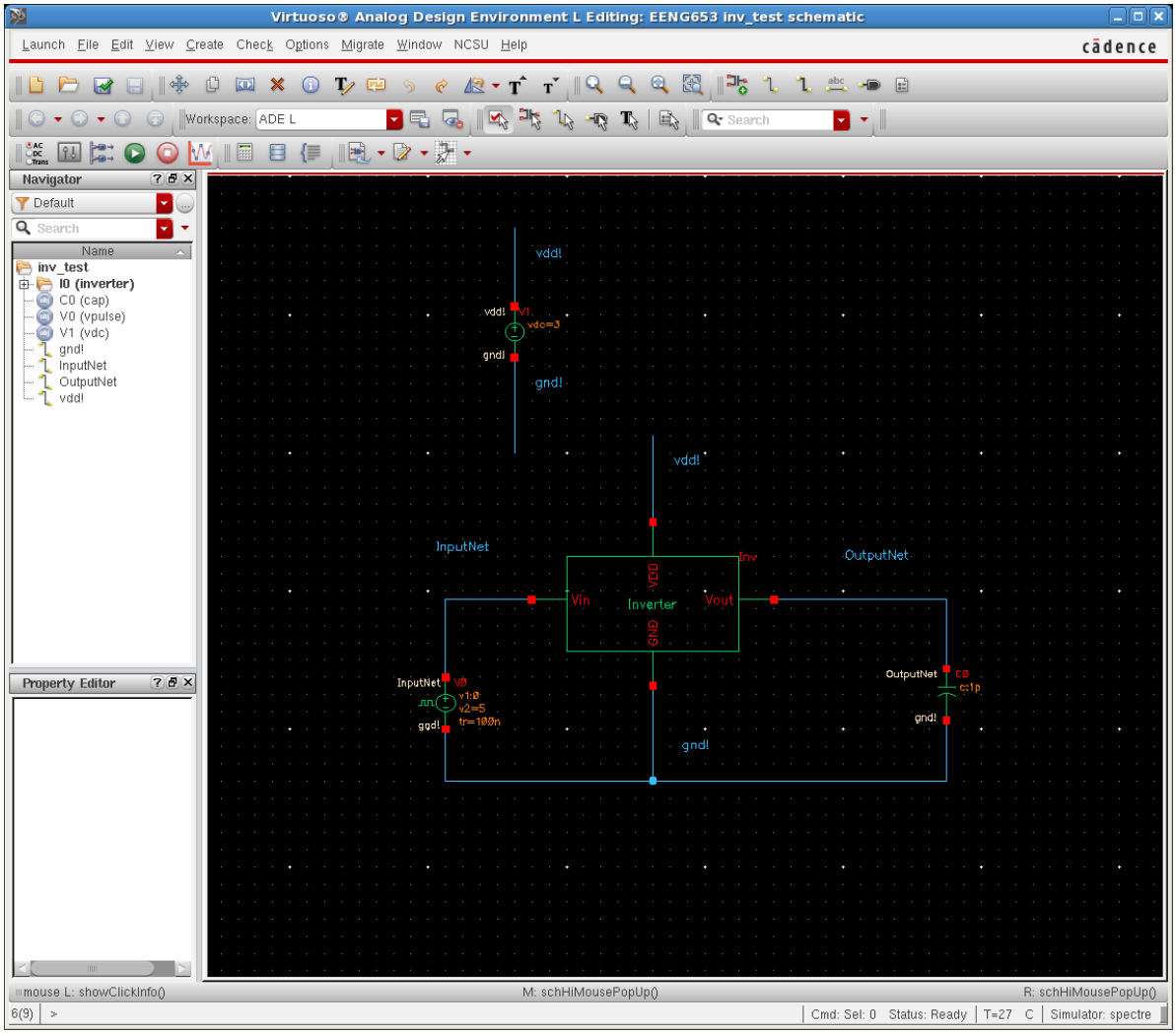
c. Open a schematic window for 'inv_test' as shown in the figure below.



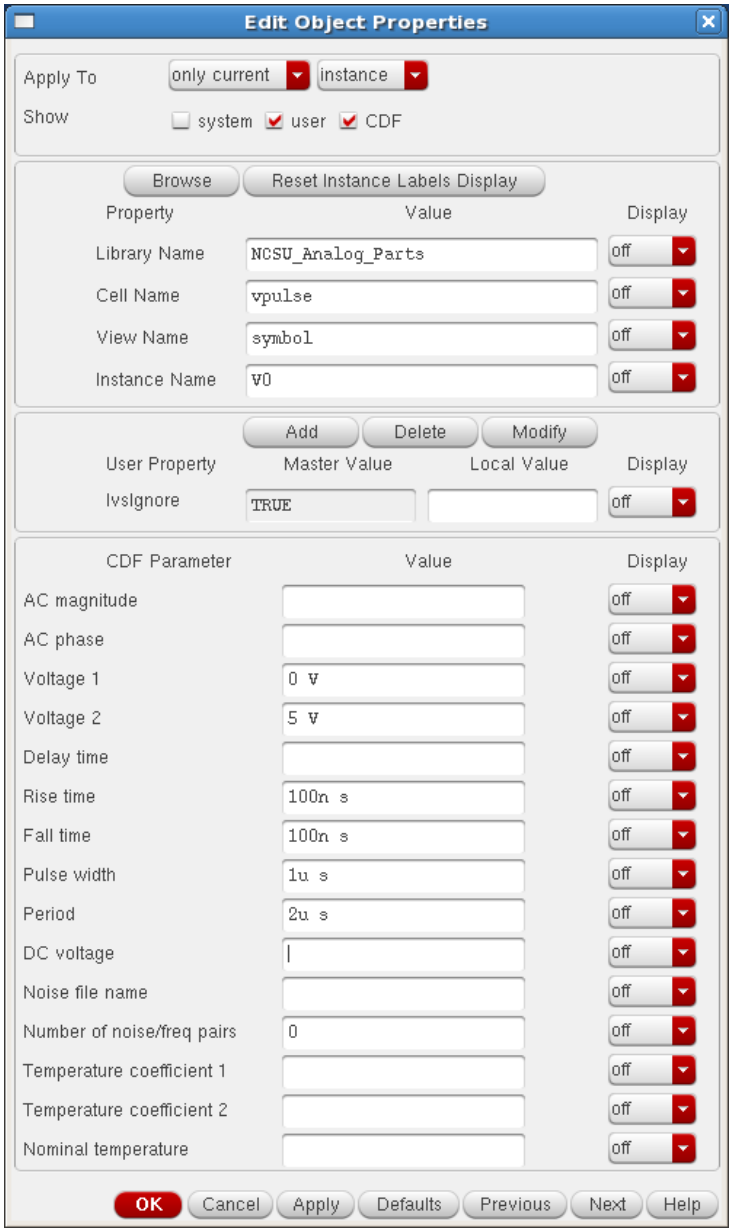
d. Create an instance of your inverter in the Schematic window. This inverter is the one that you created in the previous section. To create this inverter, click on the 'inv_test' Schematic Window and type 'i'. Then select 'EENG653 → inverter → symbol' and place the symbol in the 'inv_test' Schematic window as shown in the figure below.



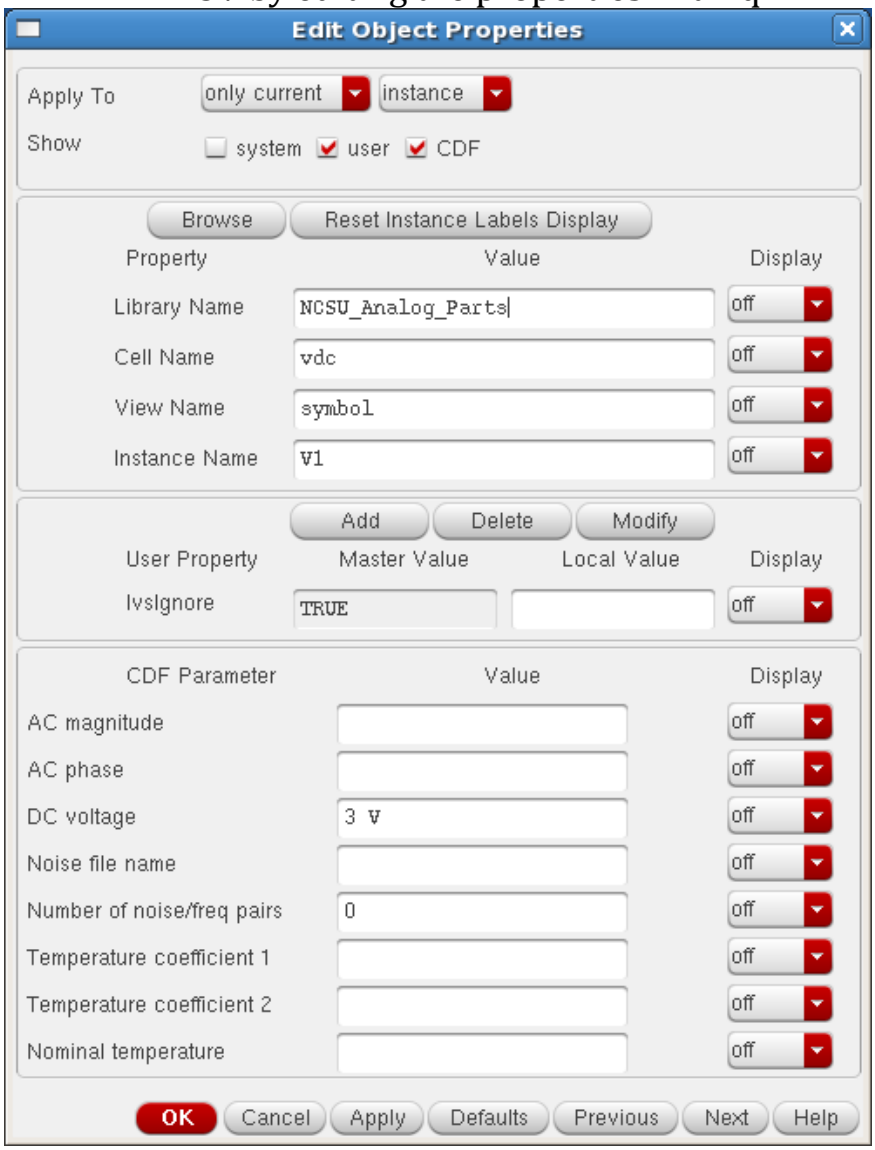
e. Now create two instances of voltage sources. First you will add a pulsed voltage source. Click on the 'inv_test' schematic window. Type 'I' in the window. Then select 'NCSU_Analog_Parts → Voltage_Sources → Vpulse' and place the instance in the 'inv_test' schematic as shown in the image below. Type "ESC".



f. Now you will edit the object properties of Vpulse as shown in the image below. For example, set 'Voltage 2' equal to 5V.



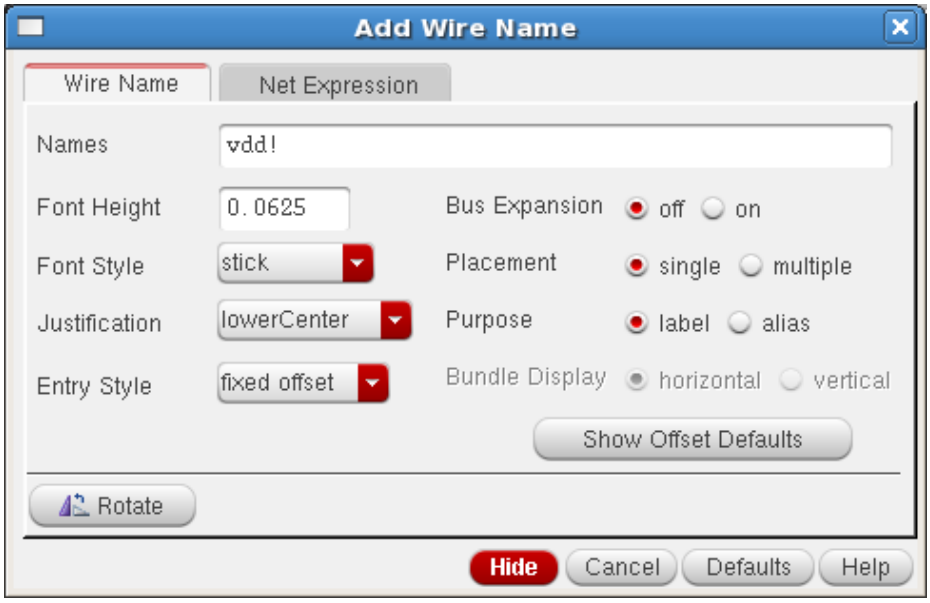
g. Now you will add a DC voltage source. Click on the 'inv_test' schematic window. Type 'I' in the window. Then select 'NCSU_Analog_Parts → Voltage Sources → VDC' and place the instance in the 'inv_test' schematic as shown in the 'inv_test' schematic image above. Type "ESC". Set the voltage source equal to 3V by editing the properties with 'q'.



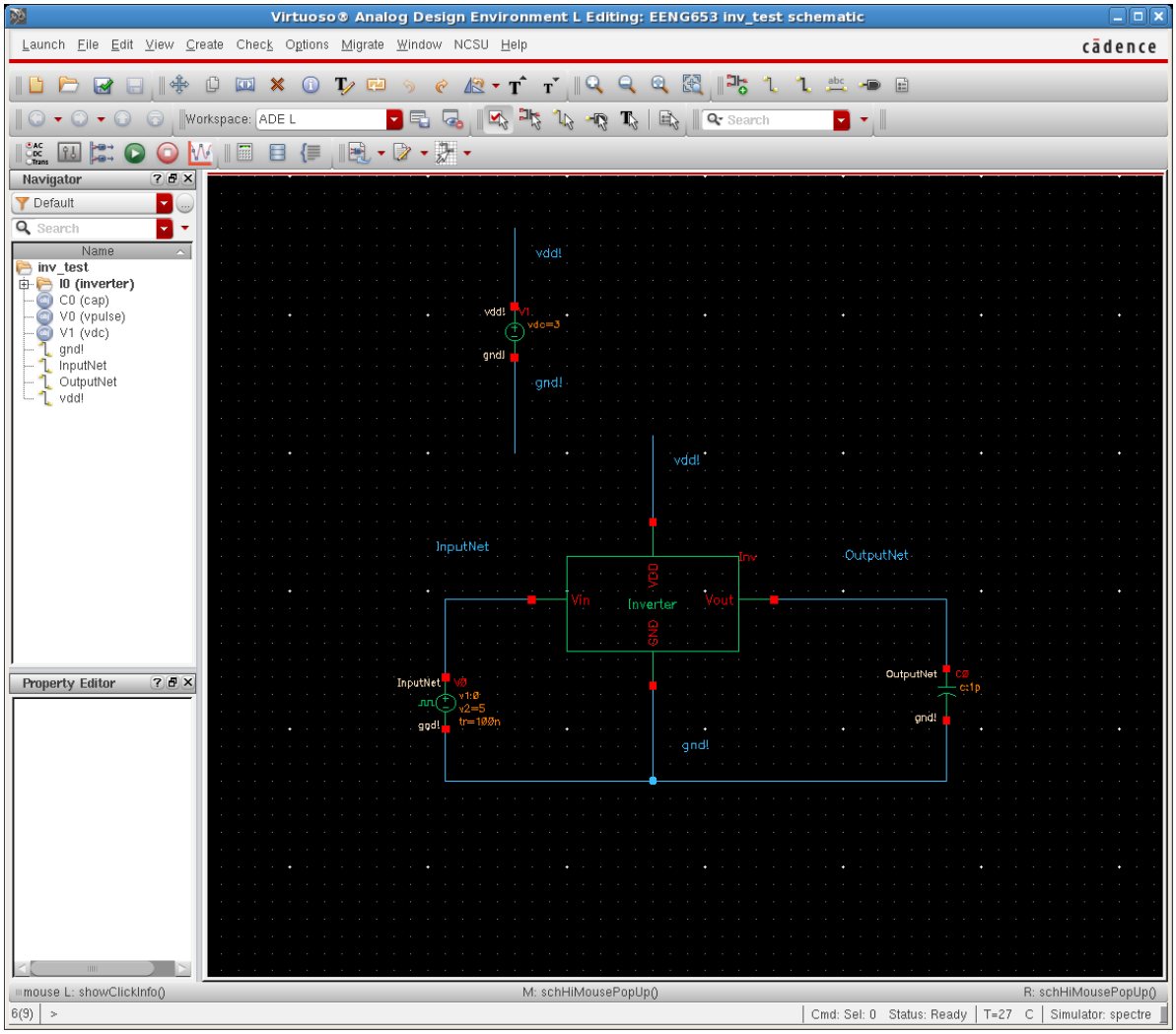
h. Now you will add a capacitor. Click on the 'inv_test' schematic window. Type 'I' in the window. Then select 'NCSU_Analog_Parts → R_L_C → cap' and place the instance in the 'inv_test' schematic as shown above.

i. Now connect these components with wires. Click on the 'inv_test' schematic window. Type 'w' in the window and add wires to connect the components as shown in the 'inv_test' schematic.

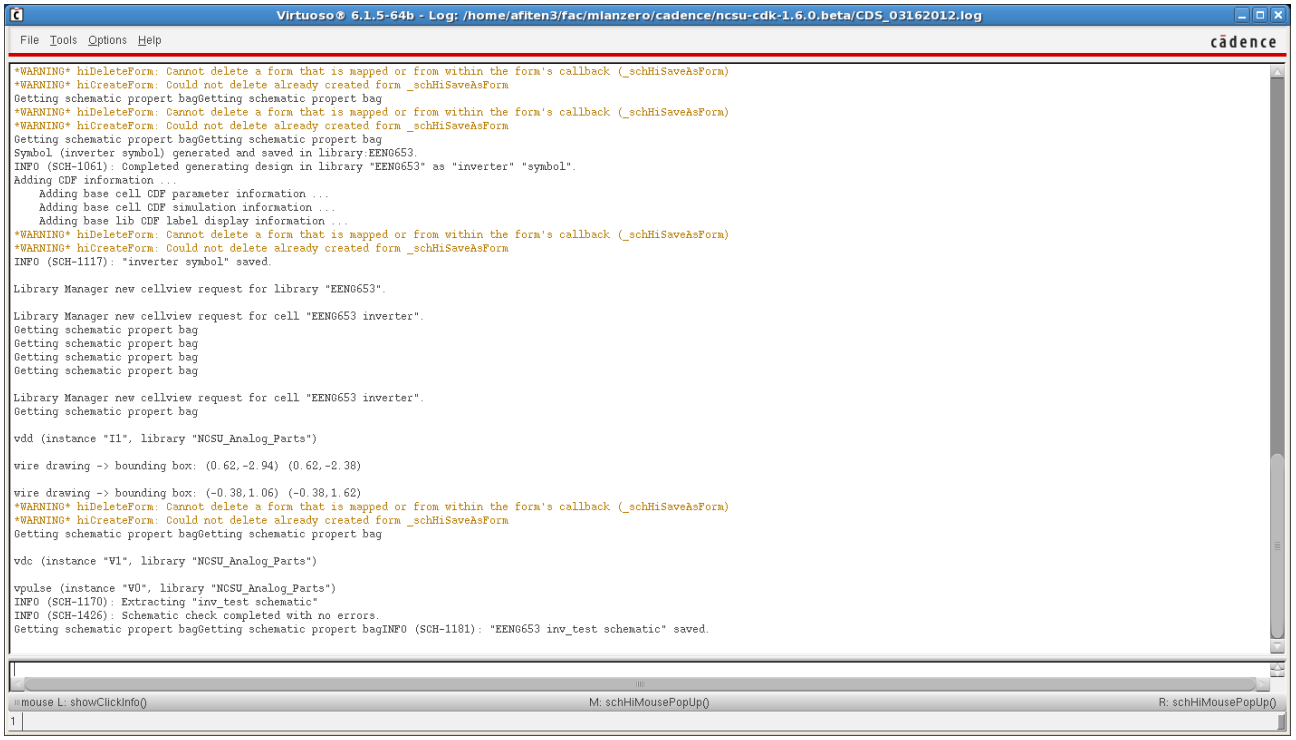
j. Label the ground and supply wires as shown in the 'inv_test' schematic by adding a wire name. To add a wire name and thereby label a wire, click on the wire and then type 'l' in the schematic. Type the desired name of the wire. This example shown the label for the wire called 'vdd!'. The use of the '!' indicates that this name is a global wire in the circuit. Two examples of global wires are 'vdd!' and 'gnd!' in your schematic. With the use of '!', you do not need to have separate pins for the supply terminals of each cell, and it is therefore convenient to use 'vdd!' and 'gnd!' to simplify the circuit.



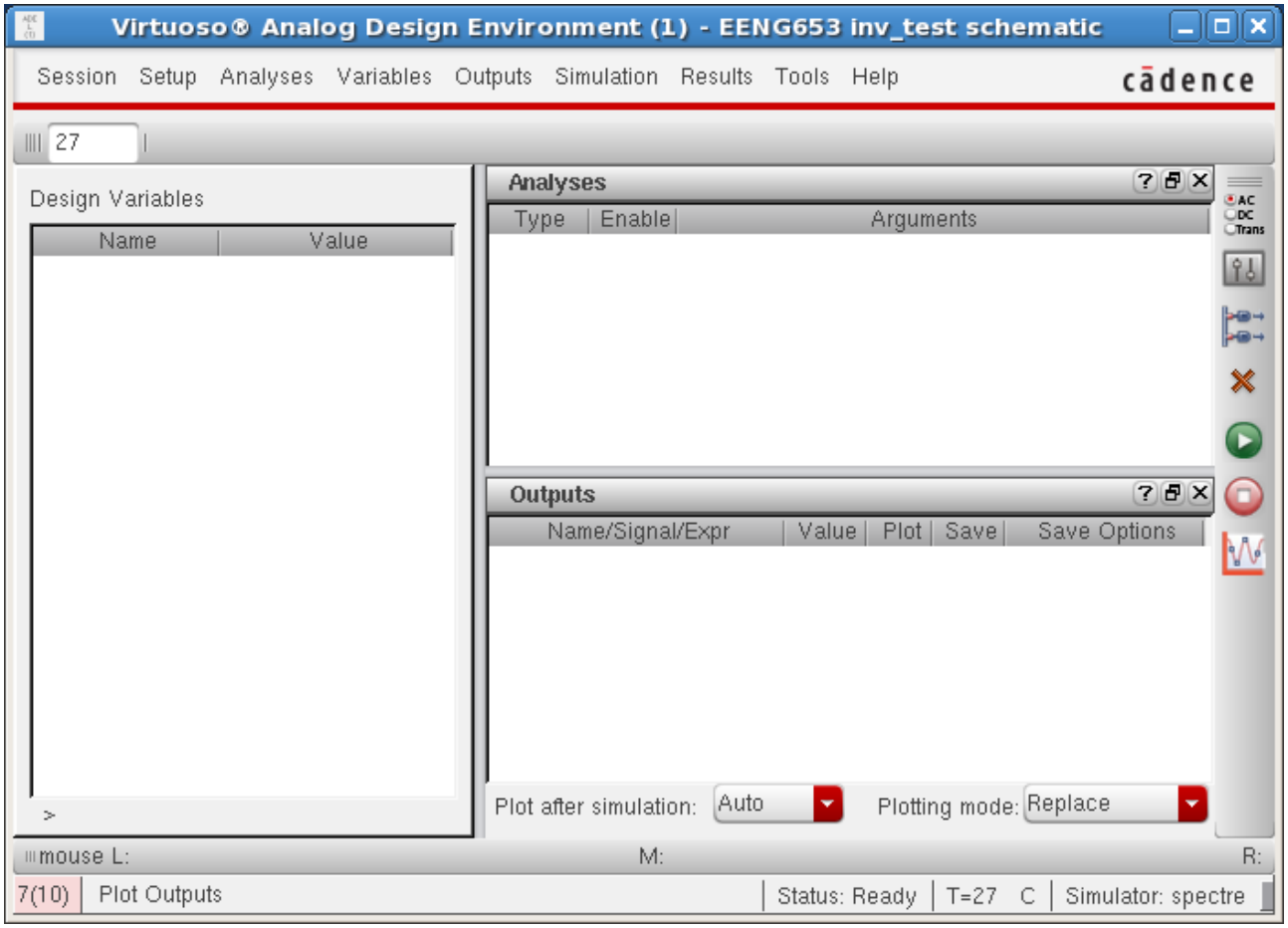
k. Label the net that is input to the inverter as 'InputNet' and the net that is output from the inverter as 'OutputNet' as shown in the schematic below. Now you have labeled all of the nets.



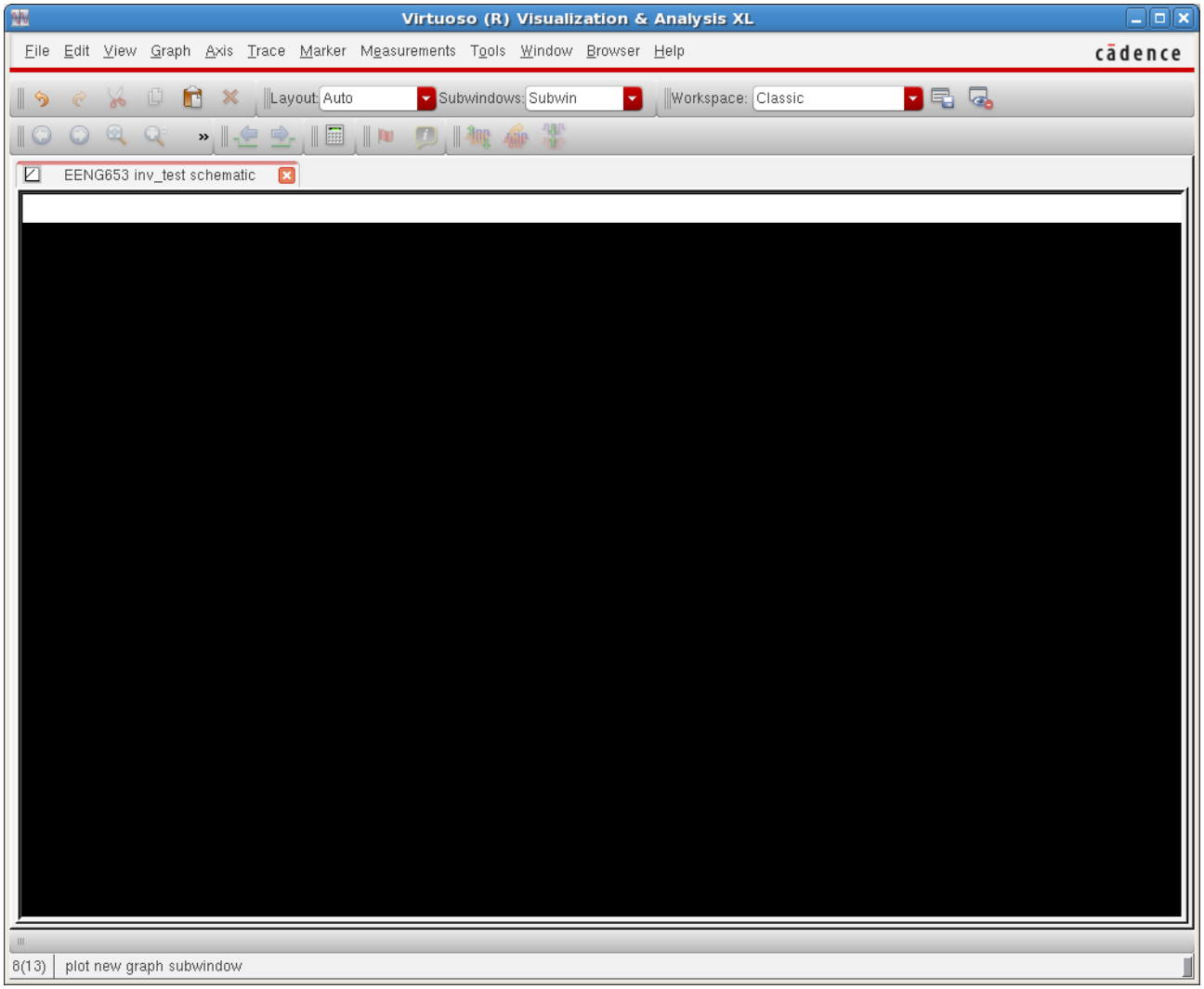
l. Now you will Check and Save your schematic. Click on the schematic editor for your 'inv_test' schematic. Select 'File → Check & Save.' The Check & Save should run without errors, as indicated in the log file in the CIW as shown in the image below.



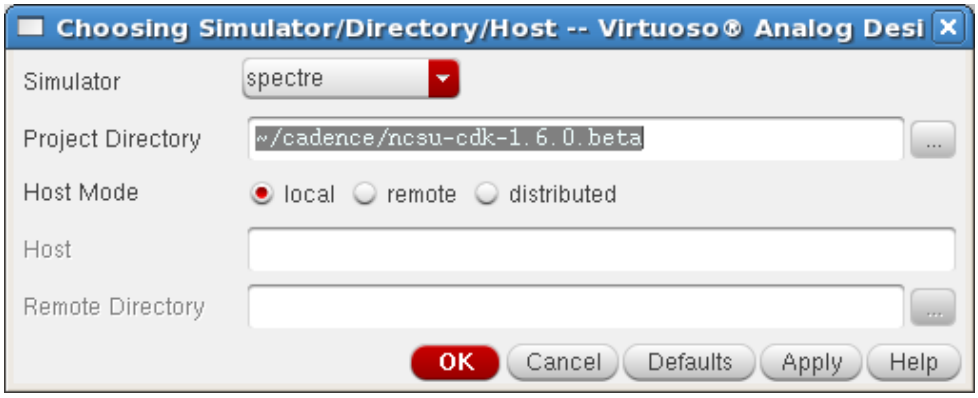
m. Now you will start the Spectre simulator. In the 'inv_test' schematic, click on 'Launch → ADE L' and click on 'Yes' to check out a license. One new window will appear with the title Virtuoso ® Analog Design Environment in the banner at the top of the window as shown below.



n. A second window may also appear titled 'Virtuoso ® Visualization & Analysis XL' window as shown below. If this window does not appear, it will show up later when you are plotting the waveforms from your schematic. (As a heads up, this will involve running a simulation and then selecting 'ADE→Results→Direct Plot→Transient Signal' after which the window will appear).

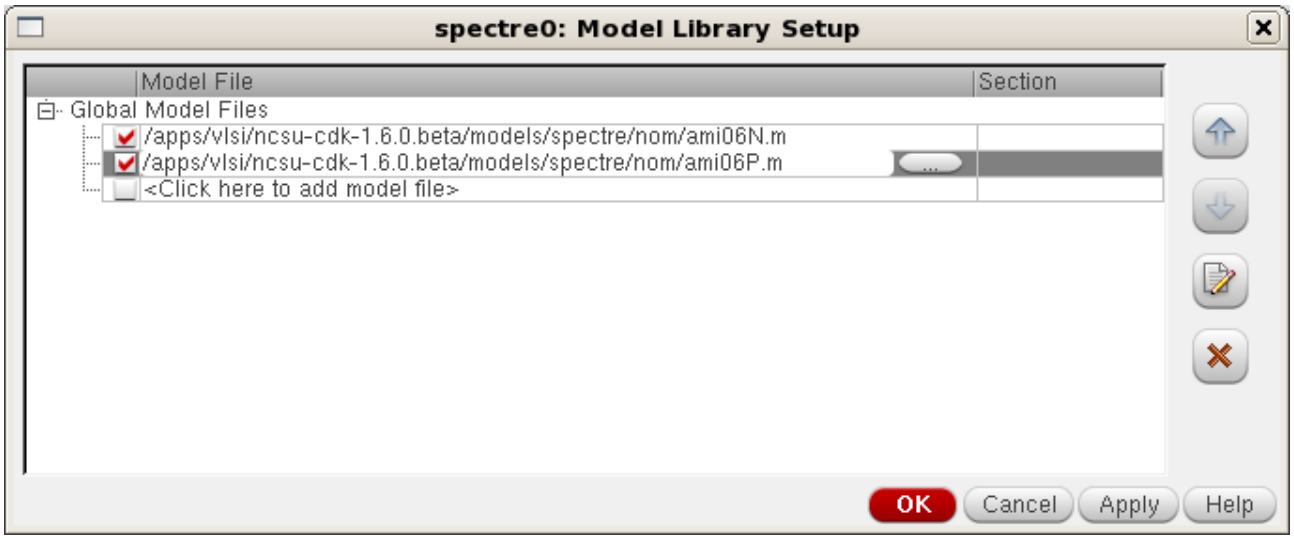


o. In the Virtuoso ® Analog Design Environment 'inv_test' schematic window, click 'Setup → Simulator/Directory/Host' and select 'spectre' as the simulator in the window that appears. Then click 'OK' in the 'Choosing Simulator/Directory/Host' window. The field for the Project Directory specifies the location where all the simulation files are written. Files in this directory should be removed regularly so that you have enough space for your simulations.

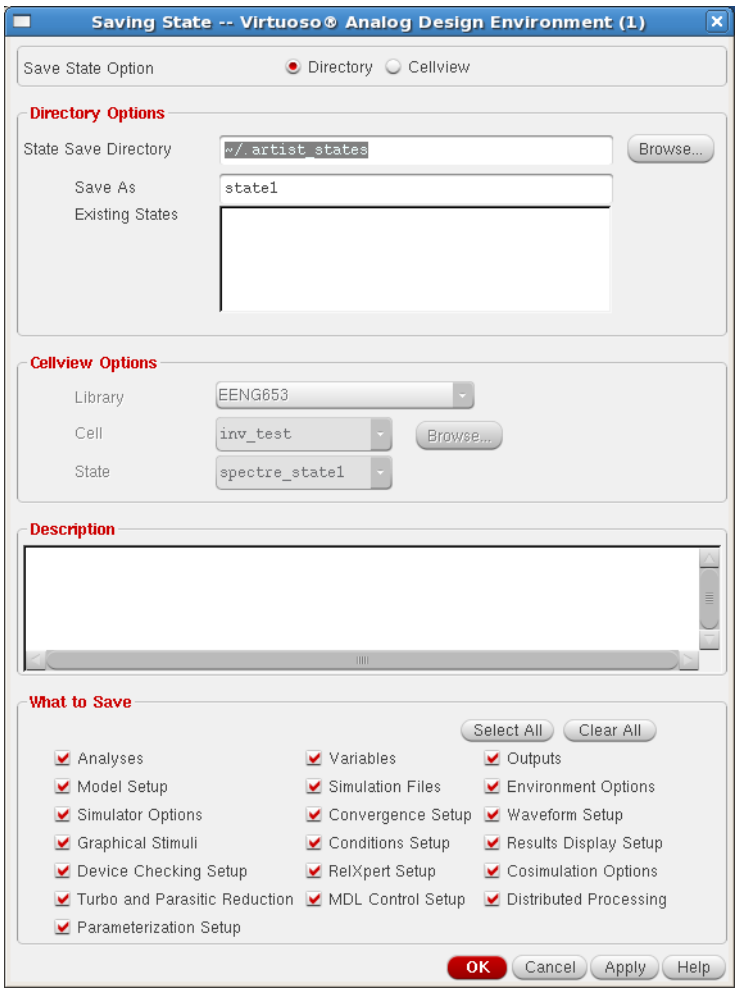


p. Now you are going to set up your model libraries to point to the models for the nfet and pfet that will simulated by spectre. Click on the Virtuoso ® Analog Design Environment window and click on 'Setup → Model Libraries'. The spectre0: Model Library Setup form will appear as shown in the image below. Select the two models for your nfet and pfet as shown in the image. At AFIT, the paths to the models for the nfet and pfet are, respectively:

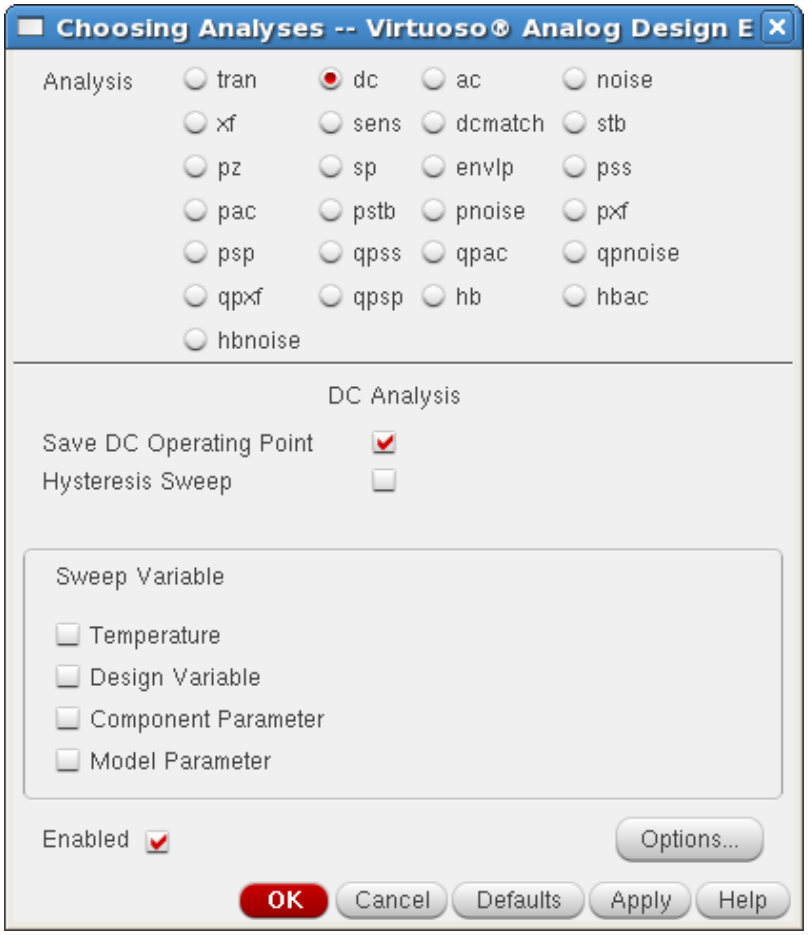
i. /apps/vlsi/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06N.m
ii. /apps/vlsi/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06P.m



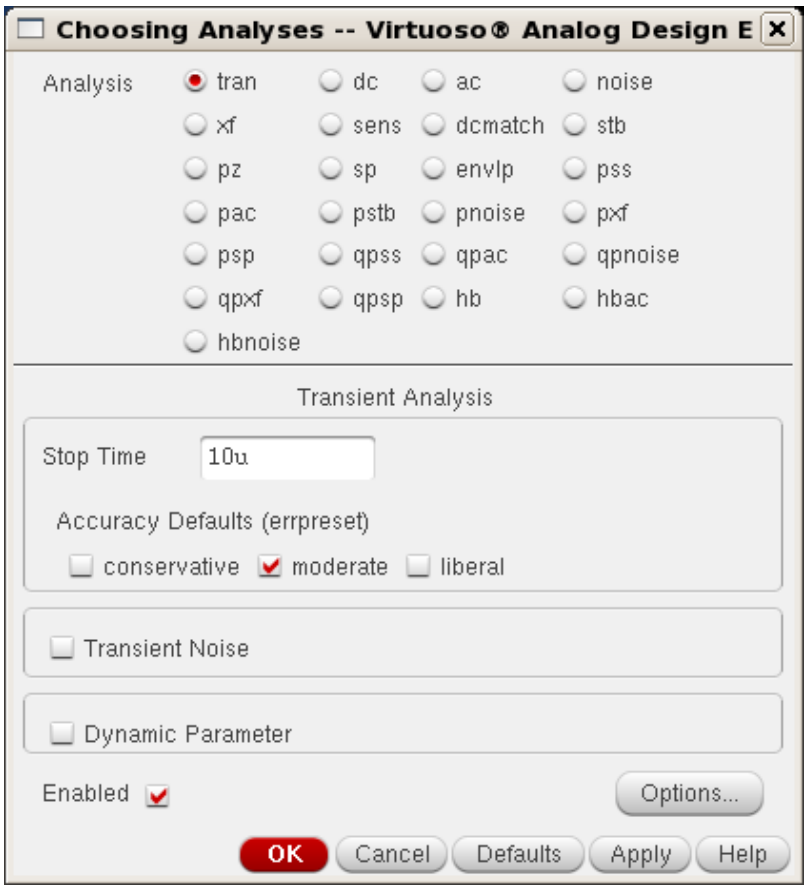
q. Now you will save these settings. In the Virtuoso ® Analog Design Environment, click on 'Session → Save State' and a window will appear. This window is the 'Saving State' window shown below. Each time you run the simulation, you can load the previous session so you do not need to load the model paths again.



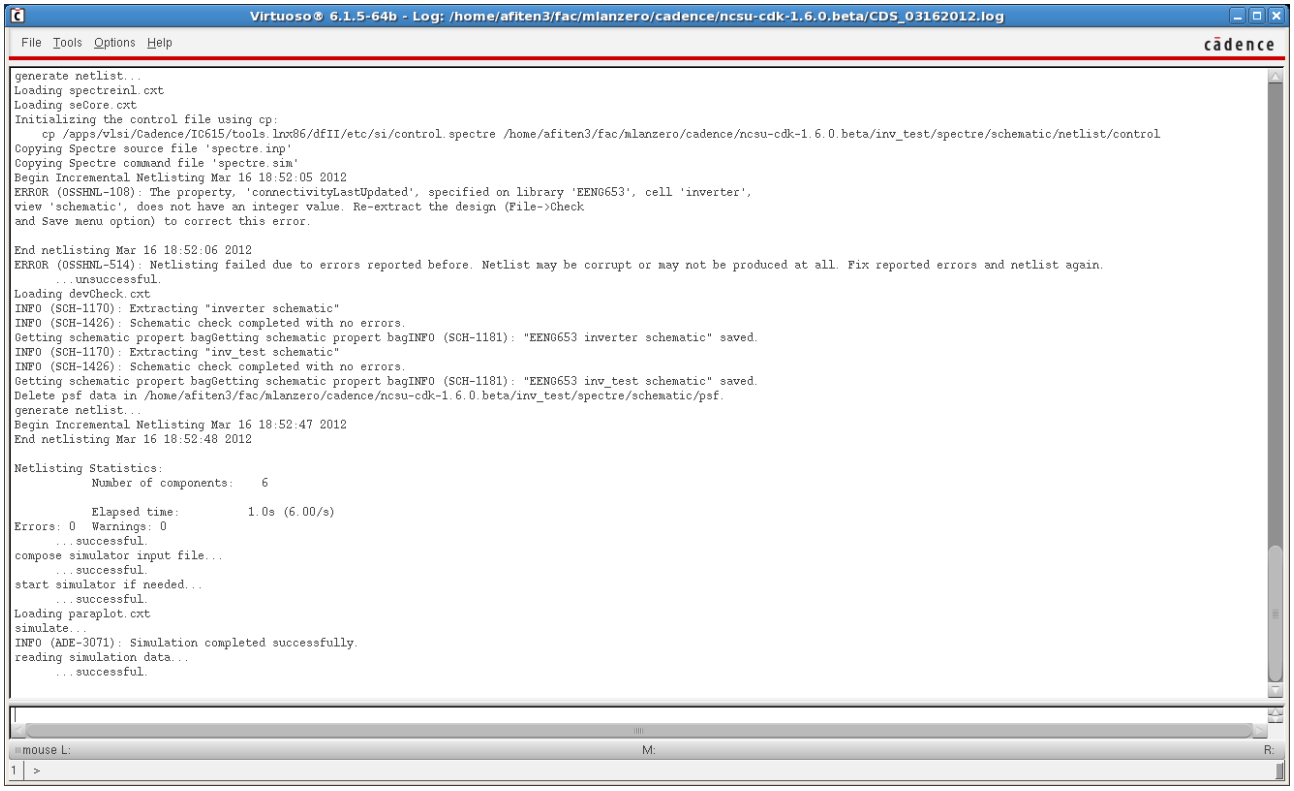
r. Now you are going to do a DC analysis and a transient (time-dependent) analysis of your inverter. To select the DC analysis type, in the Virtuoso ® Analog Design Environment window, click on 'Analyses → Choose', and a 'Choosing Analyses' window will appear as shown in the image below. In the 'Choosing Analyses' window select the 'dc' radio button and click the box for 'Save DC Operating Point'.



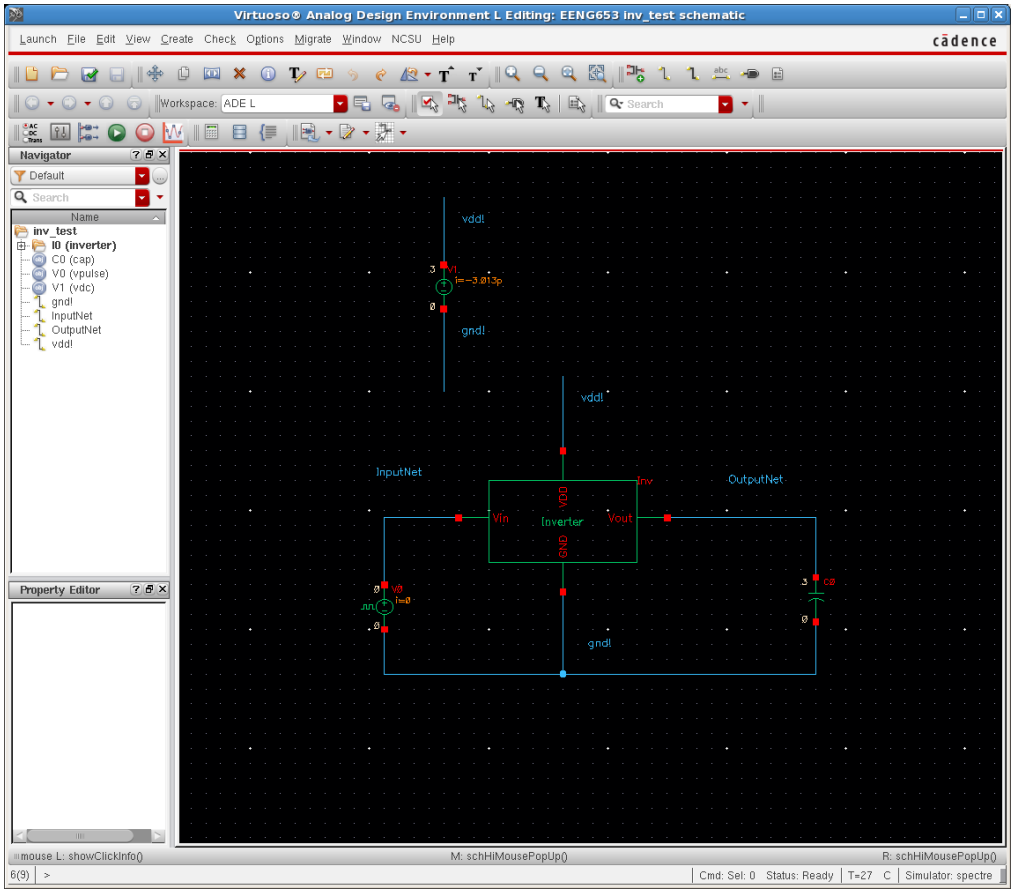
s. To select the Transient analysis type, in the Virtuoso ® Analog Design Environment window, click on 'Analyses → Choose', and a 'Choosing Analyses' window will appear as shown in the image below. In the 'Choosing Analyses' window select the 'tran' radio button and set the field 'Stop Time' equal to 10 microseconds (10 □s).



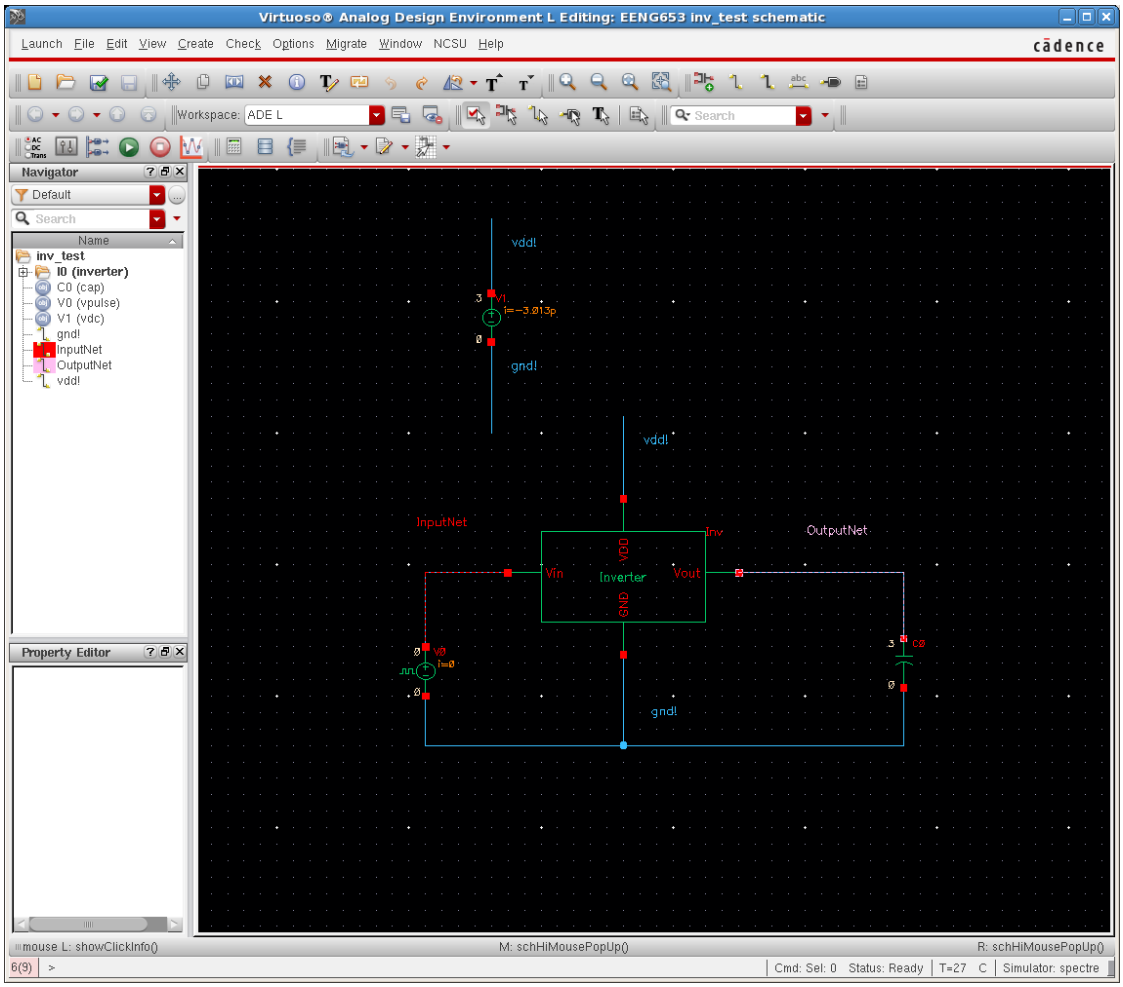
t. Now you are going to run the DC and transient simulations. In the Virtuoso ® Analog Design Environment window, click on 'Simulation → Run', and the simulation will run as shown in the CIW log file. The simulation should run successfully, as reported in the CIW log file.



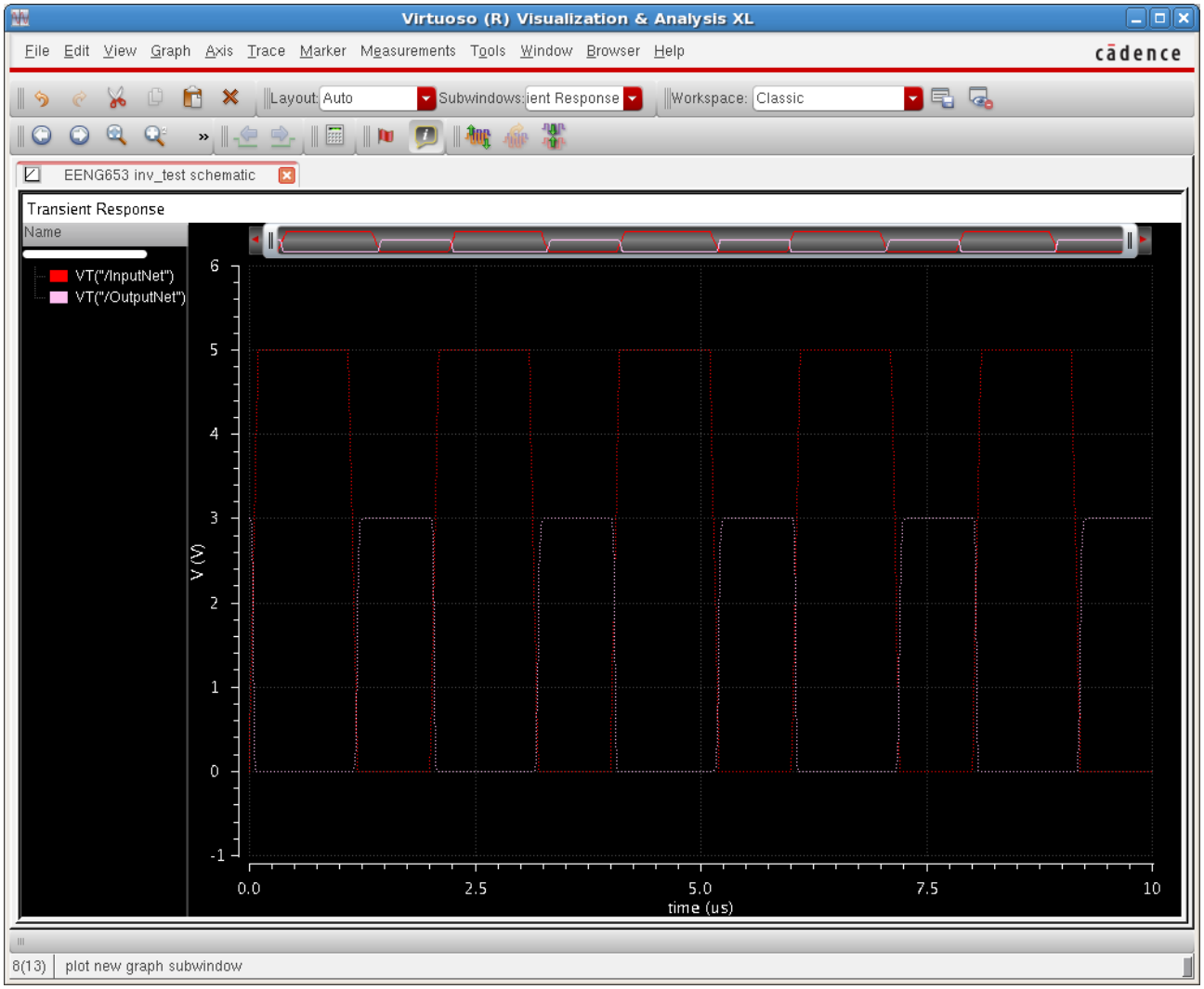
u. Now you can visualize the simulation results. To see the results of the DC analysis, in the Virtuoso ® Analog Design Environment, click on 'Results →Annotate →DC Node Voltages'. The results will be displayed in the schematic window with circuits.



v. To see the results of the transient analysis, in the Virtuoso ® Analog Design Environment, click on 'Results →Annotate →Transient Node Voltages'. Your cursor will move to the schematic window. To visualize the time-dependent values of the voltages on nets, click on the 'InputNet' and 'OutputNet' wires. The nets will become red and pink dashes after you click on them. (To visualize time-dependent values of current, click on nodes.)



w. After you have selected the wires, and they have become dashed, click 'ESC' in the window. A new Virtuoso ® Visualization & Analysis XL window appears as shown here. (Remember, this window may have appeared earlier as mentioned previously).



x. As mentioned previously, a second method to display the 'InputNet' and 'OutputNet' waveforms is to select 'ADE→Results→Direct Plot→Transient Signal.' Then on the Schematic, click on the 'InputNet' and 'OutputNet' and then click ESC. The waveforms will appear as shown in the plot above in the Visualization & Analysis XL window.

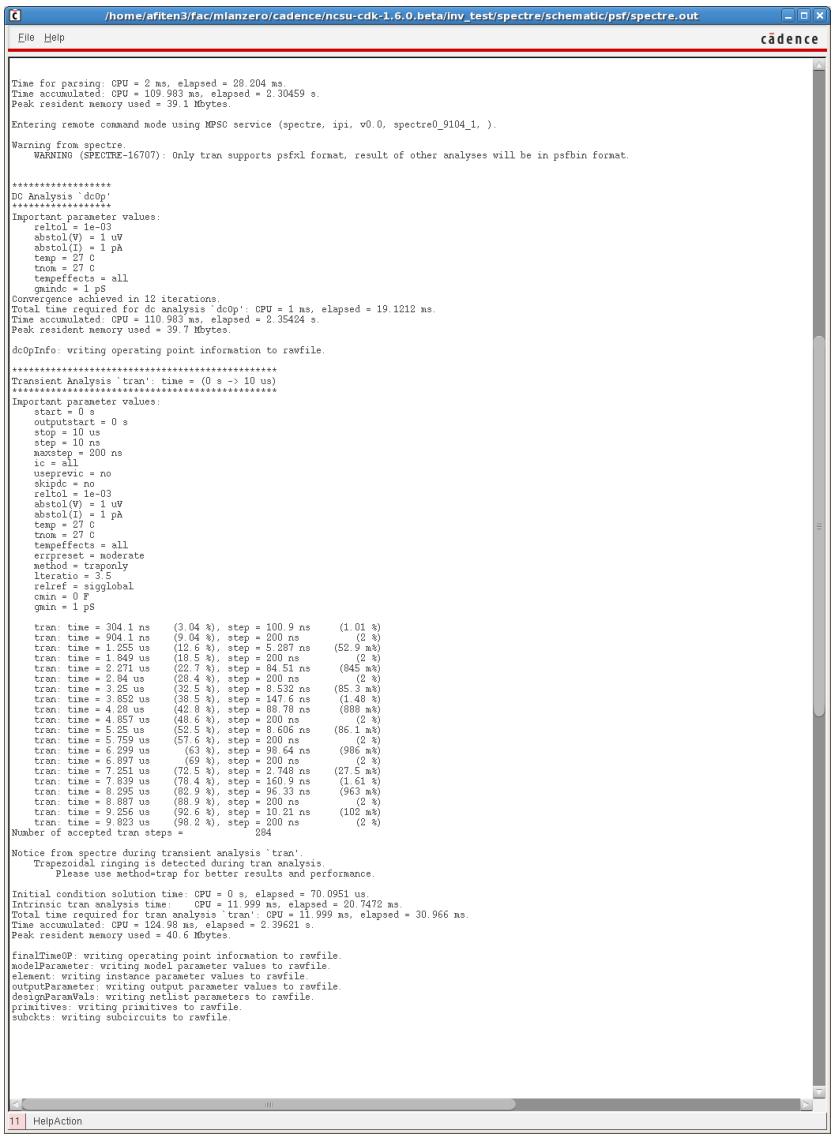
y. The spectre.out file that lists the output log file for the spectre simulator is shown below (divided into two parts for clarity).

/home/afiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/inv_test/spectre/schematic/psf/spectre.out

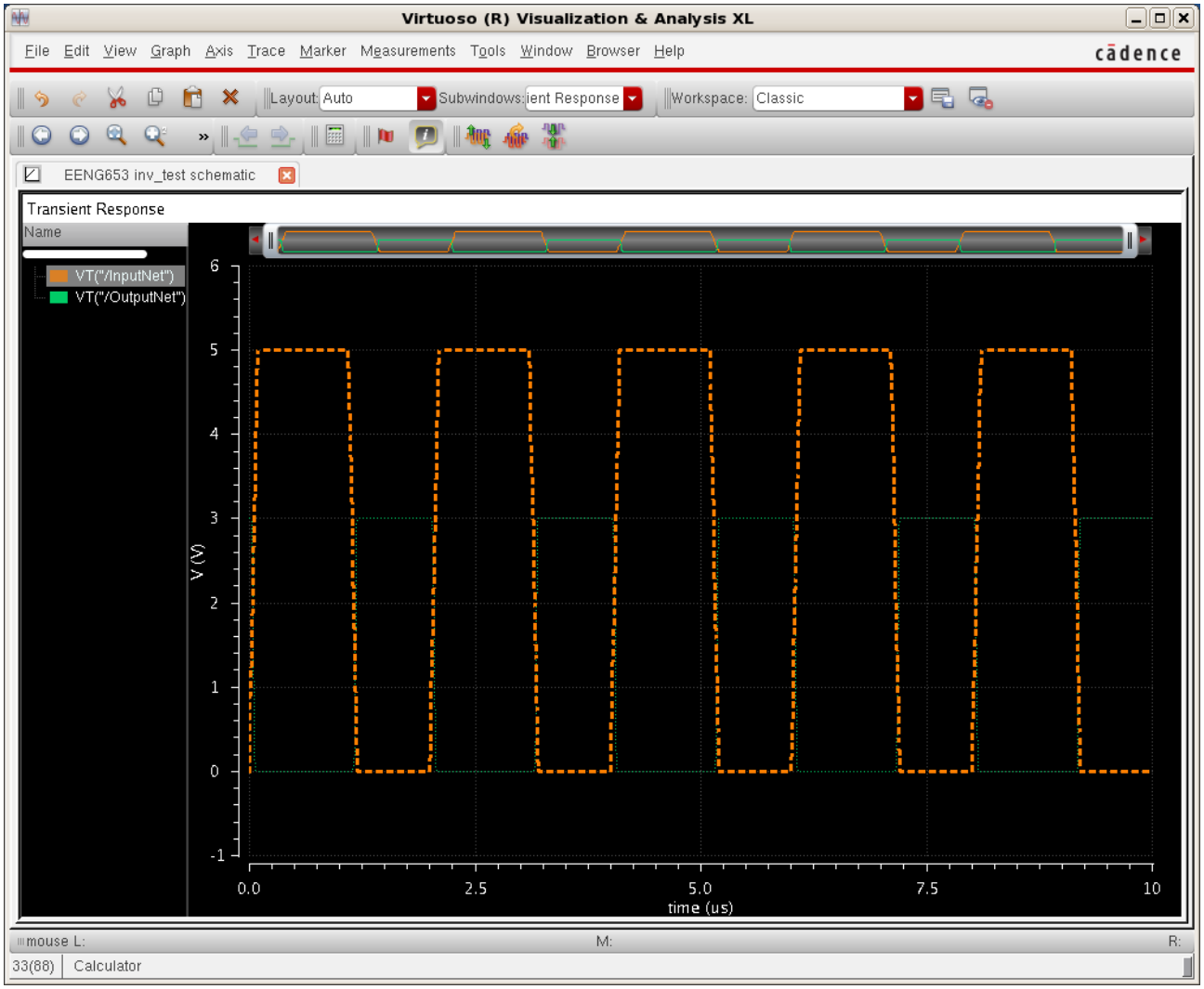
File Help cadence

```
Cadence (R) Virtuoso (R) Spectre (R) Circuit Simulator
Version 10.1.1.218.isr14 64bit -- 5 Sep 2011
Copyright (C) 1989-2010 Cadence Design Systems, Inc. All rights reserved worldwide. Cadence, Virtuoso and Spectre are registered trademarks of Ca

Protected by U.S. Patents:
        5,610,847; 5,790,436; 5,812,431; 5,859,785; 5,949,992; 5,987,238;
        6,088,523; 6,101,323; 6,151,698; 6,181,754; 6,260,176; 6,278,964;
        6,349,272; 6,374,390; 6,493,849; 6,504,885; 6,618,837; 6,636,839;
        6,778,025; 6,832,358; 6,851,097; 6,928,626; 7,024,652; 7,035,782;
        7,085,700; 7,143,021; 7,493,240; 7,571,401.

Includes RSA BSAFE(R) Cryptographic or Security Protocol Software from RSA Security, Inc.

User: mlanzero   Host: vlsilab05   HostID: 5c815119   PID: 9966
Memory  available: 23.0393 GB  physical: 25.2792 GB
CPU Type: Intel(R) Xeon(R) CPU           X5650  @ 2.670Hz
          Processor PhysicalID CoreID Frequency
              0         0        0     2660.1
              1         0        1     2660.1
              2         0        2     2660.1
              3         0        8     2660.1
              4         0        9     2660.1
              5         0       10     2660.1


Simulating `input.scs' on vlsilab05 at 6:52:51 PM, Fri Mar 16, 2012 (process id: 9966).
Environment variable:
    SPECTRE_DEFAULTS=-E
Command line:
    /apps/vlsi/Cadence/MMSIM101/tools.lnx86/spectre/bin/64bit/spectre  \
        input.scs +escchars +log  ../psf/spectre.out +inter=mpsc  \
        +mpssession=spectre0_9104_1 -format psfxl -raw ../psf  \
        +lqtimeout 900 -maxw 5 -maxn 5
spectre pid = 9966

Loading /apps/vlsi/Cadence/MMSIM101/tools.lnx86/cmi/lib/64bit/5.0/libinfineon_sh.so ...
Loading /apps/vlsi/Cadence/MMSIM101/tools.lnx86/cmi/lib/64bit/5.0/libphilips_sh.so ...
Loading /apps/vlsi/Cadence/MMSIM101/tools.lnx86/cmi/lib/64bit/5.0/libsparam_sh.so ...
Loading /apps/vlsi/Cadence/MMSIM101/tools.lnx86/cmi/lib/64bit/5.0/libstmodels_sh.so ...

Time for NDB Parsing: CPU = 90.985 ms, elapsed = 2.19821 s.
Time accumulated: CPU = 90.985 ms, elapsed = 2.19821 s.
Peak resident memory used = 34.1 Mbytes.


Time for Elaboration: CPU = 16.998 ms, elapsed = 57.3261 ms.
Time accumulated: CPU = 107.983 ms, elapsed = 2.25568 s.
Peak resident memory used = 38.1 Mbytes.


Time for EDB Visiting: CPU = 0 s, elapsed = 20.493 ms.
Time accumulated: CPU = 107.983 ms, elapsed = 2.27629 s.
Peak resident memory used = 38.4 Mbytes.


Circuit inventory:
                nodes 3
            bsim3v3 2
          capacitor 1
            vsource 2


Time for parsing: CPU = 2 ms, elapsed = 28.204 ms.
Time accumulated: CPU = 109.983 ms, elapsed = 2.30459 s.
Peak resident memory used = 39.1 Mbytes.

Entering remote command mode using MPSC service (spectre, ipi, v0.0, spectre0_9104_1, ).

Warning from spectre.
    WARNING (SPECTRE-16707): Only tran supports psfxl format, result of other analyses will be in psfbin format.


******************
DC Analysis `dcOp'
******************
Important parameter values:
    reltol = 1e-03
    abstol(V) = 1 uV
    abstol(I) = 1 pA
    temp = 27 C
    tnom = 27 C
    tempeffects = all
    gmindc = 1 pS
Convergence achieved in 12 iterations.
Total time required for dc analysis `dcOp': CPU = 1 ms, elapsed = 19.1212 ms.
Time accumulated: CPU = 110.983 ms, elapsed = 2.35424 s.
Peak resident memory used = 39.7 Mbytes.

dcOpInfo: writing operating point information to rawfile.

***********************************************
Transient Analysis `tran': time = (0 s -> 10 us)
***********************************************
Important parameter values:
    start = 0 s
    outputstart = 0 s
    stop = 10 us
    step = 10 ns
    maxstep = 200 ns
    ic = all
    useprevic = no
```

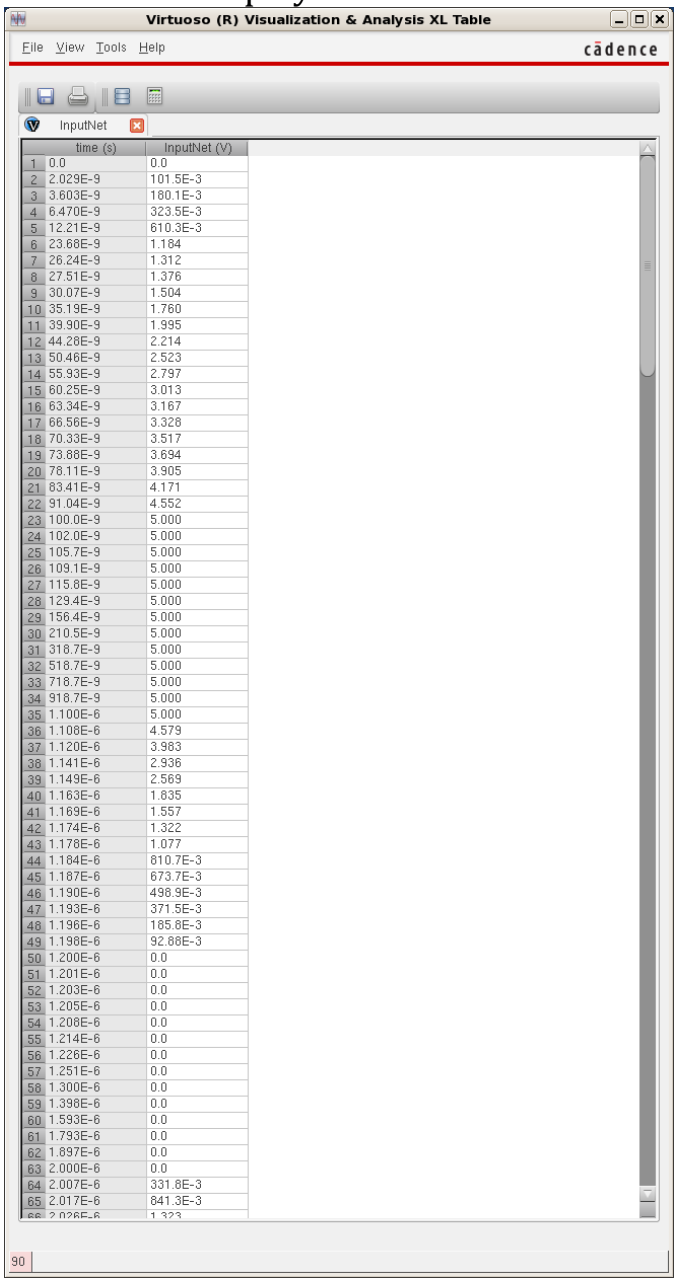
z. The second part of the spectre.out file that lists the output log file for the spectre simulator is shown below (divided into two parts for clarity).



aa. Click on the input waveform in the "Virtuoso Visualization & Analysis XL" window to display the waveform as a dashed, bold line as shown in the image below.



bb. Right-click on the bold dashed line (the input waveform) and select "Table → New Window." Notice when you move the cursor over the dashed line, the (x, y) coordinates of the waveform are displayed. The table below shows all coordinates.



Virtuoso (R) Visualization & Analysis XL Table

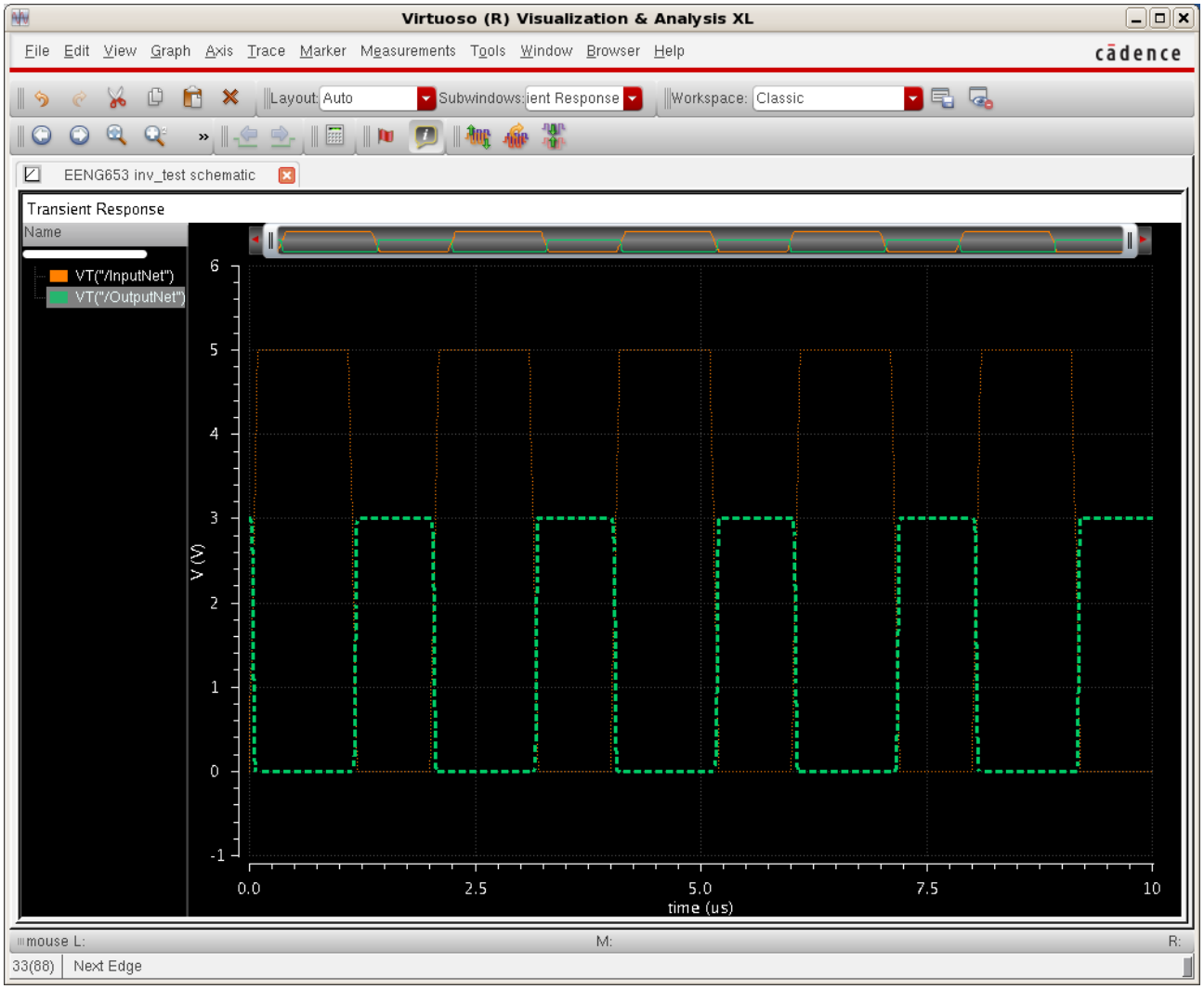
File View Tools Help cadence

InputNet

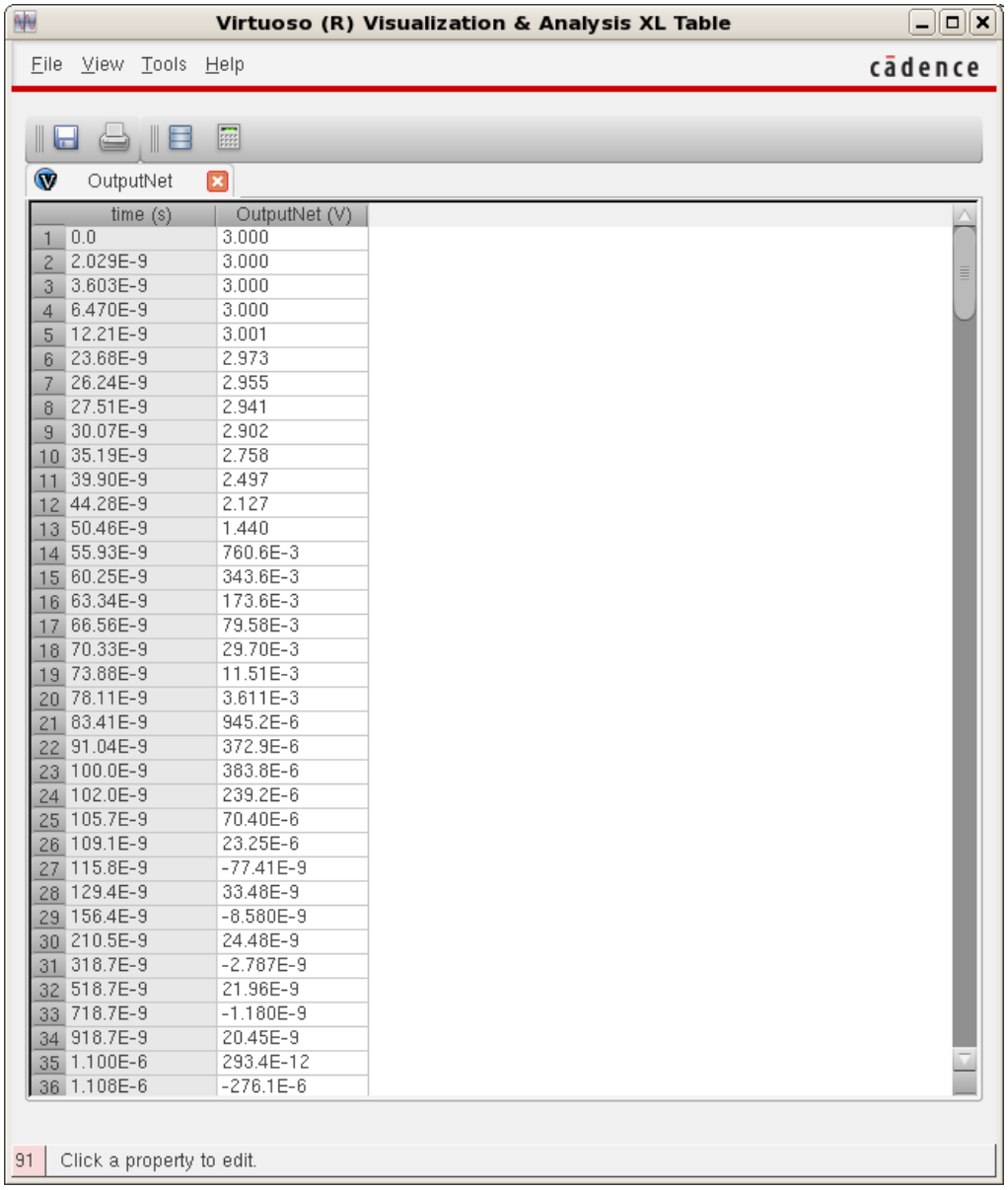
	time (s)	InputNet (V)
1	0.0	0.0
2	2.029E-9	101.5E-3
3	3.603E-9	180.1E-3
4	6.470E-9	323.5E-3
5	12.21E-9	610.3E-3
6	23.68E-9	1.184
7	26.24E-9	1.312
8	27.51E-9	1.376
9	30.07E-9	1.504
10	35.19E-9	1.760
11	39.90E-9	1.995
12	44.28E-9	2.214
13	50.46E-9	2.523
14	55.93E-9	2.797
15	60.25E-9	3.013
16	63.34E-9	3.167
17	66.56E-9	3.328
18	70.33E-9	3.517
19	73.88E-9	3.694
20	78.11E-9	3.905
21	83.41E-9	4.171
22	91.04E-9	4.552
23	100.0E-9	5.000
24	102.0E-9	5.000
25	105.7E-9	5.000
26	109.1E-9	5.000
27	115.8E-9	5.000
28	129.4E-9	5.000
29	156.4E-9	5.000
30	210.5E-9	5.000
31	318.7E-9	5.000
32	518.7E-9	5.000
33	718.7E-9	5.000
34	918.7E-9	5.000
35	1.100E-6	5.000
36	1.108E-6	4.579
37	1.120E-6	3.983
38	1.141E-6	2.936
39	1.149E-6	2.569
40	1.163E-6	1.835
41	1.169E-6	1.557
42	1.174E-6	1.322
43	1.178E-6	1.077
44	1.184E-6	810.7E-3
45	1.187E-6	673.7E-3
46	1.190E-6	498.9E-3
47	1.193E-6	371.5E-3
48	1.196E-6	185.8E-3
49	1.198E-6	92.88E-3
50	1.200E-6	0.0
51	1.201E-6	0.0
52	1.203E-6	0.0
53	1.205E-6	0.0
54	1.208E-6	0.0
55	1.214E-6	0.0
56	1.226E-6	0.0
57	1.251E-6	0.0
58	1.300E-6	0.0
59	1.398E-6	0.0
60	1.593E-6	0.0
61	1.793E-6	0.0
62	1.897E-6	0.0
63	2.000E-6	0.0
64	2.007E-6	331.8E-3
65	2.017E-6	841.3E-3
66	2.026E-6	1.323

90

cc. Click on the output waveform in the "Virtuoso Visualization & Analysis XL" window to display the waveform as a dashed, bold line as shown in the image below.



dd. Right click on the bold dashed line (the input waveform) and select "Table → New Window." Notice when you move the cursor over the dashed line, the (x, y) coordinates of the waveform are displayed. The table below shows all coordinates.



	time (s)	OutputNet (V)
1	0.0	3.000
2	2.029E-9	3.000
3	3.603E-9	3.000
4	6.470E-9	3.000
5	12.21E-9	3.001
6	23.68E-9	2.973
7	26.24E-9	2.955
8	27.51E-9	2.941
9	30.07E-9	2.902
10	35.19E-9	2.758
11	39.90E-9	2.497
12	44.28E-9	2.127
13	50.46E-9	1.440
14	55.93E-9	760.6E-3
15	60.25E-9	343.6E-3
16	63.34E-9	173.6E-3
17	66.56E-9	79.58E-3
18	70.33E-9	29.70E-3
19	73.88E-9	11.51E-3
20	78.11E-9	3.611E-3
21	83.41E-9	945.2E-6
22	91.04E-9	372.9E-6
23	100.0E-9	383.8E-6
24	102.0E-9	239.2E-6
25	105.7E-9	70.40E-6
26	109.1E-9	23.25E-6
27	115.8E-9	-77.41E-9
28	129.4E-9	33.48E-9
29	156.4E-9	-8.580E-9
30	210.5E-9	24.48E-9
31	318.7E-9	-2.787E-9
32	518.7E-9	21.96E-9
33	718.7E-9	-1.180E-9
34	918.7E-9	20.45E-9
35	1.100E-6	293.4E-12
36	1.108E-6	-276.1E-6

ee. From the information contained in the (x, y) tables obtained from the input waveform and the output waveform, values for the following quantities can be obtained:

i. For the falling transition of the input waveform
    1. Fall time (The time for the value of the waveform to fall from 90% to 10% of its maximum value, usually VDD, to GND).
    2. Delay (The time between when the value of the input waveform is halfway between its minimum and maximum values and when the value of the output waveform is halfway between its minimum and maximum values).

ii. For the rising transition of the input waveform
    1. Rise time (The time for the value of the waveform to rise from 10% to 90% of its maximum value, usually VDD, from GND).
    2. Delay

ff. The value of the width of the inverter pfet can be changed so that it is double the width of the inverter nfet (a new value of the beta ratio). New values for the following quantities can be obtained and compared with the values in (ee).

gg. The value of the width of the inverter pfet can be changed so that it is triple the width of the inverter nfet (another new value of the beta ratio). New values for the following quantities can be obtained and compared with the values in (ee) and (ff).

hh. The value of the output load (cap) can be changed to C = 10pF and to C = 100pF. For each case, calculate the Rise time, Fall time and delay for the rising transition and falling transition. Compare with results in (ee).

ii. The value of the voltage driving the input net can be adjusted to 3V (to match the output net). Simulations can then be performed for the case in which the inverter pfet:

i. Takes on the initial value of the width.
    1. values for the following quantities can be obtained:
        a. For the falling transition of the input waveform
            i. Fall time
            ii. Delay
        b. For the rising transition of the input waveform
            i. Rise time
            ii. Delay

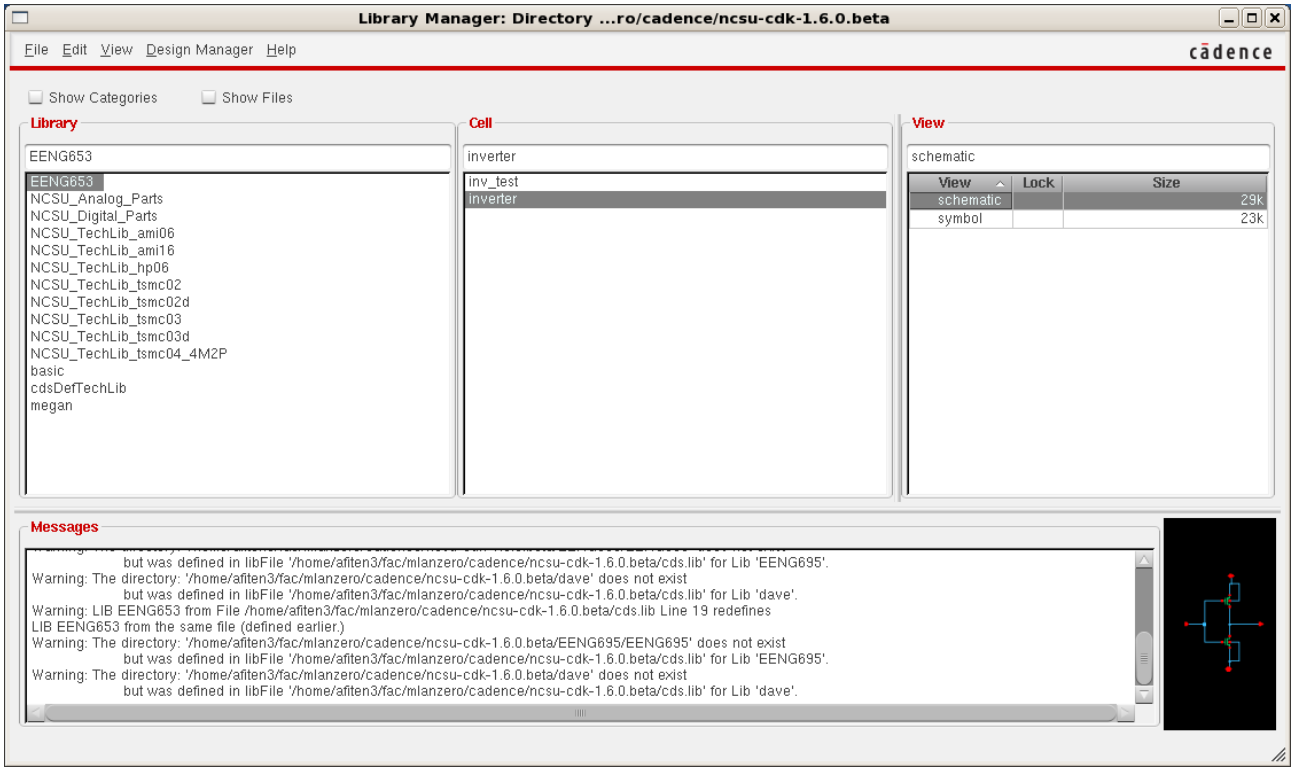
ii. Has twice the width of the inverter pfet
    1. values for the following quantities can be obtained:
        a. For the falling transition of the input waveform
            i. Fall time
            ii. Delay
        b. For the rising transition of the input waveform
            i. Rise time
            ii. Delay

iii. Has three times the width of the inverter pfet
    1. values for the following quantities can be obtained:
        a. For the falling transition of the input waveform
            i. Fall time
            ii. Delay
        b. For the rising transition of the input waveform
            i. Rise time
            ii. Delay

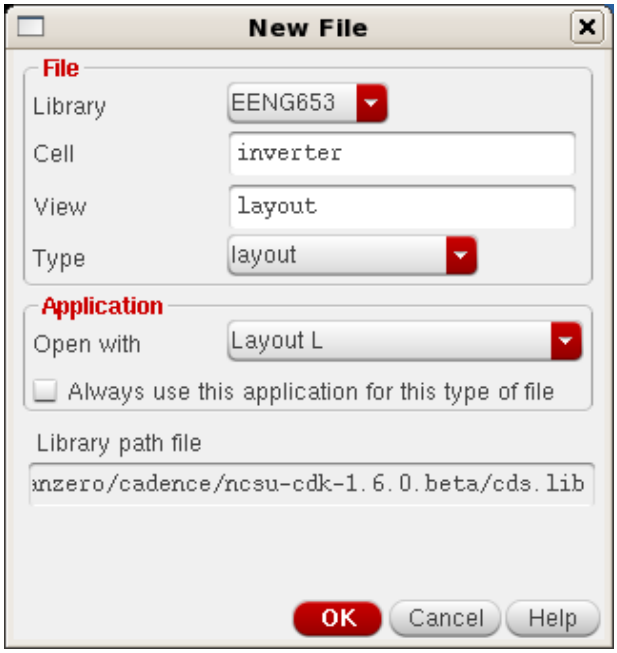
jj. Now you have simulated your inverter.

15. Inverter: Creating a Layout

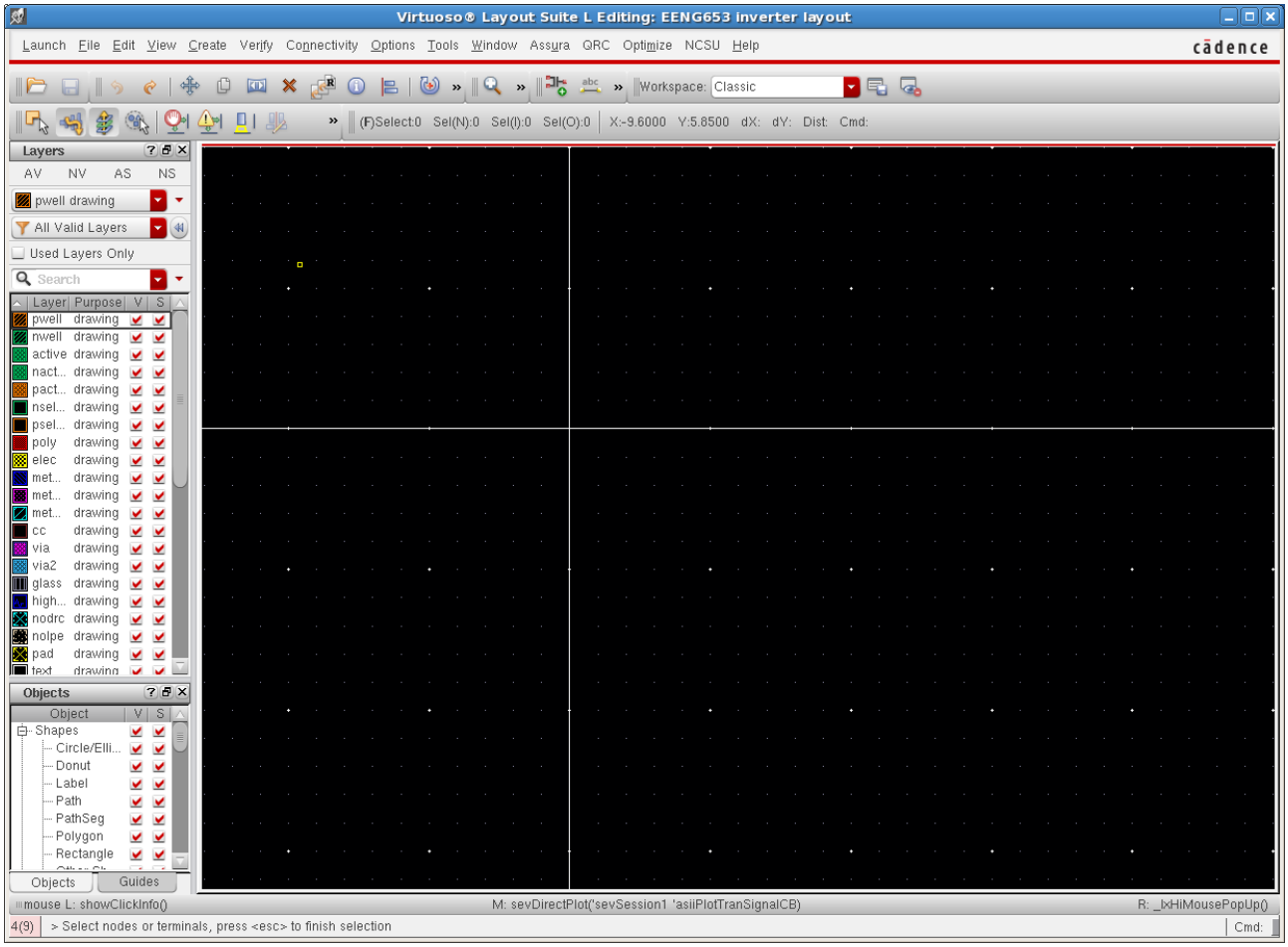
a. In the Library Manager, highlight your library "EENG653" and the Cell "inverter." Then, click on "File → New → Cell View"



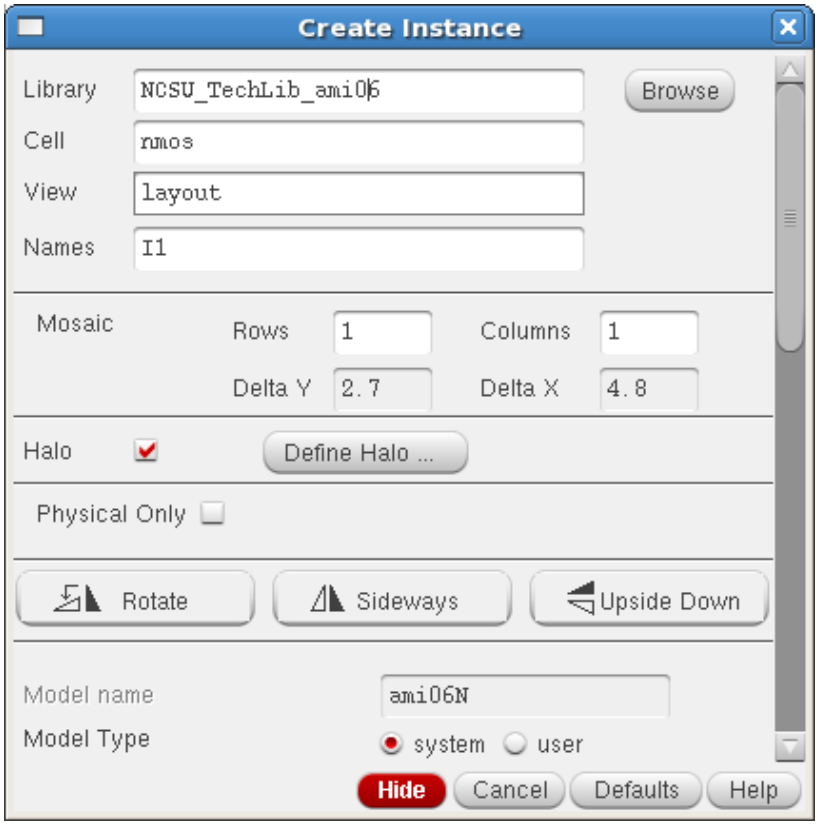
b. The window that appears is shown below. Fill in the field "View" with the word 'layout' and select "Type" as 'layout'. Then click 'OK'.



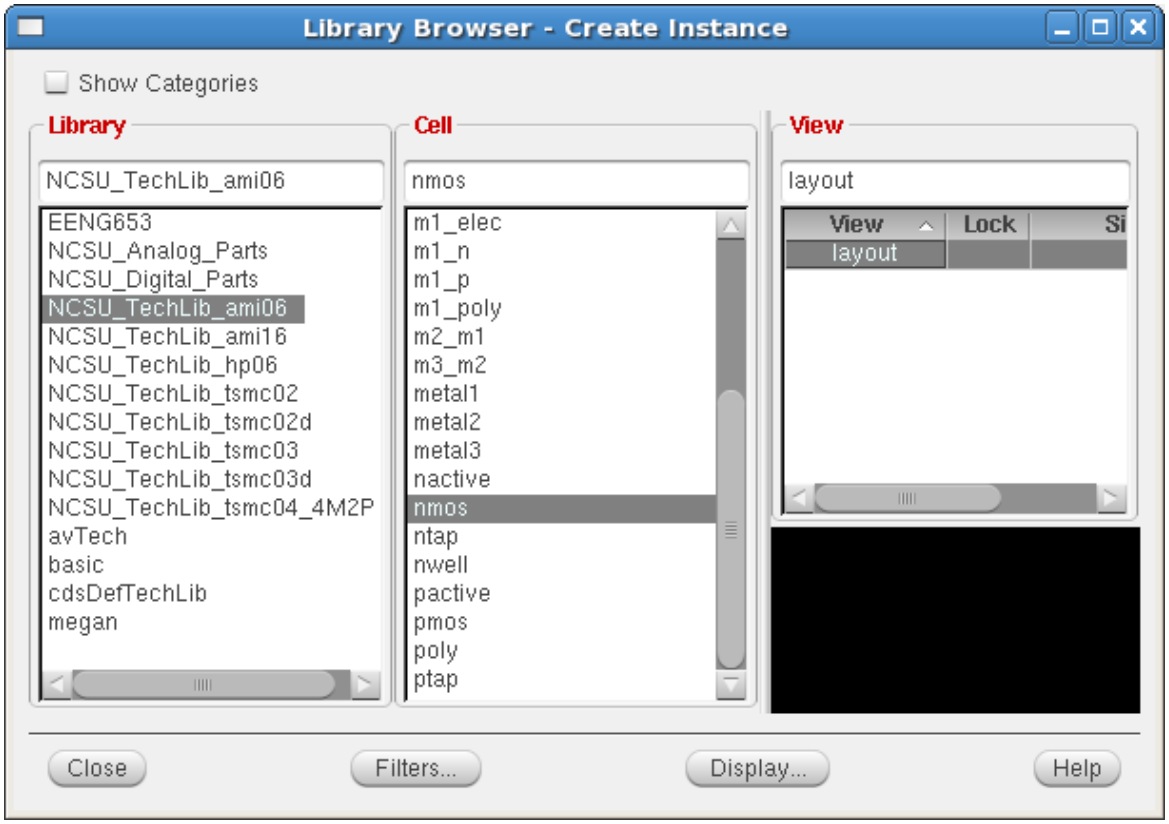
c. An empty layout window will appear in edit mode: "Virtuoso Layout Suite"



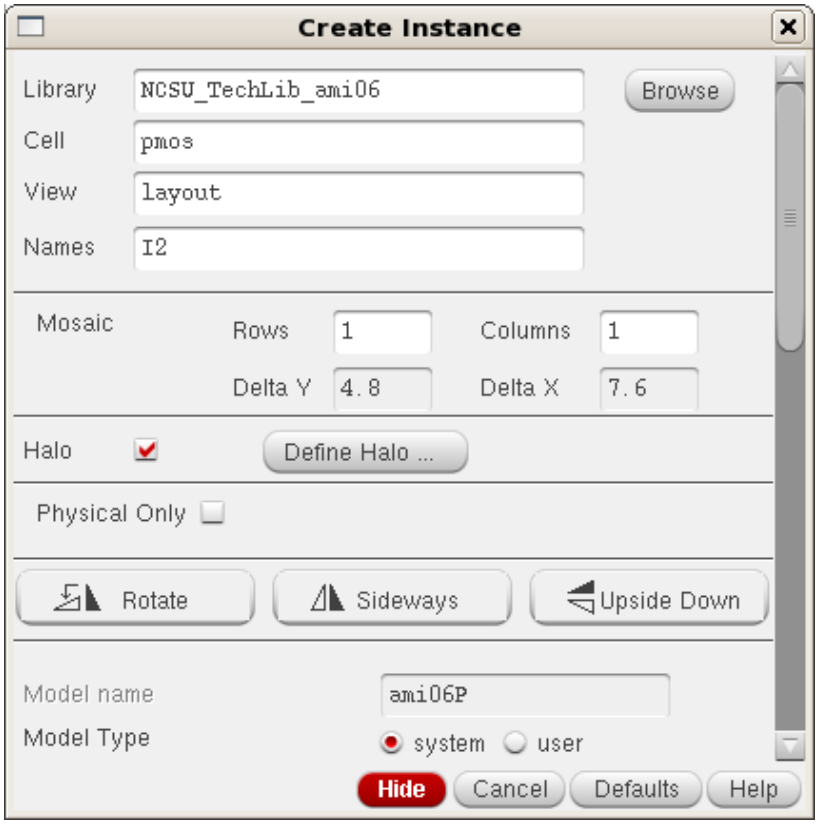
d. Click on the layout window and create an instance of the nmos4 device by typing 'i' in the layout window. Click on the Browse button, and choose "NCSU_TechLib_ami06→nmos→layout" as shown in the Create Instance image below.



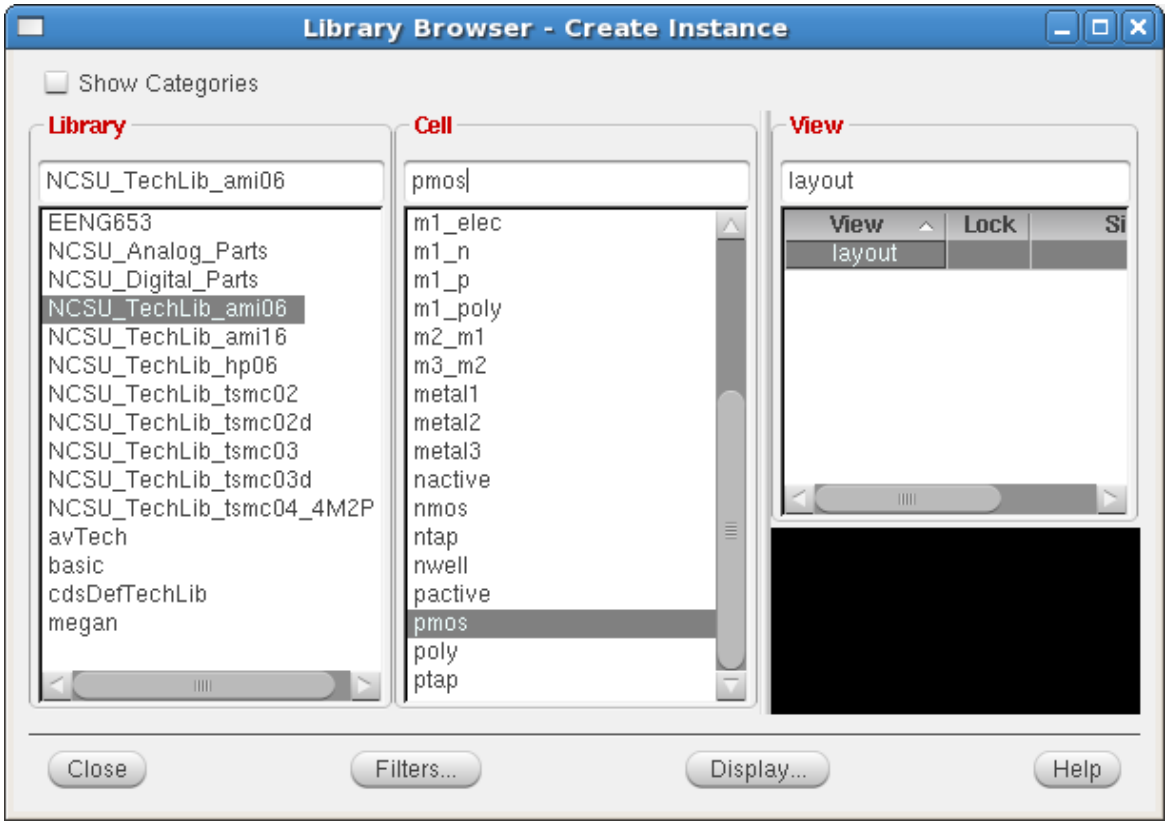
e. Instantiate this layout for the nmos device in your layout.



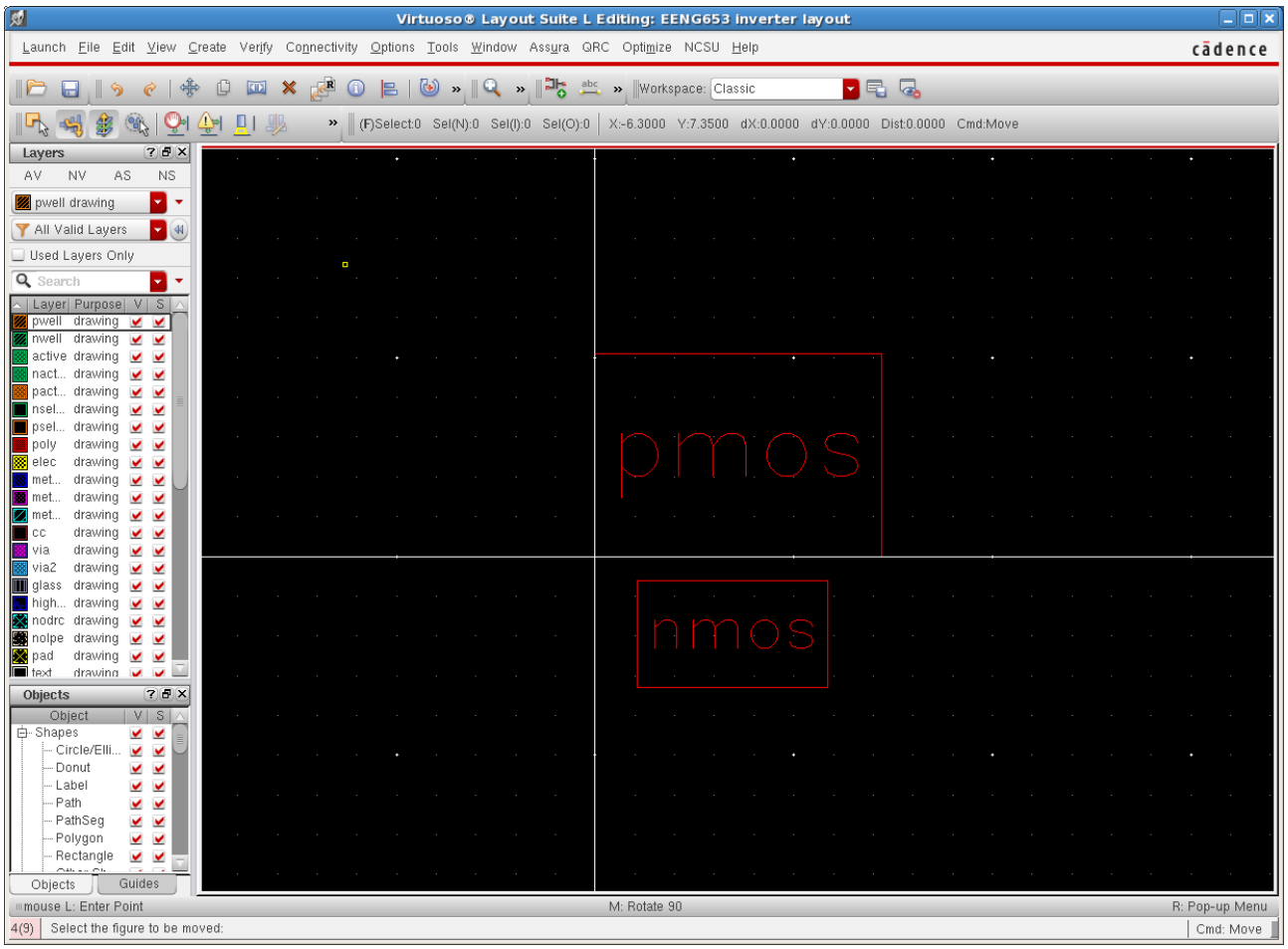
f. Click on the layout window again. Type 'I' in the layout window and fill in the "Create Instance" window.



g. Instantiate the layout of the pmos device in your layout.



h. After instantiating one instance of the nmos layout and one instance of the pmos layout, your layout window "Virtuoso Layout Suite L Editing" will look like the image below.



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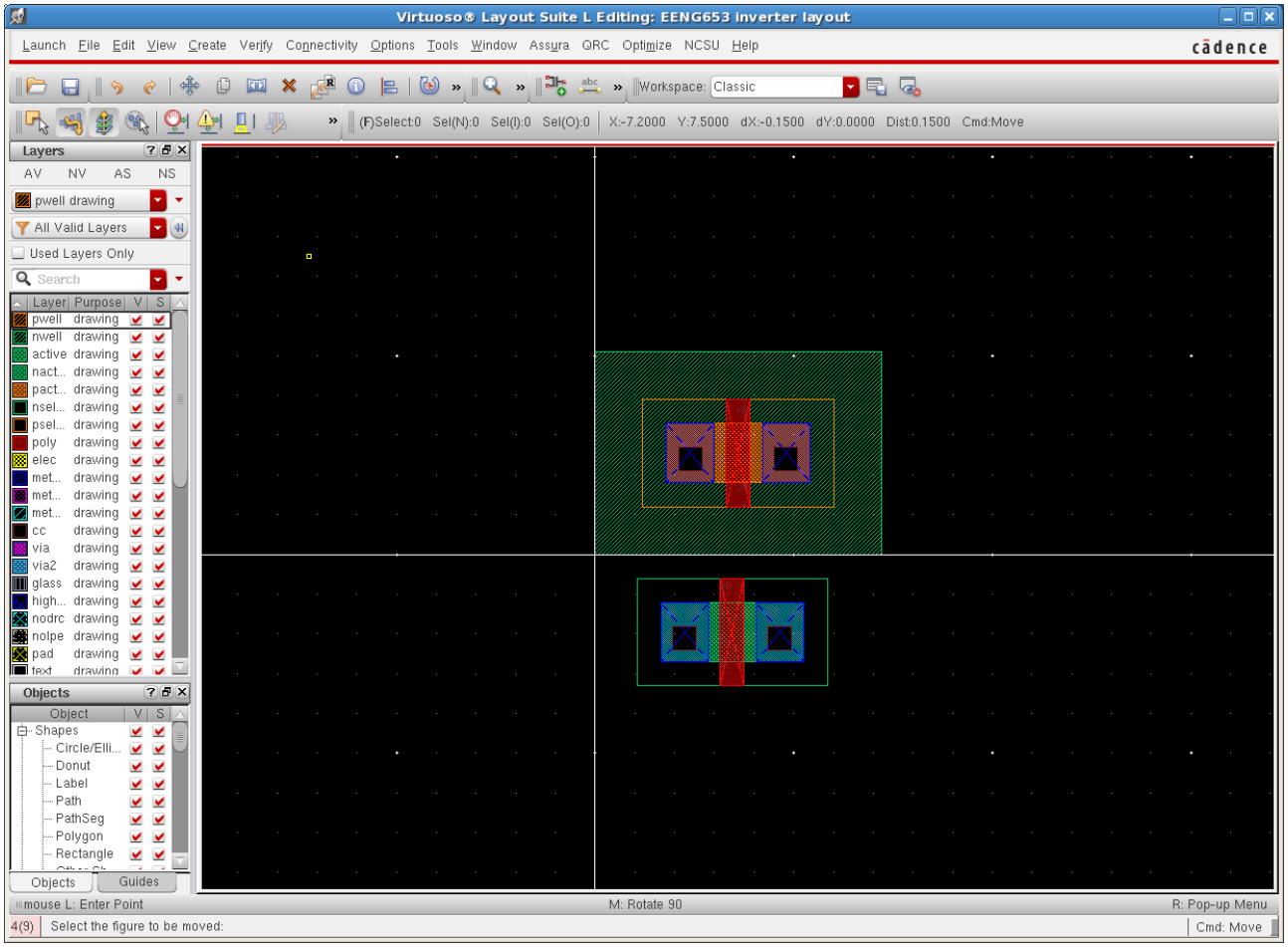
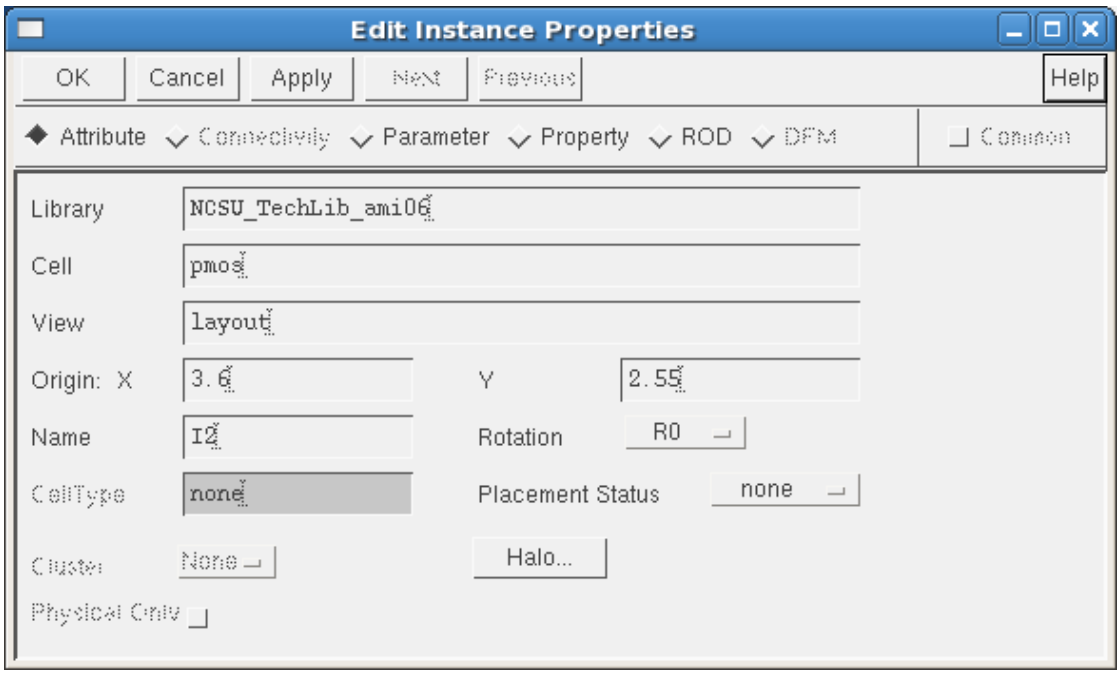
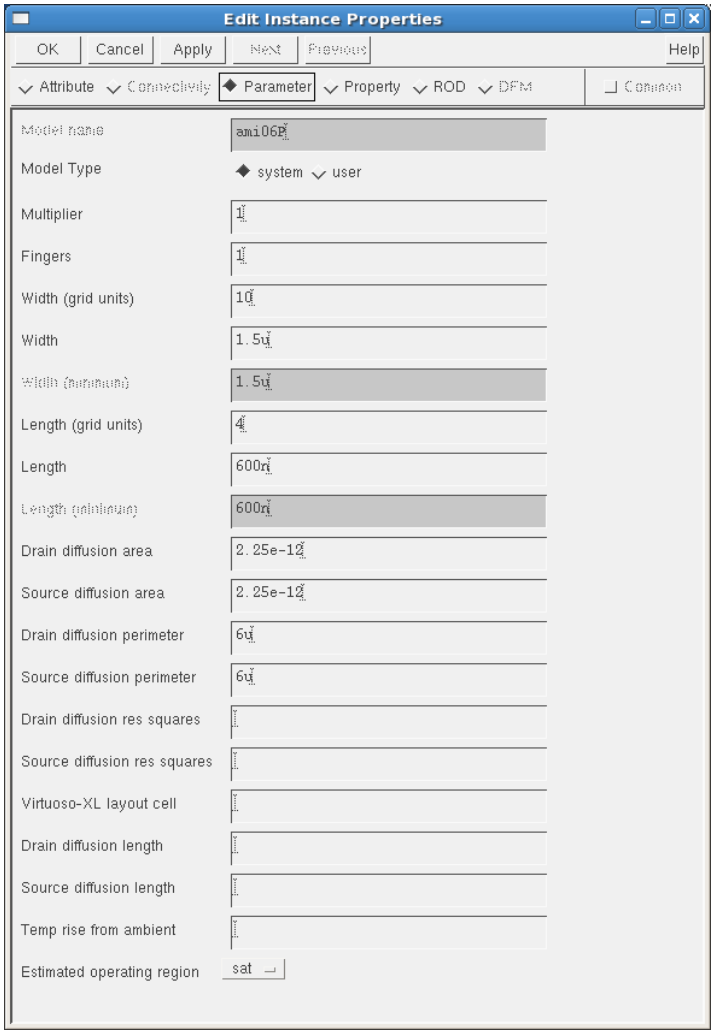
i. Type ‘shift-f’ in the layout window, and the layers for the nmos device and pmos device will be visible as shown in this image.



j. To change the properties of the pmos device, highlight the device in your layout, and then type 'q'. The "Edit Instance Properties" window will appear.



k. In the "Edit Instance Properties" window, click the 'Parameter' radio button. The following window will appear.



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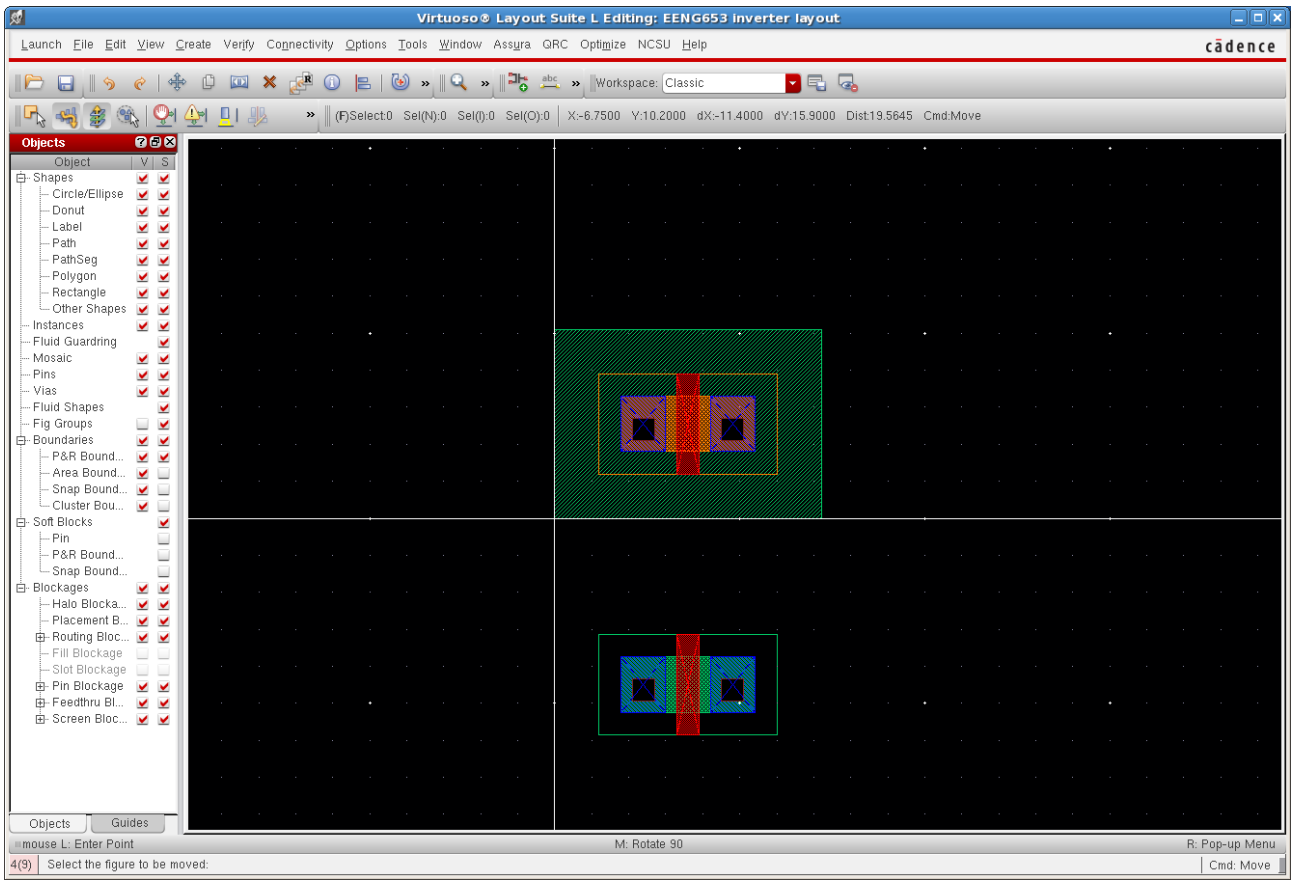
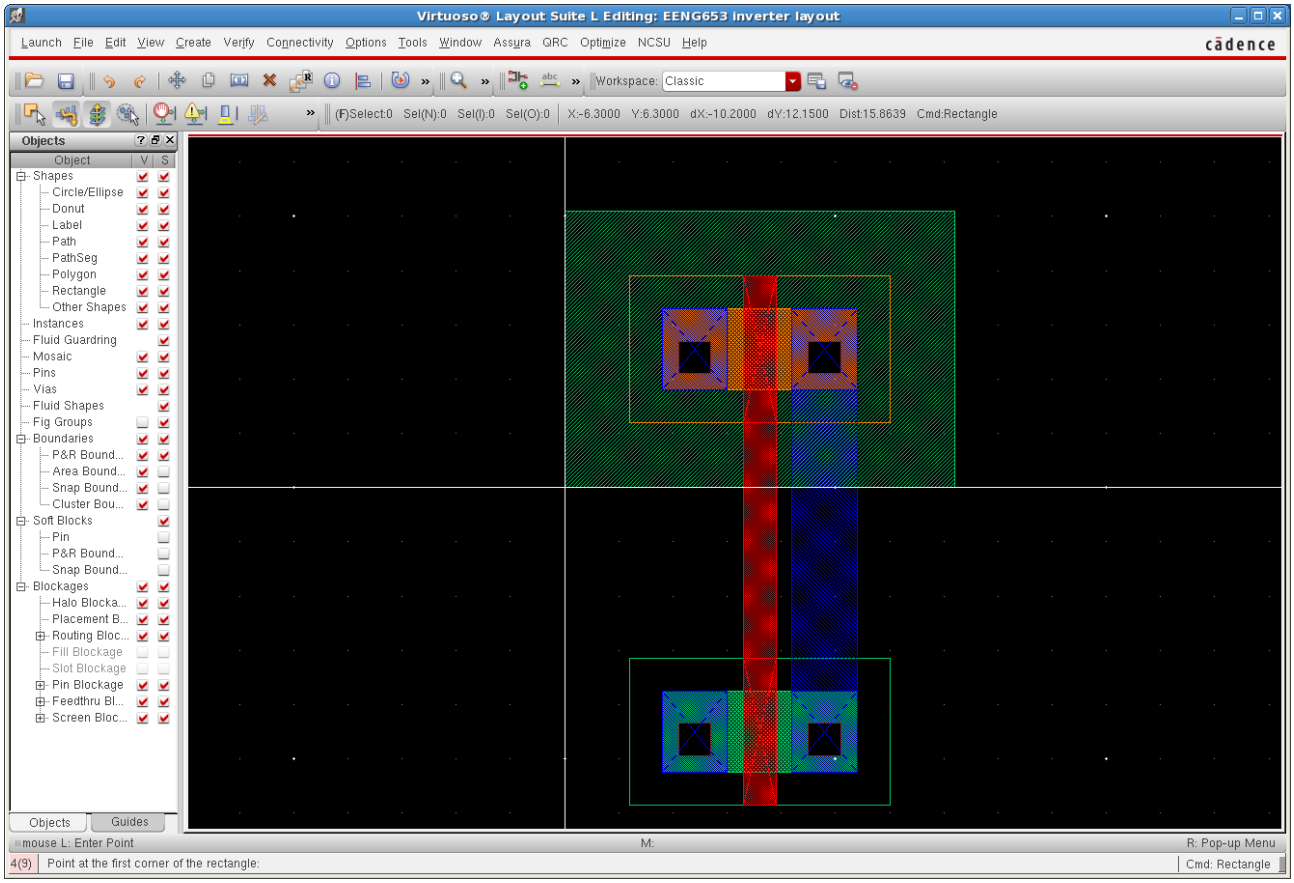
l. The LSW (Layout Selection Window) can be separated from the Virtuoso Layout Suite window which then looks like the image below.



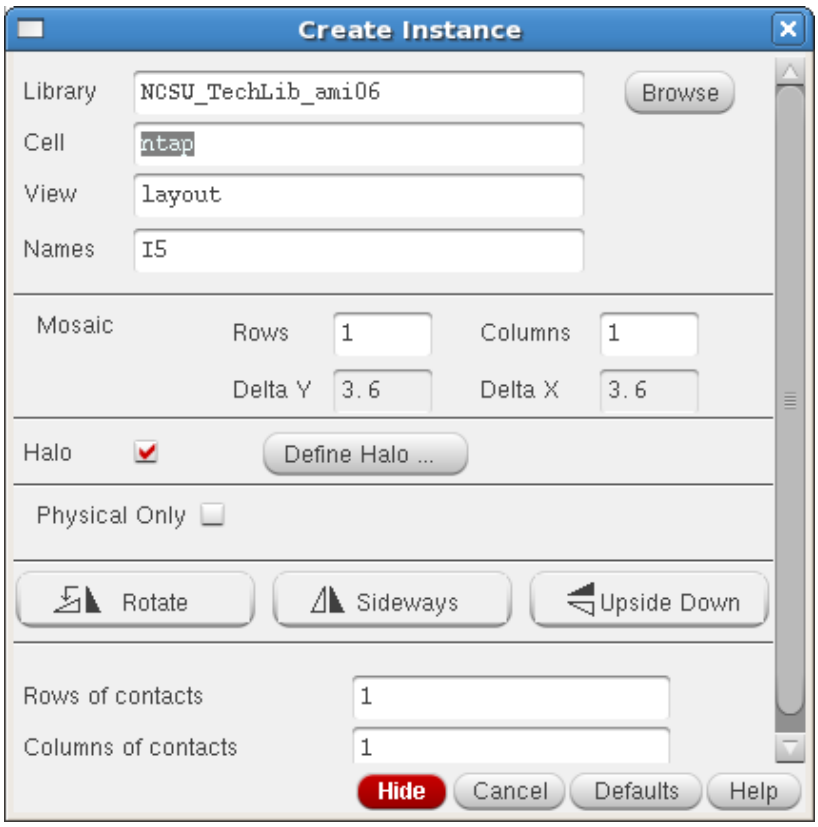
m. The floating LSW lists the metal layers and via layers in this design. For example, metal1 is blue. Polysilicon is pink.

n. Metal1 is highlighted in the LSW in the image below.

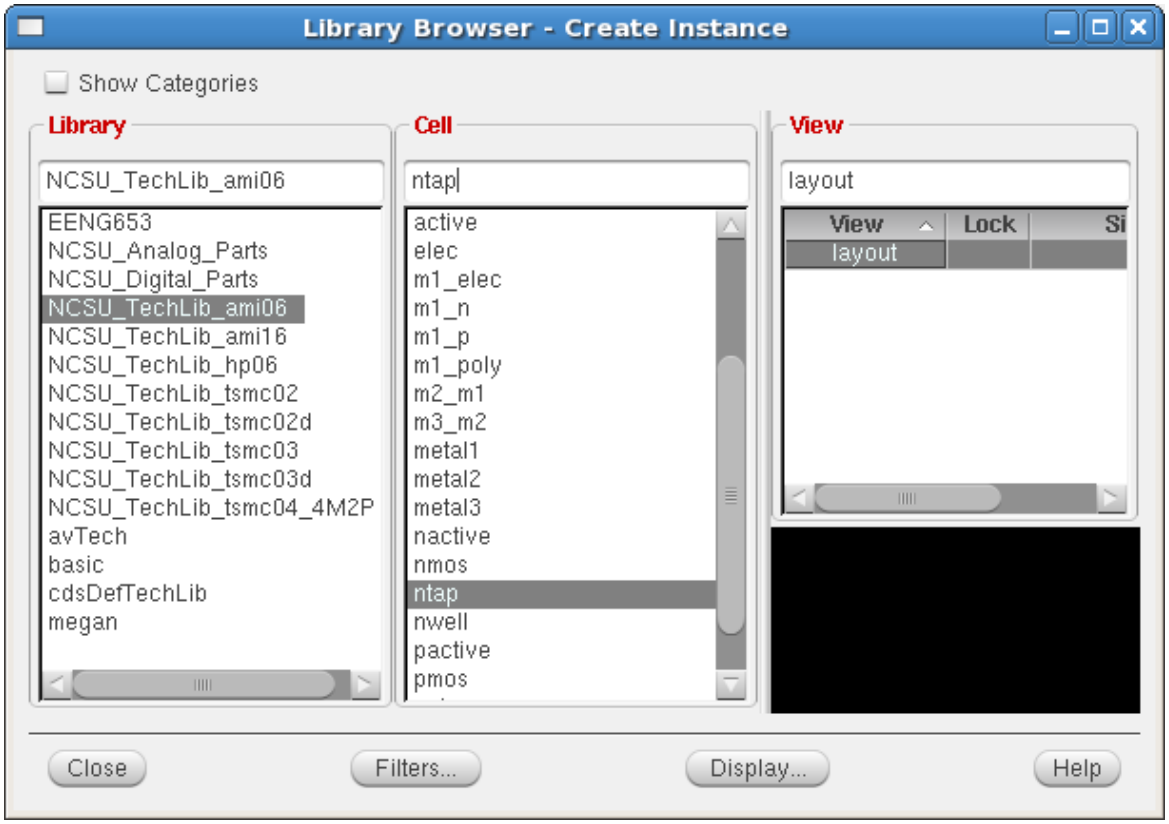
o. Now you will make connections on the metal layers between the nmos layout and pmos layout. Draw a polysilicon rectangle to connect the gate of the nmos device with the gate of the pmos device. Draw a metal1 rectangle to connect the drain/source region of one device with the drain/source region of the second device. Notice that the nmos device layout and the pmos device layout already contain the built-in active contacts between metal1 and polysilicon (the black vias).



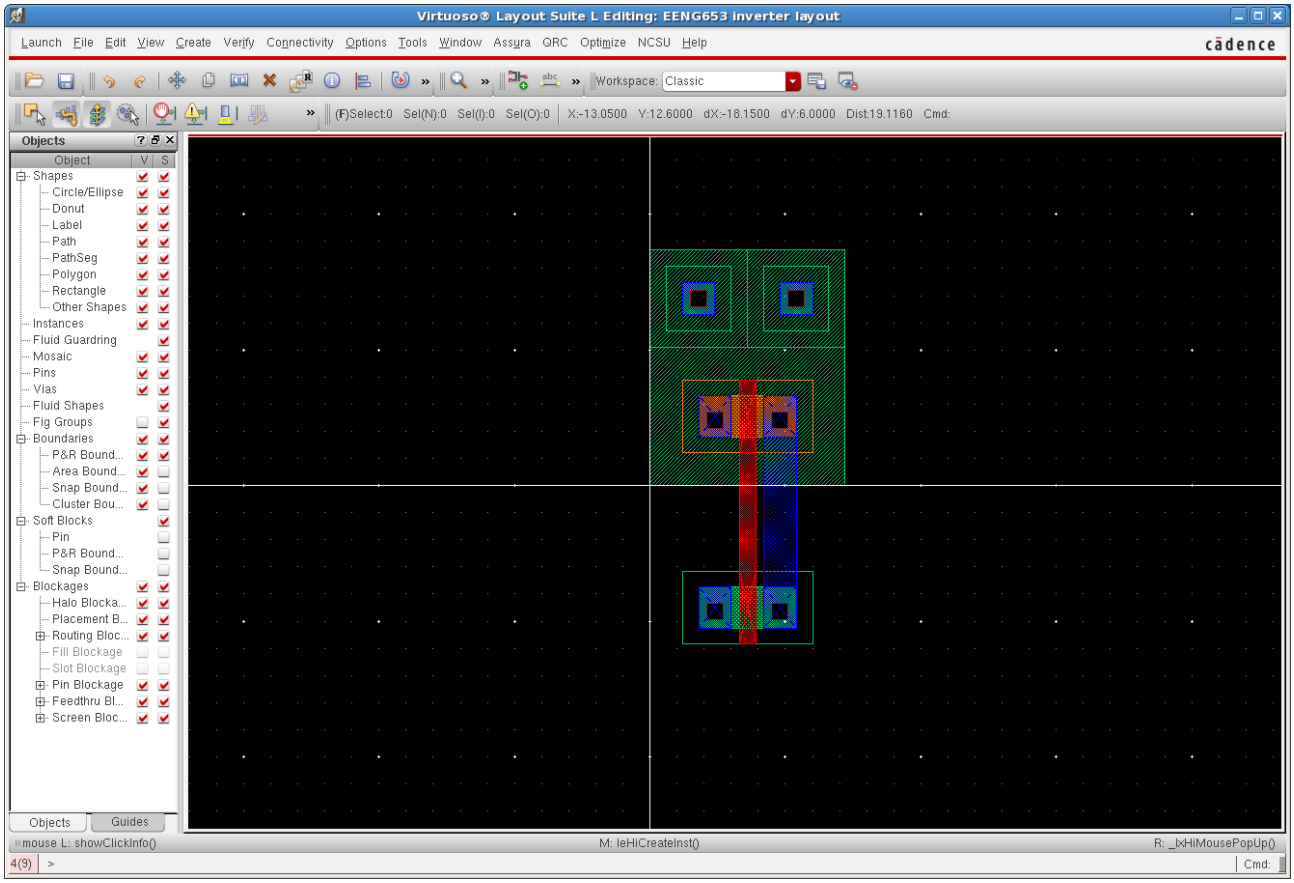
p. Click on your layout window. Type 'i' and fill in the "Create Instance" window as shown below. Instantiate two instances of an 'ntap' in the layout.



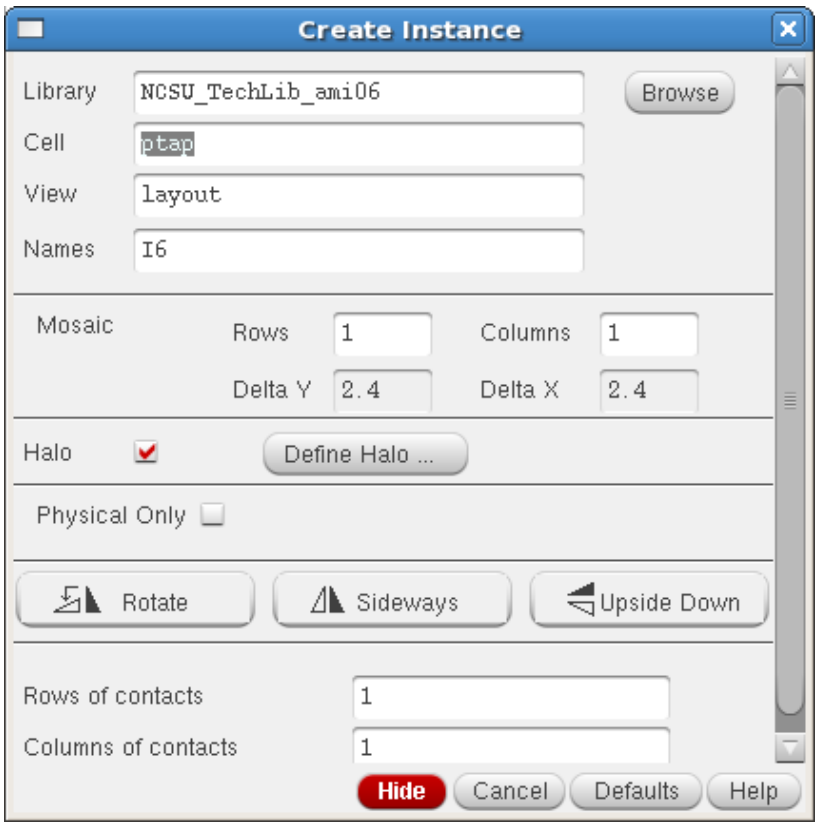
q. Locate the 'ntap' by clicking Browse and choosing "NCSU_TechLib_ami06 → ntap → layout."



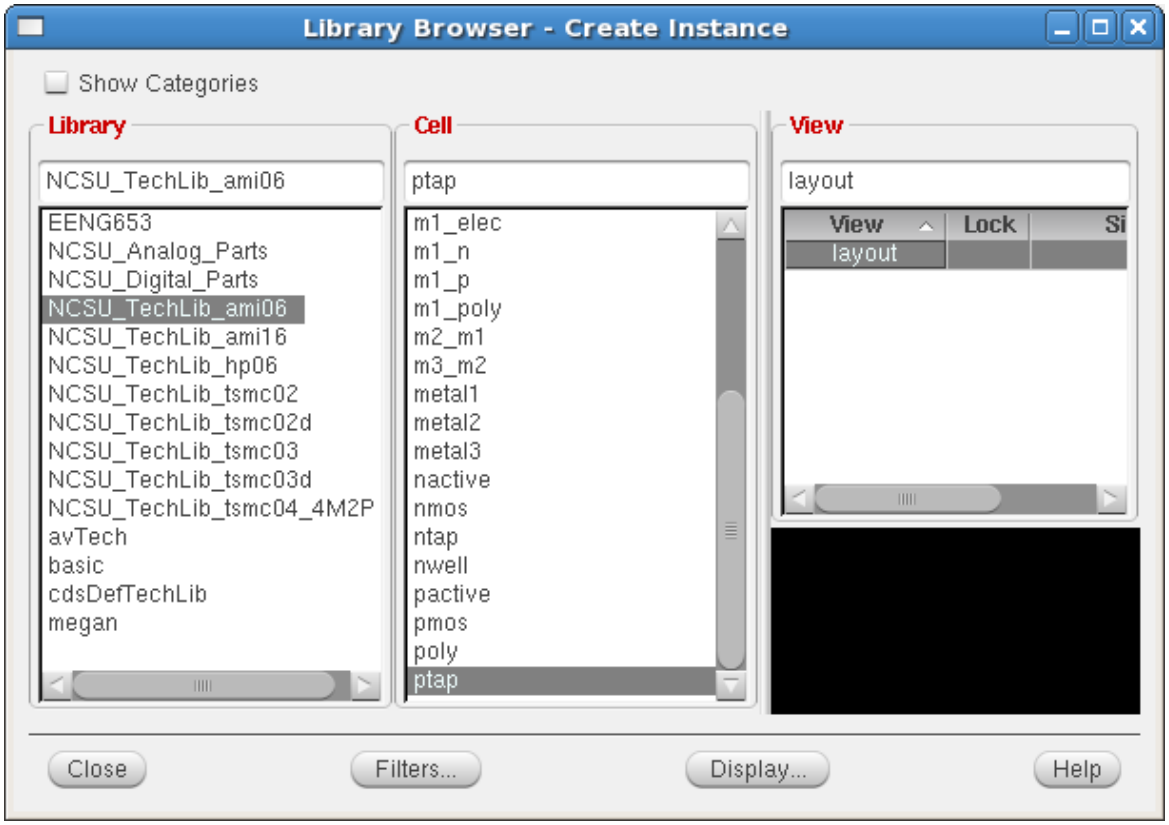
r. The ntaps will be positioned as shown in the image below. The bulk terminal for the pmos device is its nwell. The power supply layer should be overlapped with ntap using metal1 so that the bulk of the transistor is connected.



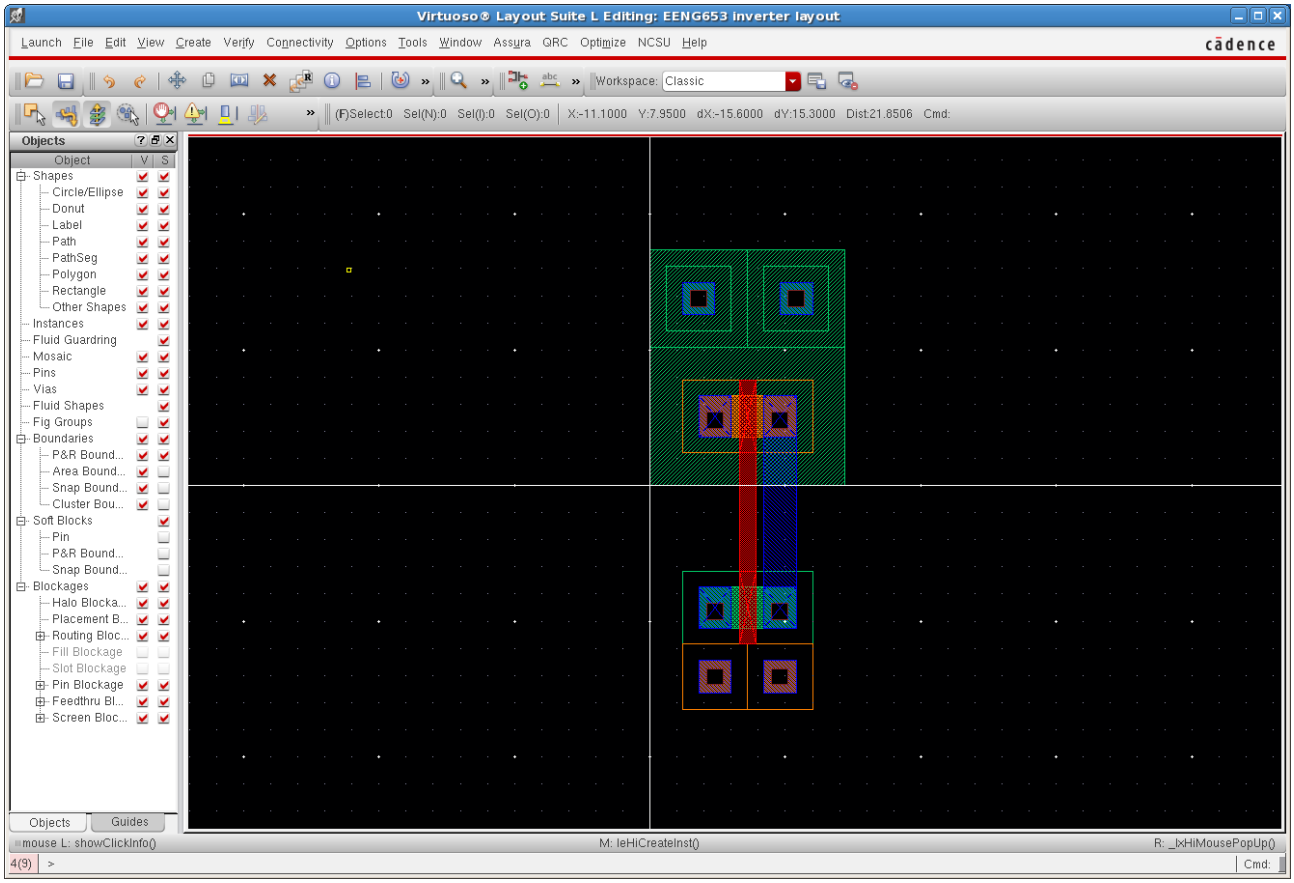
s. Now click on your layout and type 'I'. In the "Create Instance" window, fill in the form with "NCSU_TechLib_ami06 → ptap → layout" as shown in the form below.



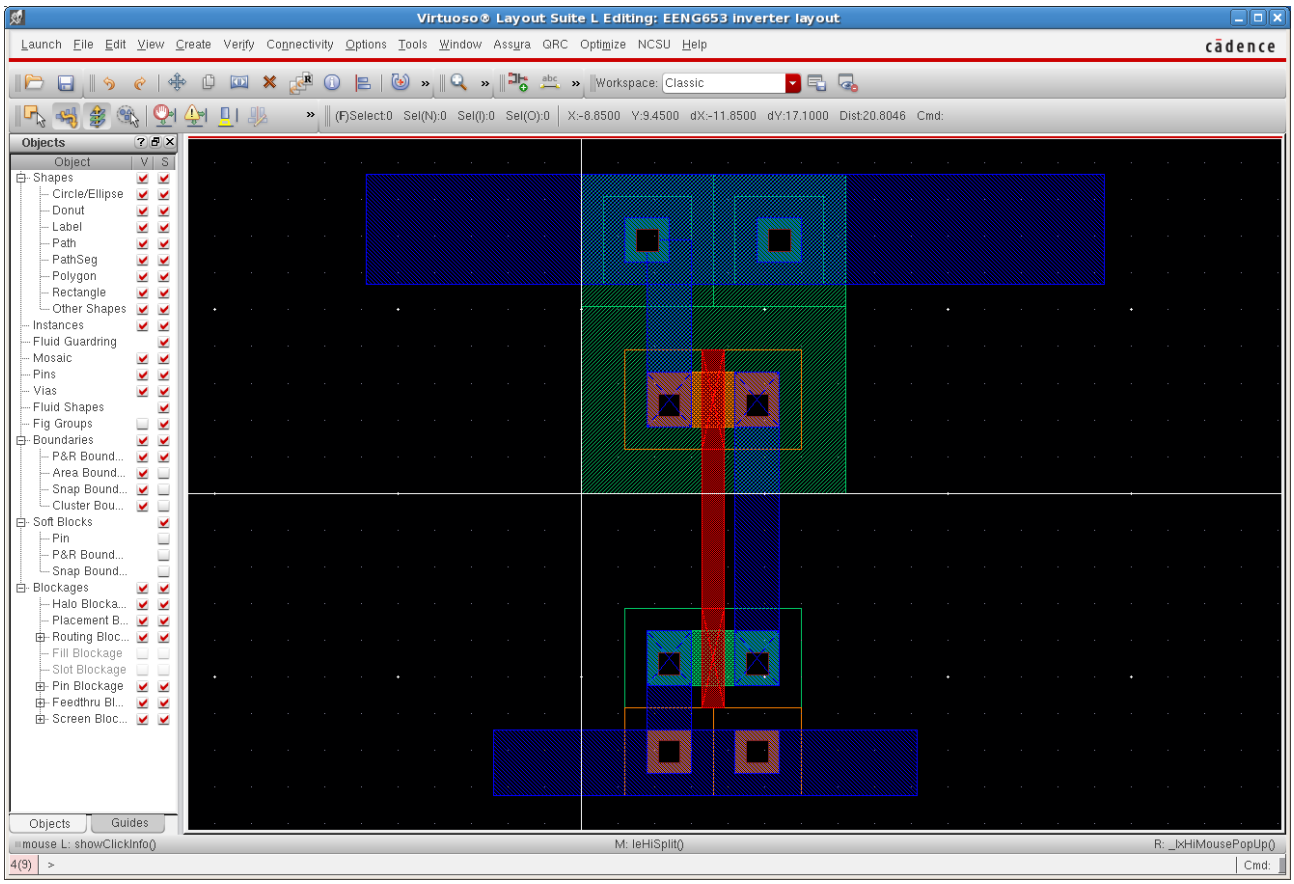
t. The "Create Instance" form will appear as shown in the figure below.



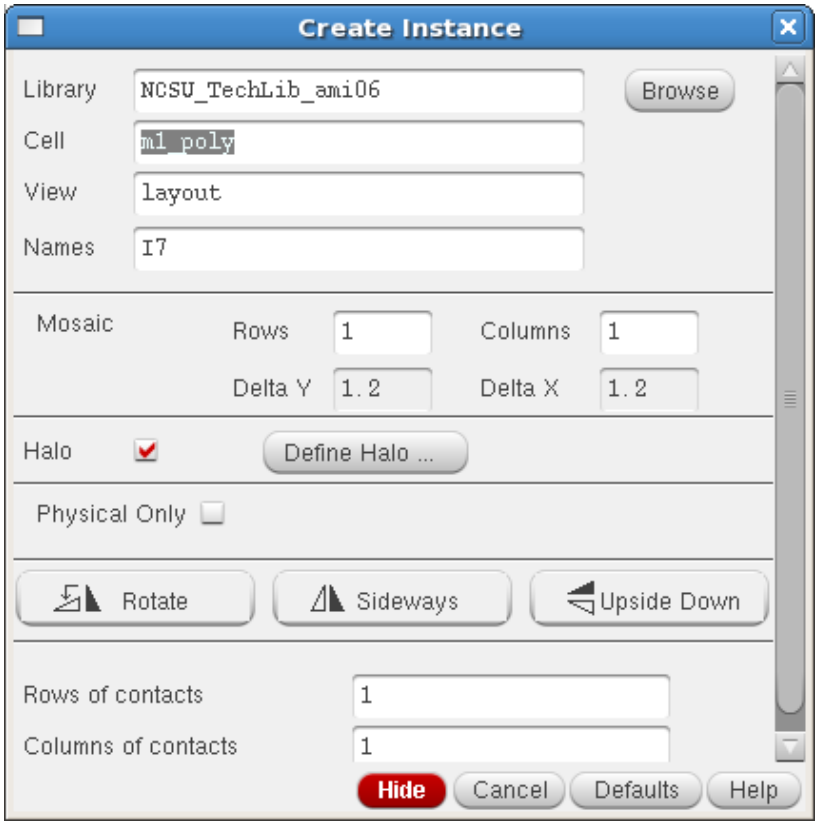
u. Instantiate two instances of 'ptap' as shown in the figure below. The 'ptap' serves as a bulk connection for the nmos device. The power supply layer should be overlapped with ptap using metal 1 so that the bulk of the transistor is connected.



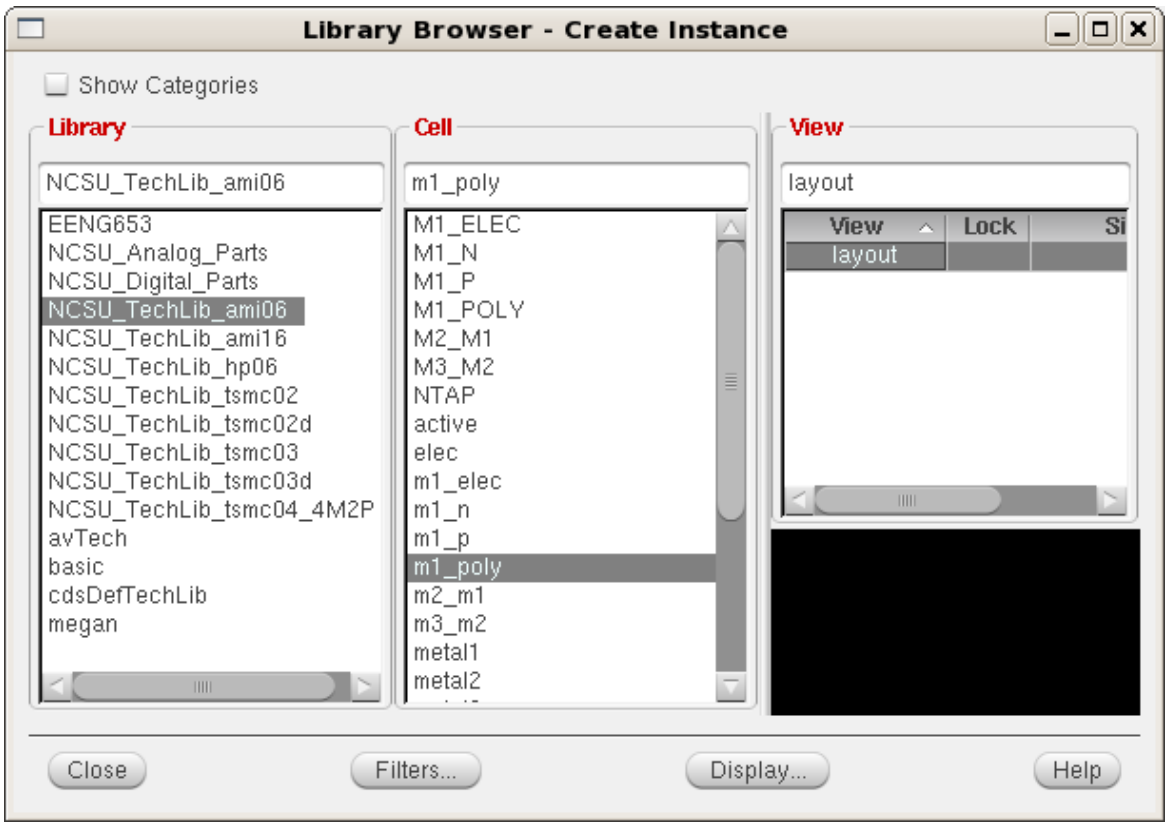
v. Draw metal1 power rails as shown in the figure below. Click on your layout, select metal1 from the LSW, and select "Create → Shape → Rectangle."



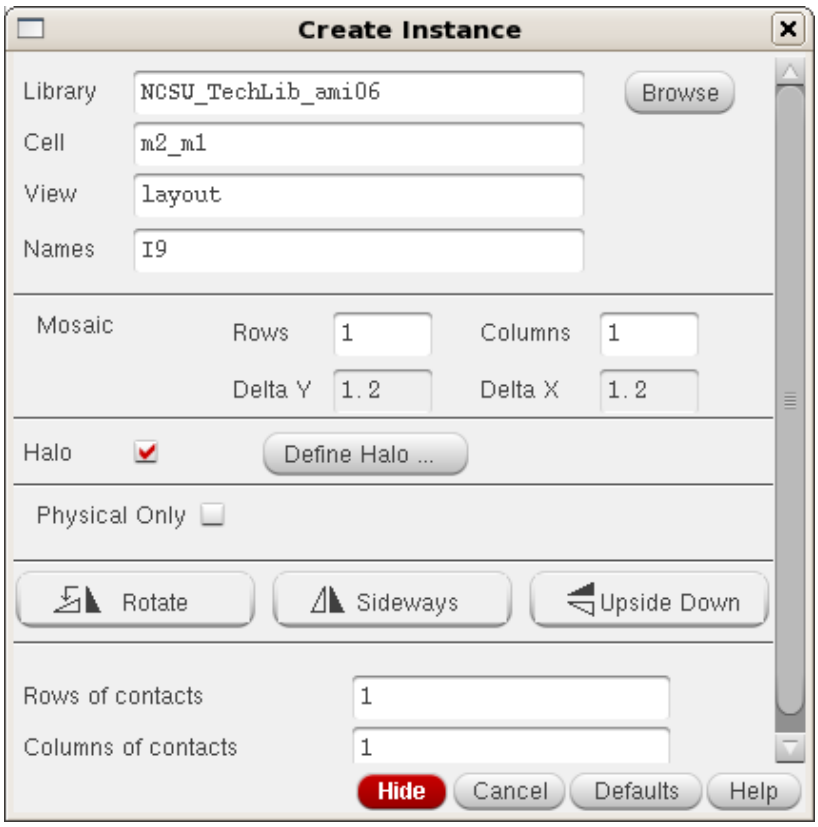
w. Click on your layout and type 'I'. Select a via between metal1 and polysilicon, which is known as a 'm1_poly' instance. Fill out the "Create Instance" window as shown below: "NCSU_TechLib_ami06 → m1_poly → layout."



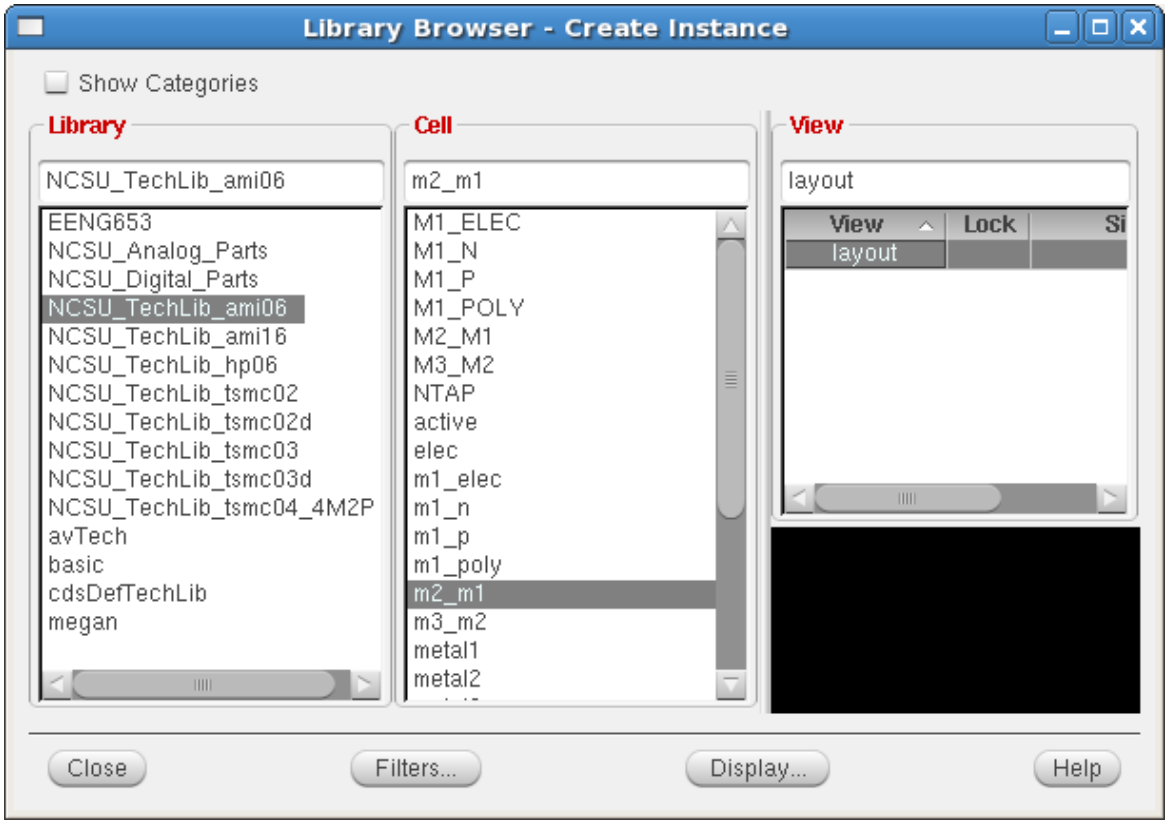
x. Select the "m1_poly" instance as shown in the Library Browser. Instantiate two instances of "m1_poly" vias at the input of your inverter.



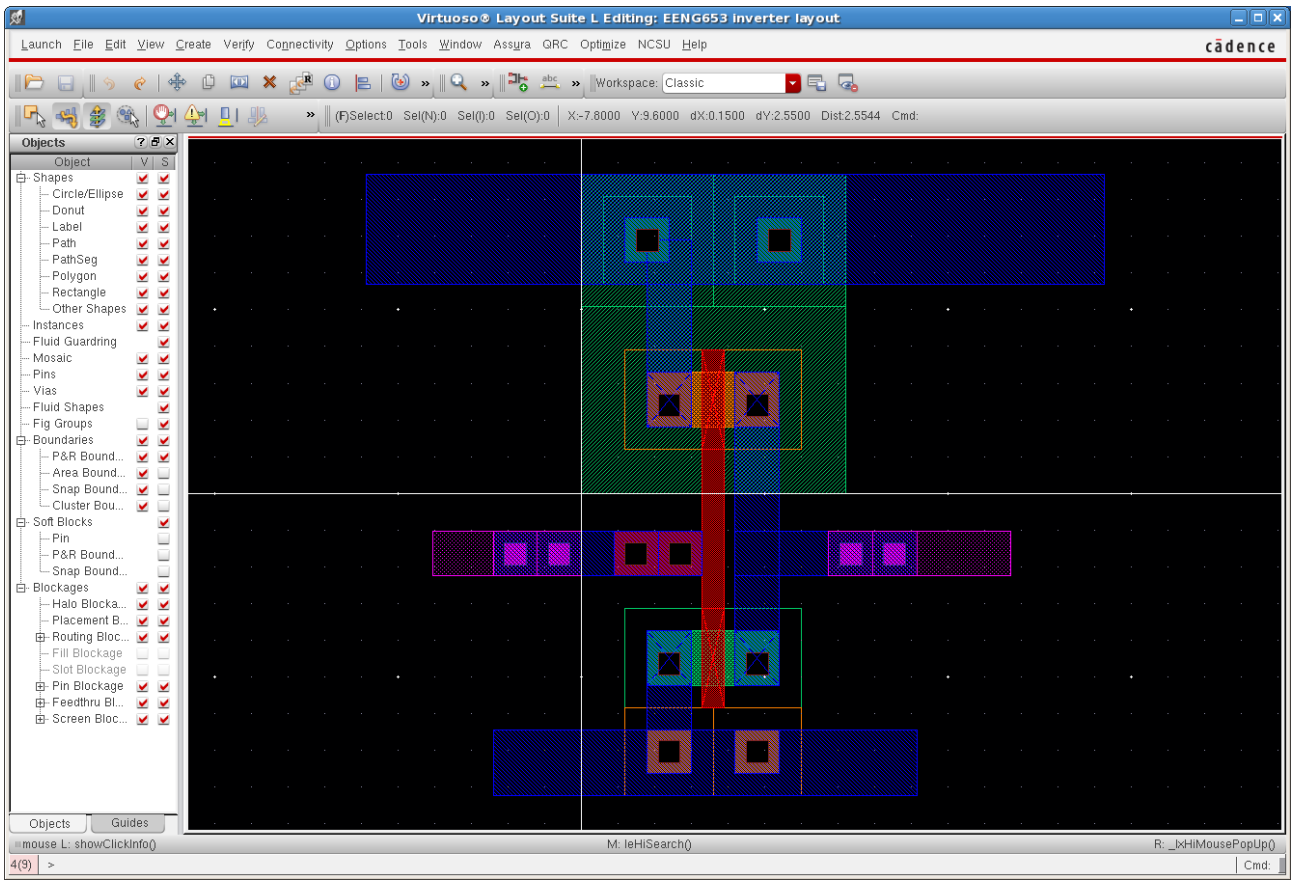
y. Click on your layout and type 'I' in the layout. Create two instances of an "m2_m1" via between metal2 and metal1. Fill in the "Create Instance" window with "NCSU_TechLib_ami06 → m2_m1 → layout."



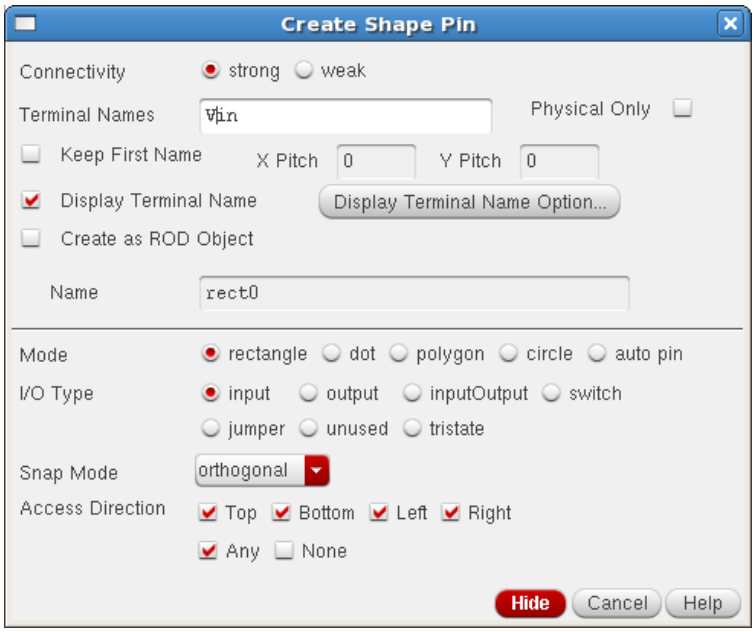
z. The "Library Browser" window for the m2_m1 via will appear as shown in the figure below.



aa. Position two instances of "m2_m1" vias at the input of your inverter and two instances of "m2_m1" vias at the output of your inverter, as shown in the image below. Also add m1 and m2 stripes at the input and output (as shown in the image) to cover the m2_m1 vias.



bb. You will now create pins for "Vin" and "Vout". Click on your inverter layout and select "Create → Pin". Fill in the windows as shown below to create these pins and place "Vin" pin at the input (I/O type is input) and "Vout" pin at the output (I/O type is output). These pins should be on the same metal layer as the metal they are connected to; their purpose, however, is 'pin' (pn) rather than 'drawing' purpose of the metal rectangle. Also create "VDD" and "GND" pins (set I/O type to be inputOutput) on the Create Shape Pin form for these pins. Be sure to check the box next to 'Display Terminal Name' to display the terminal name in the layout.



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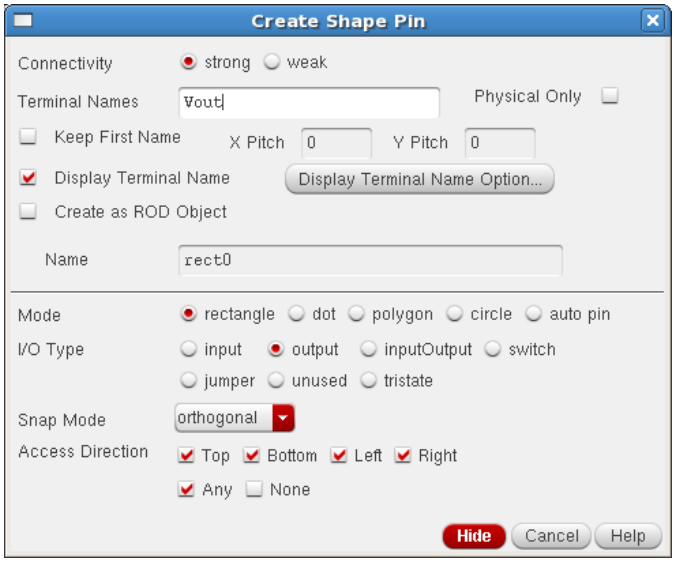
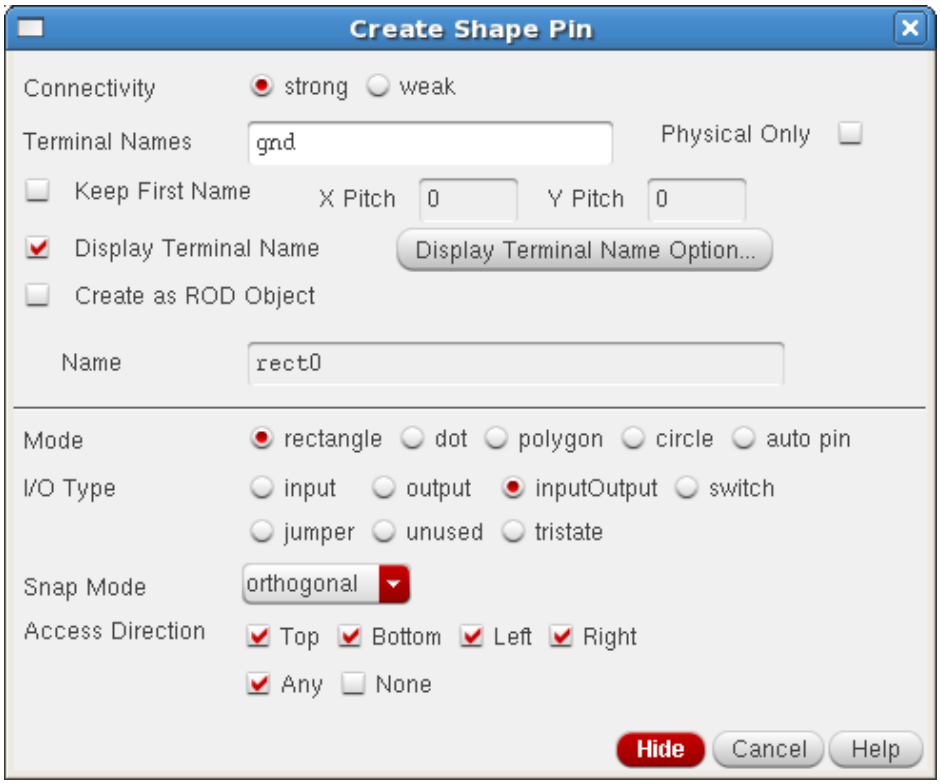
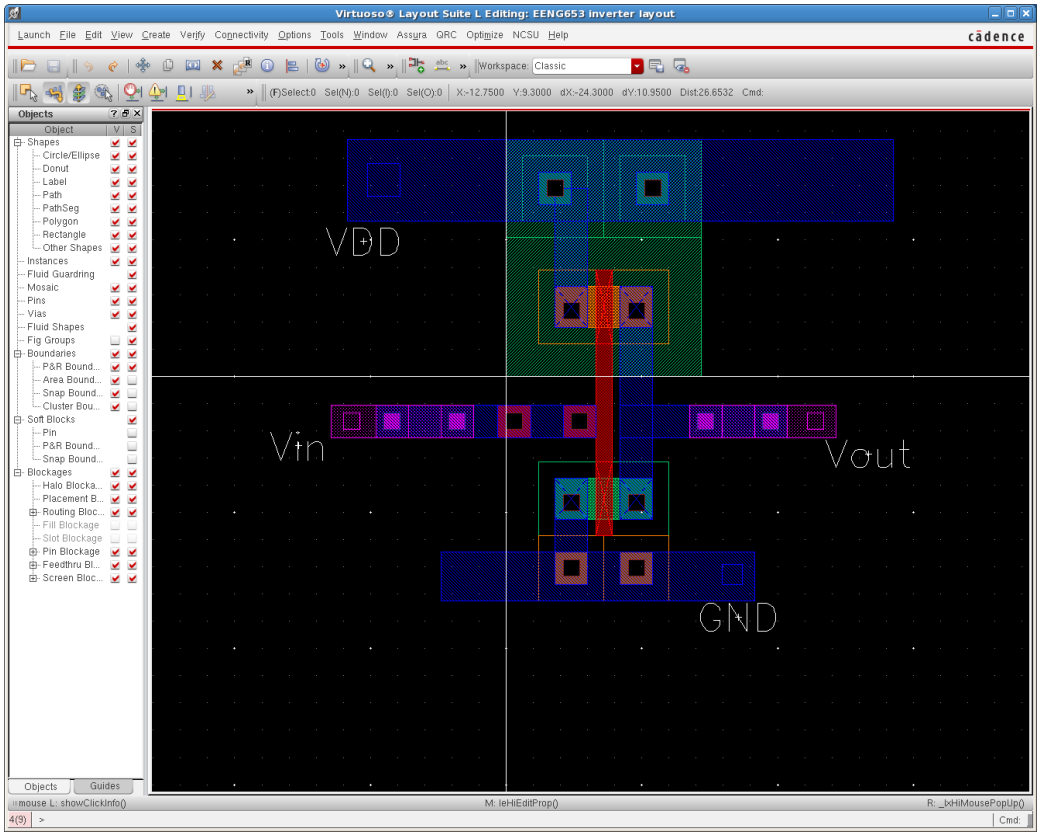




cc. Make sure to label the pins with the same name as in the schematic, namely "VDD," "GND," "Vin," and "Vout." You will need to separate the vias as shown in the layout below (the separation is required in order to pass Design Rule Checks – DRC – as discussed below in the next section).

After creating the "Vin" pin, highlight the pin and type 'Q.' In the 'Edit Rectangle Pin Properties' window, click on the 'Attribute' radio button. Set the 'Pin Name' to 'Vin' and set 'Terminal Name' to 'Vin.'

After creating the "Vout" pin, highlight the pin and type 'Q.' In the 'Edit Rectangle Pin Properties' window, click on the 'Attribute' radio button. Set the 'Pin Name' to 'Vout' and set 'Terminal Name' to 'Vout.'

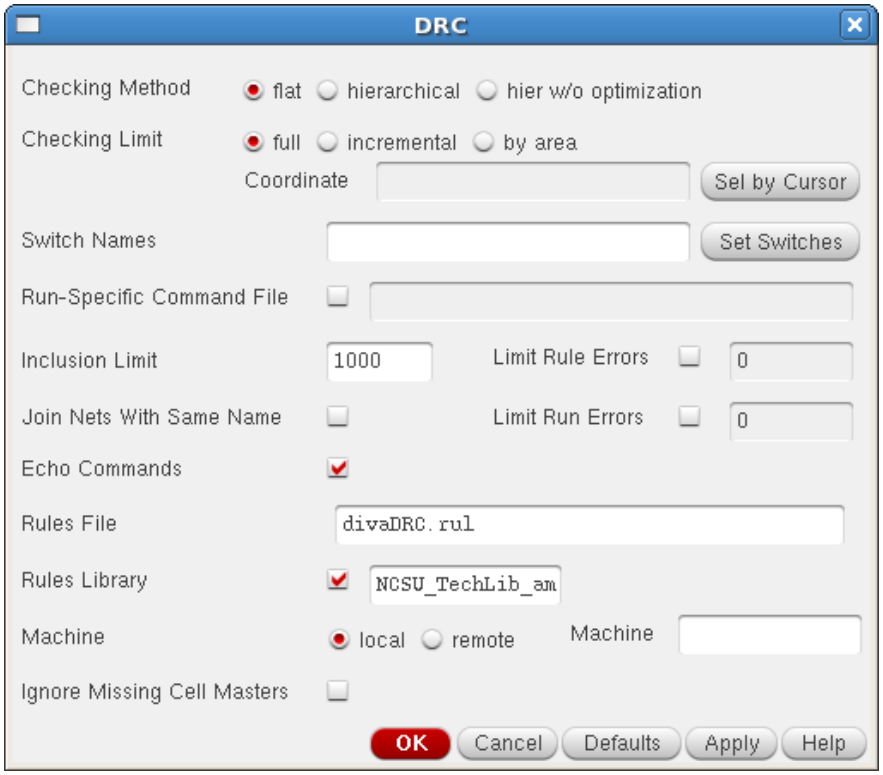


dd. You have now generated a layout for your inverter.

Useful hotkeys for Designing Custom Layouts	
m	Move
Keyboard arrows: up, down, left, right	Move around the layout screen
Ctrl/Shift z	Zoom in/out
F2	Save the design
ESC	Cancel the previous command
Shift f	Reveal all mask layers within each instantiated layout cell (metal layers and via layers)
Cntl f	Hide the mask layers and display the red instance boxes instead
q	Properties
p	Create a path (Paths are convenient for making interconnections between I/O pins of a layout cell; be sure to select the desired metal layer from the LSW first before typing 'p').
r	Create a rectangle
Cntl p	Create a pin
i	Instantiate a cell layout
Hold down shift key and click on each layer	Select more than one mask layer simultaneously. (Use cntl to deselect a particular layer)
u	Undo
c	Copy
d	Delete
s	Stretch
k	Display the ruler (very helpful)
Shift-k	Hide the ruler

16. Inverter: Running Design Rule Check (DRC)

a. Now you will run Design Rule Check (DRC) on your layout. DRC is a software program that inspects your layout for violations of the design rules and inserts markers at locations where any design rule violations are found. To run DRC, click on your layout. From the banner at the top of the layout, select "Verify → DRC." The "DRC" window will appear. Check the boxes as shown, making sure to check the Rules Library checkbox and setting the field to "NCSU_TechLib_ami06" as shown in the two windows below (note that the name of the TechFile is long).



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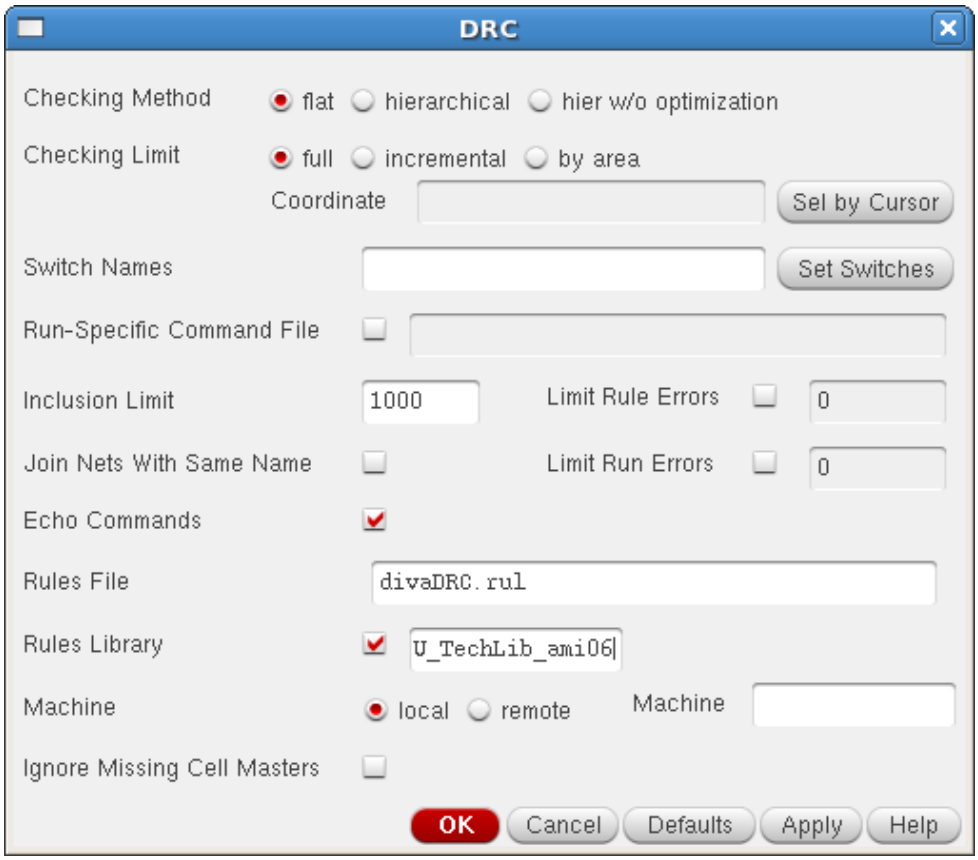
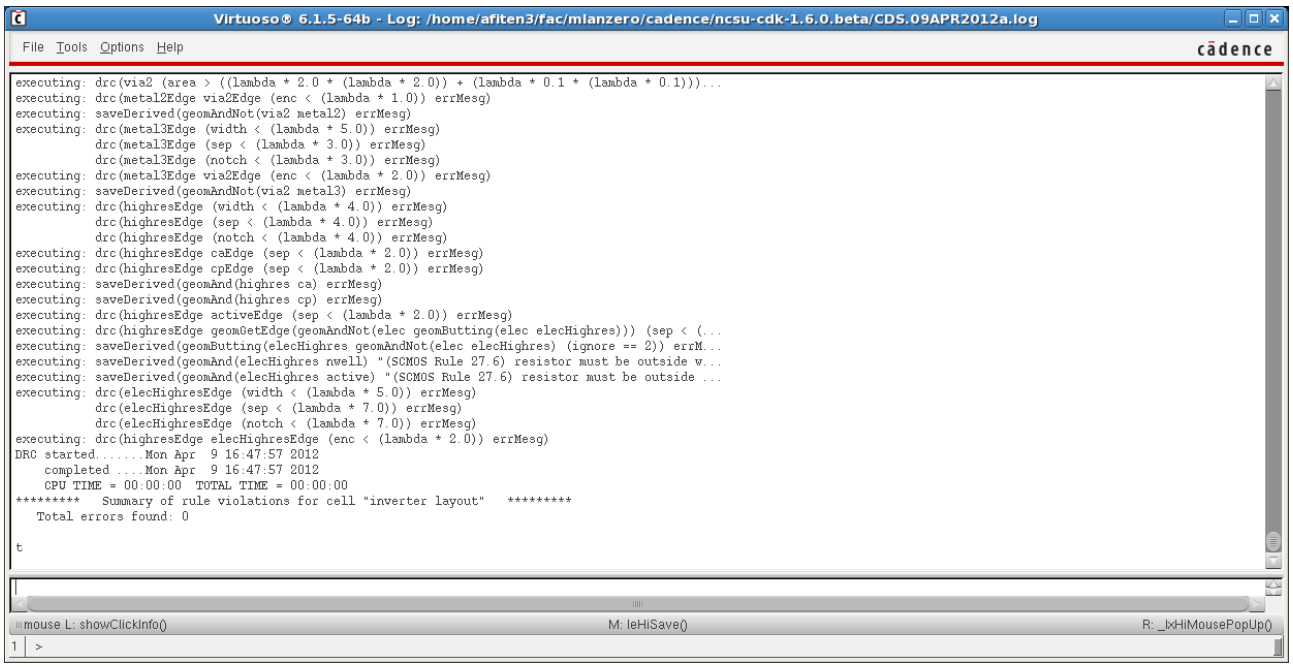


b. Click "OK" in the DRC window. "DRC" will run, and if it completes successfully, the log file in the CIW will report "Total errors found: 0" as shown in the window below.



c. If there are errors in the layout as identified by "DRC," the errors will be identified with white markers in the layout. To see these errors, click on the layout window. Then, click on "Verify → Markers → Find" to look at the errors.

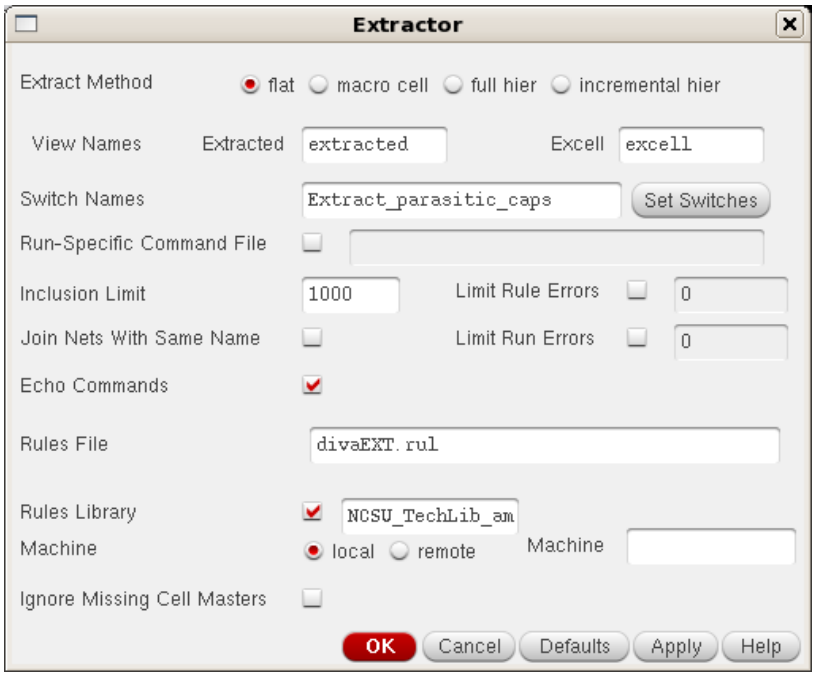
d. Correct the errors and re-run "DRC." Proceed to the next step, Extraction, only after "DRC" passes with no errors.

e. You have now completed Design Rule Check.

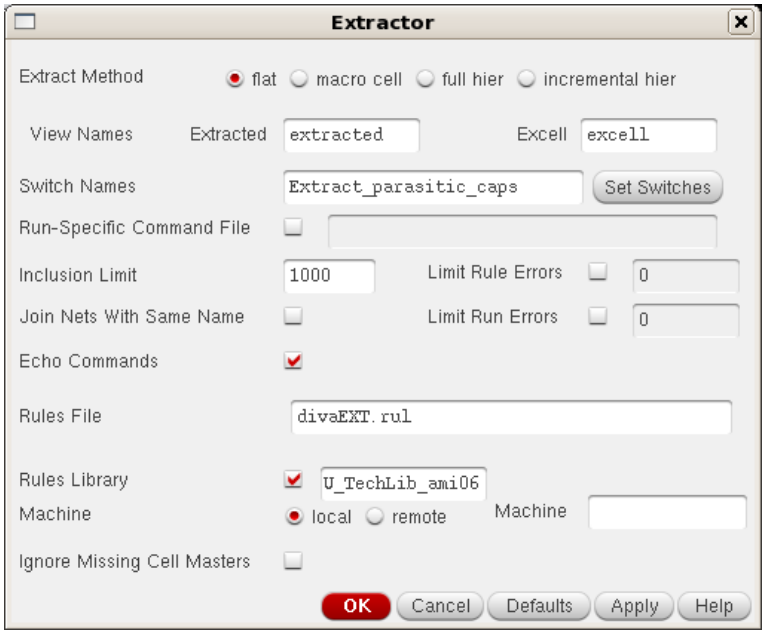
17. Inverter: Running Extraction

a. In this step, you will run extraction to extract circuit models from your layout. Click on your layout. Then select "Verify → Extract" from the banner. The "Extractor" window will appear as shown below in the two images. Note that the Rules library field should be set to "NCSU_TechLib_ami06." (note that the 'Rules Library' window in each image is slightly different because the name is too long for the field width).

In the 'Extractor' form, click on 'Set Switches,' and a window titled 'Set Switches' will appear as shown in the third image below (next page). In the 'Set Switches' window, select 'Extract_parasitic_caps' which will highlight this text as shown in the image. Click 'OK' in the 'Set Switches' window.

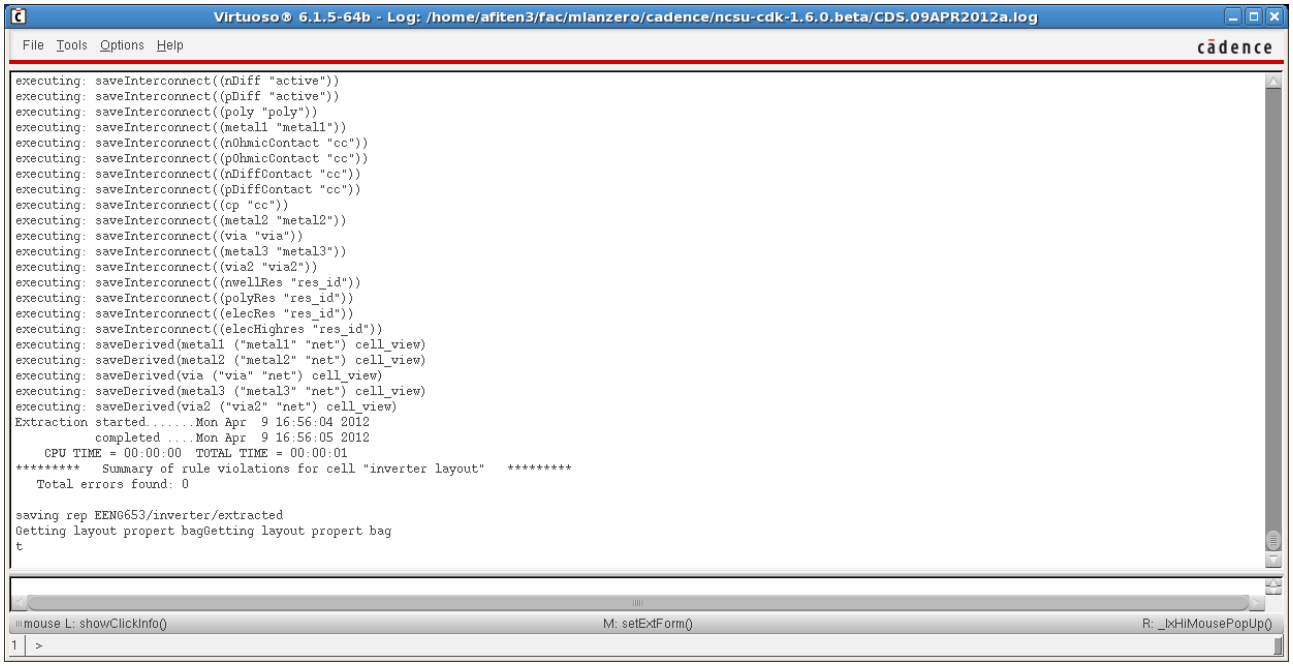


Integrated Circuit Design CAD Tool Information

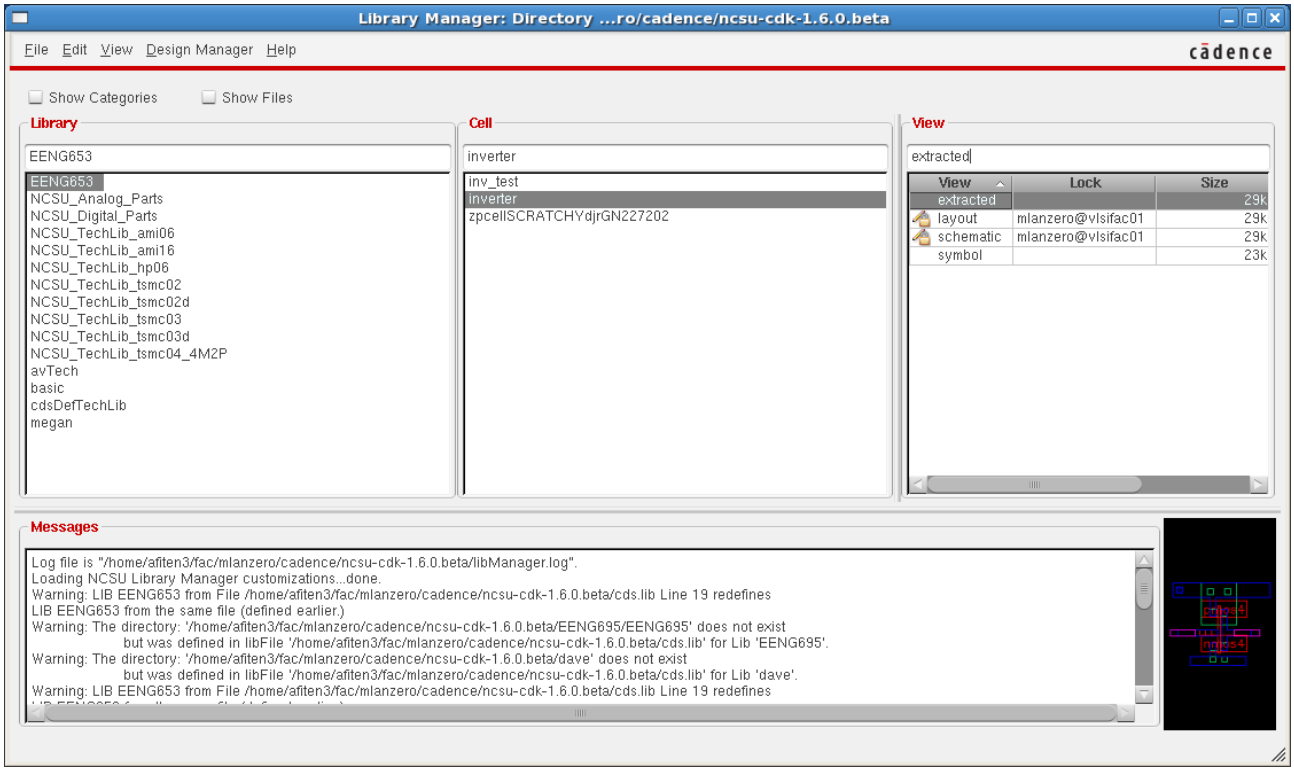


b. Click "OK" on the Extractor form.

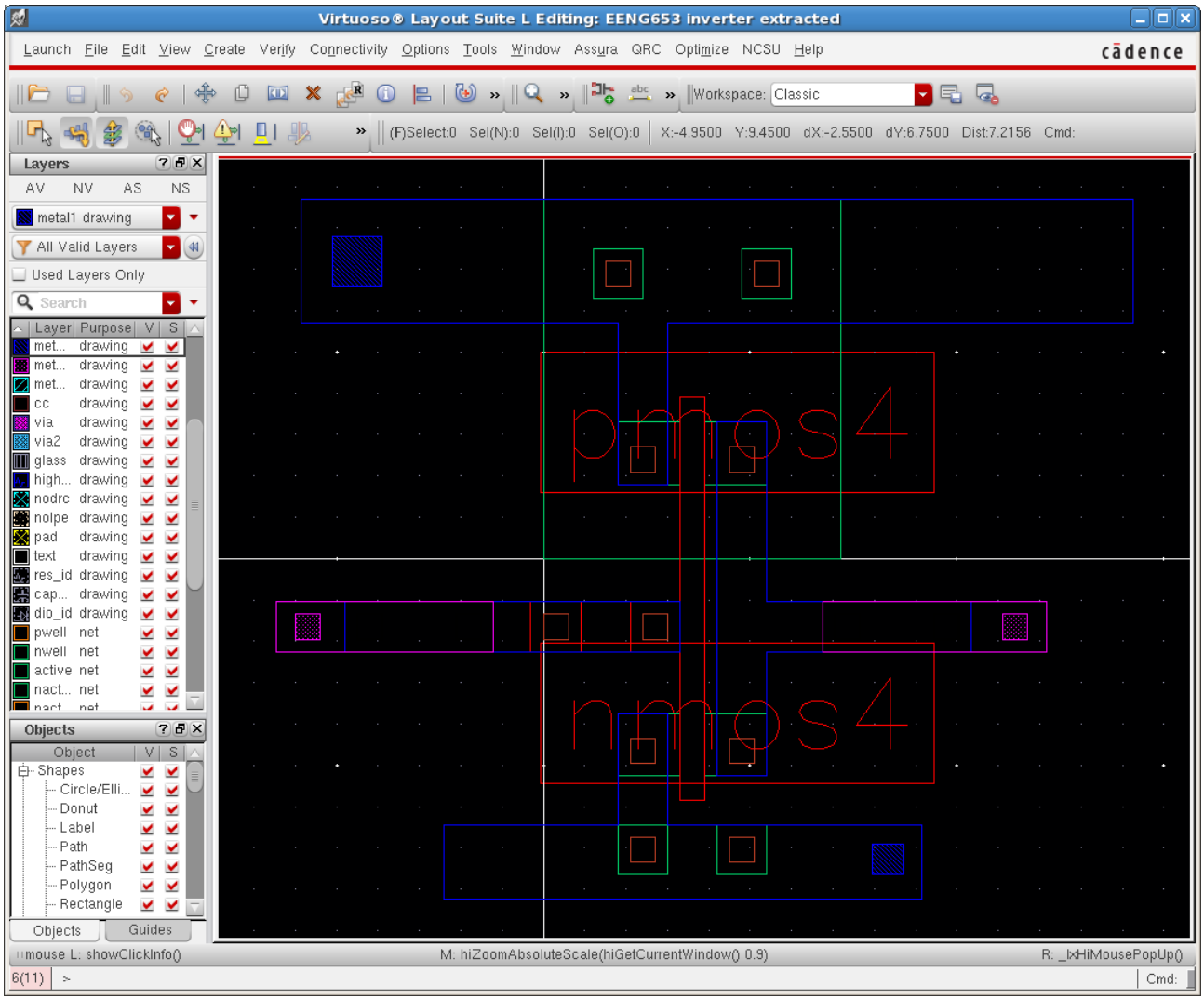
c. After Extraction runs, the log file in the CIW will report any errors. If there are no errors, the log file will report that "Total errors found: 0" as shown in the image below.



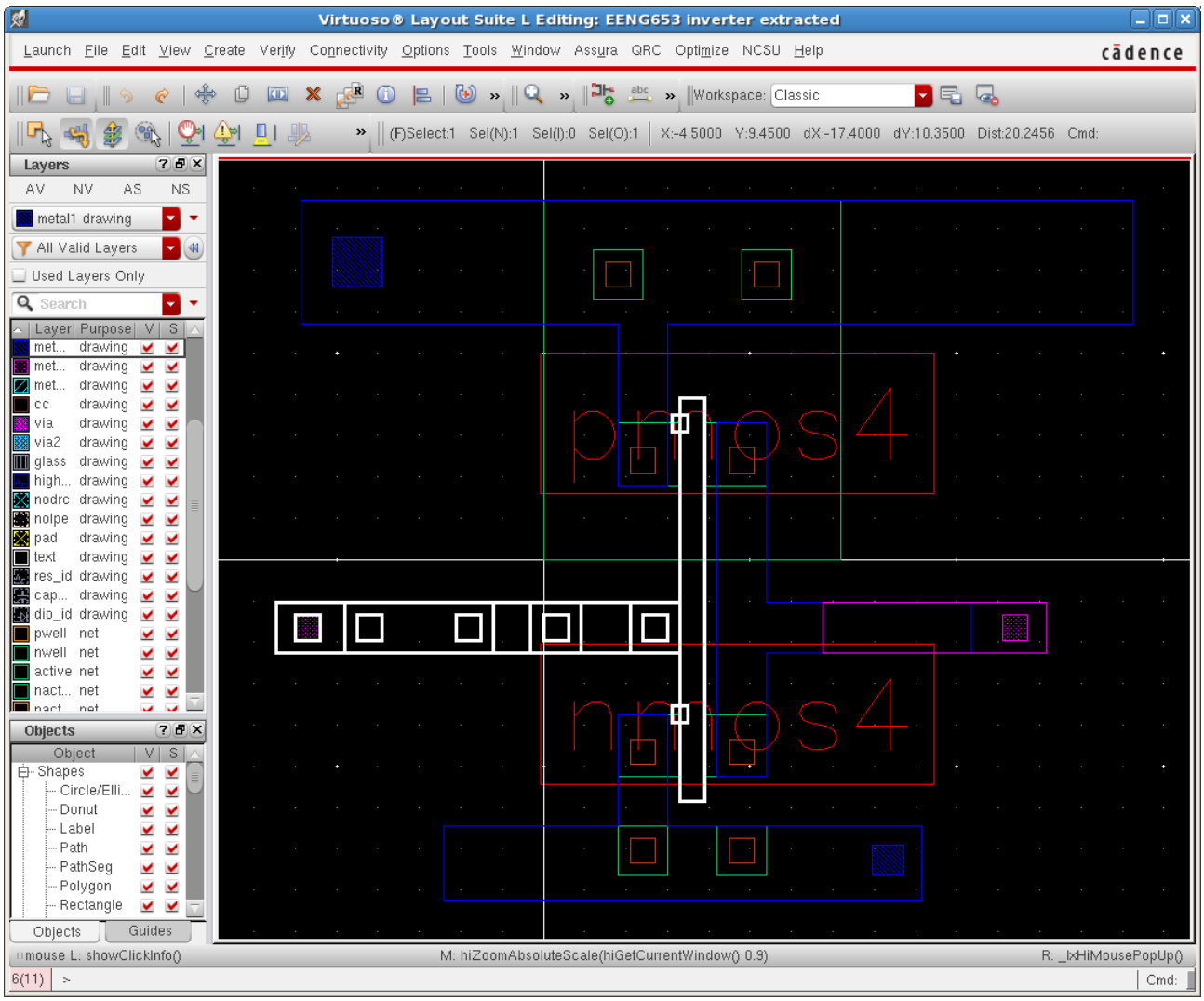
d. The 'extracted' view will appear in the Library Manager for the layout as shown in the image below. Note that your layout for the cell 'inverter' in the library 'EENG653' now contains four cellviews: an 'extracted' view, a 'layout' view, a 'schematic' view, and a 'symbol' view.



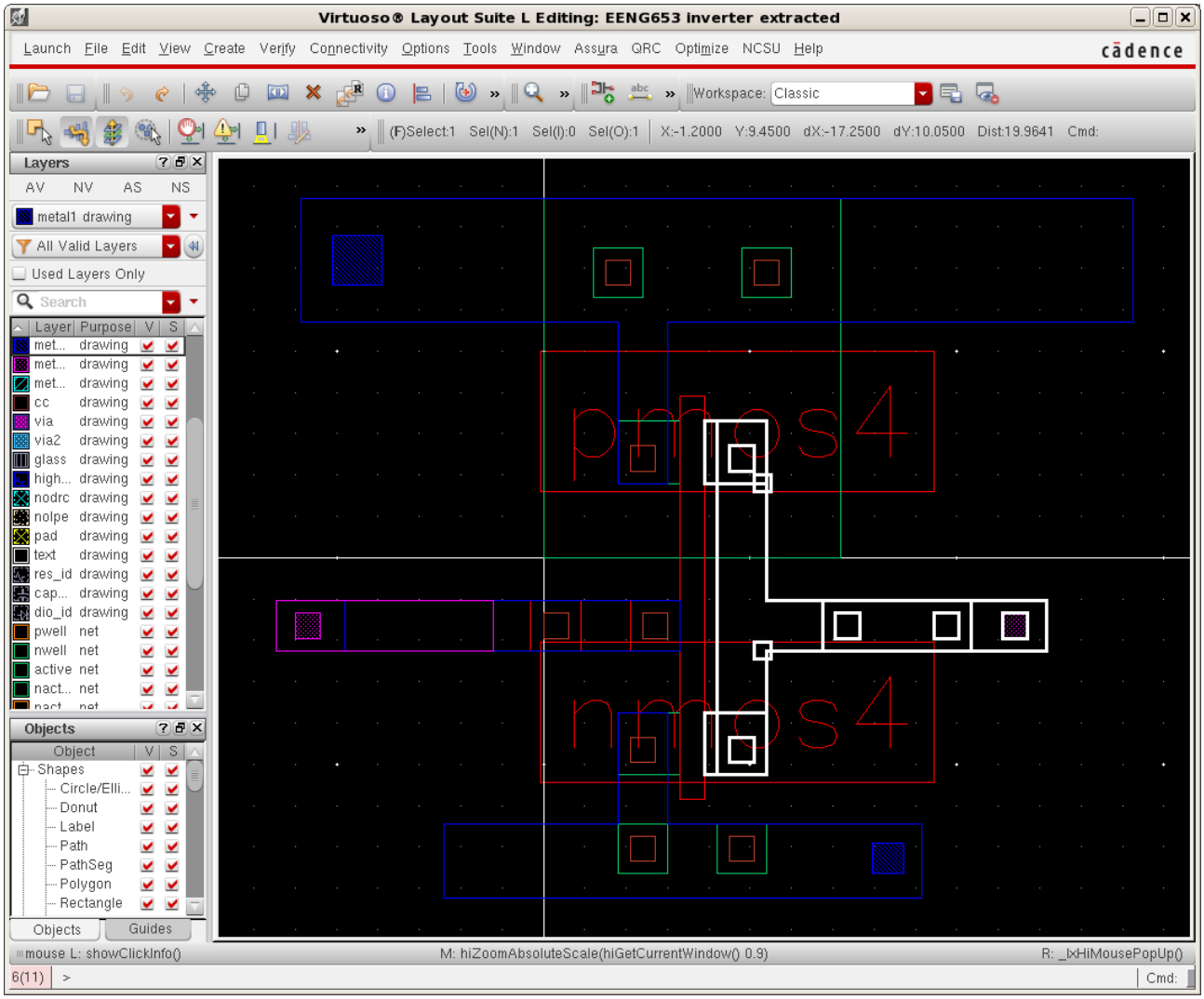
e. Double-click on the 'extracted' view to open it and obtain the image shown below. Notice the pins: VDD, GND, Vin, and Vout. Outlines are shown for the metal layers: polysilicon, metal1, metal2, vias, and wells. The outlines show the connectivity of the circuit (the shapes are merged together to show the shapes that are electrically connected).



f. You can click on the 'Vin' pin and obtain the image shown below. Notice that all shapes connected to 'Vin' are highlighted in white.



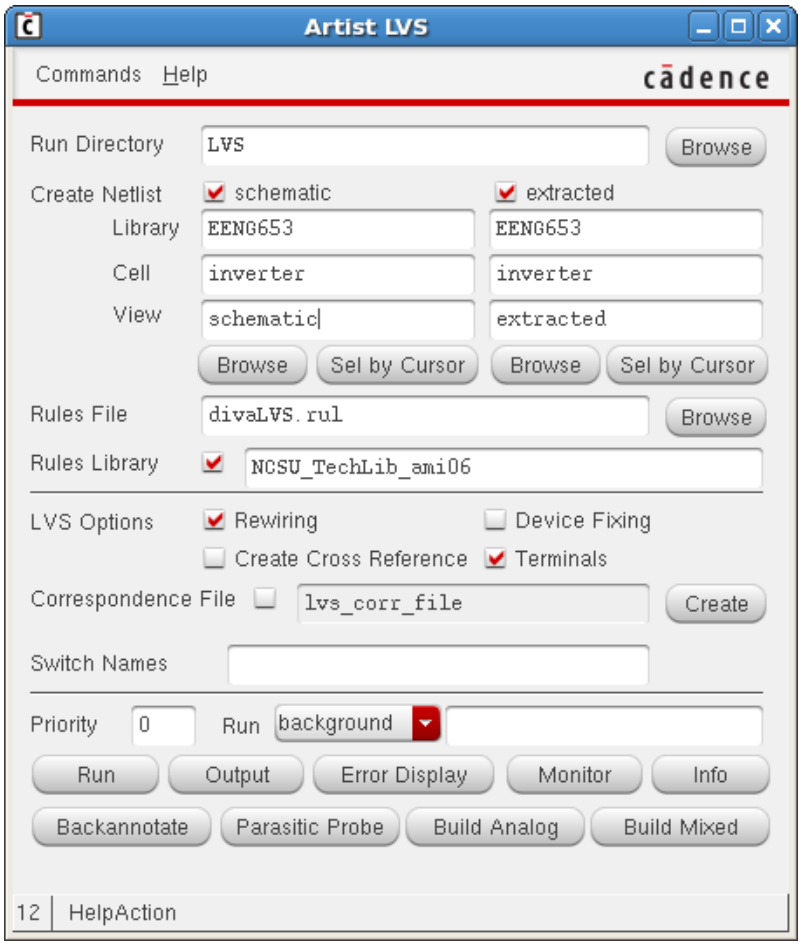
g. You can also click on the 'Vout' pin and obtain the image shown below. Notice that all shapes connected to 'Vout' are highlighted in white.



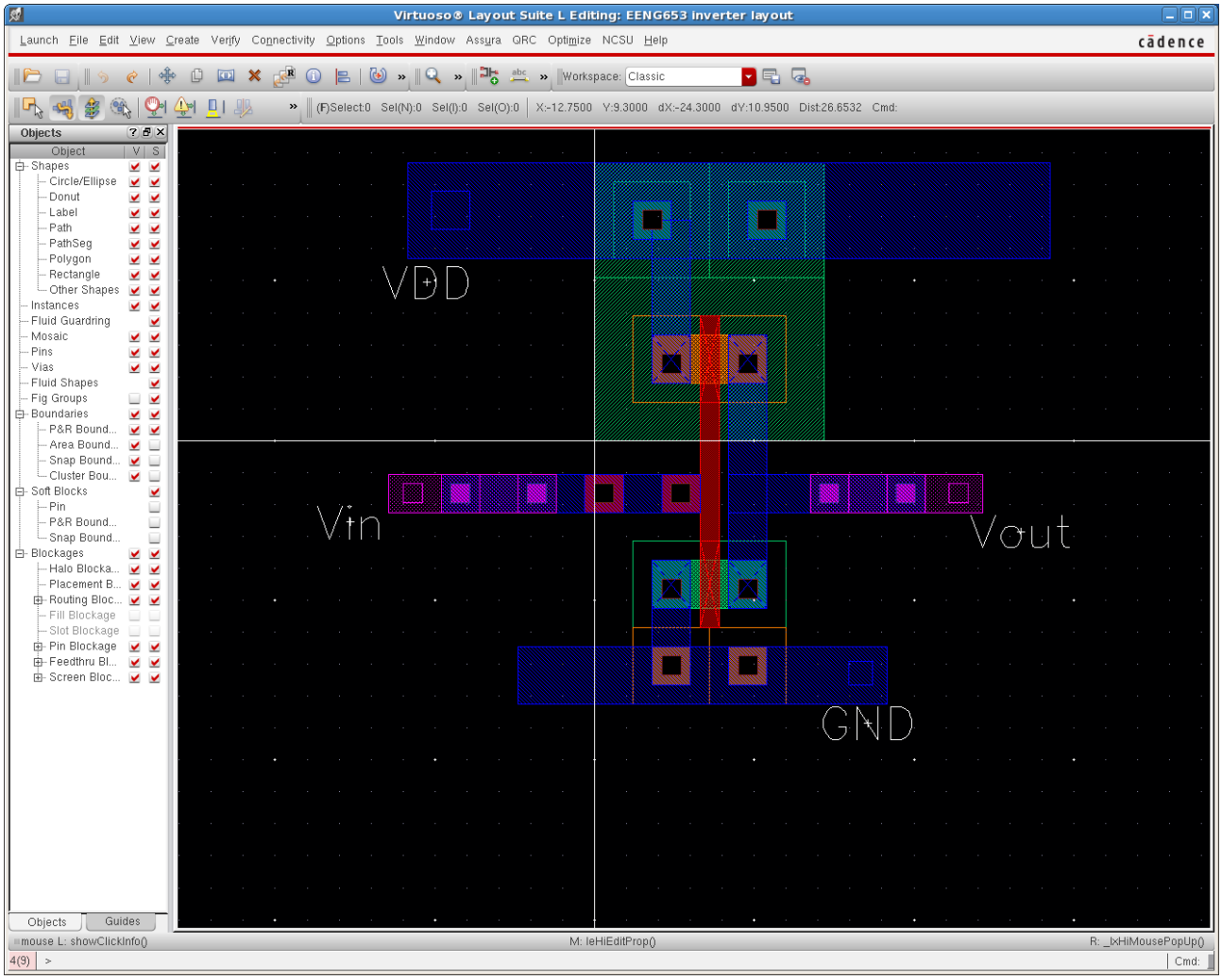
h. You have now completed Extraction of your layout.

18. Inverter: Running Layout Versus Schematic (LVS)

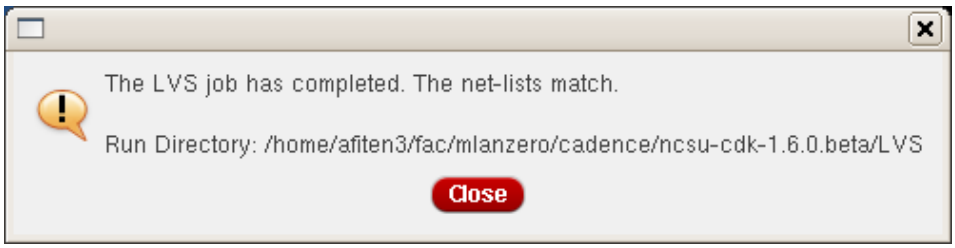
a. Now you will compare your layout with your schematic. Ideally, the connectivity in the layout will match the connectivity in the schematic. Running the software tool "LVS" will help you to verify if the netlist of your layout does match the netlist of your schematic. First, click on your layout. From the banner at the top of the layout, select "Verify → LVS." The "Artist LVS" window will appear as shown in the image below. Fill in the fields as shown in the image.



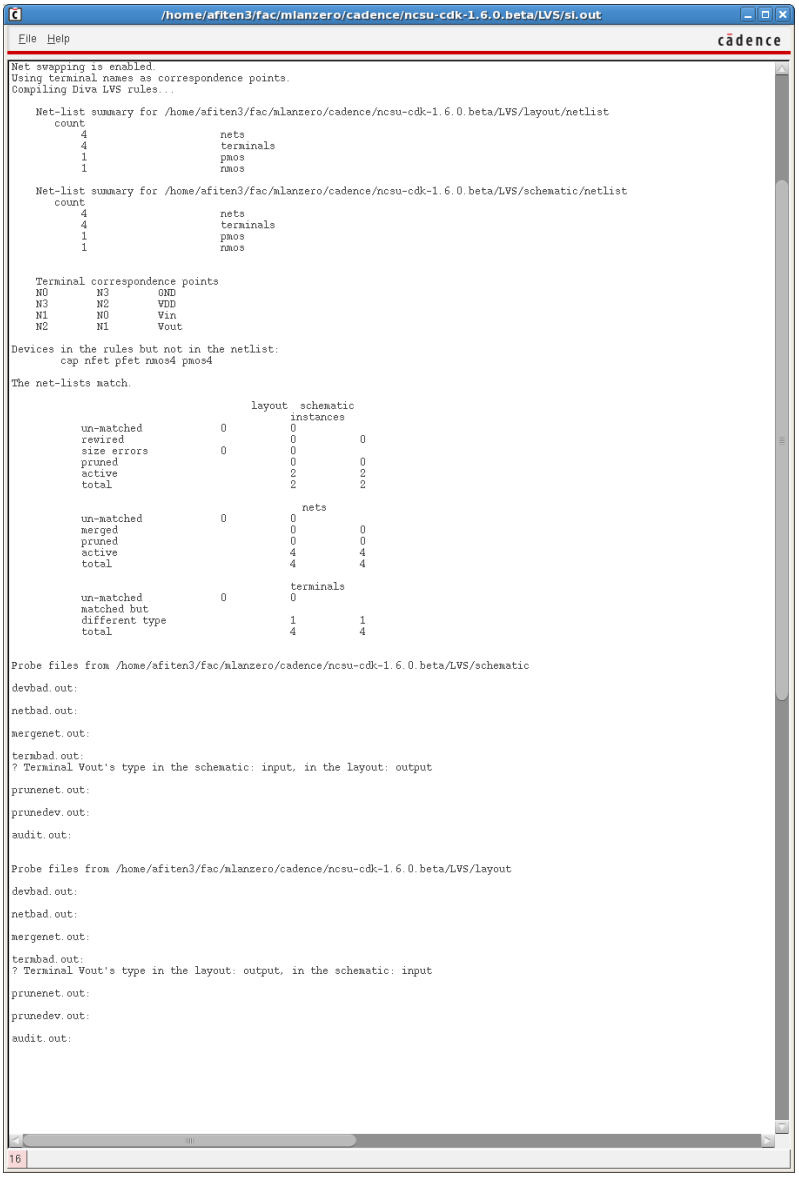
b. LVS will now run and compare the connectivity in the layout cellview (in the image below) with your schematic.



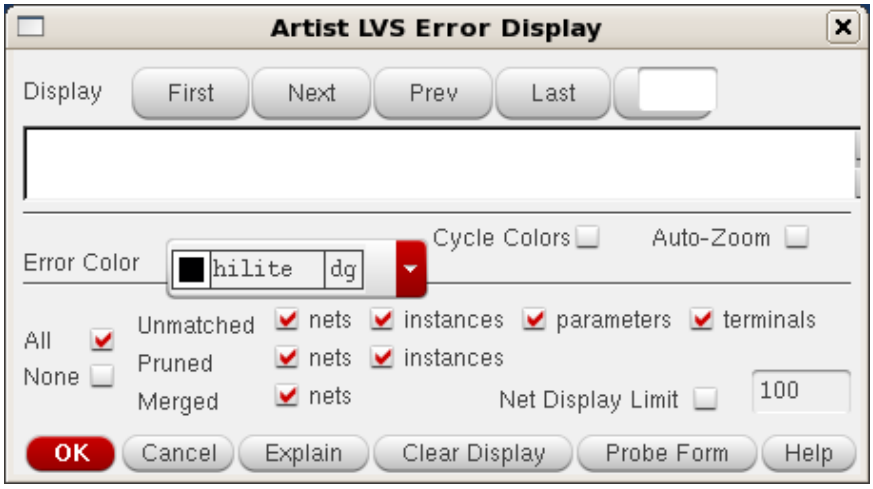
c. When LVS completes, and if the net-lists match, a window will appear showing that "The LVS job has completed. The net-lists match," and the window will provide the path to the Run Directory.



d. After running "LVS," the CIW will report the si.out file (log file for the LVS run) as shown in the image below. Notice that when LVS passes, the si.out file indicates that "The net-lists match."



e. If errors are found by LVS, a window "Artist LVS Error Display," can be used to identify the error markers.

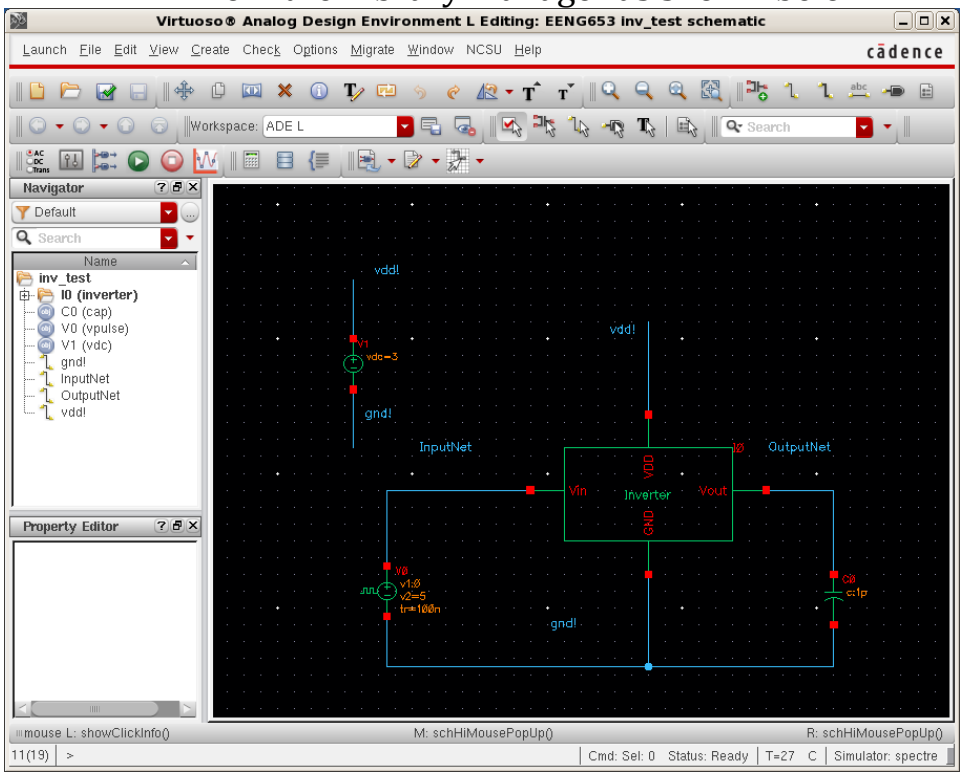


f. Fix any errors that may exist in the layout. Re-run LVS until no errors are reported. If LVS passes with no errors, you have now completed LVS.

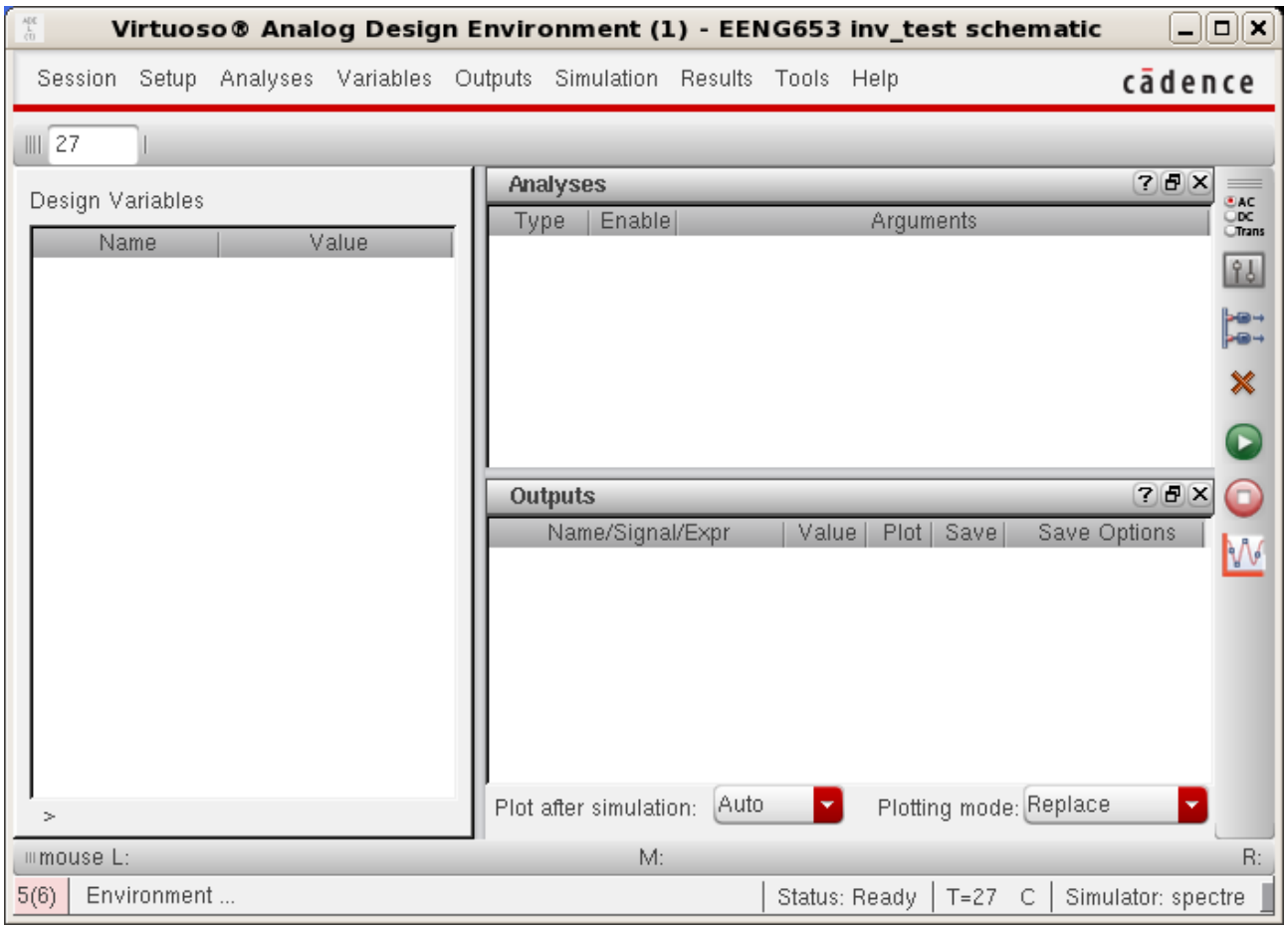
19. Inverter: Running Extracted-Layout Simulation

a. Now you will simulate your design using the extracted capacitances that you obtained during the "Extraction" step. The extraction cellview will change as the layout changes, and a post-layout simulation will indicate how the layout of your inverter will perform compared with your idealized schematic (your schematic does not contain any parasitic capacitances). The procedure that you will use is the same as the procedure for simulating the schematic view (described in a previous step).

b. Open your library "EENG653" cell "inv_test" cellview "schematic" from the Library Manager as shown below.

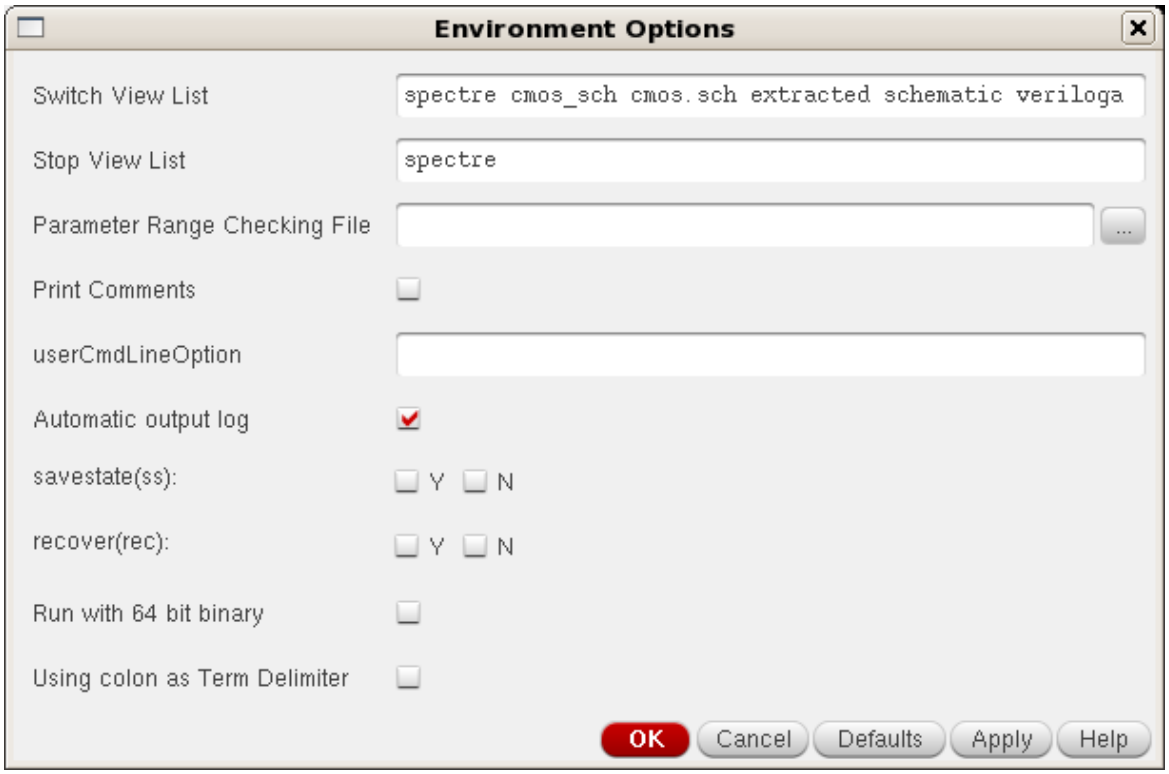


c. Click on the schematic window. Using the banner at the top of the schematic window, click on "Launch → ADE L" to bring up the 'Virtuoso Analog Design Environment' window shown below.

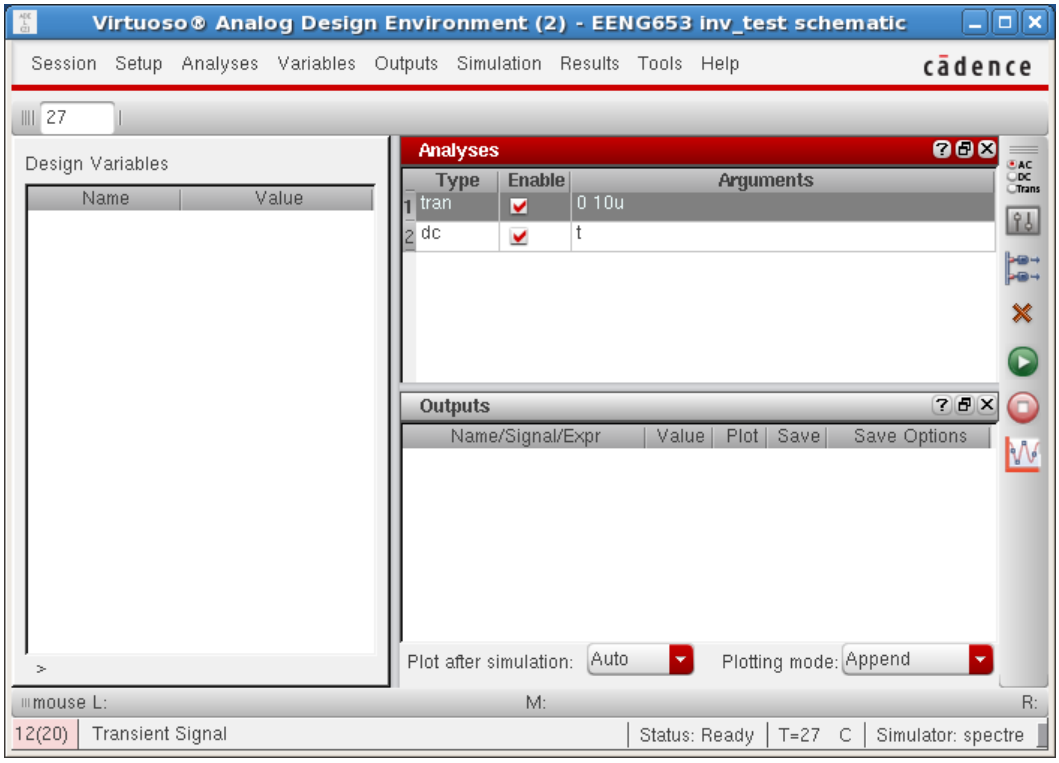


d. Now we will set up to display the simulation results for your schematic and for your extracted view in the same window. The first step is to first simulate your schematic with DC mode and transient mode options as before and display your results in the display window. (Be sure to follow all of the steps involved in setting up a simulation that were shown in previous sections).

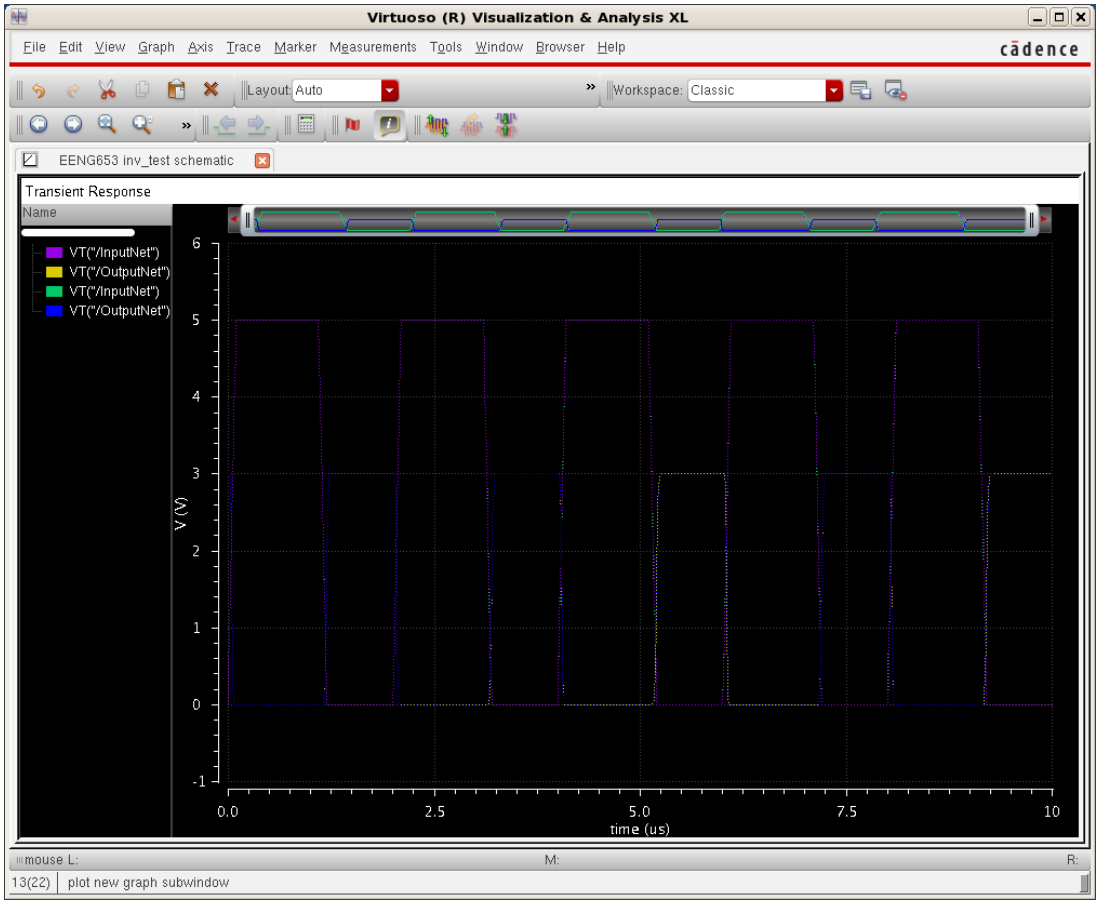
e. Click on the "Virtuoso Analog Design Environment" window for your "EENG653 inv_test schematic". On the banner at the top of the window, select "Setup → Environment," and a window named "Environment Options" will appear as shown in the image below. In the 'Switch View List' in the 'Environment Options' window, add 'extracted' between 'cmos.sch' and 'schematic' so that the field appears as shown in the image.



f. Open the "Environment Options" window and resimulate with your extracted view as shown in the image in (e) (above). In the "Virtuoso Analog Design Environment" window for your "EE653 inv_test schematic", select the "Append" radio button next to the "Plotting mode" at the lower right-hand corner of the form.



g. When you append the results of the extracted simulation to the results of the schematic simulation, the results will be shown together, as shown in the image below where the waveforms show that the simulations match well (Note that you can measure waveforms with the cursor in the window):

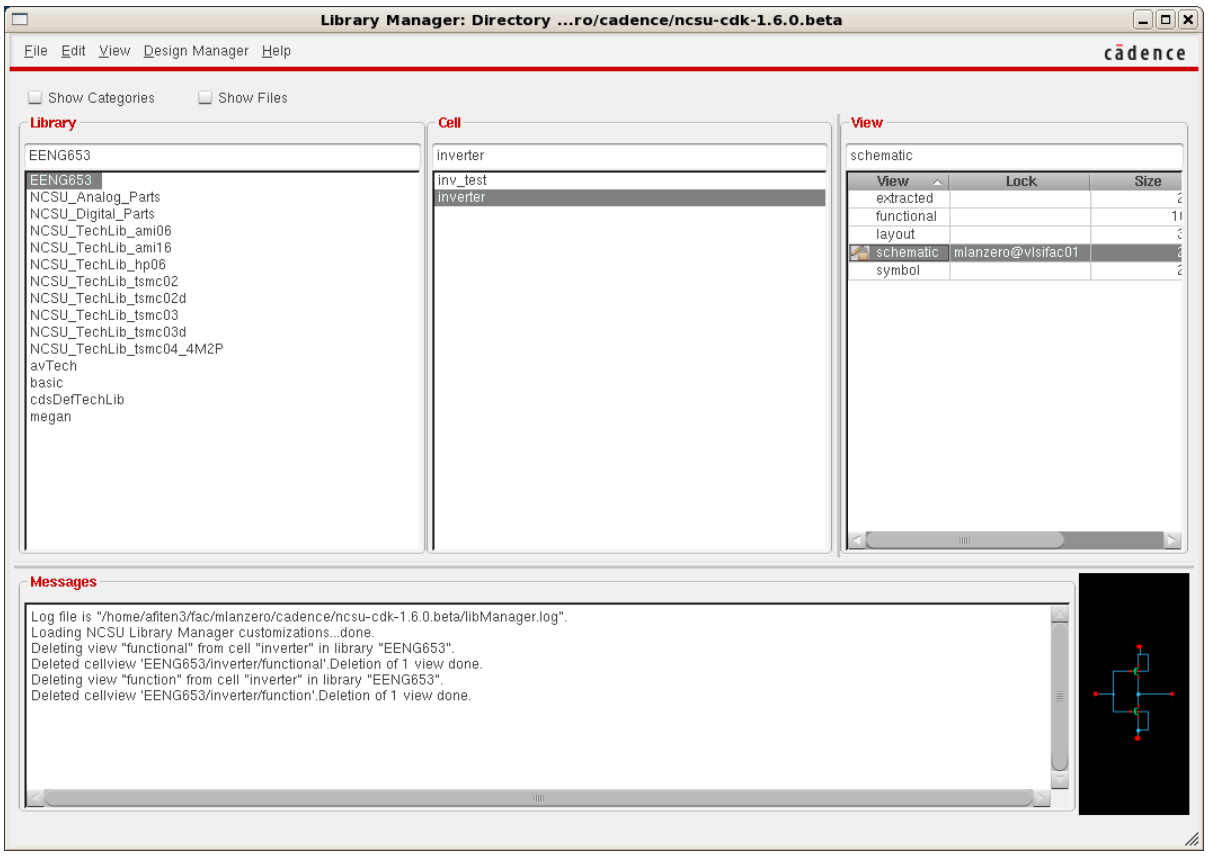


h. Now you have simulated your schematic view and your extracted view of your inverter. For a layout with a lot of extra wire (extra metal layer), the simulation of the extracted view will not closely match the simulation of the schematic view.

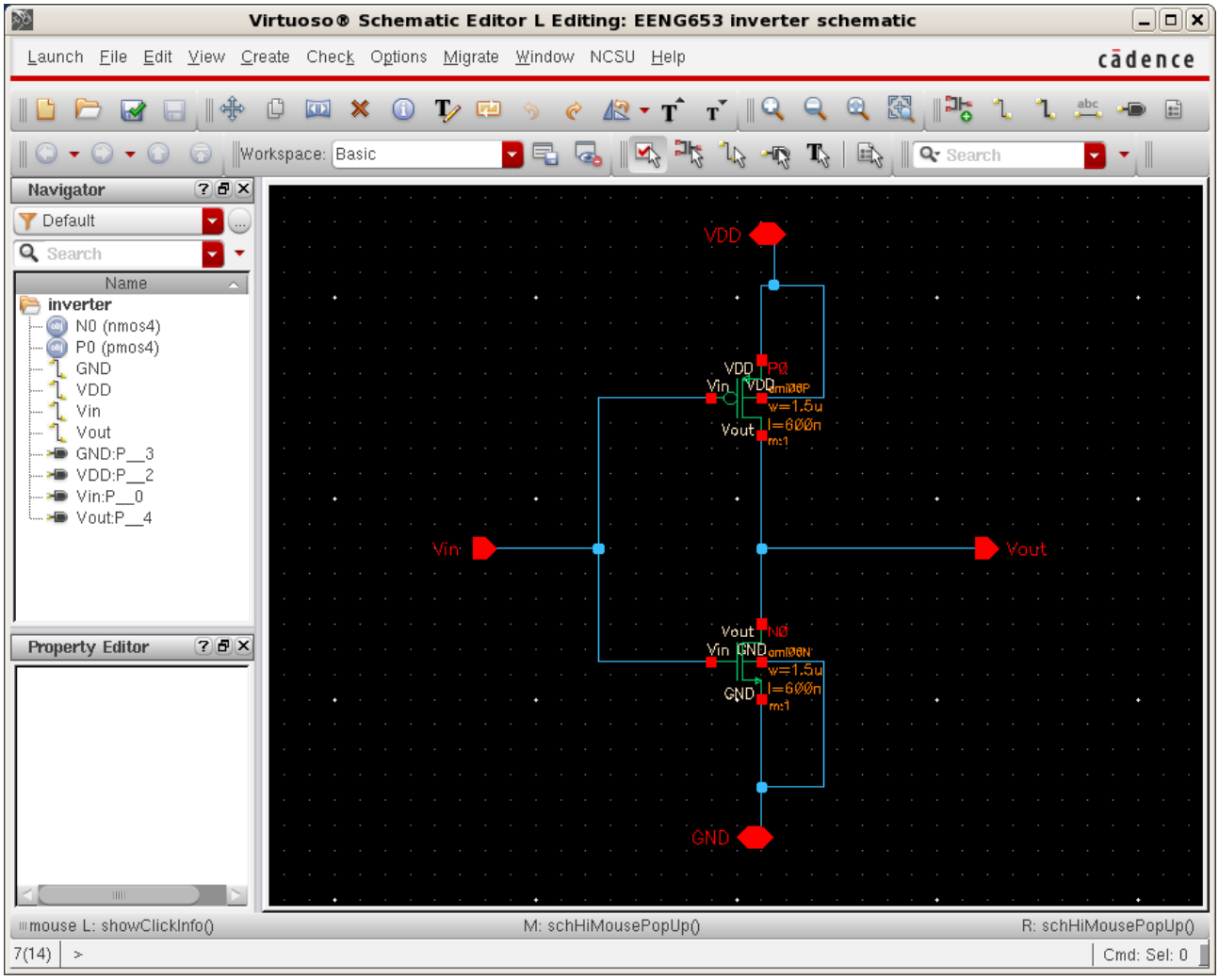
20. Inverter: Simulation with NC-Verilog

a. You will now learn to perform digital logic design in the Cadence environment with a software tool called "NC-Verilog." "NC-Verilog" performs logic design at the functional level, such as logic design of your inverter. In this section, you will create a verilog file for your inverter design and will simulate the function of this inverter using Cadence.

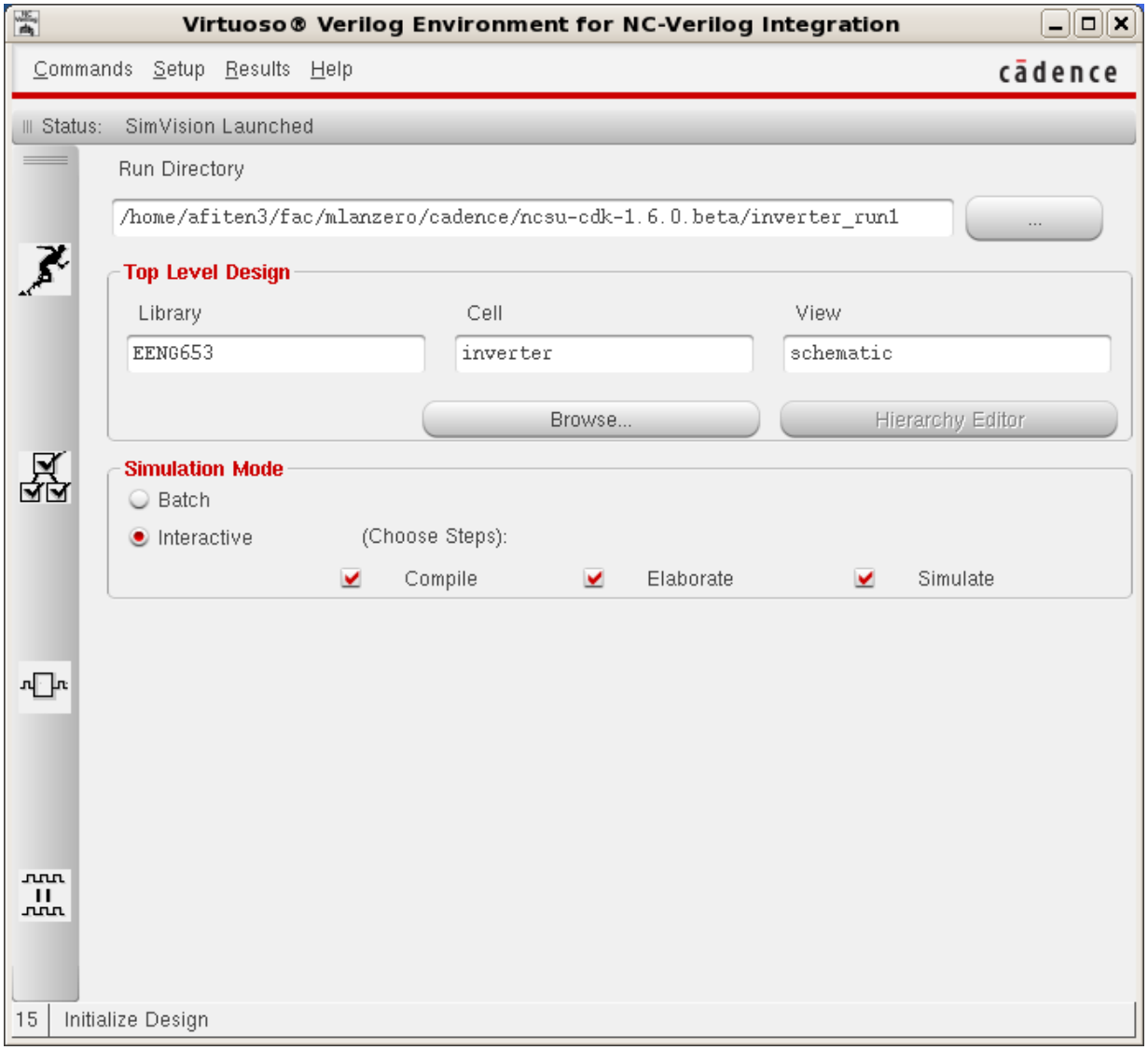
b. First, open the Library Manager. Select your library "EENG653", the cellname "inverter" and viewname "schematic" as shown in the image below.



c. Open the schematic. The "Virtuoso Schematic Editor" window will display your schematic as shown in the image below.

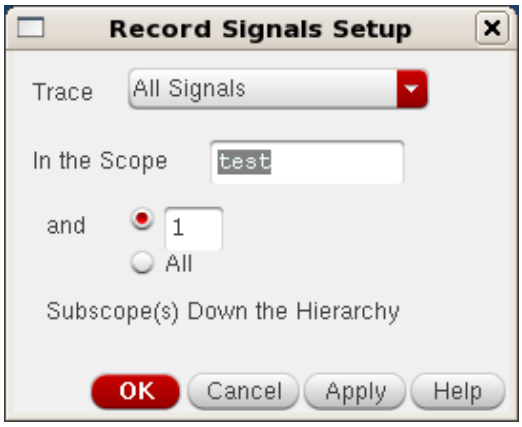


d. Click on your schematic. At the banner of the schematic, select "Launch → Simulation → NC-Verilog" which will launch the "Virtuoso Verilog Environment for NC-Verilog Integration" window shown in the image below.



e. On the "Virtuoso Verilog Environment for NC-Verilog Integration" form, select "Setup → Record Signals." The window "Record Signals Setup" will appear as shown in the image below. Complete this form, change the depth of '1' to a depth of '100,' click "All" and click "OK" on the form. (It is reported that this is a bug in Cadence.)

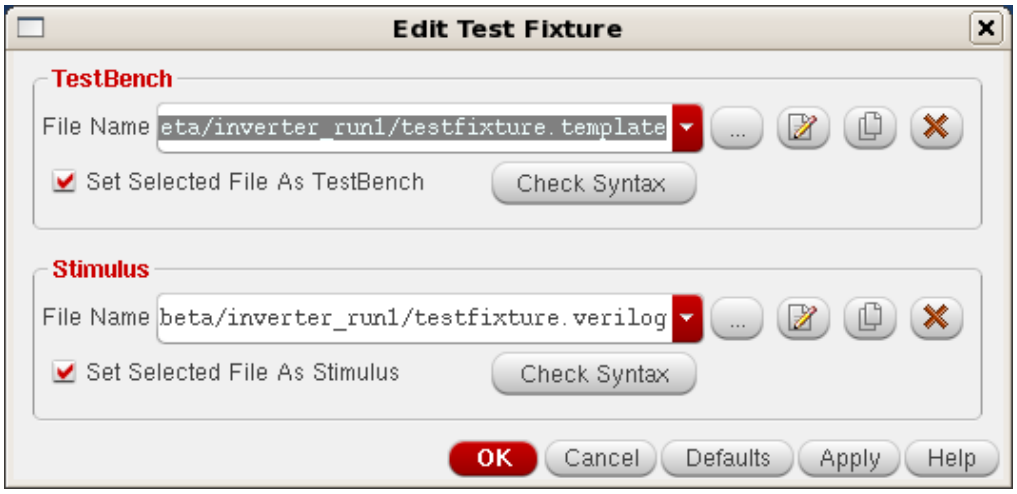
If this step does not work the first time, click "Initialize Design" (the runner on the left-hand side of the window) in the "Virtuoso Verilog Environment for NC-Verilog Integration" window. Then click on "Setup → Record Signals" and follow the previous steps in (e).



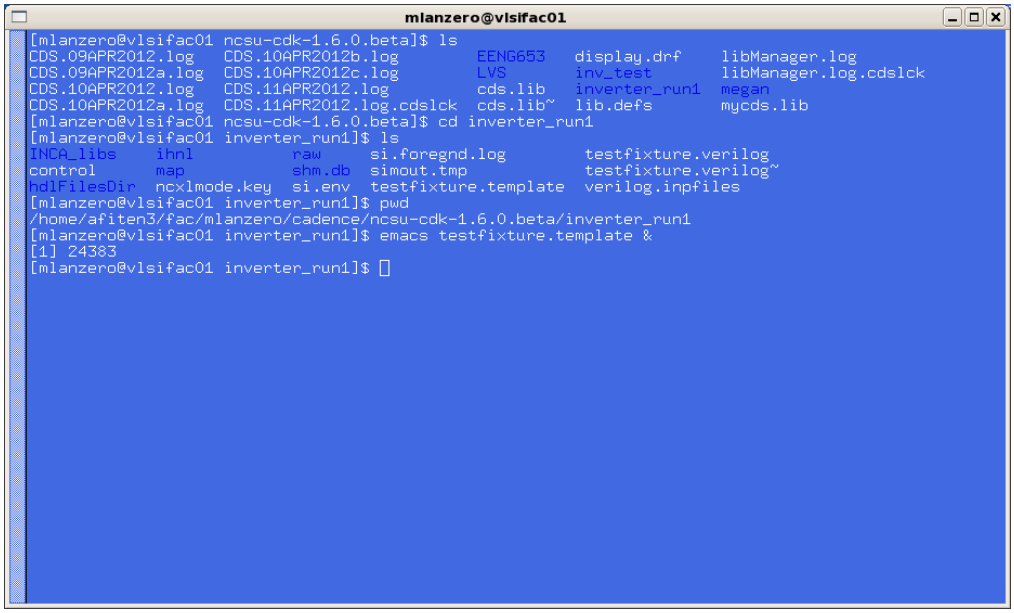
f. In the "Virtuoso Verilog Environment for NC-Verilog Integration" window, click "Initialize Design" (the runner on the left-hand side of the window.

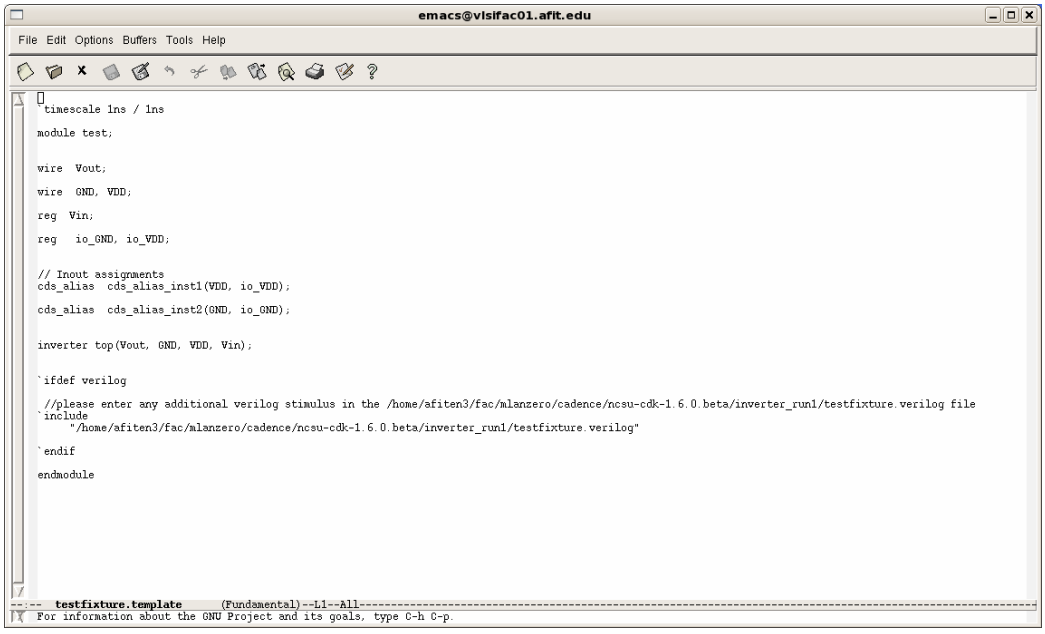
g. Then in the "Virtuoso Verilog Environment for NC-Verilog Integration" window, click "Generate Netlist" (the three boxes with checks on the left-hand side of the window. Each time that you change your design, you need to re-netlist it.

h. In the "Virtuoso Verilog Environment for NC-Verilog Integration" window, click "Commands → Edit TestFixture," and the "Edit Test Fixture" window will appear as shown in the image below.

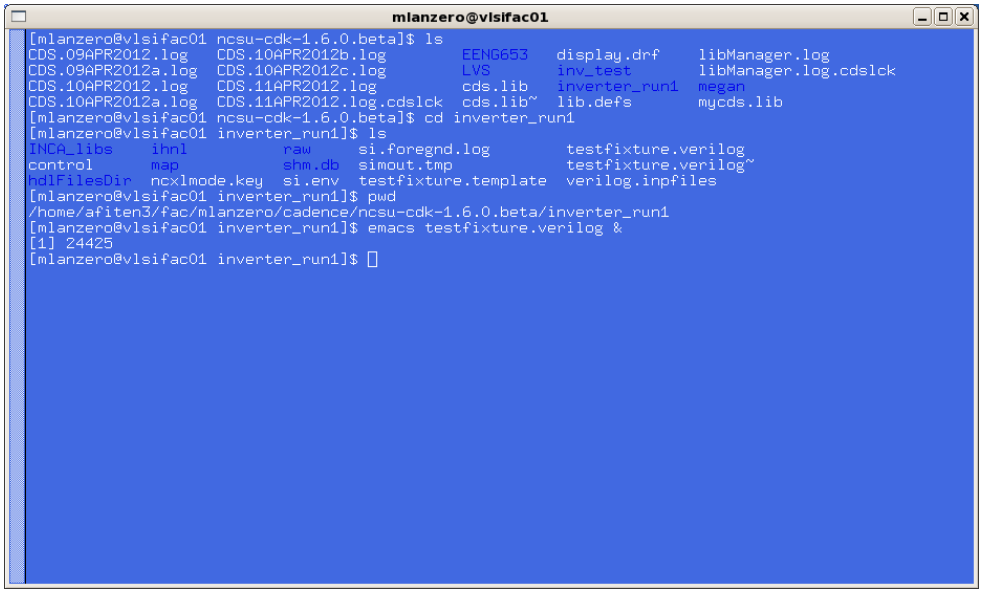


i. You may view the testfixture.template file. Emacs is one editor that can be used to edit the file as shown in the images below.

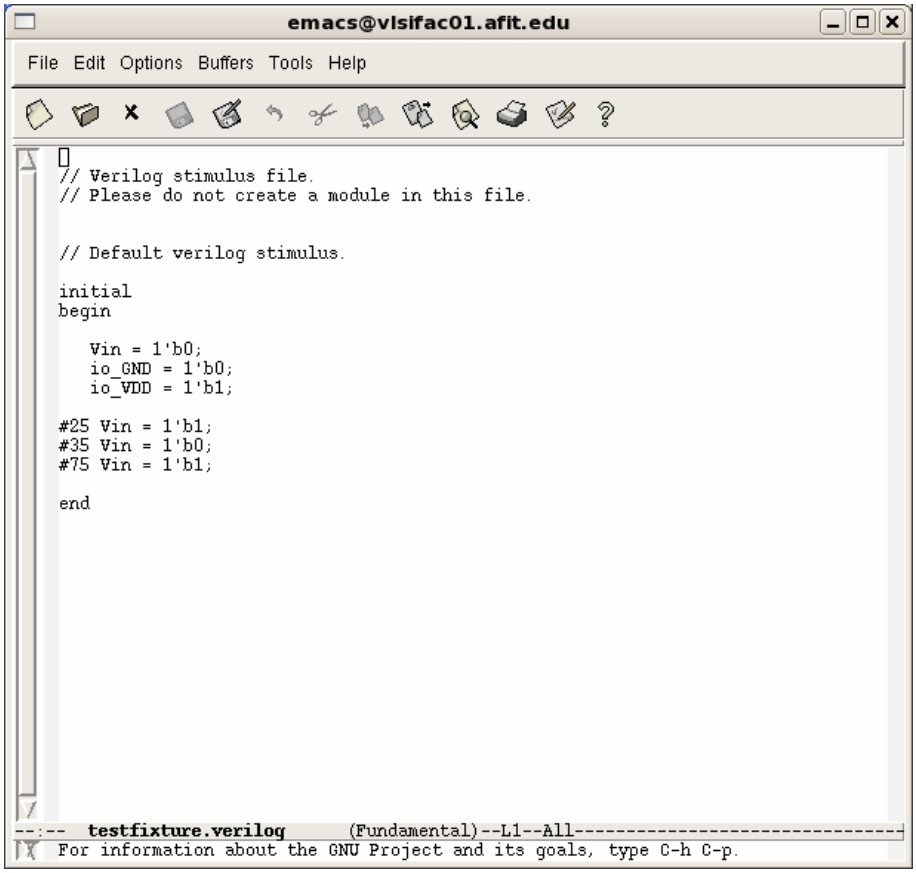




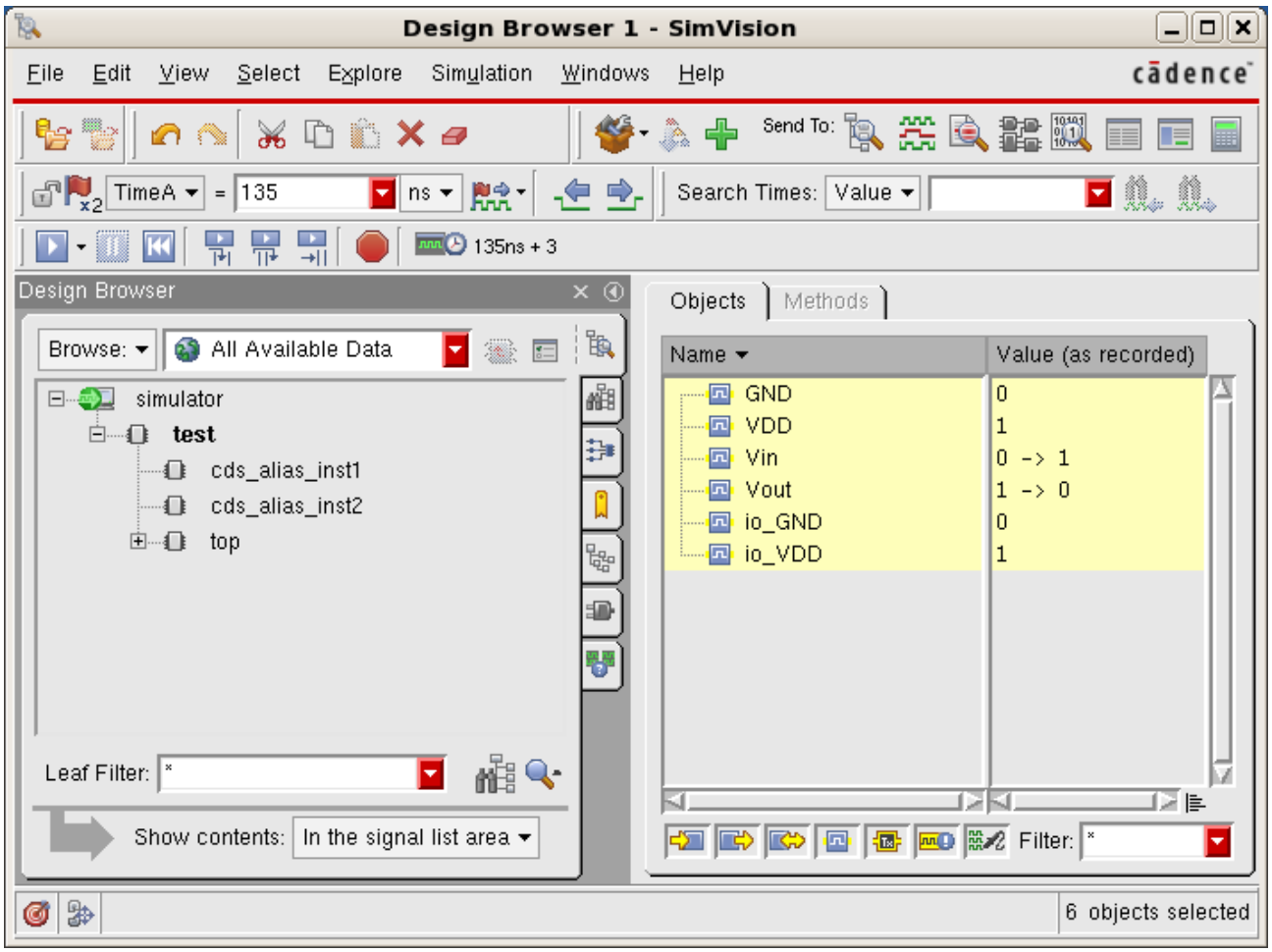
j. You may view the testfixture.verilog file. Emacs is one editor that can be used to edit the file as shown in the image below.



k. Edit the testfixture.verilog file so that it matches the file shown in the image below.



l. Then click 'Simulate' on the "Virtuoso Verilog Environment for NC-Verilog Integration (the third button on the left-hand side of the form showing an input waveform, a block diagram, and an output waveform). Two windows will appear: "Design Browser 1 – SimVision" and "Console – SimVision" as shown below.



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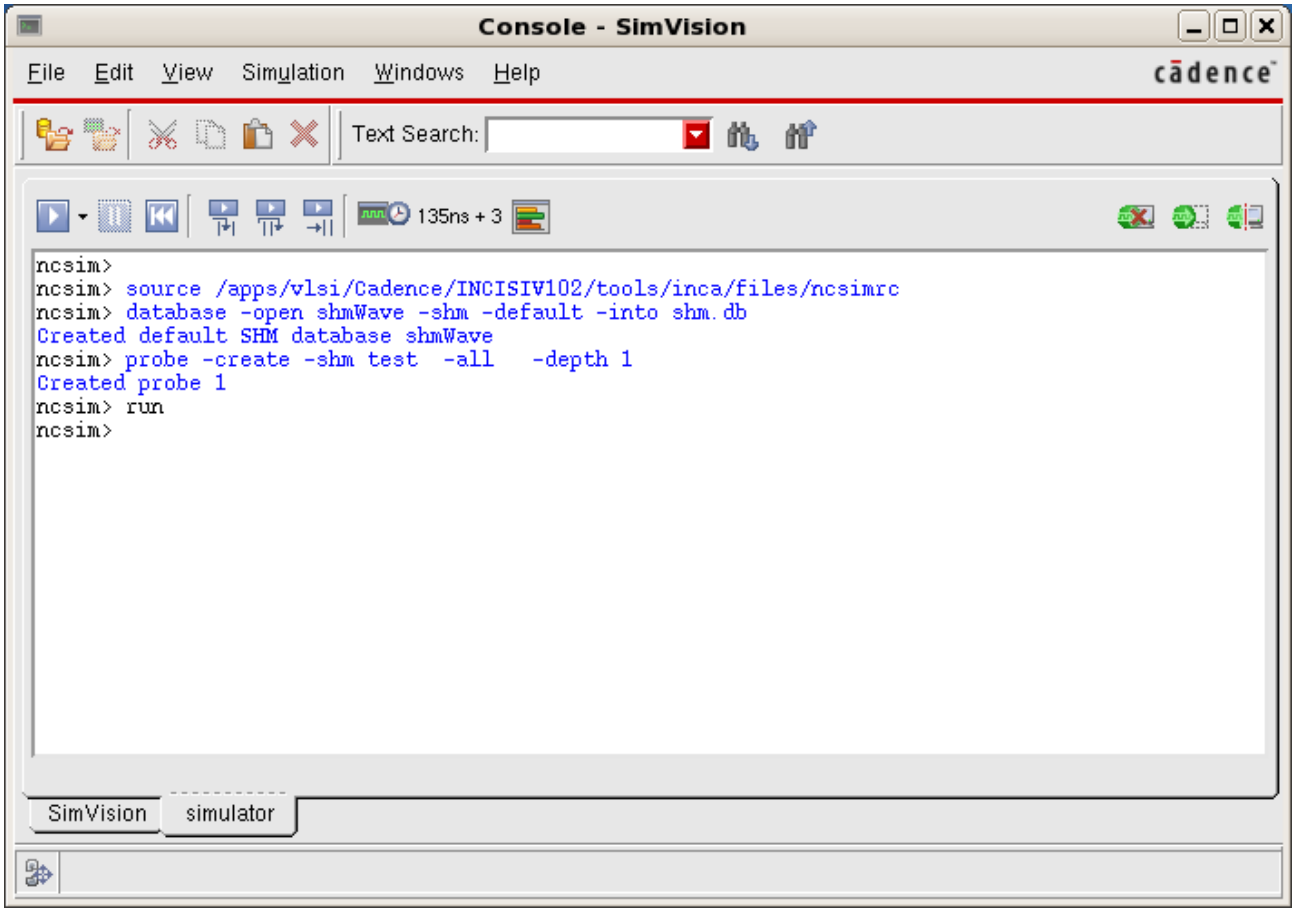
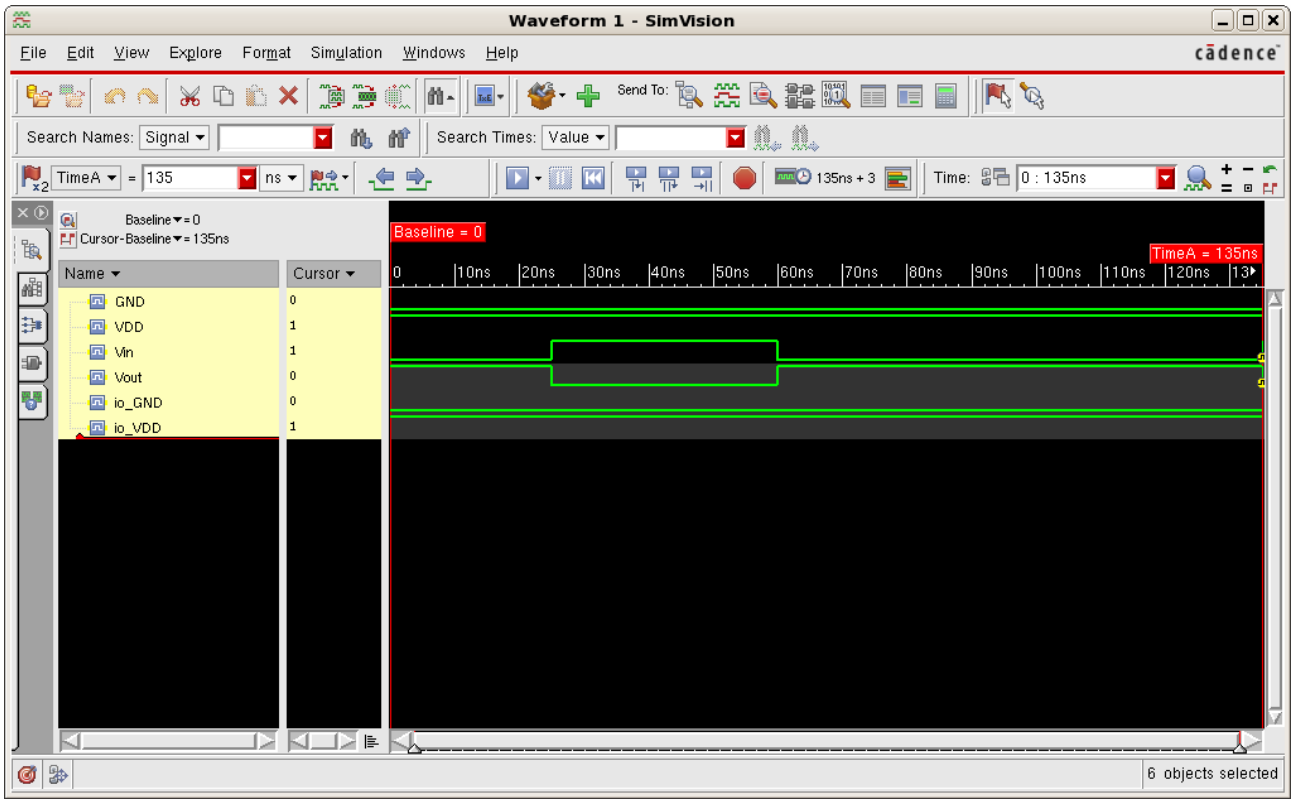
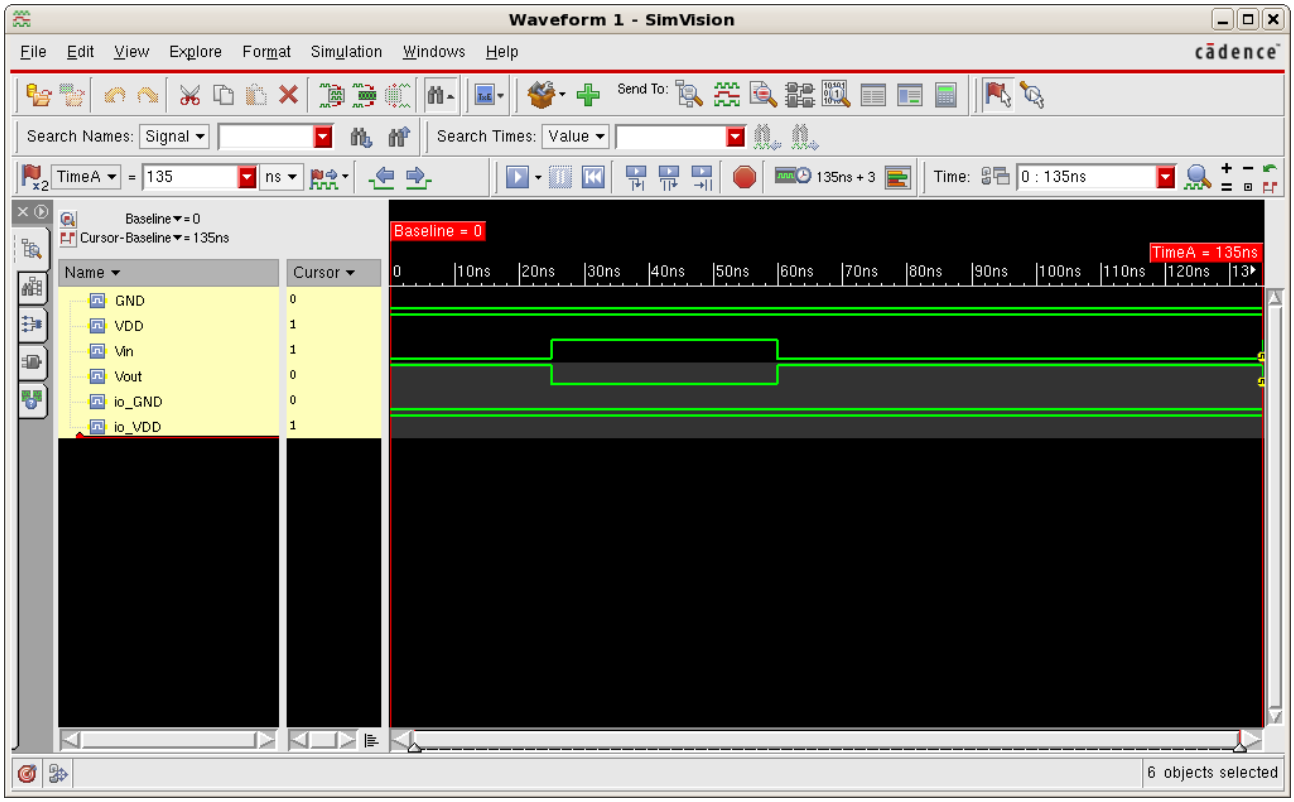


m. In the "Design Brower 1 – Sim Vision" window, click on 'test' and then select the nodes in the 'Objects' window on the right-hand side of the window. Select the nodes so that they turn yellow: "GND," "VDD," "Vin," "Vout," "io_GND," and "io_VDD." Right-click on the yellow nodes and select "Send to waveform window." A new window, "Waveform 1 – SimVision" window will appear as shown in the image below.



n. In the "Waveform 1 – SimVision" window, click on the blue 'Run' button (the blue button with the white arrow pointing to the right). The waveforms for the nodes will appear as shown in green. Notice that the "Vin" signal transitions from 0 → 1 at 25ns as you specified in the testfixture.verilog file. Also notice that the "Vin" signal transitions from 1 → 0 at 60ns as you specified in the textfixture.verilog file (that is, it transitions 35 ns after the first transition). Finally, notice that the "Vin" signal transitions from 0 → 1 again at 135 ns (75 ns after the previous transition), as you specified in the testfixture.verilog file.



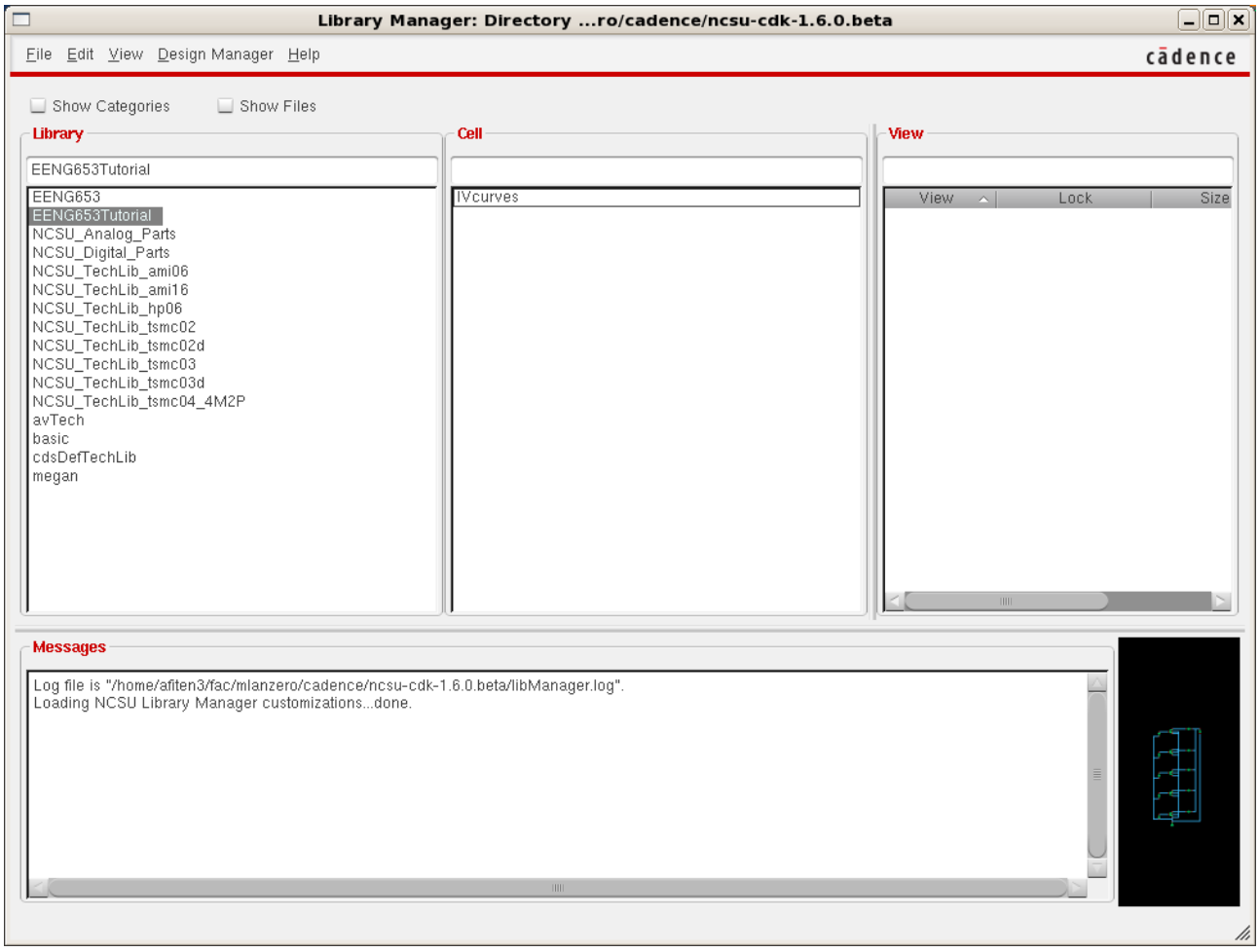
o. Notice that in the "Waveform 1 – SimVision" window, the "Vout" node is the 'not' of the "Vin" node. This behavior is expected for an inverter.

p. You have now completed the step of running NC-Verilog on an inverter schematic.

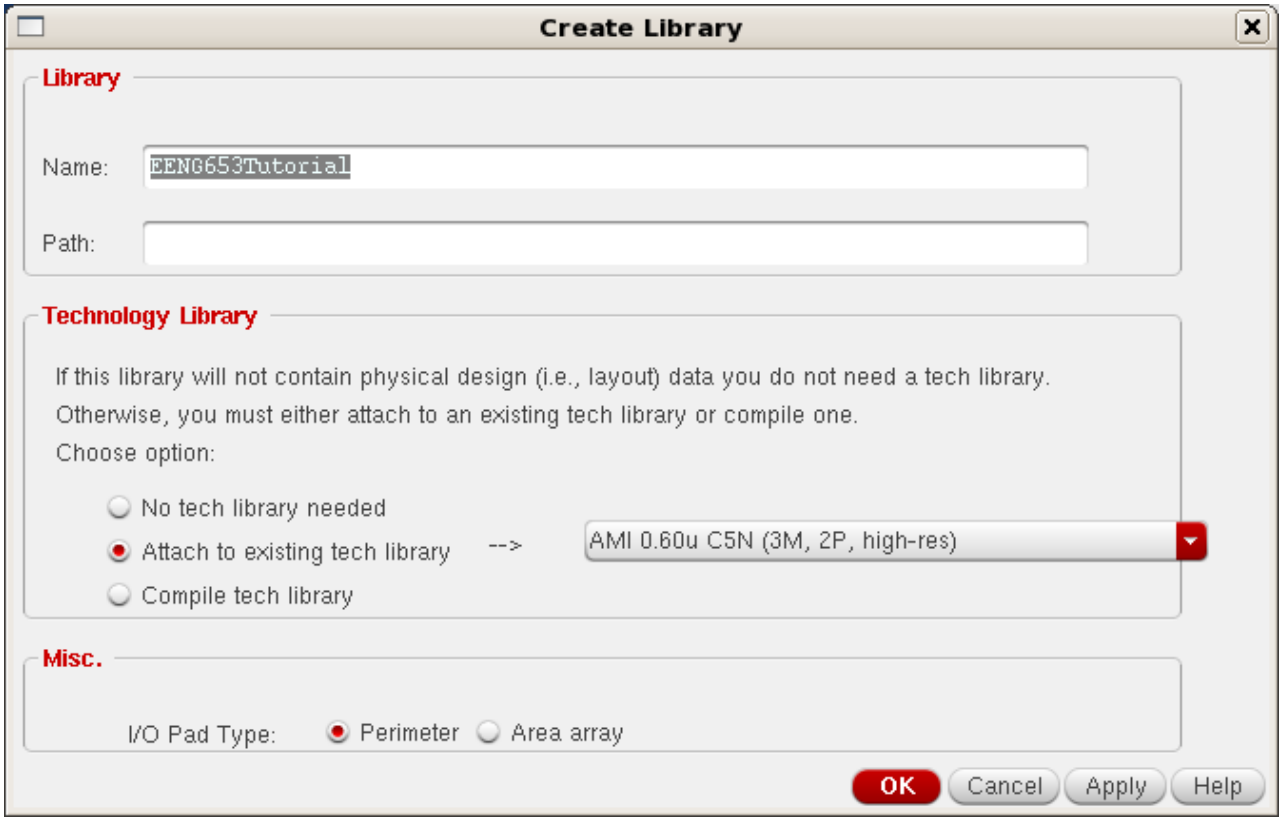
q. Note that each time you want to re-run the simulation, you must close SimVision, re-netlist, and click the simulate button again.

21. nFET: Generating I-V Curves for an nFET

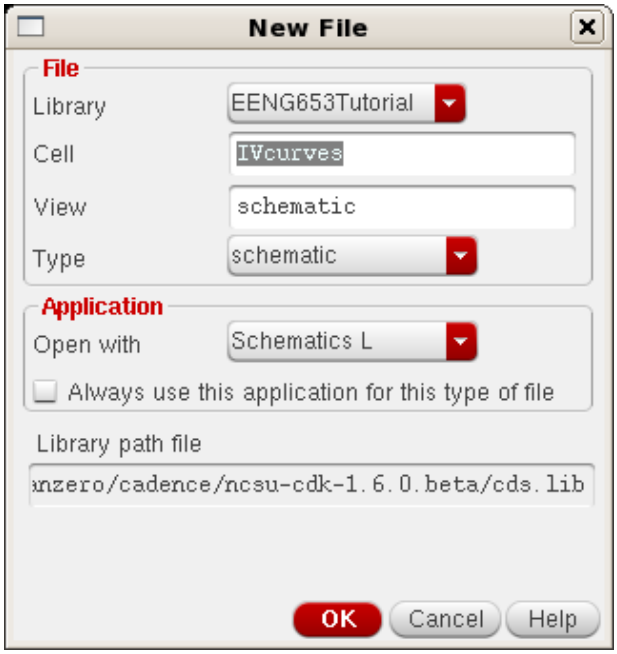
a. You are now going to generate I-V curves for an nFET with technology AMI 060u C5N (3M, 2P, high-res). Open the Library Manager and create a new library called "EENG653Tutorial" as shown in the image below.



b. In the Library Manager, click on "File → New → Library" to open the "Create Library" window and complete it as shown. Attach the new library to existing technology library "AMI 0.60u C5N (3M, 2P, high-res)." Then click "OK."

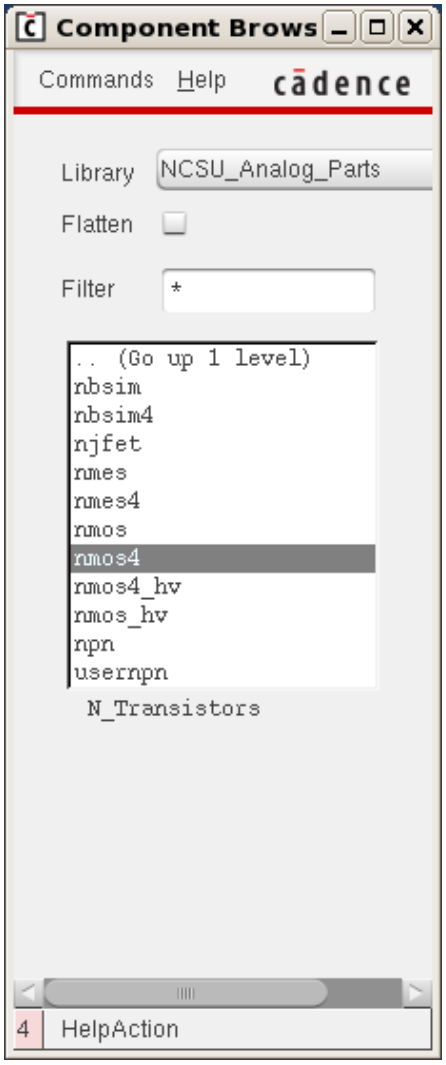


c. The library "EENG653Tutorial" should now appear in the Library Manager. You are now going to open a new schematic. Click on the Library Manager. Select the library "EENG653Tutorial" and then click "File → New → Cell View" and complete the "New File" window that appears below. Set "Cell" to "Ivcurves" and "View" to "schematic." Then click "OK."



d. Now you will see the schematic editing window. Spend some time analyzing the window. On the left side, you will see shortcuts to commonly-used commands such as: placing component instances (it looks like an IC), drawing wires, placing ports, stretching, copying, zooming in and out, saving, and so on. If you pass the mouse pointer on top of the buttons you will see short pop-up help messages. You also have access to these commands (and others) from the menu. It is not possible in this tutorial to explain all the functionality of Virtuoso Schematic so you are strongly encouraged to read the on-line user manuals (select "Help").

e. You will now generate a schematic which will be used to generate and plot I-V curves. Click 'I' in the schematic editor window to bring up the "Component Browser" and "Add Instance" windows as shown below. Select "NCSU_Analog_Parts → N_Transistors → nmos4."



f. These choices will automatically fill in the other pop-up window, called the "Add Instance" window (You could have also filled in this window directly).

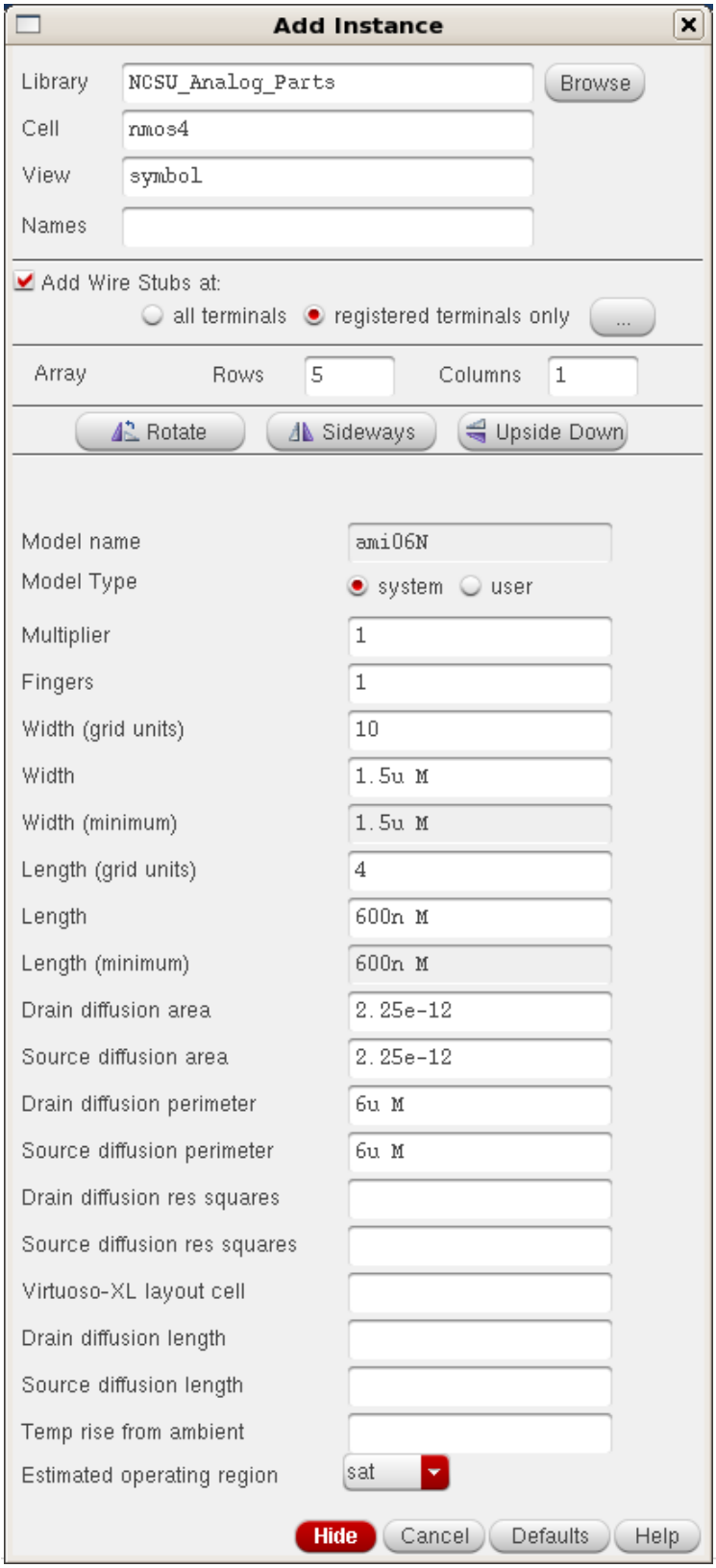
Now move the mouse over the Virtuoso Schematic window, and you will see an 'outline' (or ghost) of the transistor. You can move, rotate, and/or flip this outline until the transistor is in the desired orientation; when you are satisfied that the transistor is oriented correctly, you can click on the left-mouse button to place the transistor in the schematic.

It is possible to place the transistors one at a time, but it is easier to place several transistors at one time as long as you know in advance the required number.

In this case, you need five transistors, so select 5 rows and 1 column in the "Add Instance" window as shown in the image on the next page.

It is a good idea to save your design from time to time in case the system crashes.

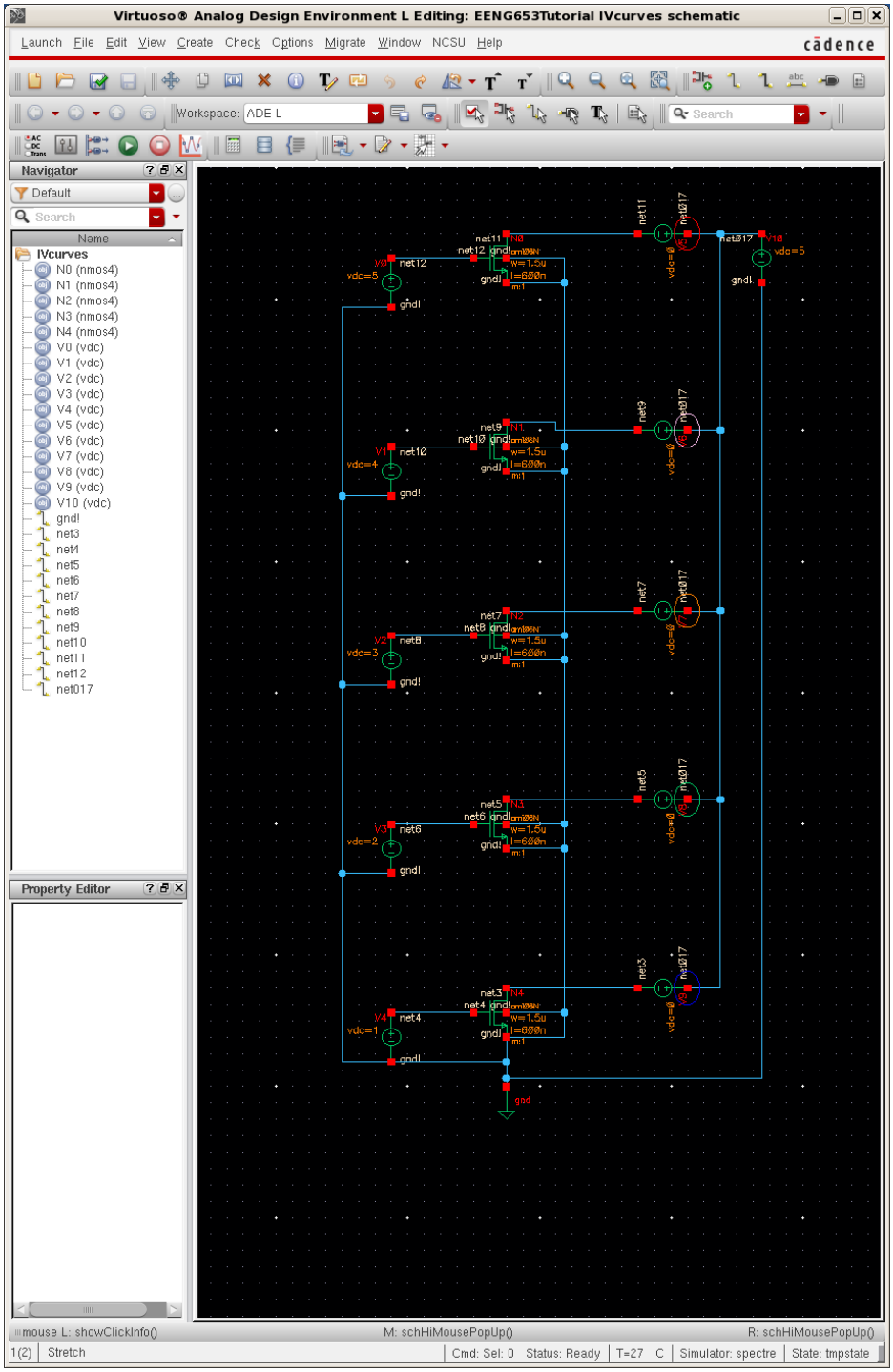
Integrated Circuit Design CAD Tool Information



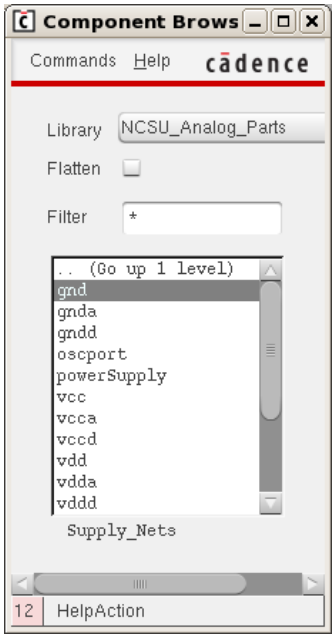
g. Now you can place the five transistors by clicking on the left mouse button for the first transistor and then moving the mouse vertically downward and clicking again. Do these five clicks now. If you make mistakes, you can always go to "Edit → Undo" and try again. You can press the ESC key on the keyboard to get out of the place instance mode, or you can keep placing other parts.

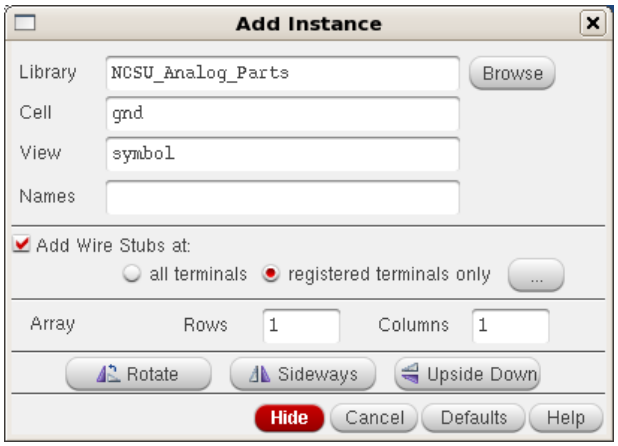
You can also move parts and delete parts. Please explore the different editing functions.

h. The schematic that you are building is shown below.



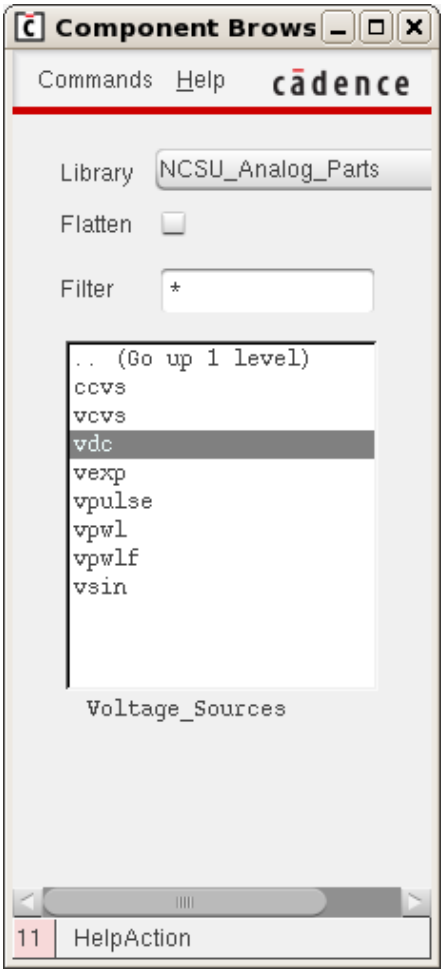
i. Now you need to add ports, wires, and the power supply. First, add ground by clicking 'I' again and then choosing "Supply-Nets" and then 'gnd' in the Component Browser window. Place one gnd below the five transistors as shown in the image on the previous page.



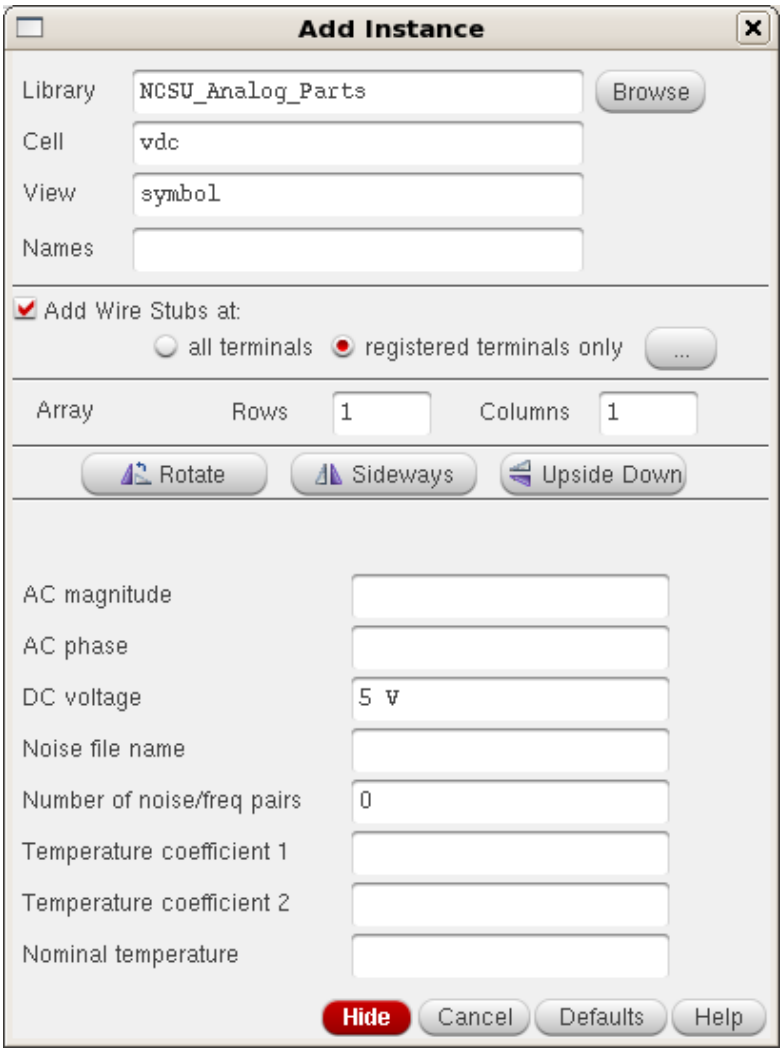


j. Now add wires by typing 'w' in the schematic to connect all the transistor sources and transistor bodies to ground.

k. Now add six DC voltage sources, one for VDS and one for each VGS. The DC voltage sources are in the "Voltage_Sources" directory with the name 'vdc.' Remember to save your design. More information about adding the six DC voltage sources are in the next step. The first one should be added with the windows shown below.



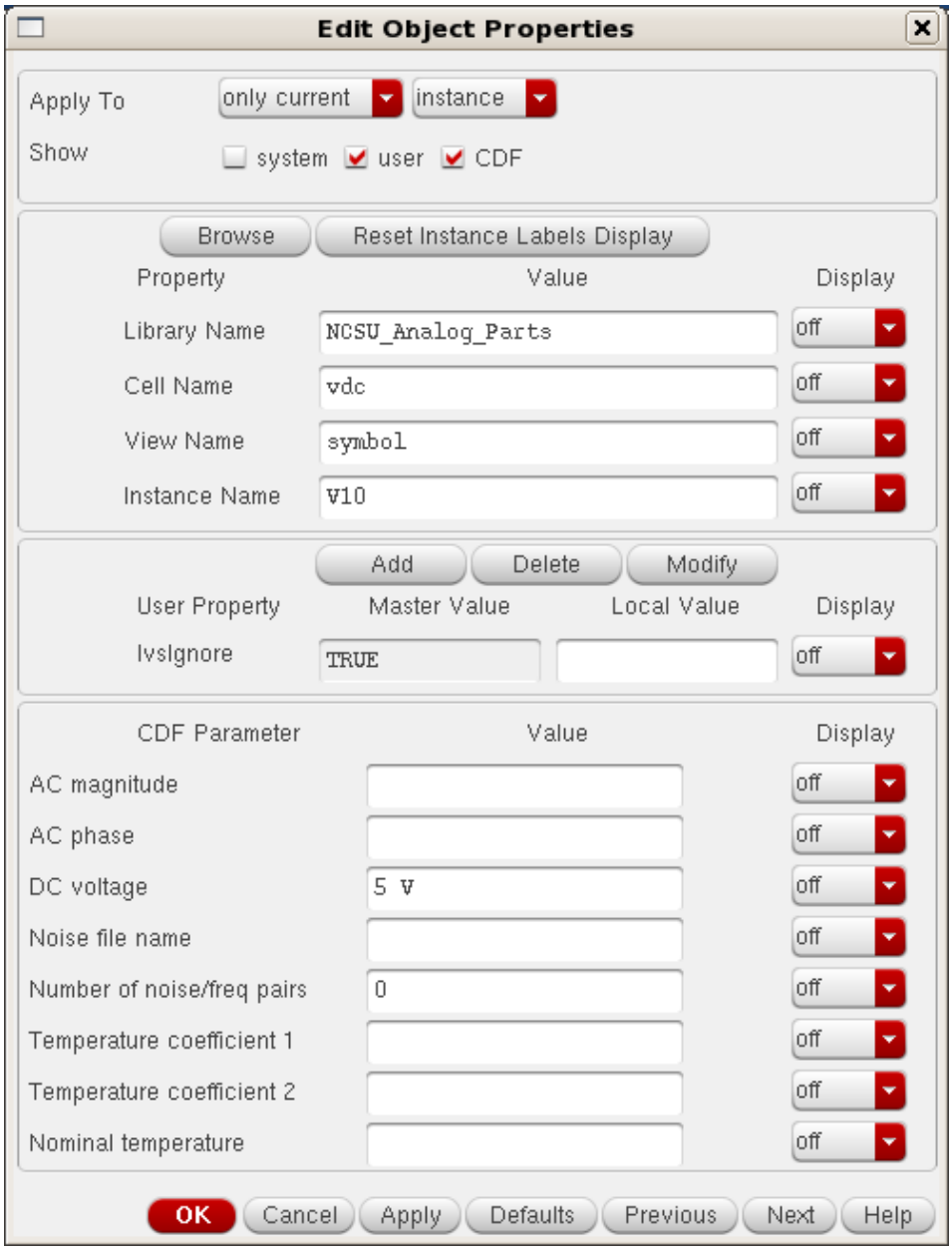
Integrated Circuit Design CAD Tool Information



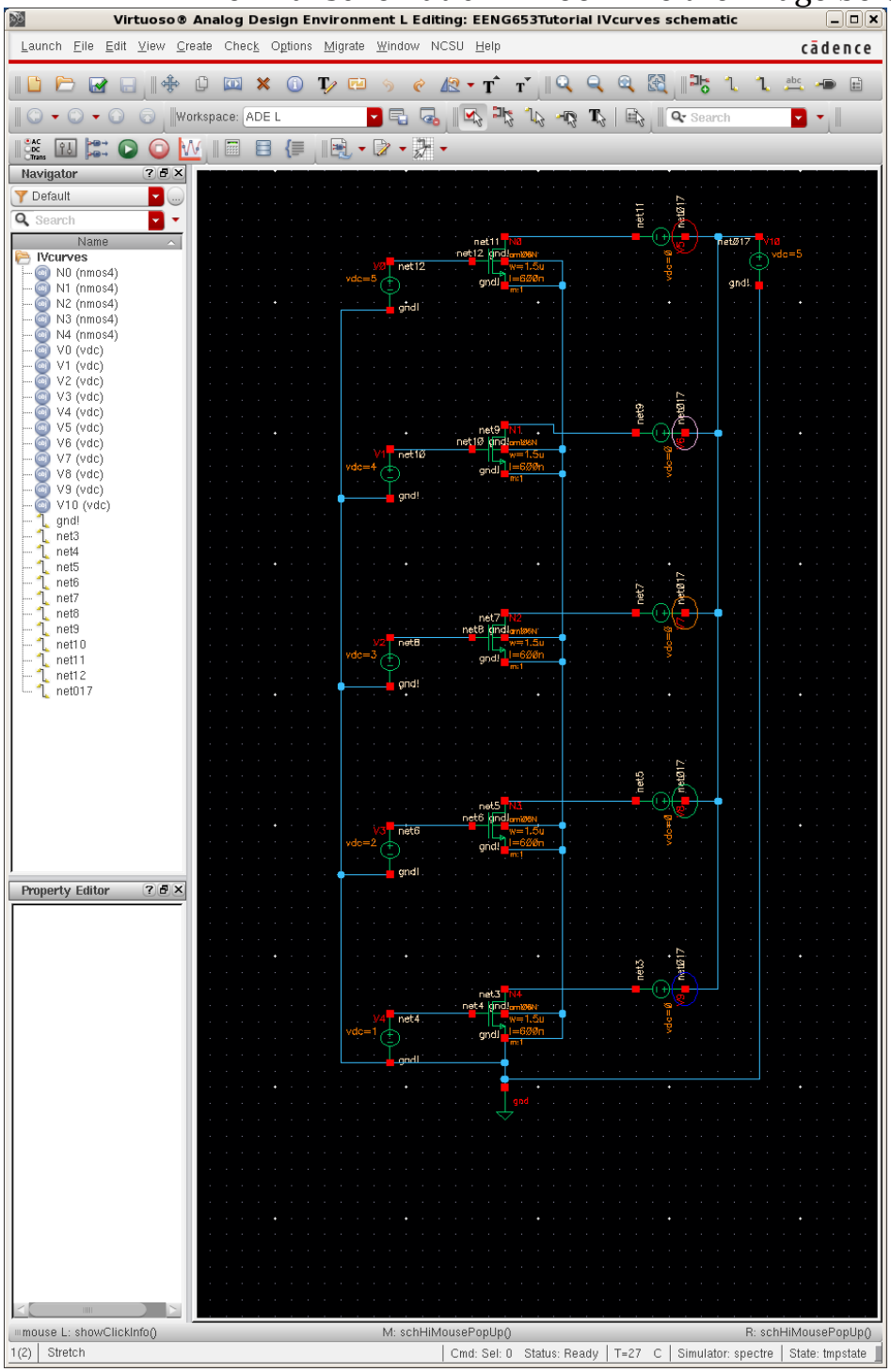
l. Now connect the DC voltage sources with wires to the transistors. As you place each vdc source (you can place them one after the other, no need to click on 'instance' in between), change the VGS power supplies to be 5 V, 4 V, 3 V, 2 V, and 1 V respectively, by inserting the appropriate value for the DC voltage property. The form on the previous page has 5 V inserted, for example, in the "DC voltage" field.

m. You now need to add five more 'dummy' voltage sources (each with a value of 0 V) so that you can plot the current in each transistor (it seems from existing tutorials that there is a bug with the transistor models right now, and the transistor currents cannot be plotted directly). Add the five 'dummy' '0 V' sources in series with the drains, and a voltage source vdc of '5 V' for VDS. Press the ESC key to exit from the 'Add Instance' mode. In case you make a mistake, you can perform 'Edit → Undo', or you can correct the mistake by some form of editing. For example, if you typed the wrong value for the DC voltage source for 'vdc', you can change the value later by first selecting the instance (click on it in the schematic) and then type 'q' (or "Edit → Properties → Objects"). Then, a pop-up window will appear where you can change the field, as shown in the image below.

Integrated Circuit Design CAD Tool Information



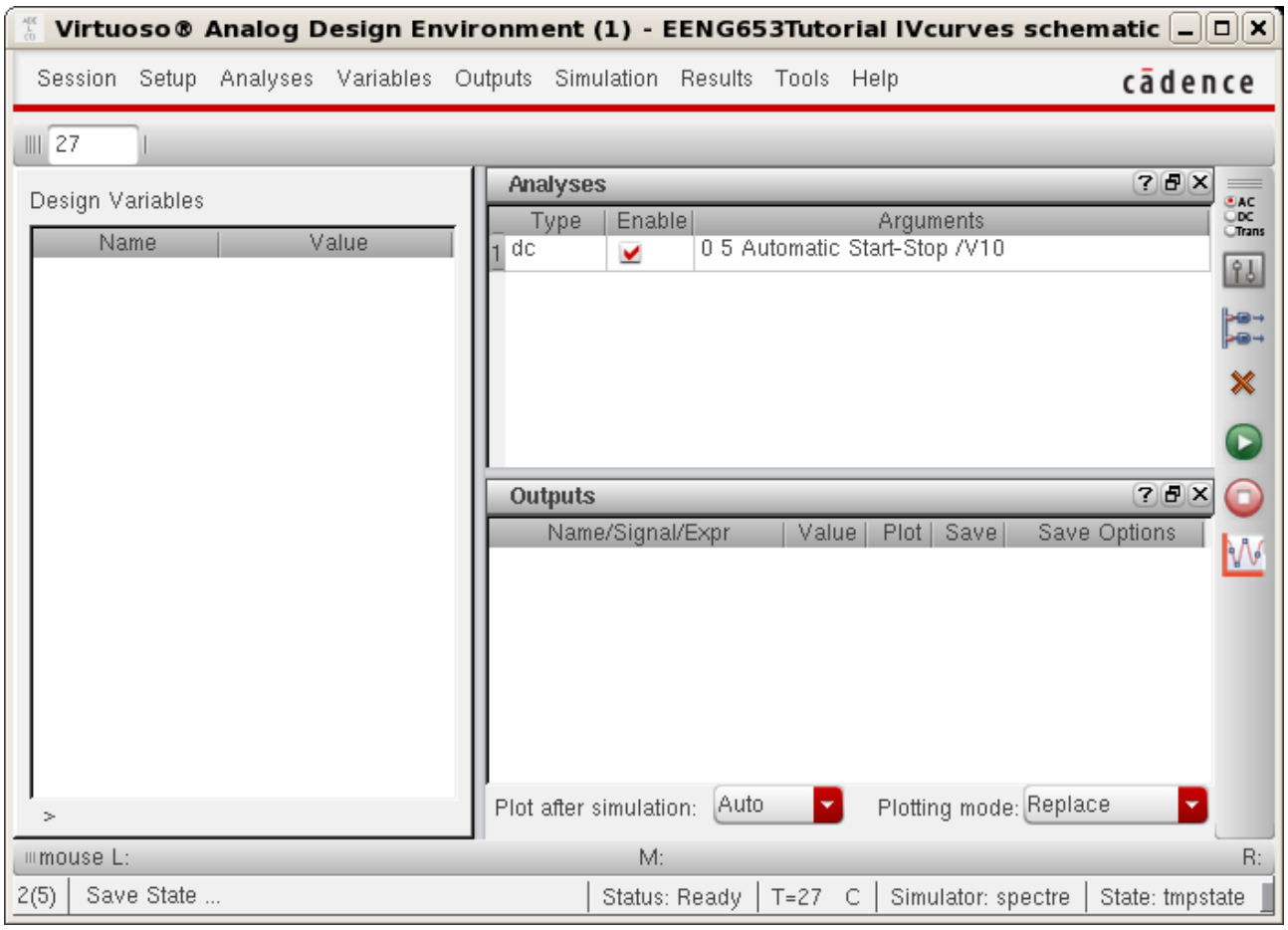
n. The final schematic will look like the image below.



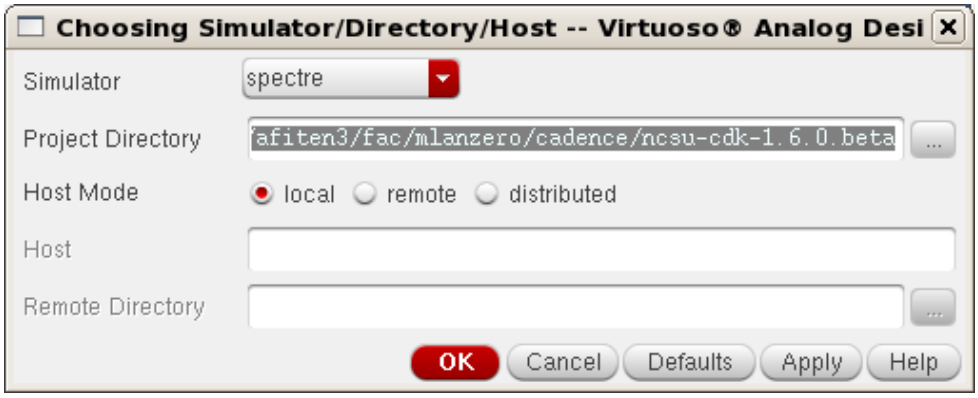
o. Now you need to check and save your design. In the Schematic window, select "File → Check & Save." Make sure to read the log file reported in the CIW window to be sure that Check & Save completed with no errors. There should be no errors and no warnings. If there are any errors and/or any warnings, you will need to fix them in the schematic. After fixing any errors and/or warnings, you will need to Check & Save the schematic again. You will need to Check & Save the schematic each time you make changes to the schematic.

p. Assuming there are no errors, and that the design passed Check & Save, you can now proceed to the simulation step.

q. In the Virtuoso Schematic window, click on "Launch → ADE L" to launch the Virtuoso Analog Design Environment window as shown in the image below.

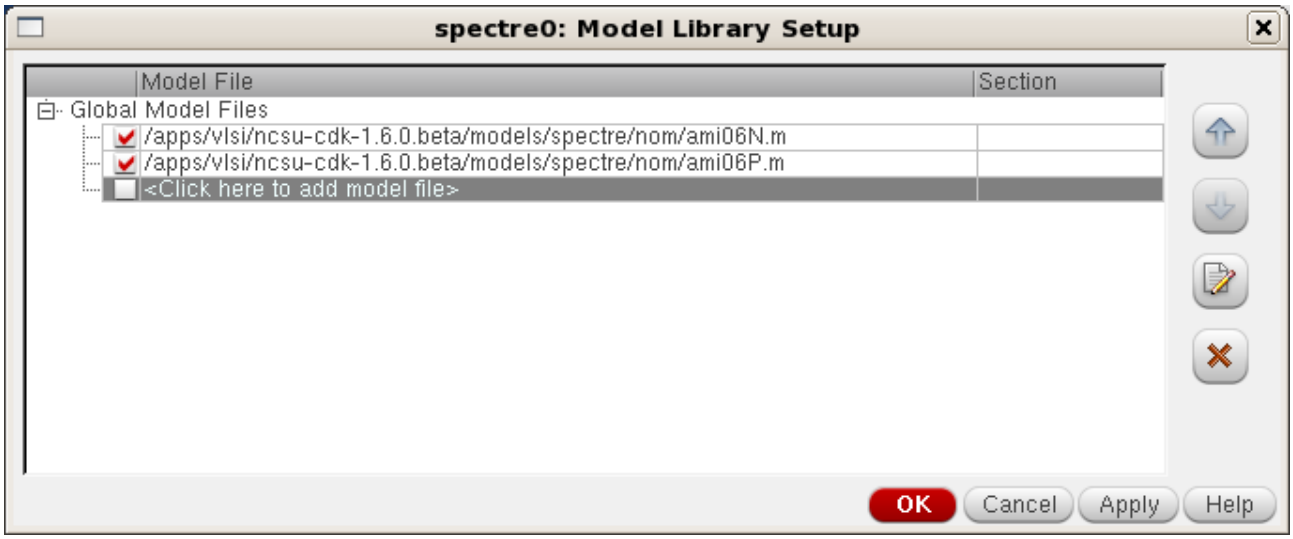


r. First you need to choose the simulator. In the Analog Design Environment window, select "Setup → Simulator/Directory/Host" and the window below will appear. This window is "Choosing Simulator/Directory/Host" window. Choose 'spectre' in the Simulator pull-down menu and then click OK.

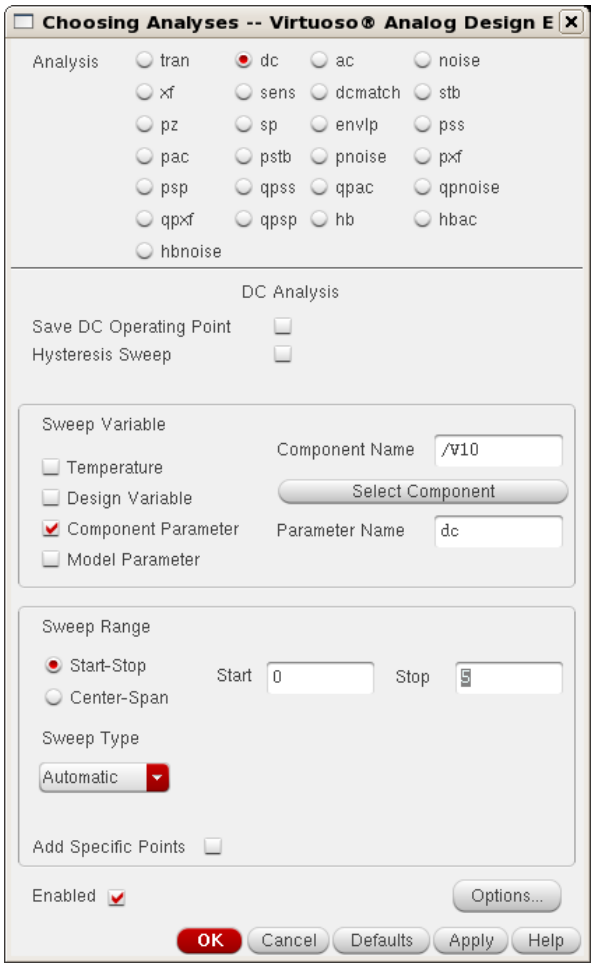


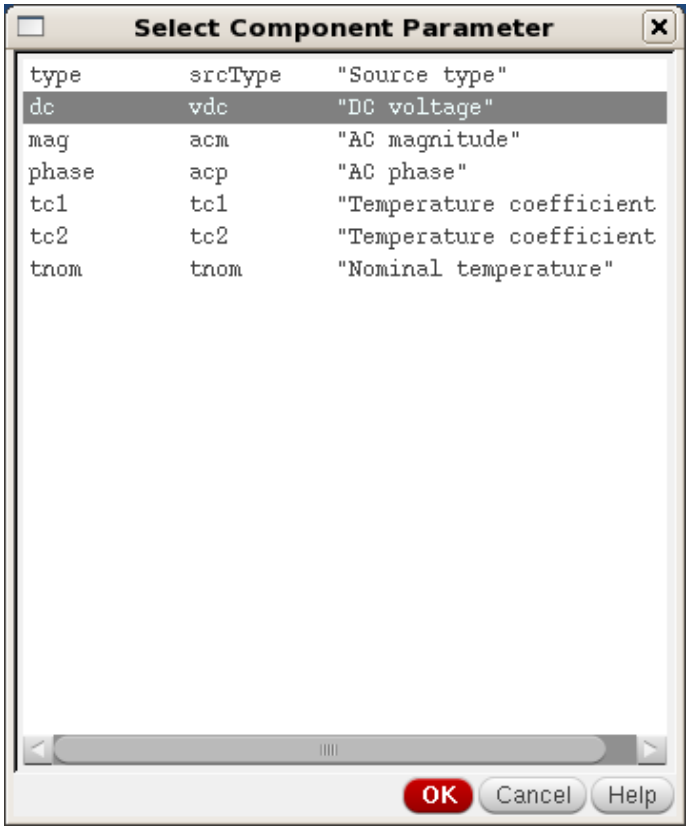
s. Next you will choose model libraries. Click on the Virtuoso Analog Design Environment window and select "Setup → Model Libraries." Select the following paths in the "spectre0: Model Library Setup" window. These are the paths to the model for the NMOS device and the PMOS device:

i. /apps/vlsi/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06N.m
ii. /apps/vlsi/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06P.m
iii. Then click OK.



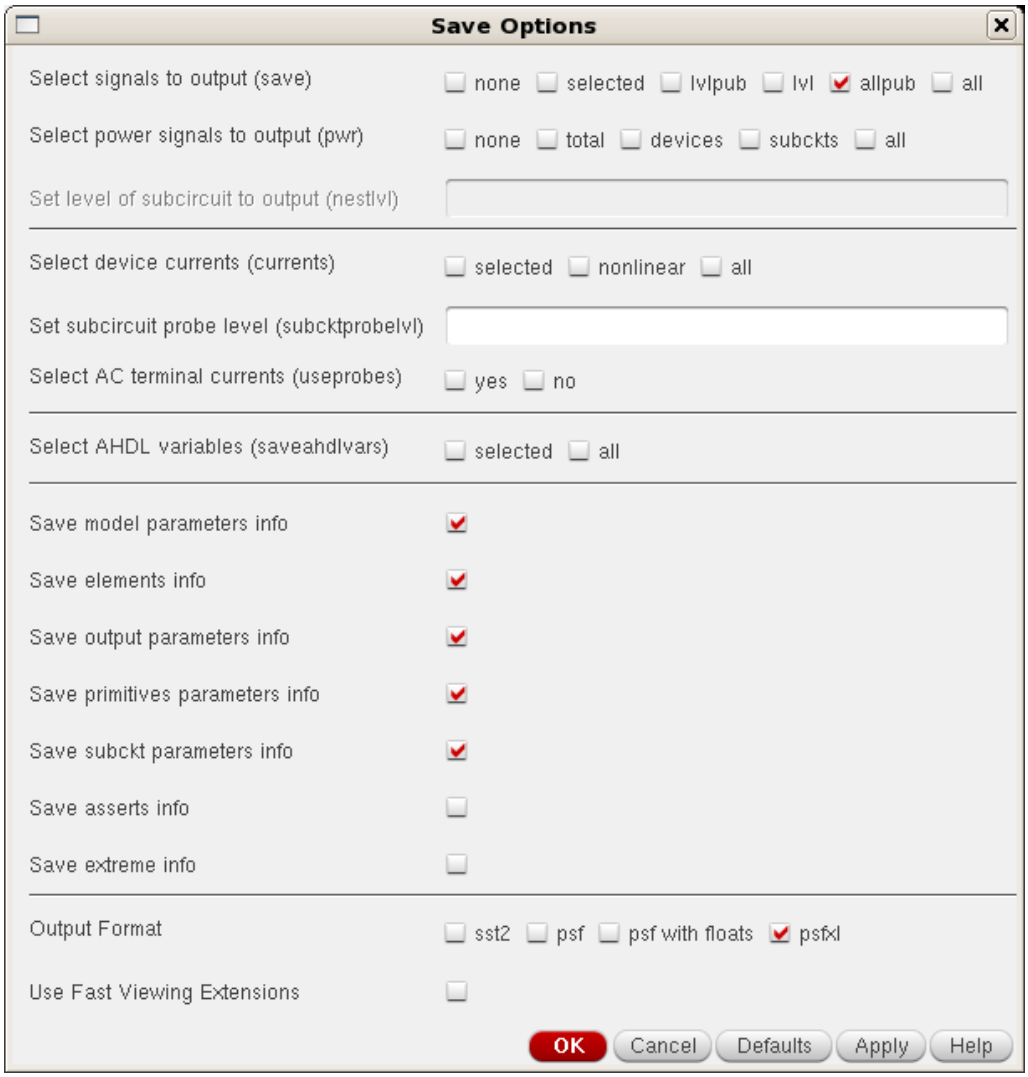
t. Now you will choose the type of simulation. Click on the Virtuoso Analog Design Environment window. Select "Analyses → Choose" and the window below will appear. This is the "Choosing Analyses" window. You are doing a DC sweep, so click on the 'dc' radio button, and then click on 'Component Parameter' check-box. Then click on the VDS component in the Schematic window and choose dc in the Select Component Parameter pop-up window and click 'OK'.





u. Then, back in the "Choosing Analyses" window, set Start to '0' and set Stop to '5'. Set the 'Sweep Type' to 'Automatic.' Setting the sweep type to automatic will do a dc sweep of VDS from 0 V to 5 V. Then click 'OK' in the "Choosing Analyses" window.

v. Click on the "Virtuoso Analog Design Environment" window. Select "Outputs → Save All" which will bring up the 'Save Options' form shown below. In this form, select 'allpub' for signals to save (the default). In general, you will want to save only a subset of signals so that you save computing resources, but this schematic is small enough that it is OK to save all the signals. Click "OK" in the 'Save Options" form.



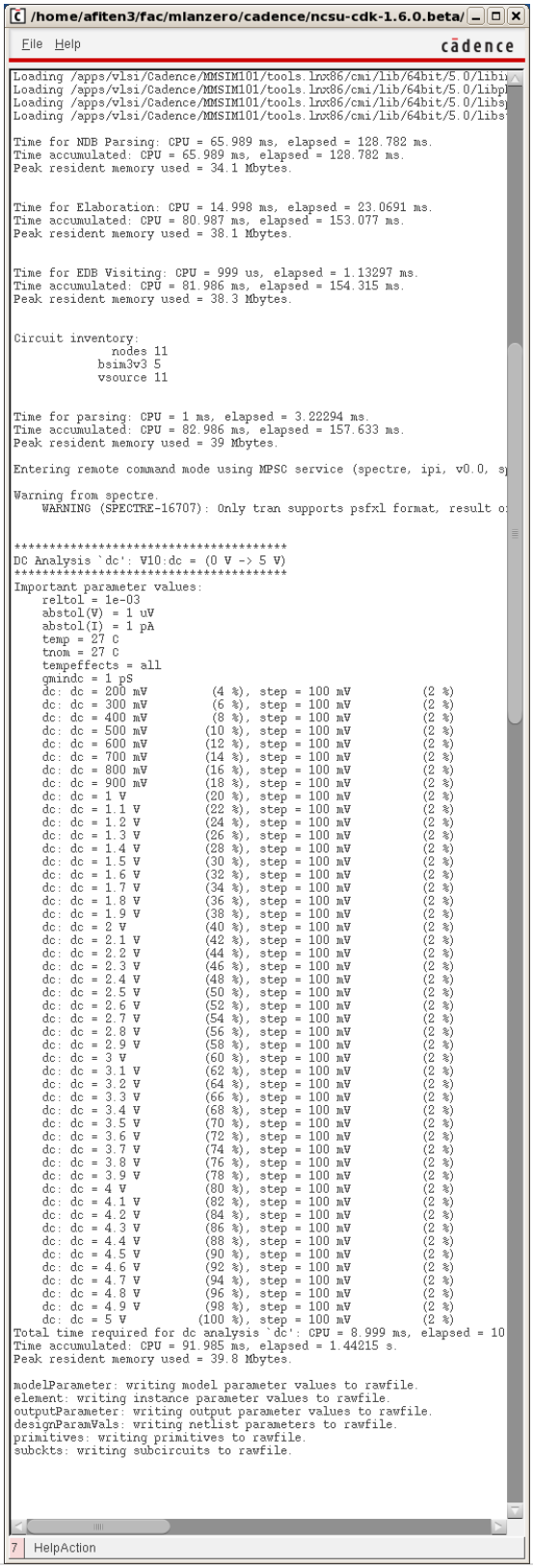
w. Now you are ready to simulate your schematic. In the "Virtuoso Analog Design Environment" window, click on "Simulation → Netlist → Create raw" to create the netlist.

x. Now you are ready to run the simulation. Click on the "Virtuoso Analog Design Environment" window. Click on "Simulation → Run." The CIW reports a successful simulation, and the file below will appear. This file will appear in the case that there are no errors.

In case you have errors, you will need to go back and correct them. This process can be tricky. You may need to do to "Simulation → Netlist" and "Simulation → Run" each time you change the schematic.

Note: Each time you change the schematic, you will need to do a Check & Save.

Integrated Circuit Design CAD Tool Information



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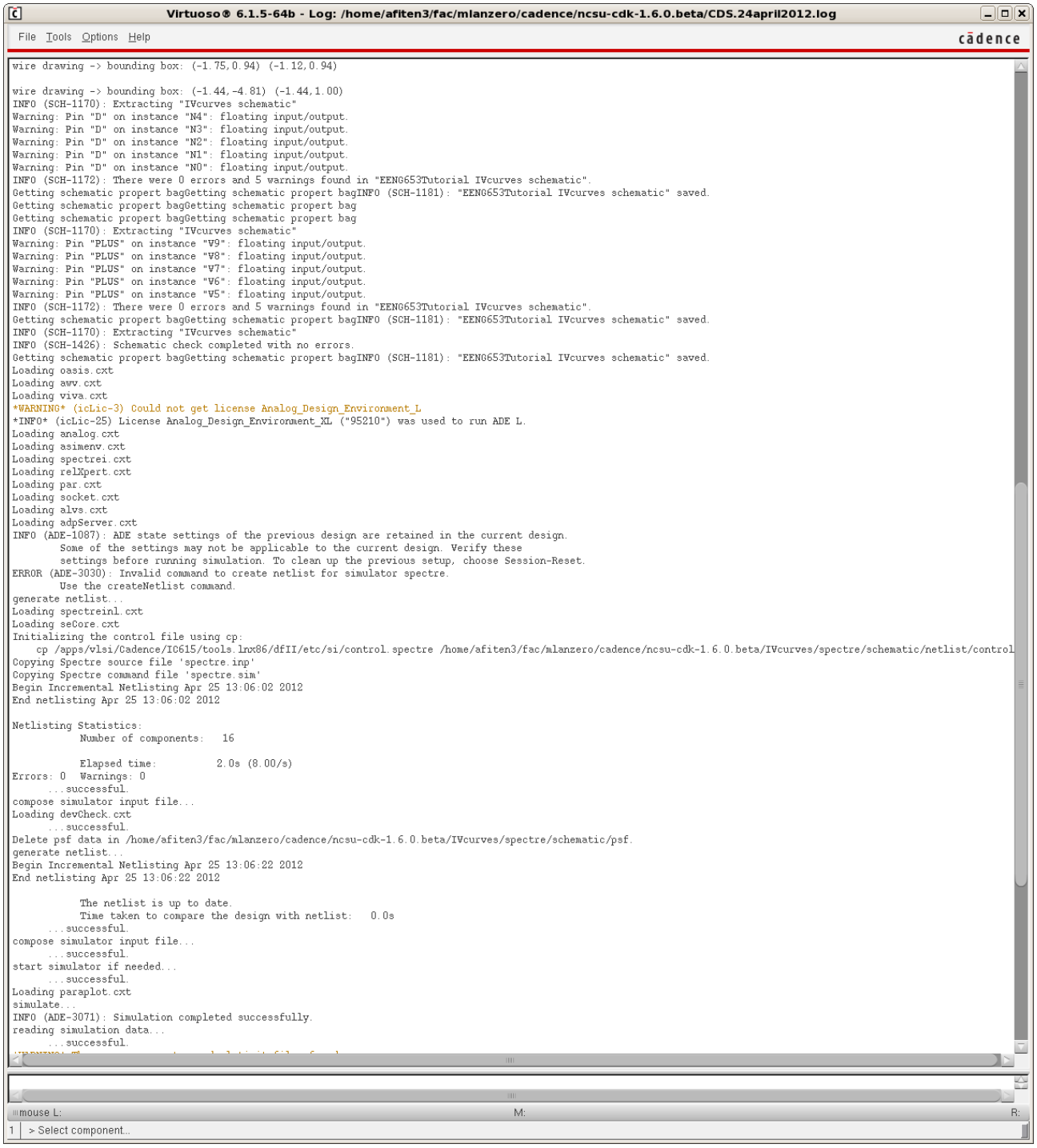

y. If there are no errors in the simulation, you are now able to plot the simulation results. Click on the "Virtuoso Analog Design Environment" window. Select "Results → Direct Plot → DC" which will pop-up your schematic window. Now you have to click on the signals that you want to see. Since this is a DC-sweep, you want to see the drain currents into the five transistors. In order to see these, you have to click on the small red square at "+" terminal of each of the dummy power supplies in series with each drain. Make sure you click on the red square (the pin) which means current, versus any other part which means net, or voltage. Click on all five (5) power supplies. If you are clicking correctly on the pins, a circle (in color) should appear around each chosen pin as shown in the figure below. Note that the circle around each pin will be a different color.

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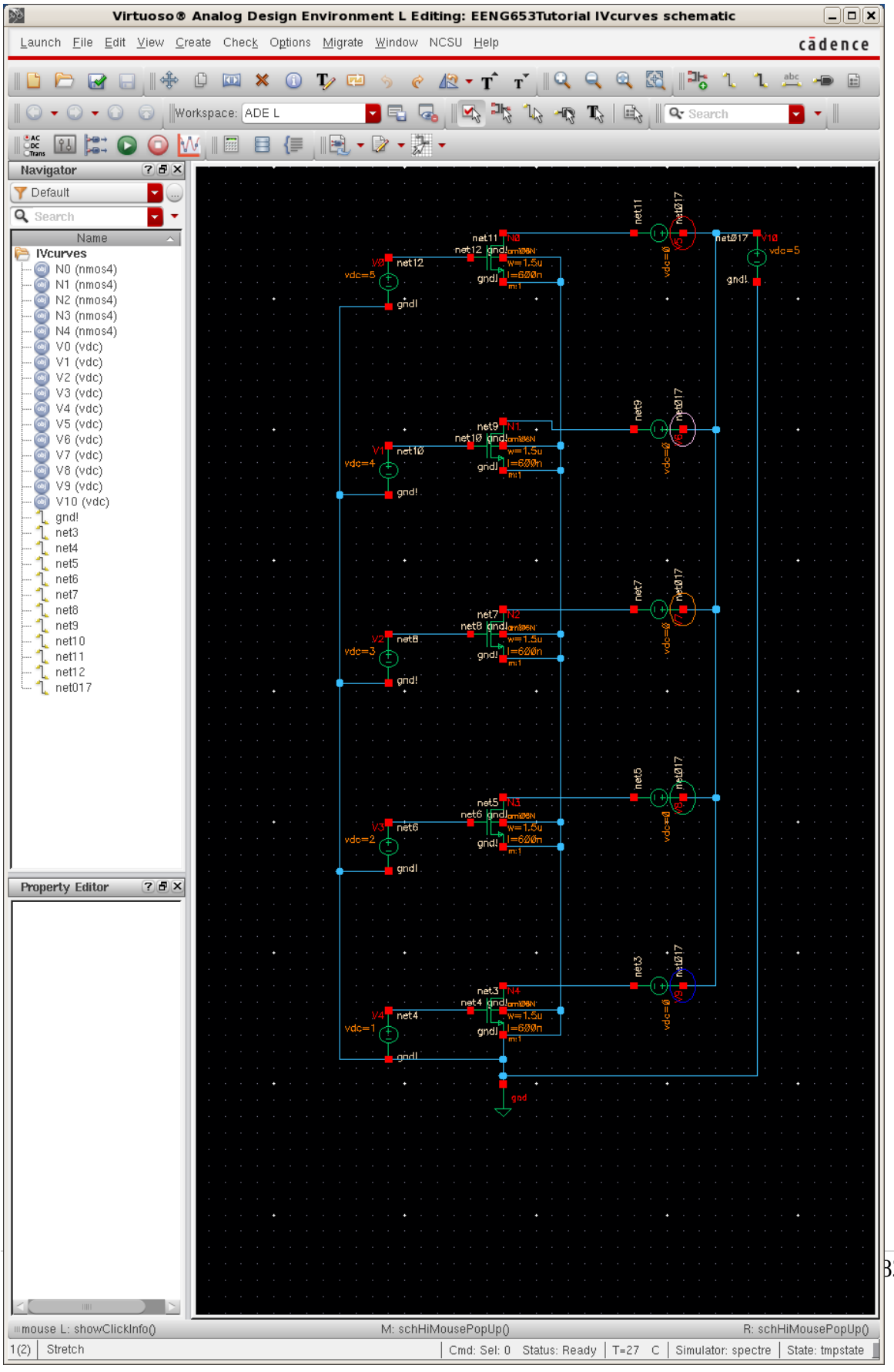
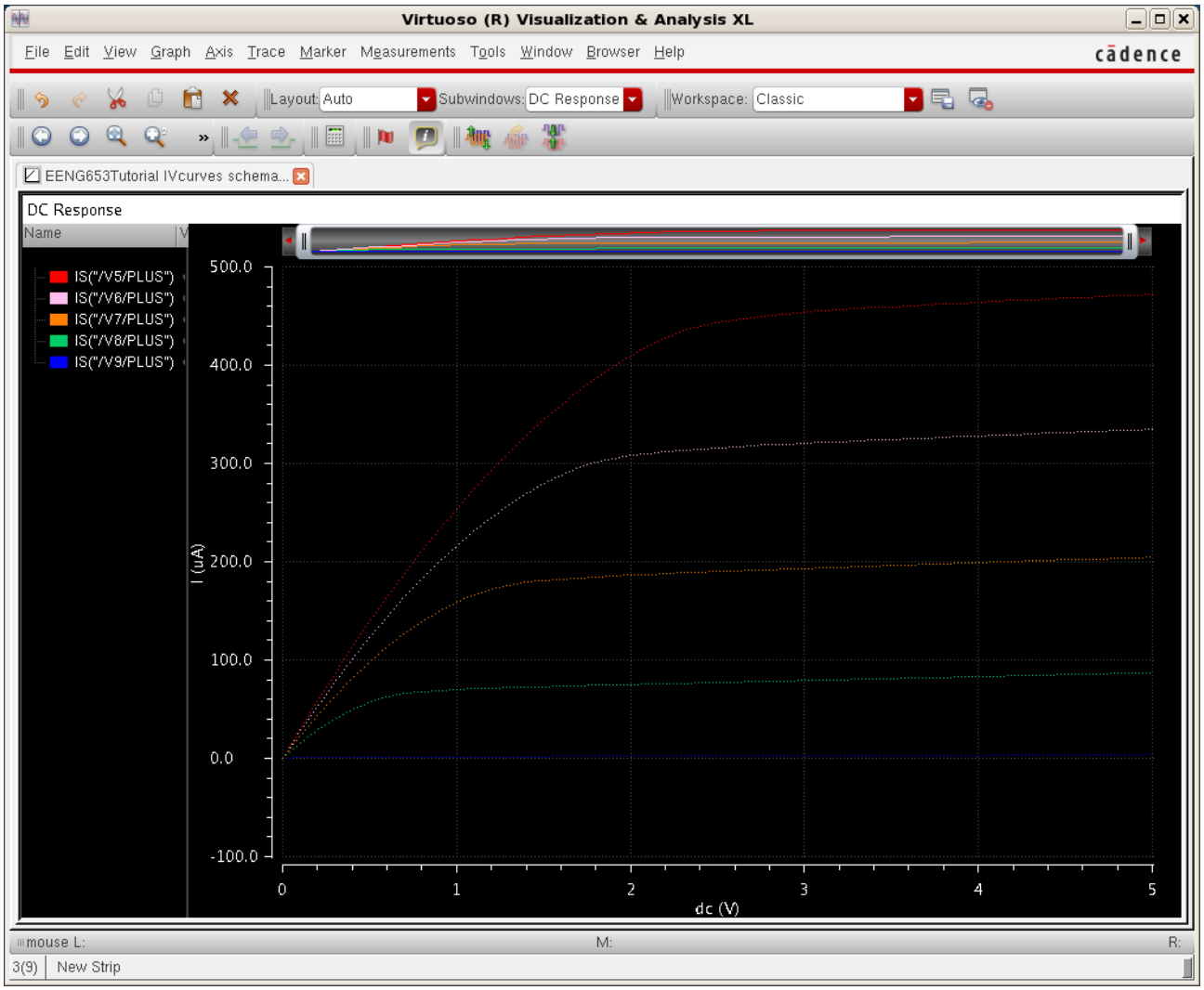
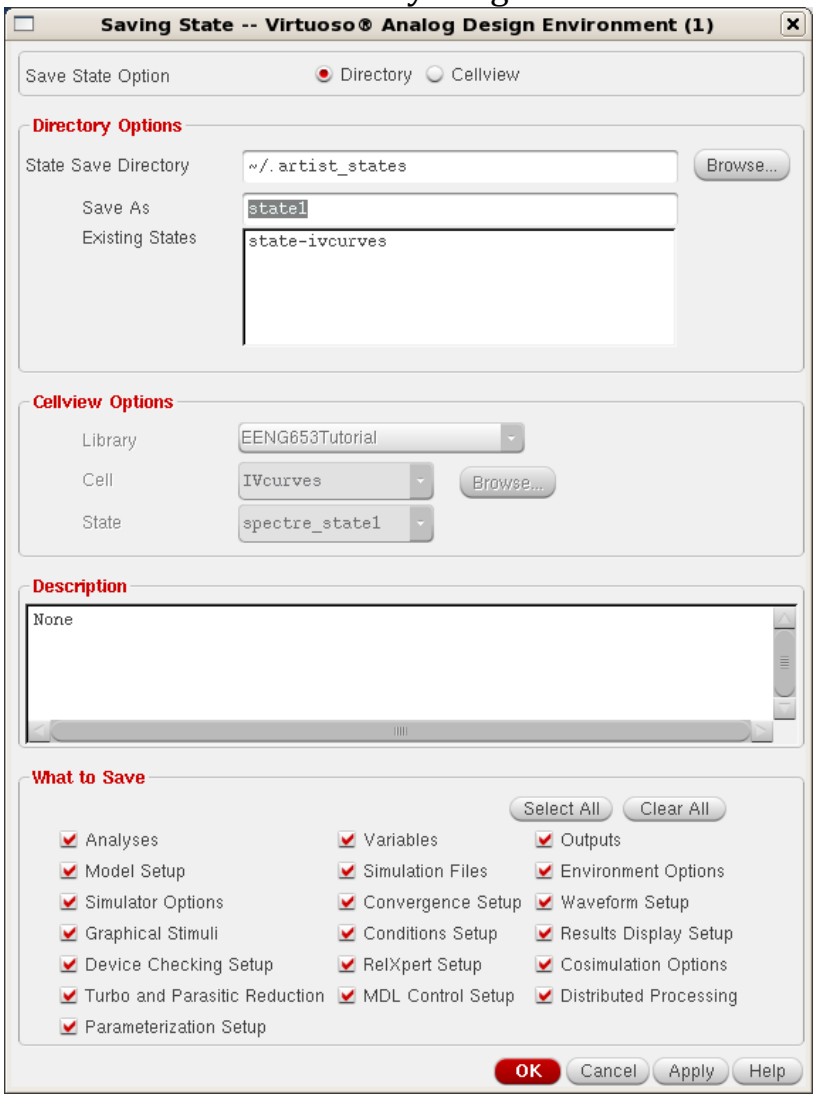


z. Now you can press on the 'ESC' key to finish choosing the signals. You should finally get the desired simulation results, five IV-curves.



aa. It is a good idea to save the state of your simulation before you exit the simulation window. You can save the state of your simulation by clicking on the "Virtuoso Analog Design Environment" window. Then click on "Session → Save state" which will bring up the "Saving State" window shown in the image below. This will be helpful if you want to redo any of the simulations without having to re-enter everything from scratch.



bb. You have now saved the state of your simulation of five IV-curves.

22. nFET: Parametric Simulation of I-V Curves (nFET)

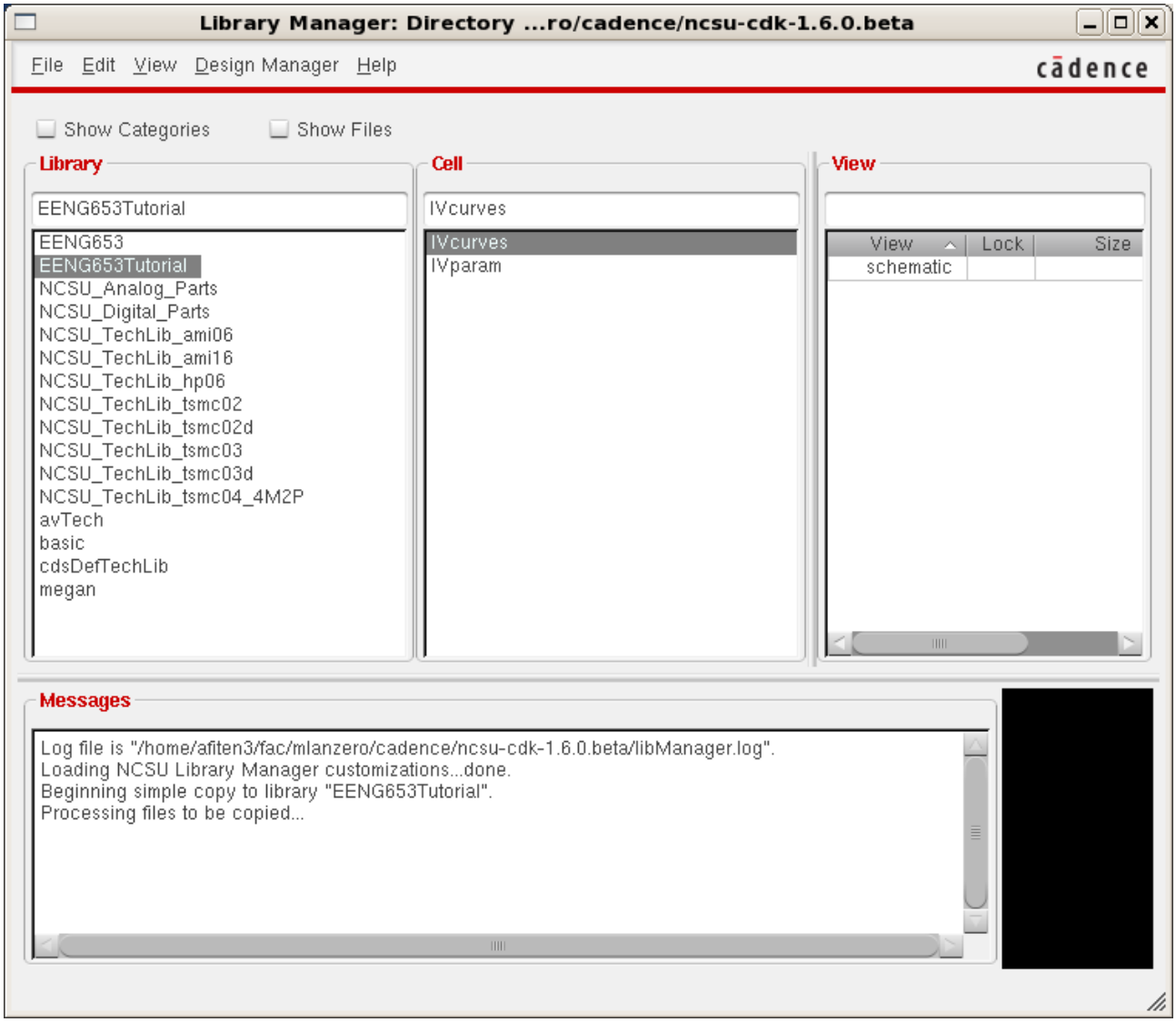
a. You will now learn another way to perform the same type of simulation as in the previous section. The idea behind this section is to show another choice about how to achieve the same result within the Cadence Design tool framework. To review, in the previous section, you used multiple devices (five devices) to obtain the five IV curves. You are now going to achieve the same results (and expand to ten IV curves) by using a single transistor for which you will change the voltage VGS.

Close the Analog Environment and the IV curves schematic, now you will start another schematic that you will call "IVparam."

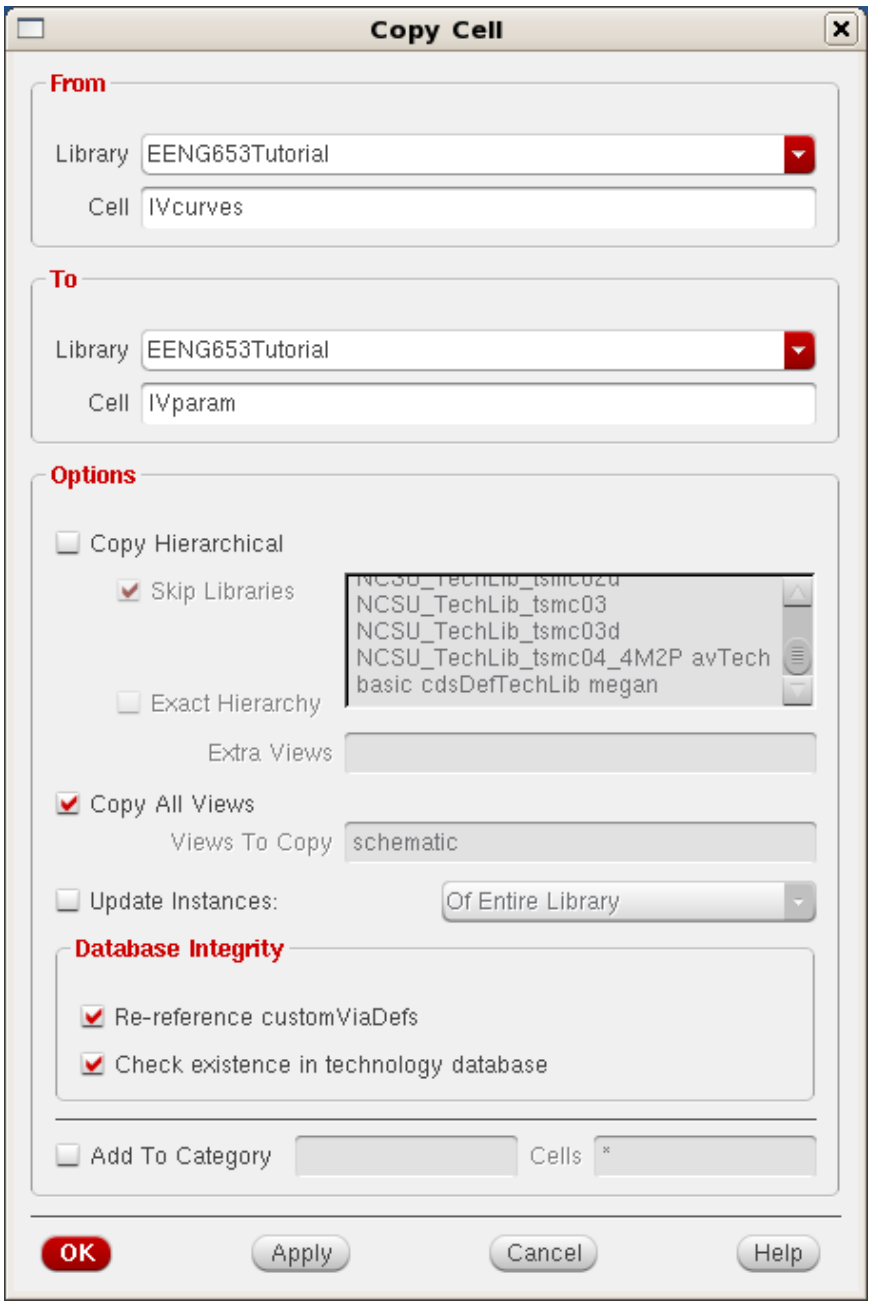
Instead of starting with a new schematic window, you will start from your IVcurves schematic that you made in the previous section.

Open the Library Manager as shown in the figure below. Click on the Library Manager window, and in the window, select the IVcurve cellView and choose "Copy."

Integrated Circuit Design CAD Tool Information



b. The "Copy Cell" window will appear as shown in the image below. Complete the "Copy Cell" window as shown with the name of the new cell as "IVparam."



c. After copying to the new cell "IVparam," click on the "IVparam" cell and then double-click on the schematic view of this cell. A schematic should appear which is identical to the "IVcurves" schematic that you made in the previous section. You are now going to delete the bottom four transistors and their connections, as well as the bottom four VGS and dummy power supplies. You may use "Edit → Delete," or clicking and using the mouse button to select regions of the schematic to delete, and then clicking the delete button. You may also click 'd' to delete.

Now you will change the value of the VGS power supply to "parameter" as shown in the figure below. Note that the value "parameter" will be a variable that you will set later in this section. For now, change the value to the word "parameter."

Finally, move the symbol for 'gnd' upwards in the schematic and reconnect it to the rest of the schematic, as shown in the image below.

Your final schematic should look like the image below.

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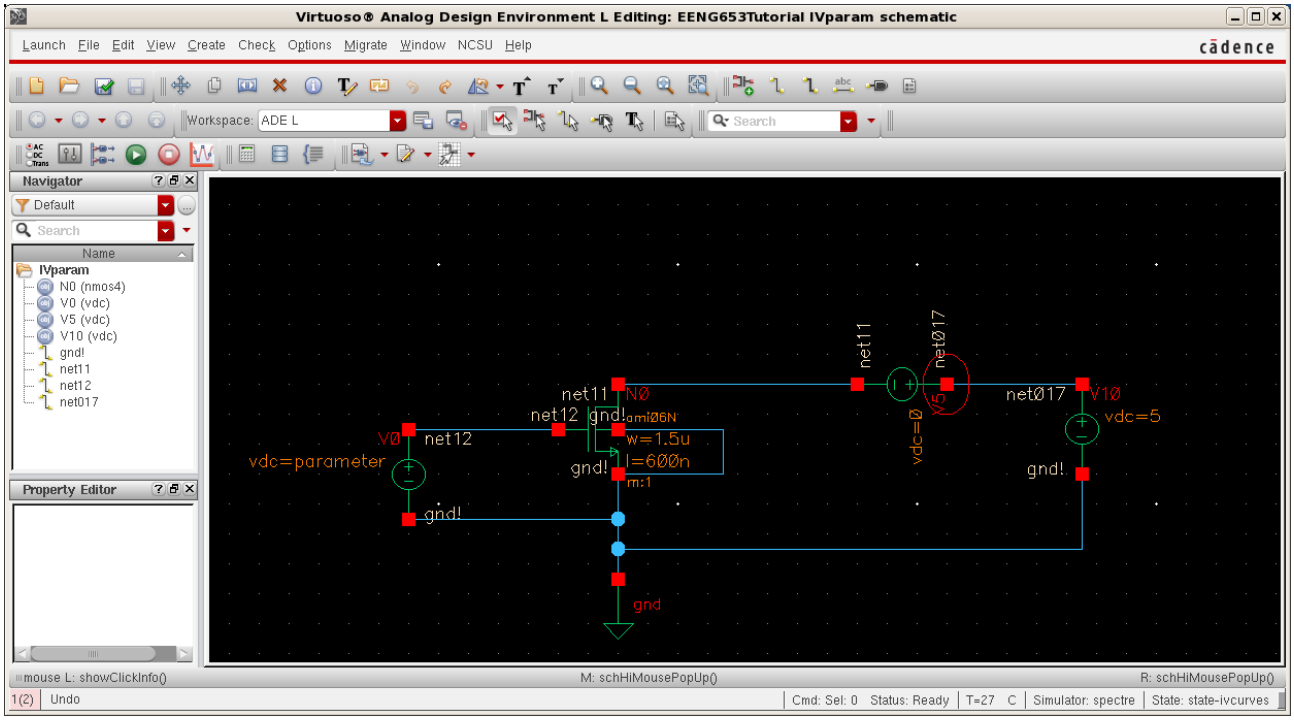
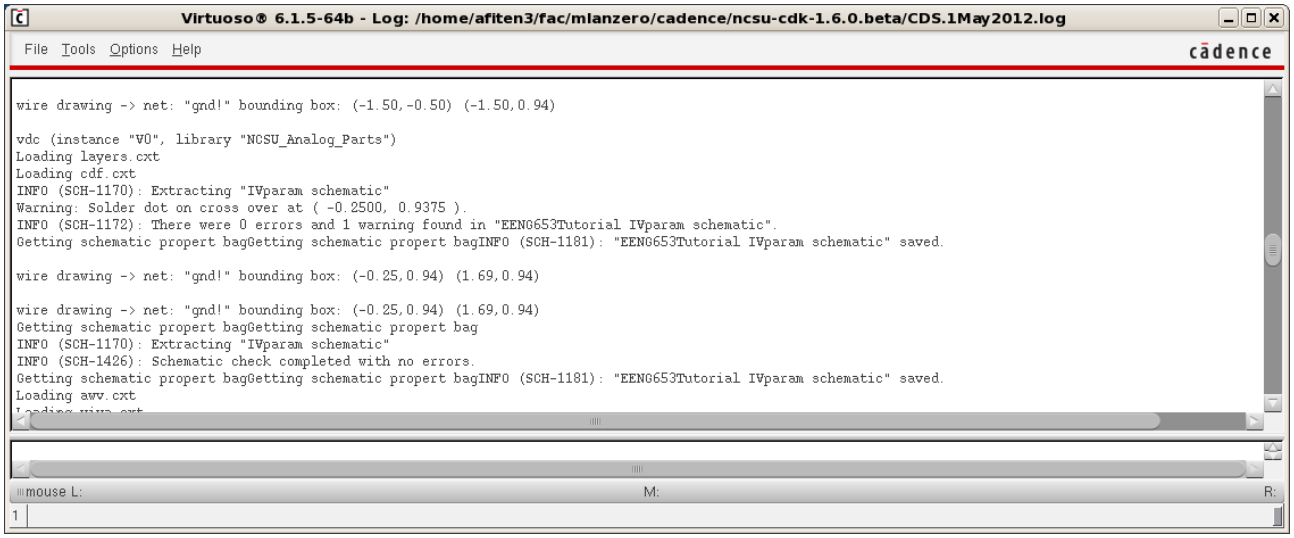
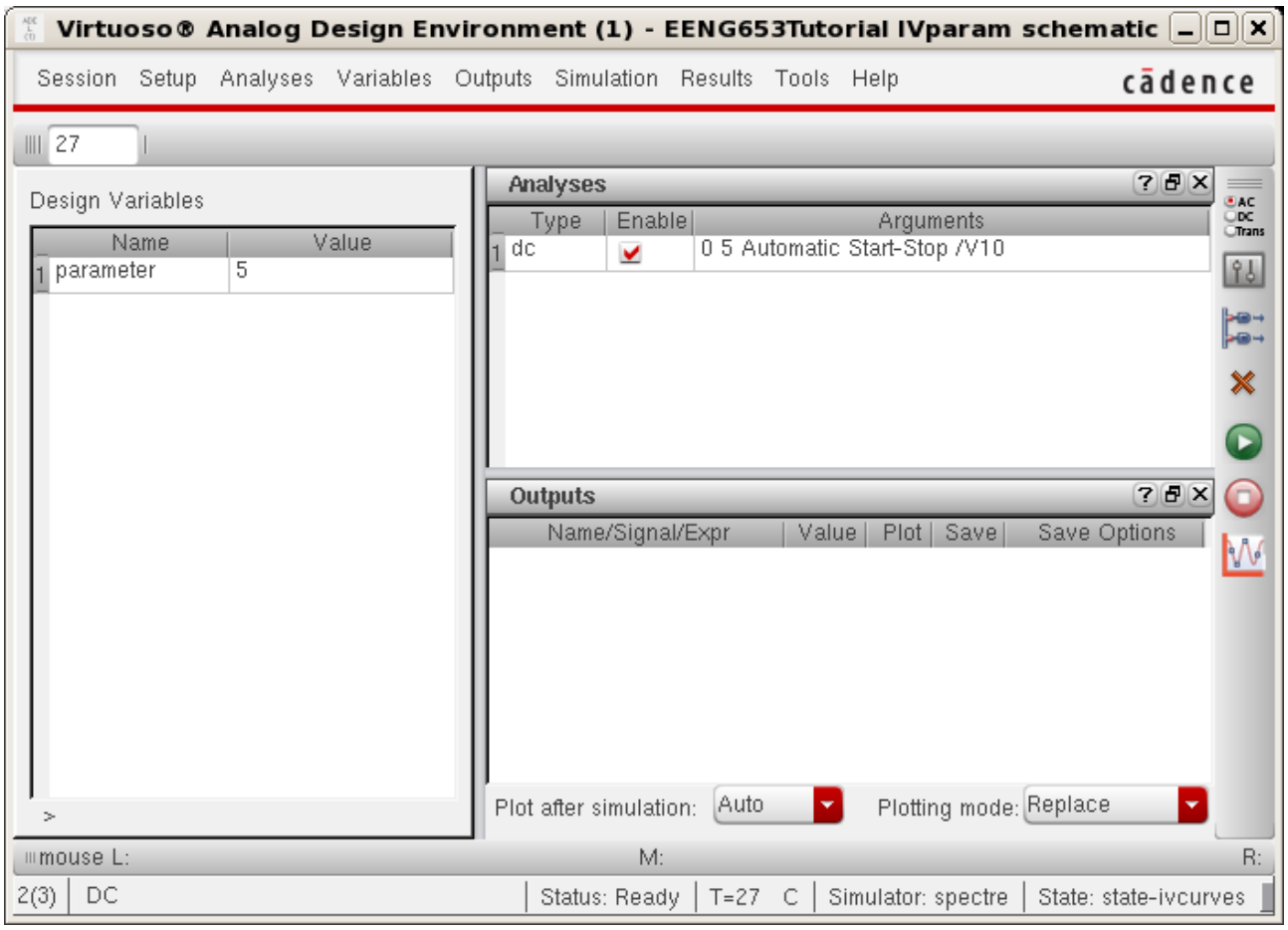


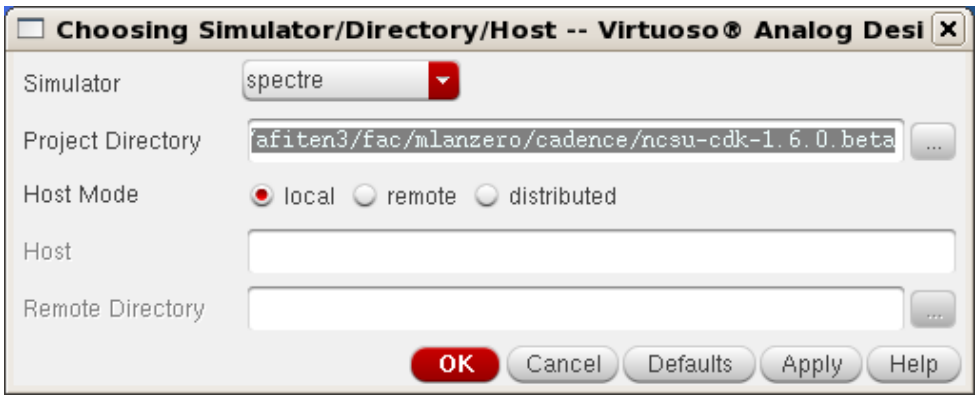
d. Remember to "Check & Save" your schematic. Look in the CIW to make sure that your schematic checks & saves without any errors.



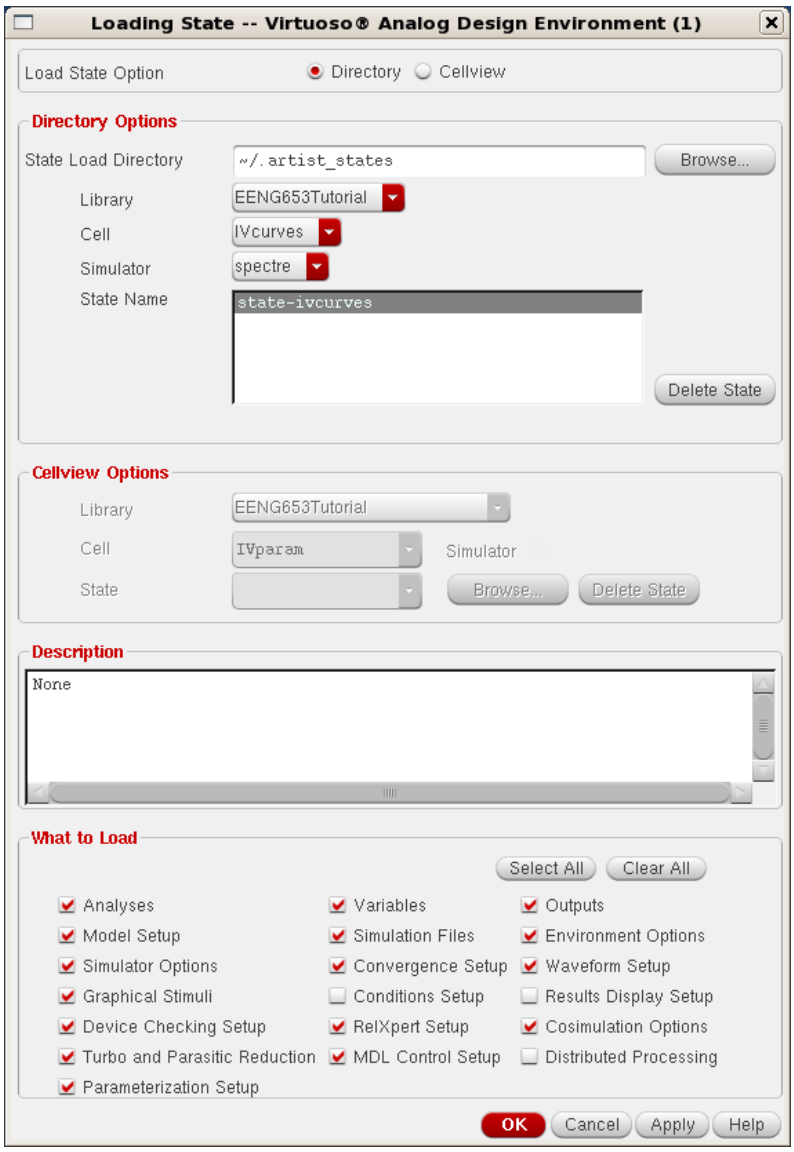
e. Now Click on the "IVparam" schematic and select "Launch → ADE L" to bring up the Analog Design Environment window as shown below.



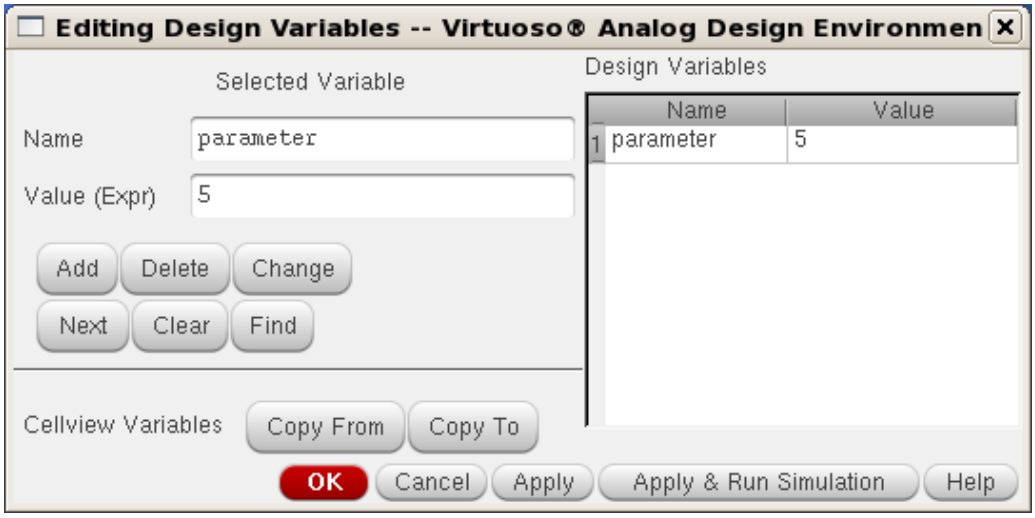
f. In the Analog Design Environment window, select "Setup → Simulator/Directory/Host" and choose Spectre as your simulator. Select "OK."



g. Now you will load the state that you saved in the previous session. In the Analog Design Environment window, select "Session → Load State" which brings up the "Loading State" window shown below. Select "IVcurves" as your cell and select the state name that you saved in the previous section as shown.

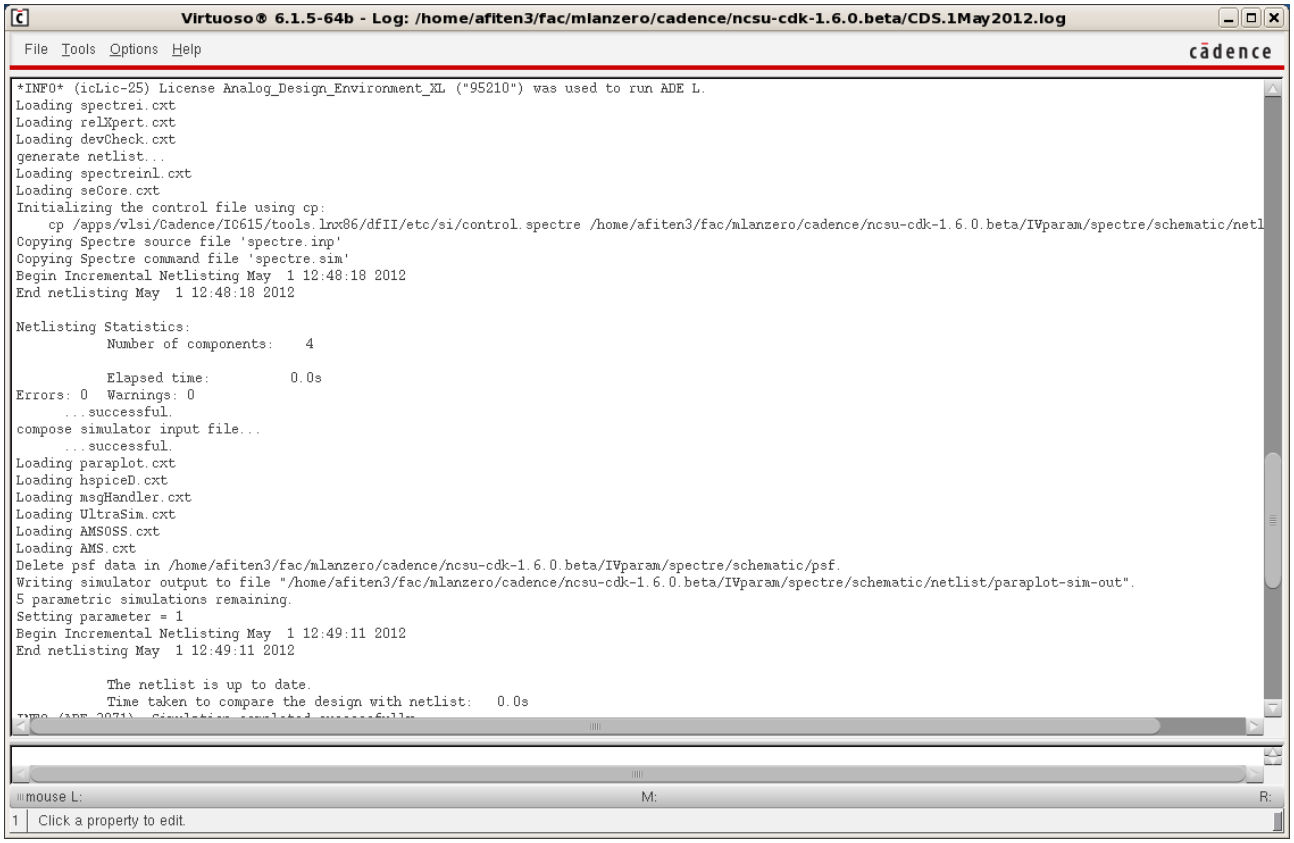


h. Now you will edit the design variable "parameter" that you set in your "IVcurves" schematic. Click first on the Virtuoso Analog Design Environment window. Then click on "Variables → Edit" which will bring up the "Editing Design Variables" window shown below. In this window, set "Name" to "parameter" and "Value" to "5." Click on "Add" that will move the word "parameter" to the right-hand side of the form under the "Name" column and will move the value '5' to the right-hand side under the "Value" column.

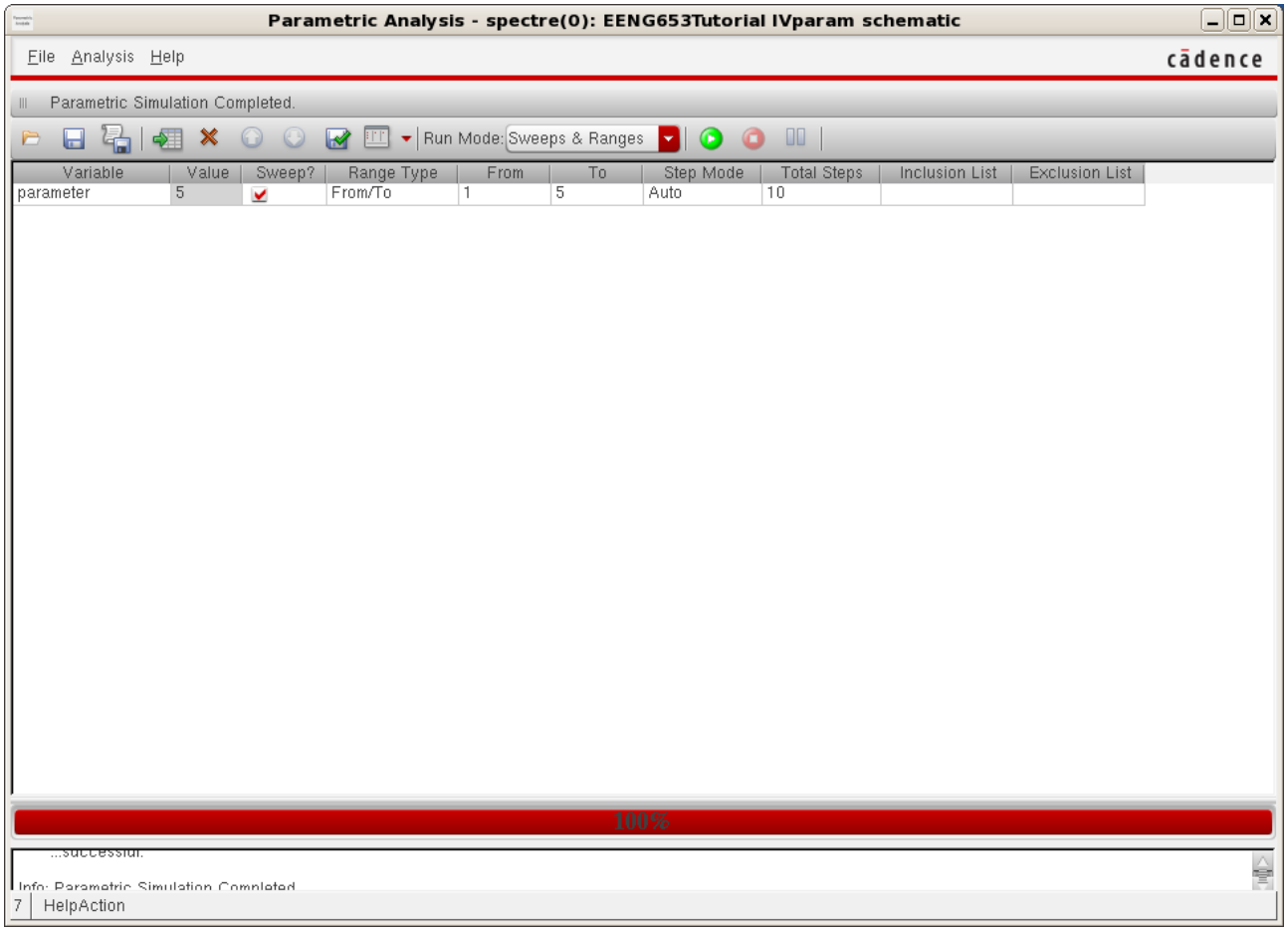


i. Now you can netlist your "IVcurves" schematic. Click on the Virtuoso Analog Design Environment window. Select "Simulation →Netlist → Create Raw" which will netlist your schematic as shown in the image below.

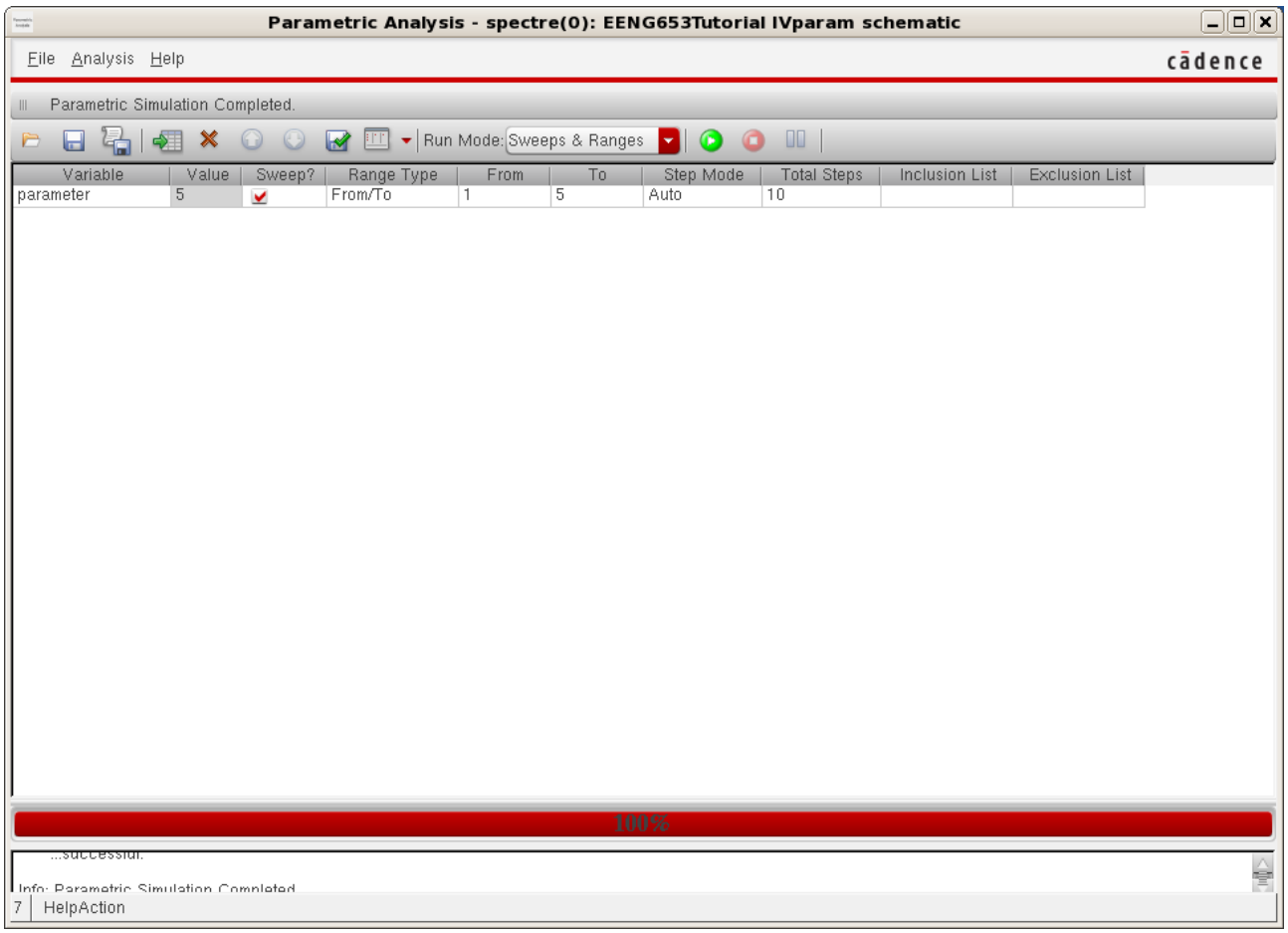
j. Inspect the CIW to make sure that your netlist was created OK.



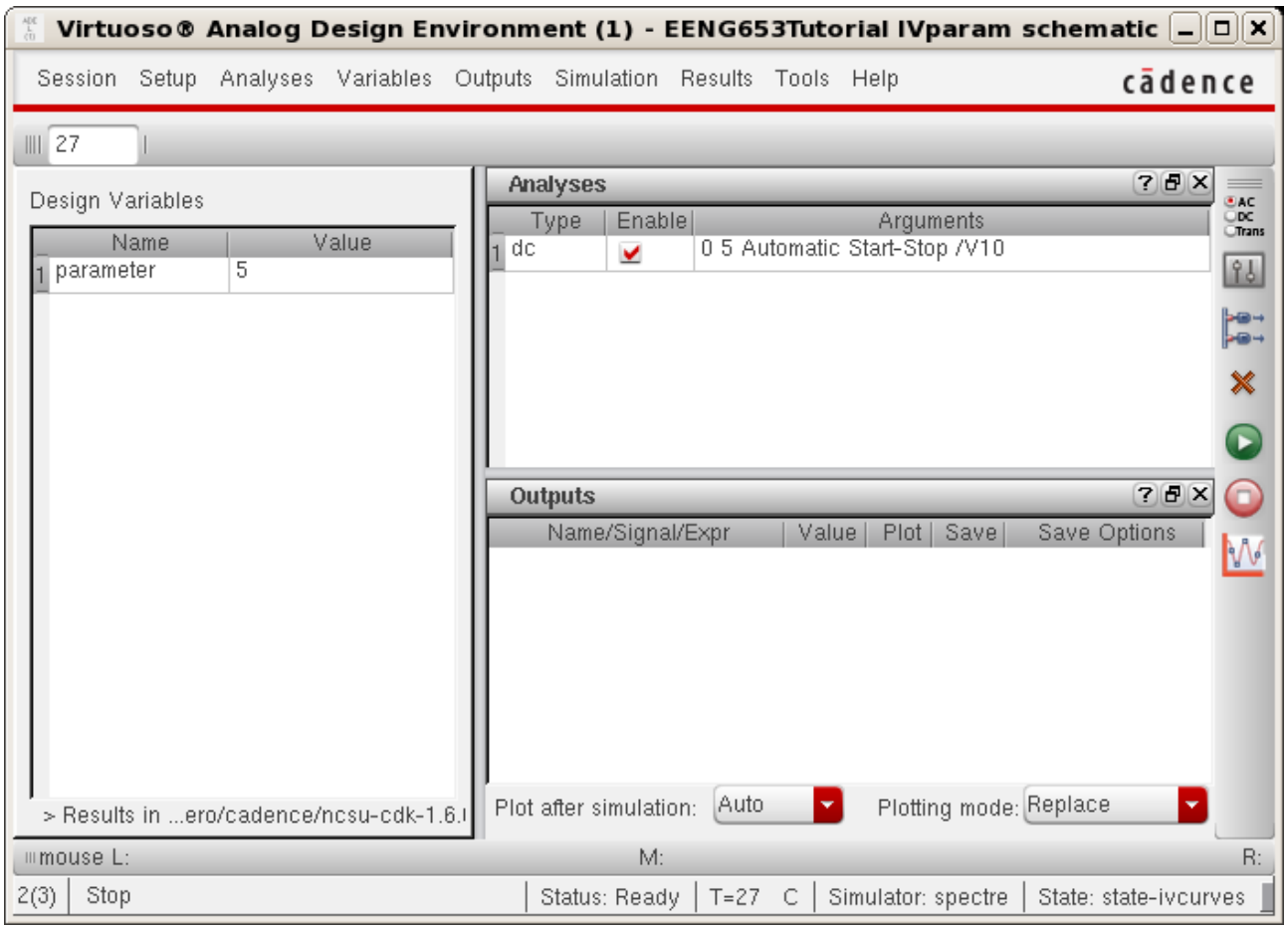
k. Now you will set up the parametric simulation. Click on the Virtuoso Analog Design Environment window. In this window, select "Tools → Parametric Analysis," and the "Parametric Analysis" window will appear as shown below. In this window, set "Variable" to 'parameter', "Value" to '5', "From" to '1', "To" to '5', and "Total Steps" to '10'. The value of '10' will give you 10 IV-curves with one parametric simulation (To duplicate the results of the previous section, set "Total Steps" to '5'). Here, 10 is suggested so you can see the ease with which multiple simulations can be performed.



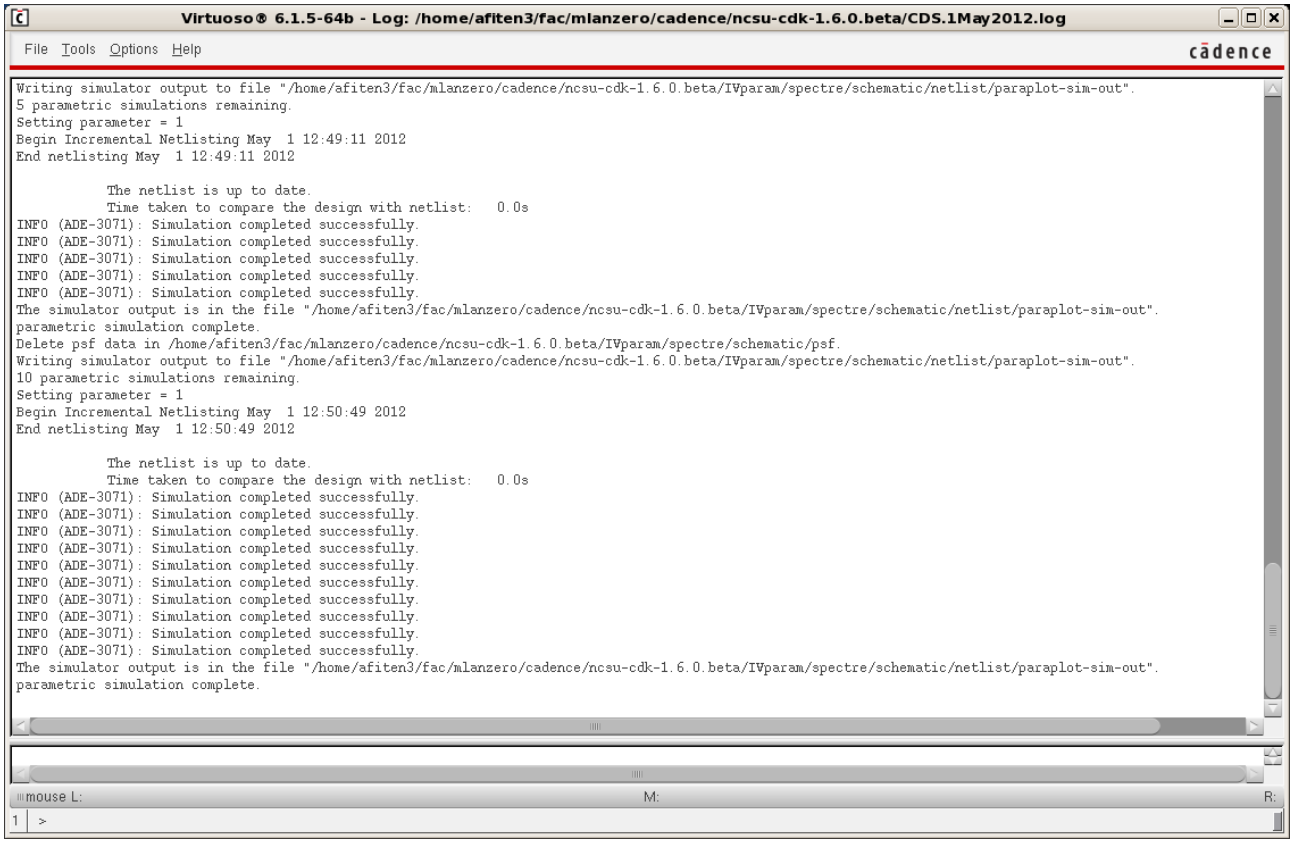
l. Now you will perform the parametric simulation. Click on the "Parametric Analysis" window. Select "Analysis → Start All." The window will appear as shown in the image below.



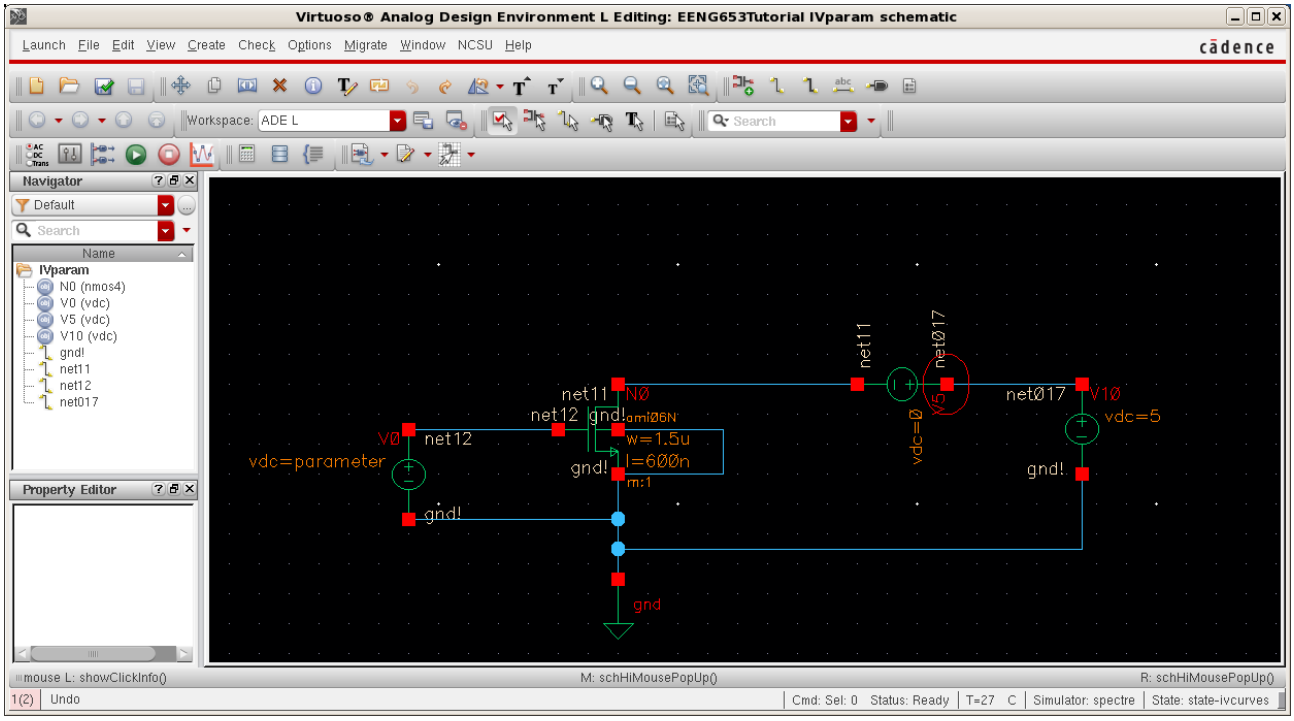
m. The Virtuoso Analog Design Environment will look like the image below.



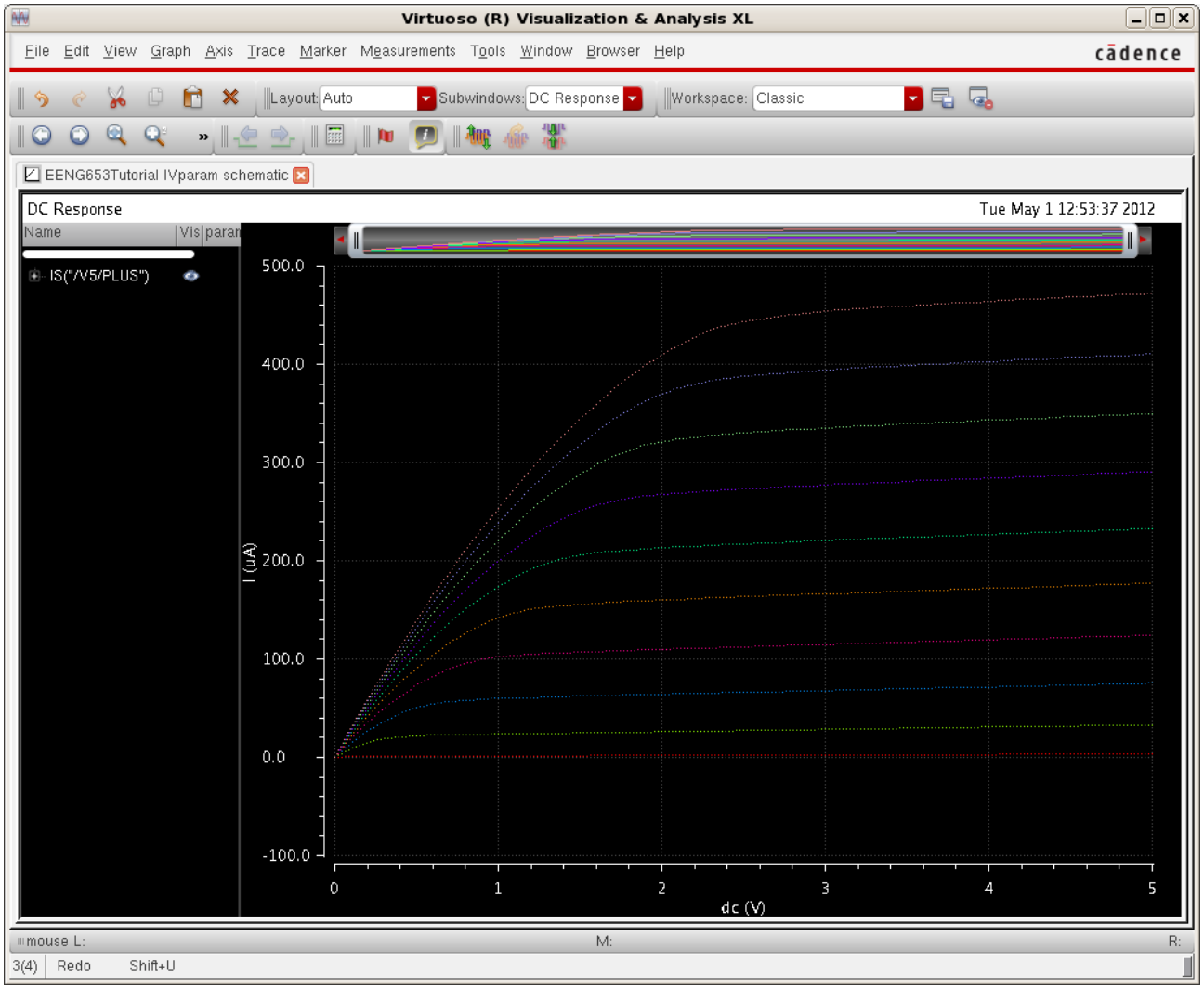
n. Look at the CIW to make sure that the parametric simulation completed successfully, as shown in the image below.



o. After the parametric simulation completes successfully, you are ready to look at the results of your simulation (the 10 IVcurves). Click on the "Virtuoso Analog Design Environment" window and select "Results → Direct Plot → DC." Then click on the terminal of the dummy supply in the drain of the transistor. After clicking the terminal, the terminal will then be surrounded by a circle, as shown in the image below (where the circle is red).



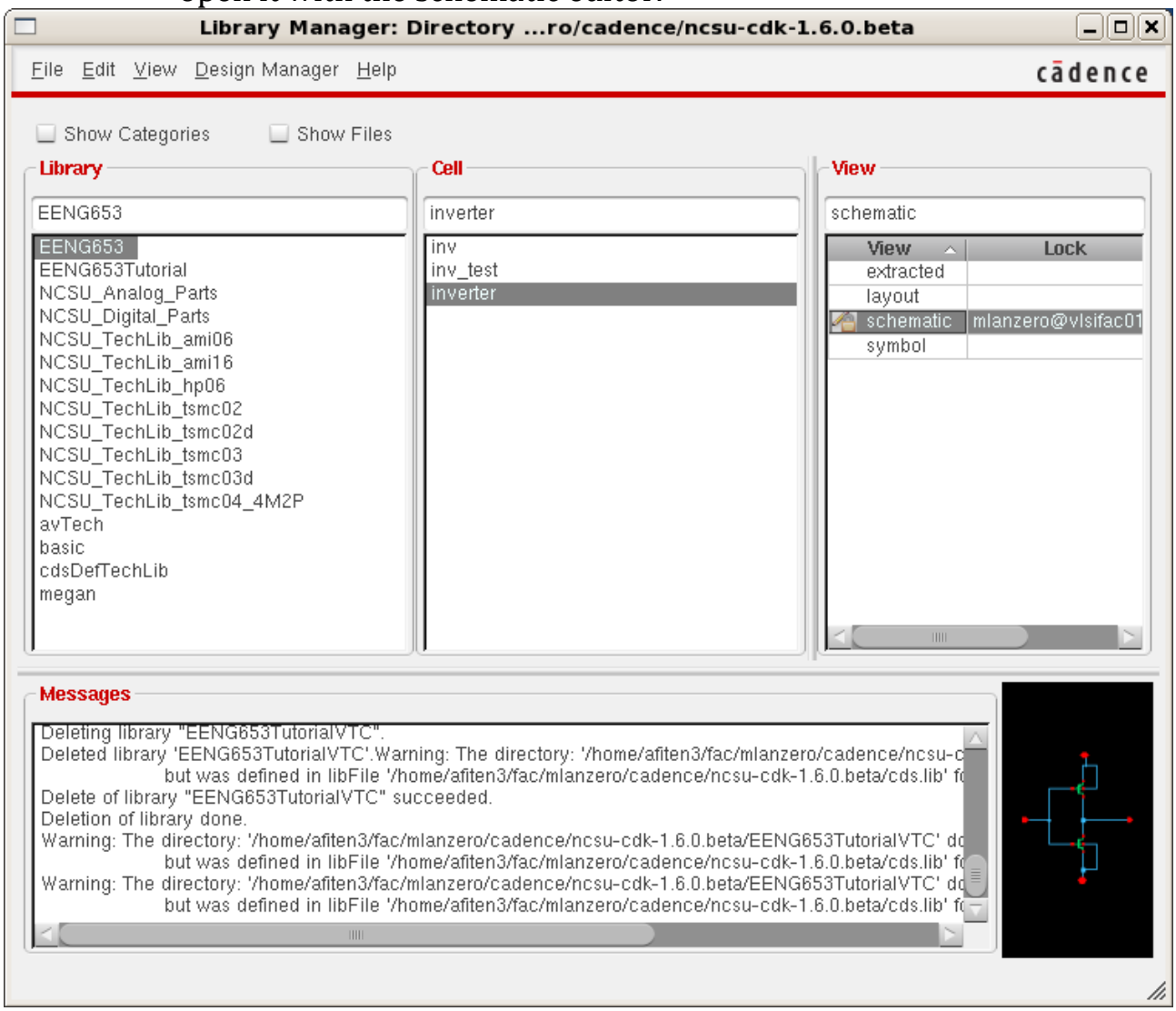
p. Now click the "ESC" key. You will see a family of 10 IVcurves displayed in the "Virtuoso Visualization & Analysis XL" window as shown below. Count the number of IV curves; the figure below shows '10' IV curves.



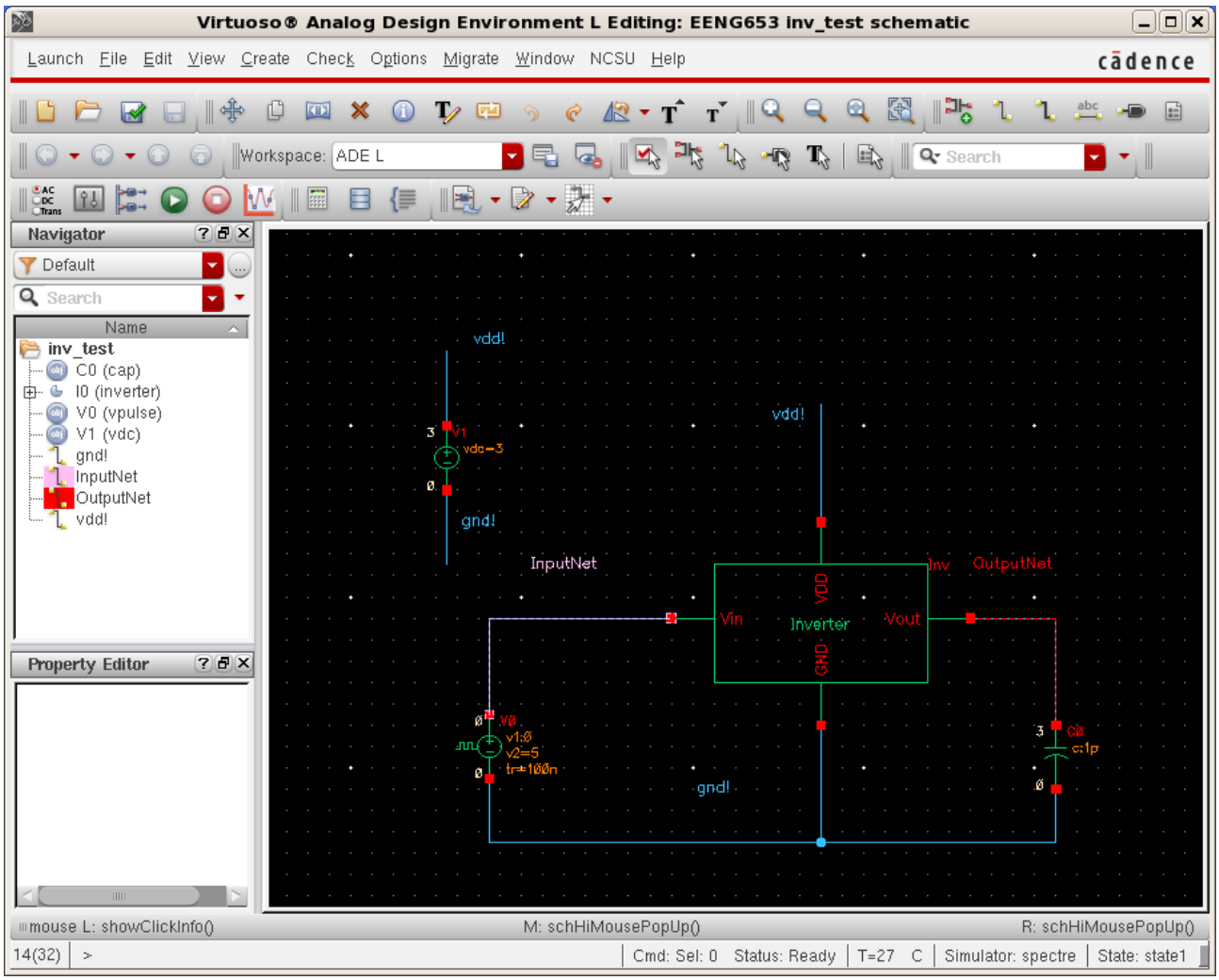
q. You have now completed the parametric simulation tutorial.

23. Inverter: Generating a Voltage Transfer Curve (VTC) of an Inverter

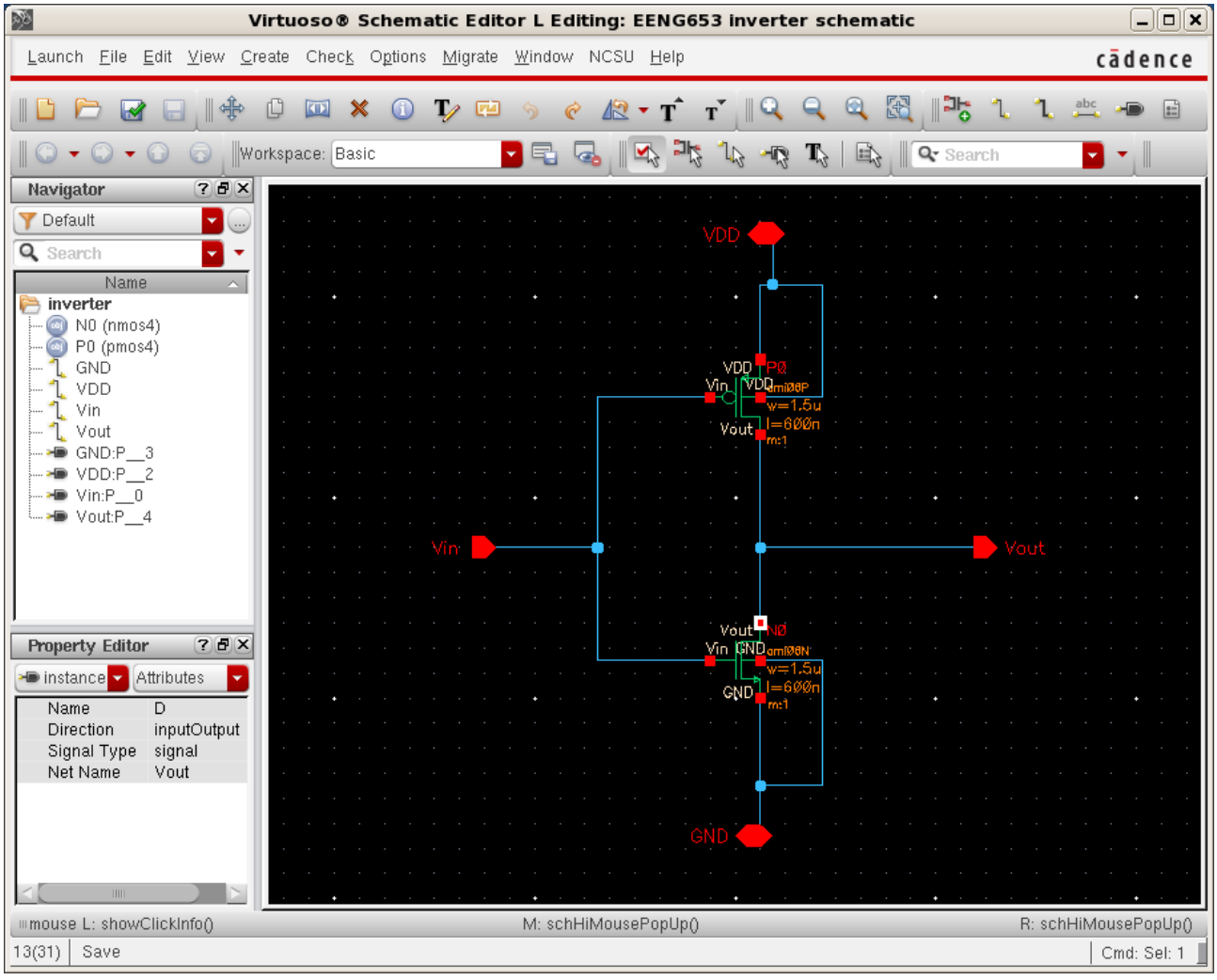
a. In this tutorial, you will generate a voltage transfer curve (VTC) of an inverter. Open the Library Manager and select the EENG653 library that you created previously. Select the inverter schematic and open it with the schematic editor. The select the inv_test schematic and open it with the schematic editor.



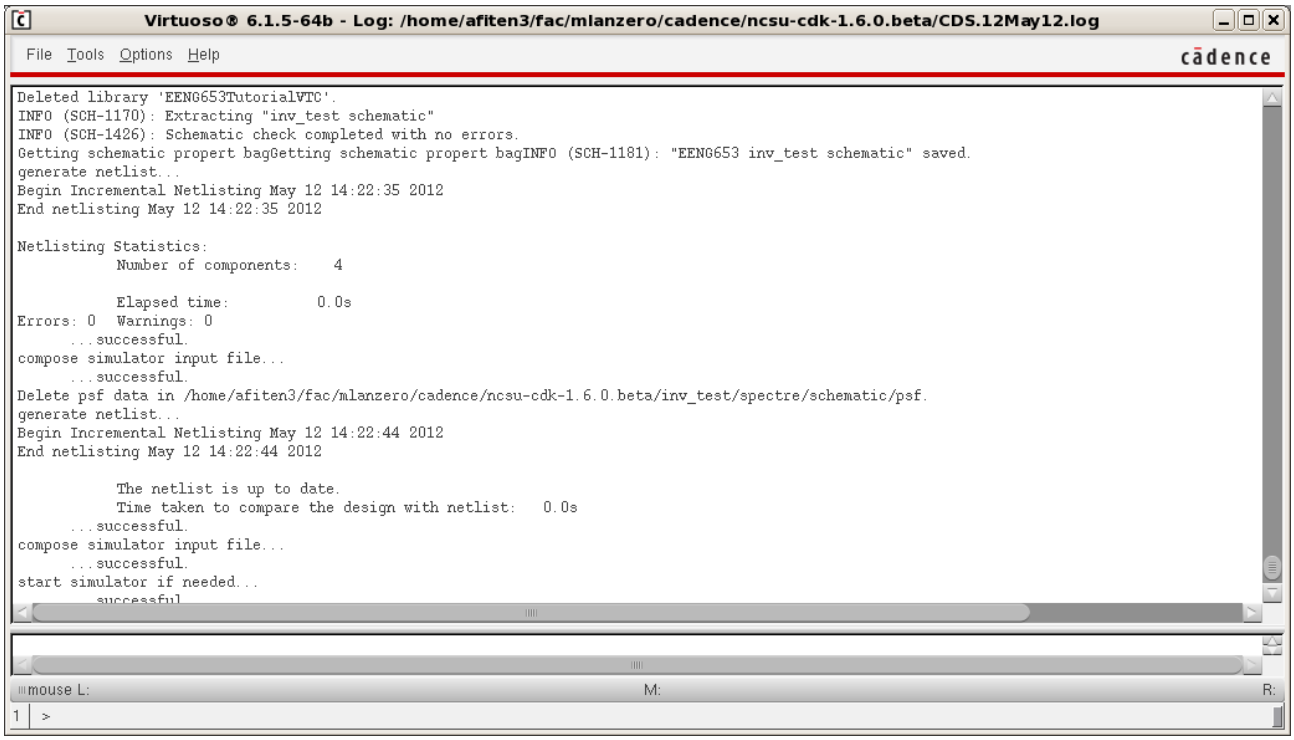
b. Your inv_test schematic will look like the image below.



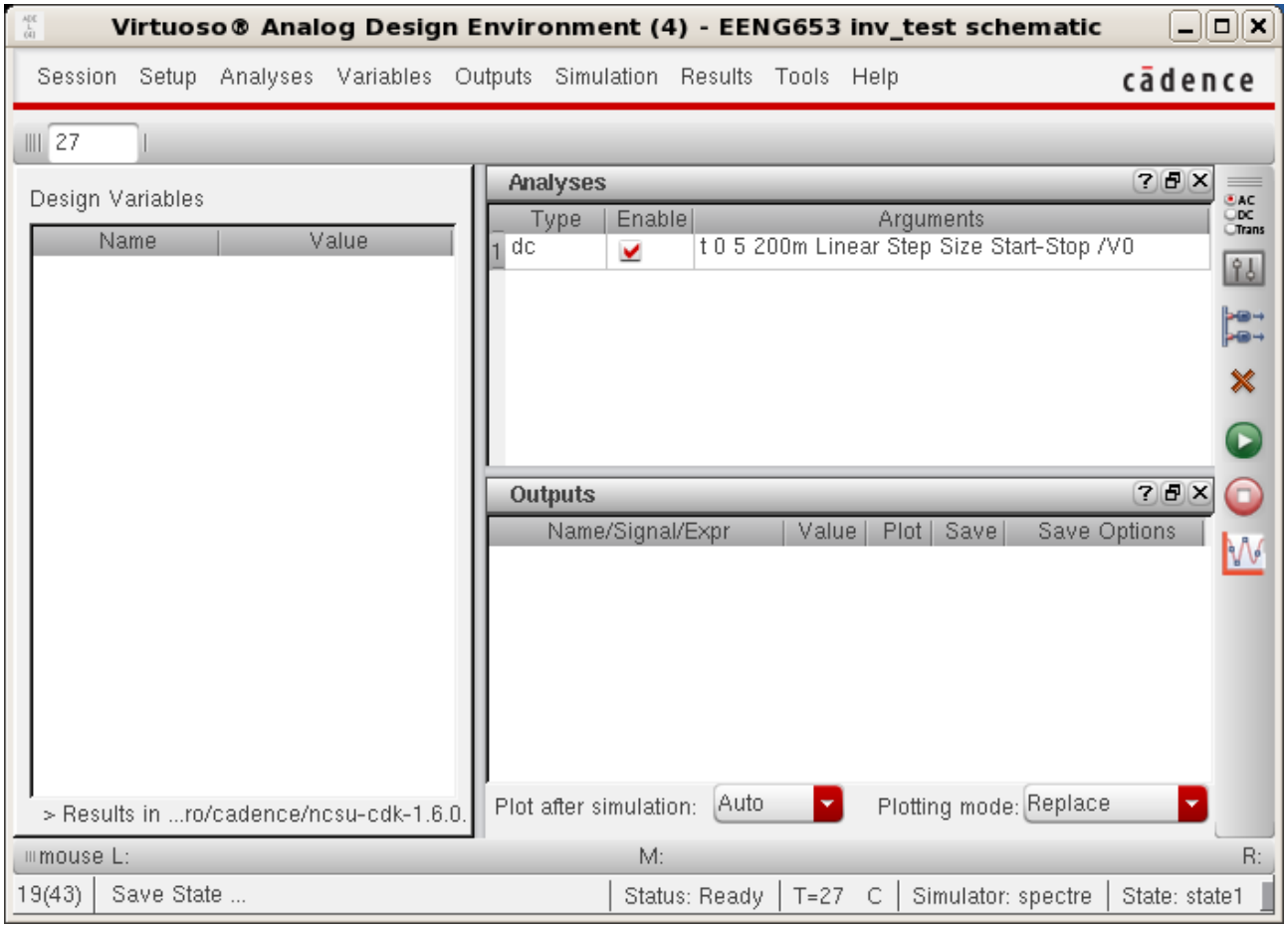
c. Your inverter schematic will look like the image below.



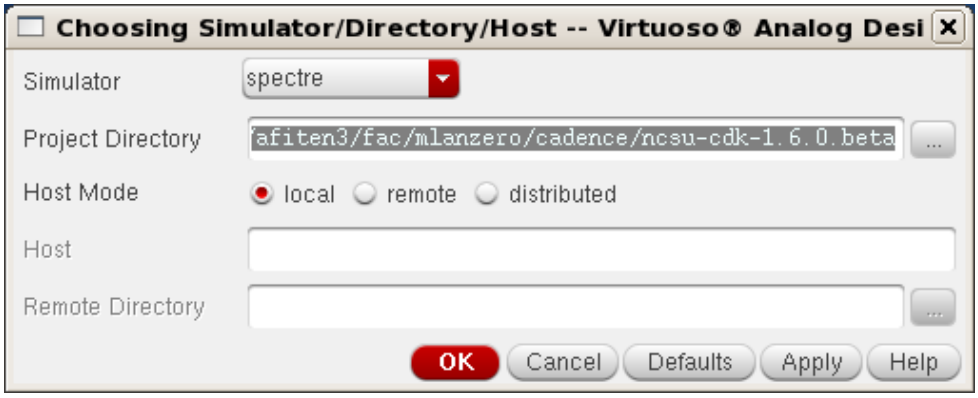
d. Click on the inv_test schematic. Select "File → Check & Save" and check & save the schematic. If the schematic completes "Check & Save" successfully, the CIW will report that the "Schematic check completed with no errors," as shown in the image below. Make sure that your schematic completes "Check & Save successfully." Otherwise, you will need to fix your schematic and redo this step.



e. Click on the "EENG653 inv_test schematic" and select "Launch → ADE L" to launch the Virtuoso Analog Design Environment. The Virtuoso Analog Design Environment window will appear as shown below. In the next steps, you will populate the 'Analyses' portion of this window.

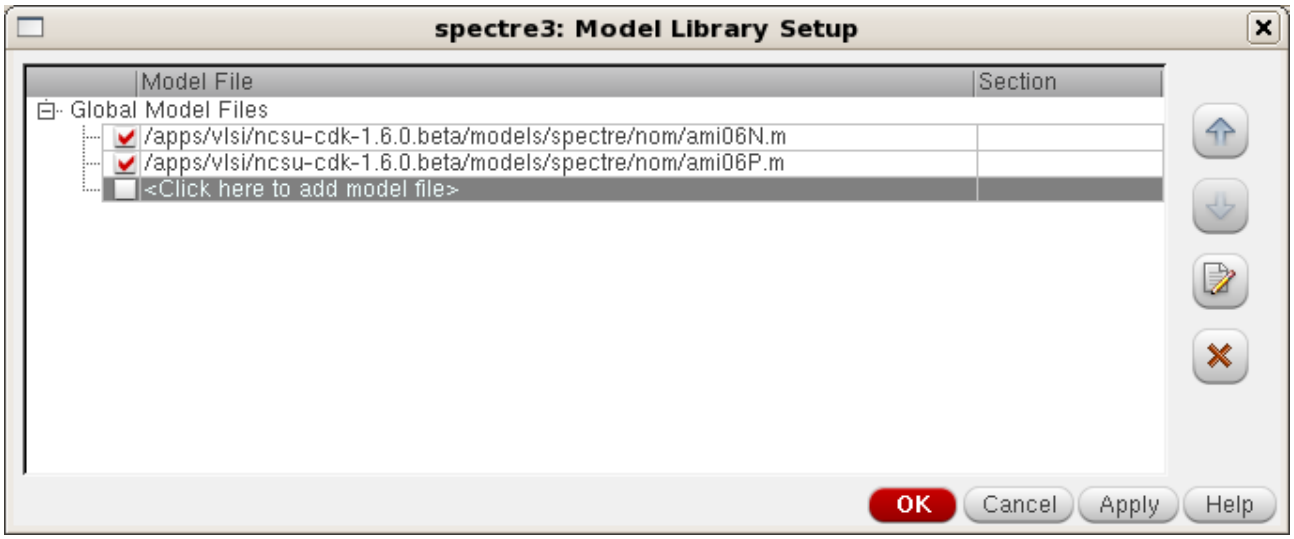


f. In the Virtuoso Analog Design Environment window, select "Setup → Simulator/Directory/Host." In the "Choosing Simulator/Directory/Host" window, select 'spectre' as the Simulator as shown in the image below.

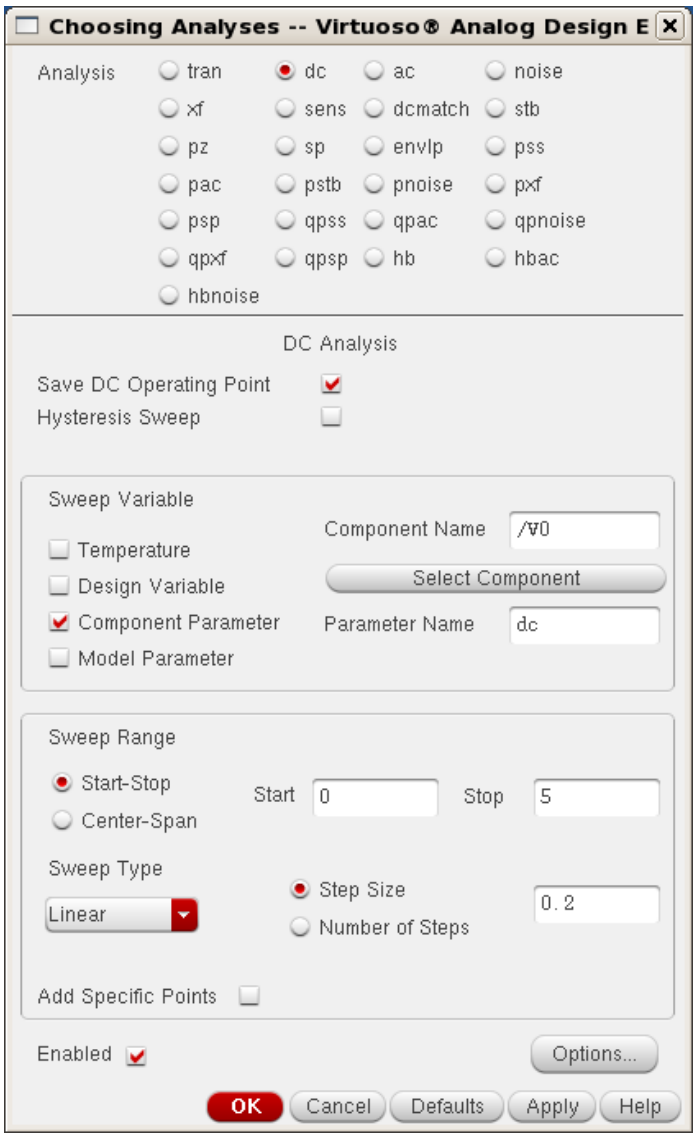


g. Now you will set up the Model Libraries. In the Virtuoso Analog Design Environment window, select "Setup → Model Libraries." In the "Model Library Setup" window, point the Global Model Files to the models for the nmos4 and pmos4 in your schematic. The two paths that you need to add to your Global Model Files are shown in the image below and are:

i. /apps/vlsi/ncsu-cds-1.6.0.beta/models/spectre/nom/ami06N.m
ii. /apps/vlsi/ncsu-cds-1.6.0.beta/models/spectre/nom/ami06P.m

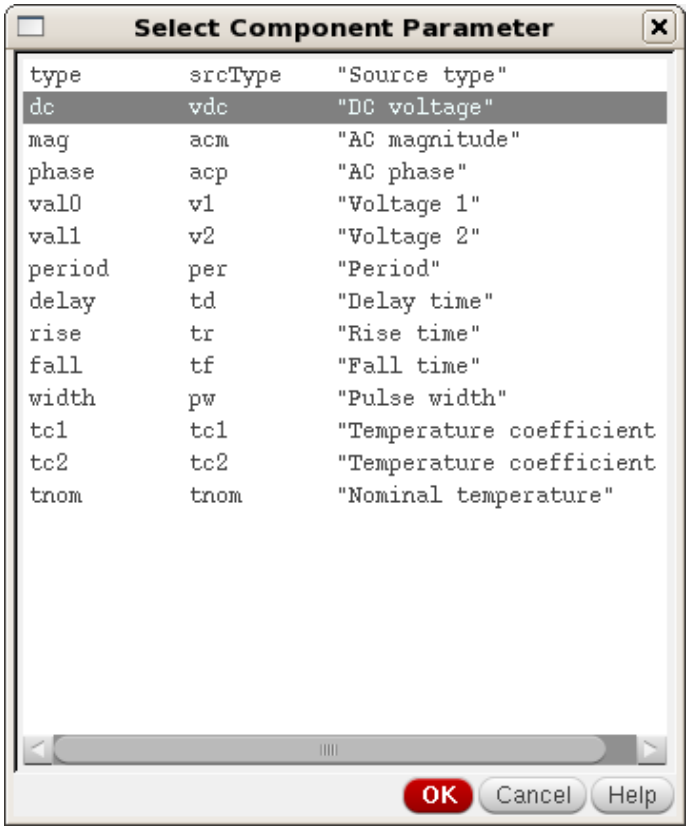


h. Now click on the Virtuoso Analog Design Environment window and select "Analyses → Choose." In the "Choosing Analyses" window, select 'dc' because you will be doing a dc analysis. Select "Component Parameter," and enter the Component Name /V0 for the vpulse in the inv_test schematic. Then click 'Select Component.'

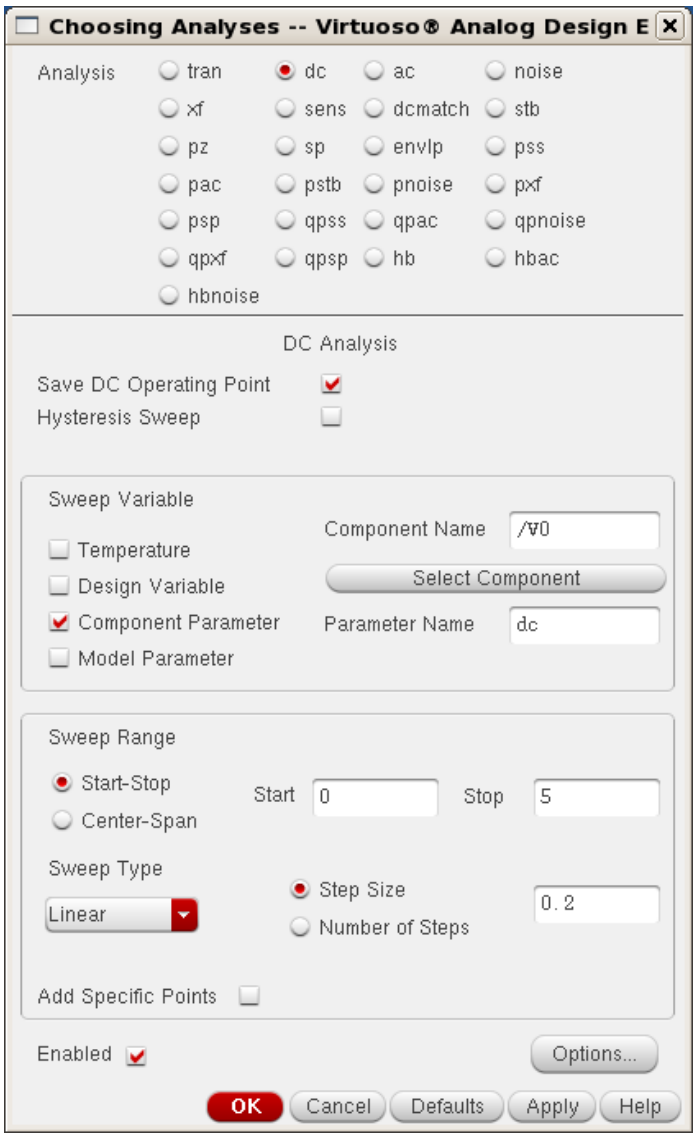


i. After clicking 'Select component,' the 'Select Component Parameter' window will appear as shown in the image below. Select the line 'dc vdc "DC voltage" ' with your cursor as shown in the image below, and then select 'OK."

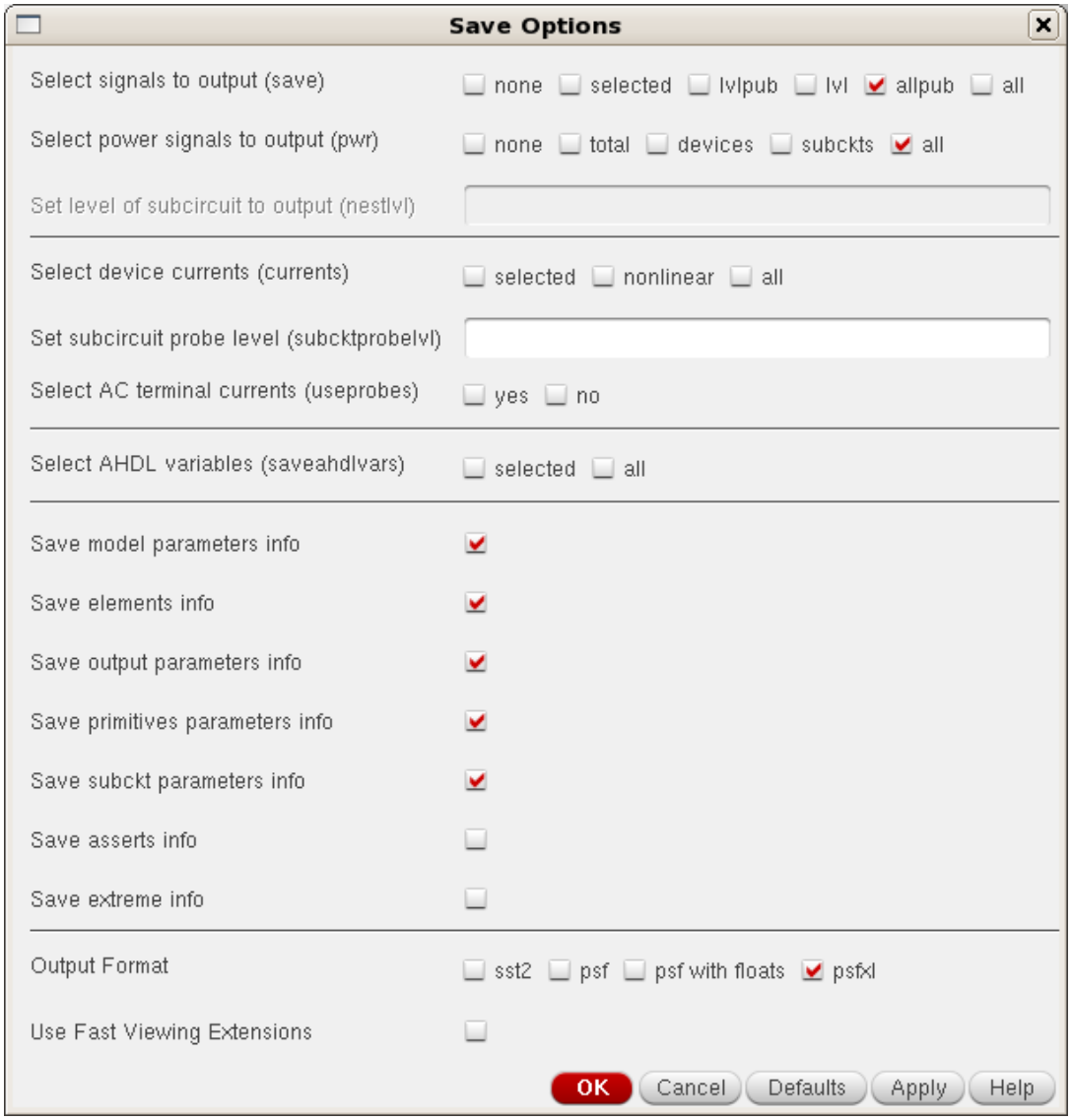
If the 'Select Component Parameter' window does not appear, then go to your schematic and click on the vpulse instance which will bring up the 'Select Component Parameter' window as shown in the image below.



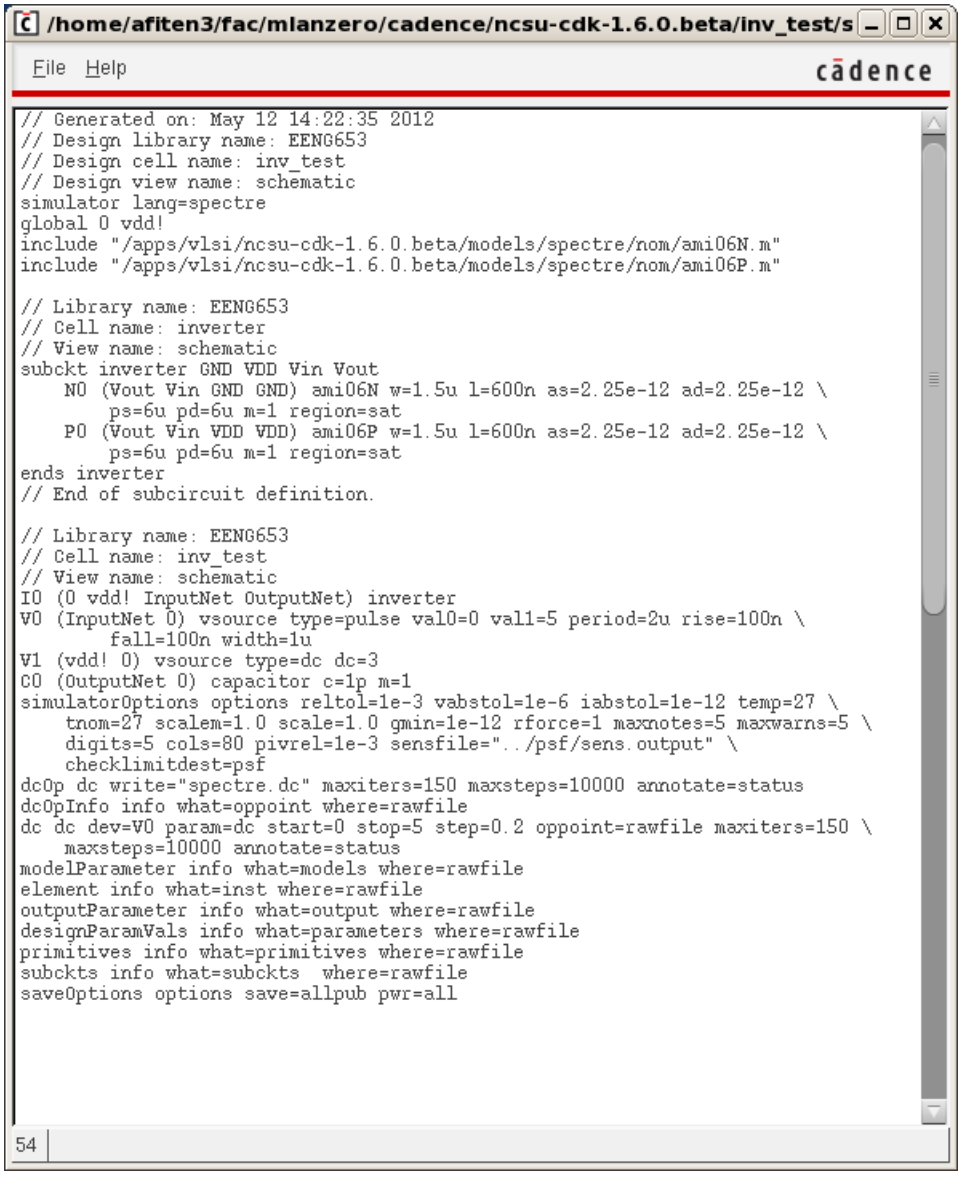
j. Now return to the "Choosing Analyses" window. In this window the "Parameter Name" will now be set to 'dc.' Set 'Start' to '0' and 'Stop' to '5' as shown in the image below. Also select 'Sweep Type' to 'Linear' using the pull-down and set 'Step Size' to '0.2' as shown. Click 'Enabled' and select 'OK.'



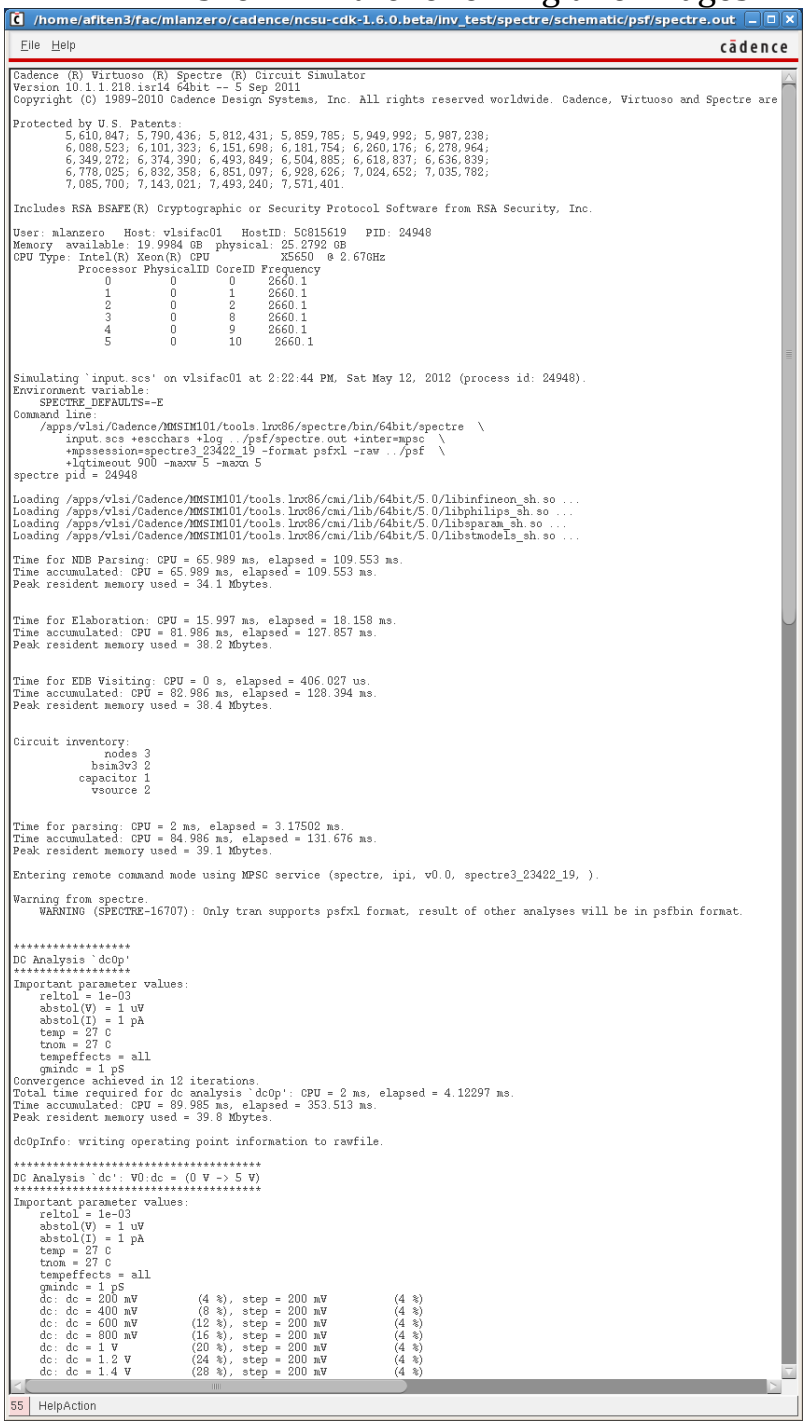
k. Now click on the "Analog Design Environment" window. Select "Outputs → Save All." The "Save Options" window will appear as shown below. For 'Select signals to output (save),' select 'allpub.' For 'Select power signals to output (pwr),' select 'all.' Select the other options as shown, and then click 'OK.'



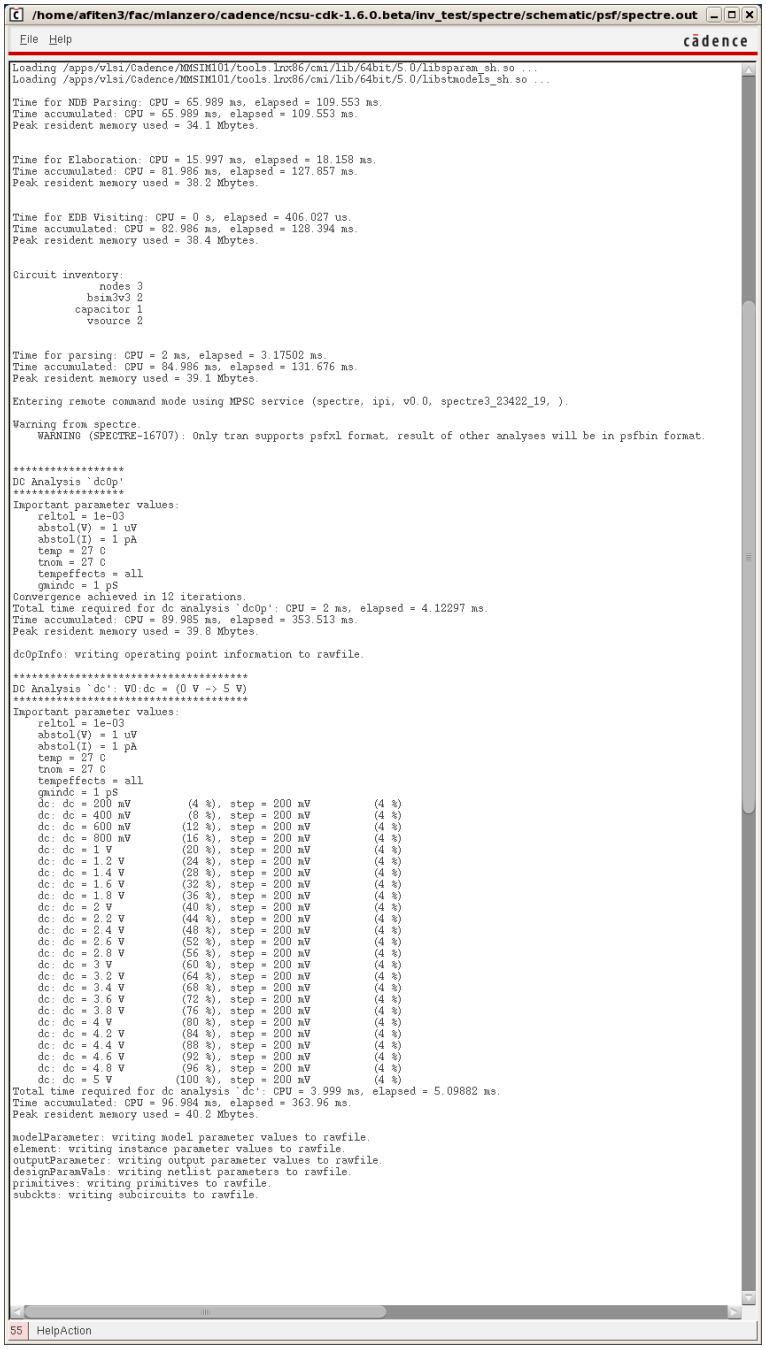
l. Now you can get ready for the simulation. Click on the Virtuoso Analog Design Environment window and select "Simulation → Netlist → Create Raw." The netlist will appear as shown in the image below.



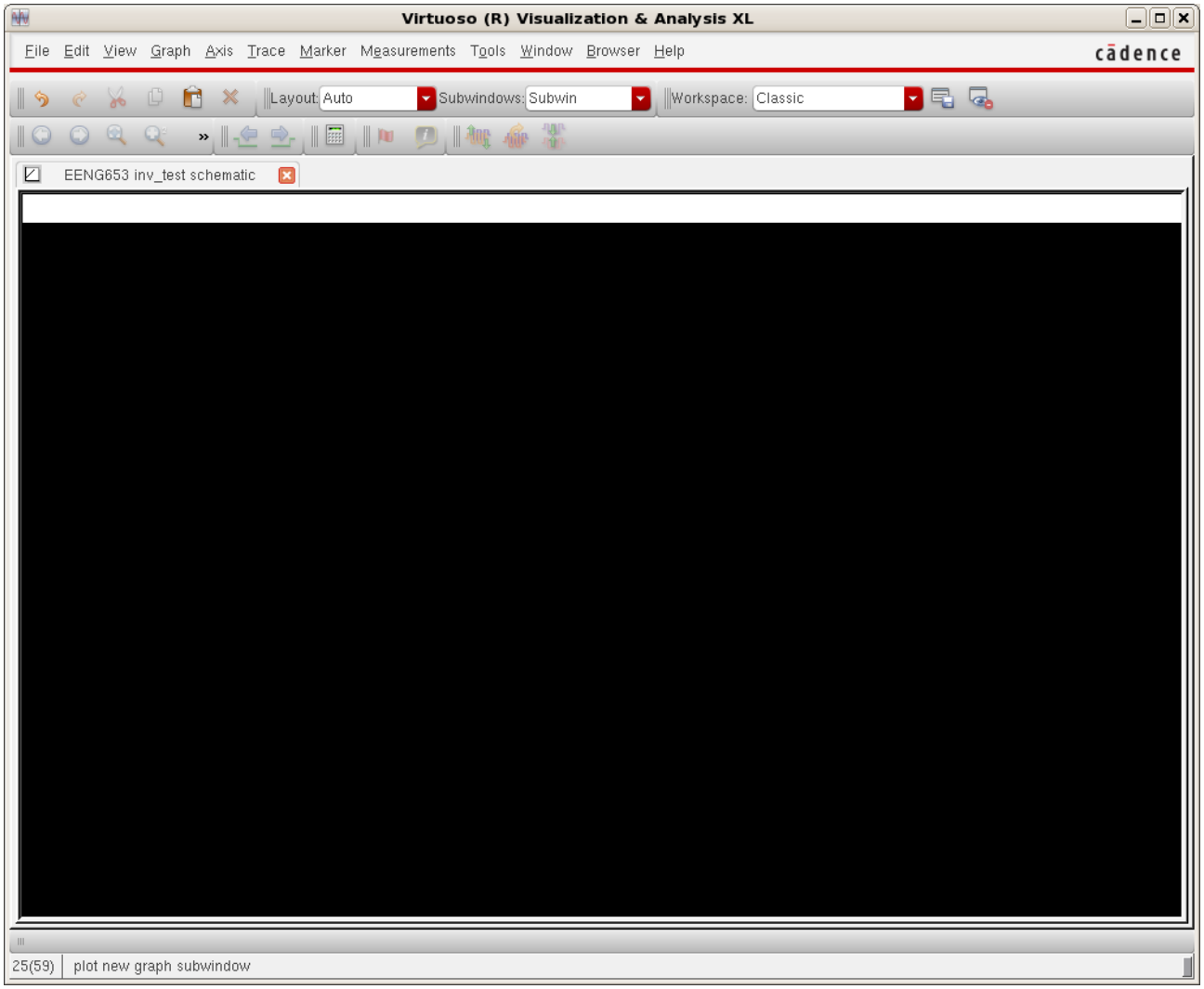
m. Now click on the Virtuoso Analog Design Environment window and select "Simulation → Run." The simulation will run and appear as shown in the following two images.



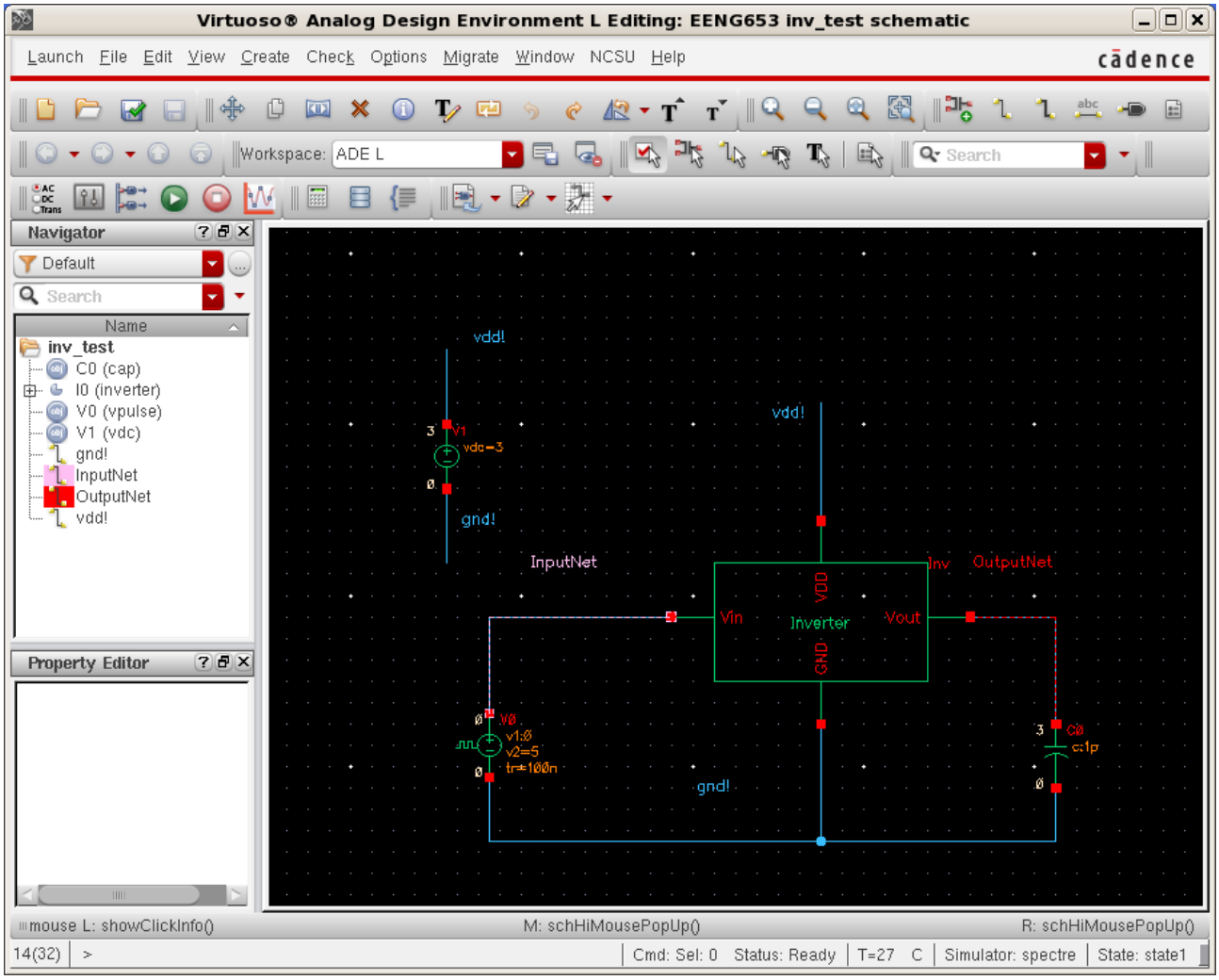
n. This is the second half of the results of the simulation (see the image below).



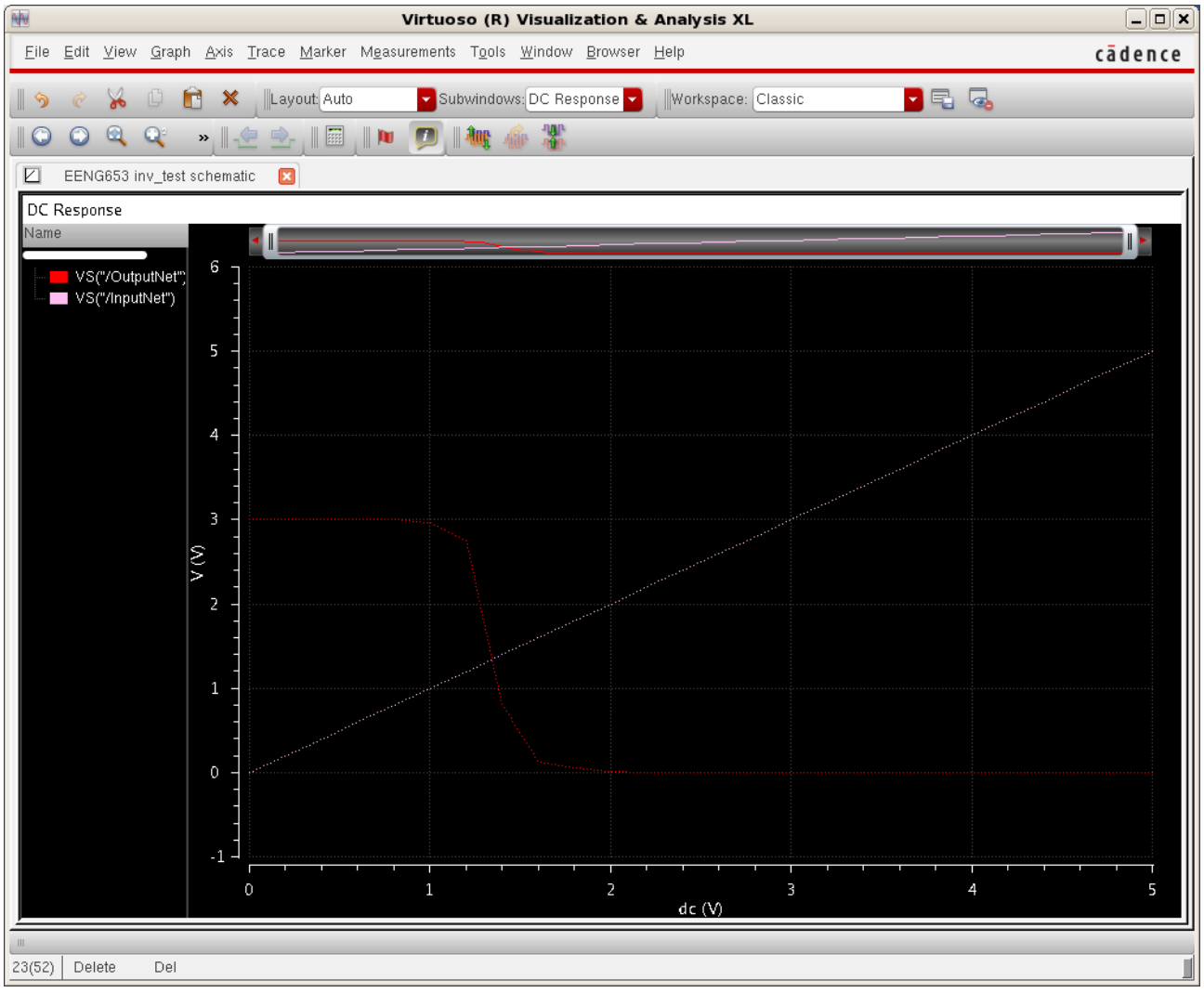
o. Now click on the Virtuoso Analog Design Environment window. You are going to generate a Voltage Transfer Curve for your schematic. Click on "Results → Annotate → DC Node Voltages." Then click on "Results → Direct Plot → DC." The "Virtuoso ® Visualization & Analysis XL" window will appear as shown below. It will be empty (blank).



p. In the Virtuoso Analog Design Environment window, select the nets for which you wish to display the voltages in the voltage tranfer curve. The two nets are the "InputNet" and the "OutputNet." Select these two nets by clicking on them, and the nets will become dashed lines as shown in the inv_test schematic image shown below.

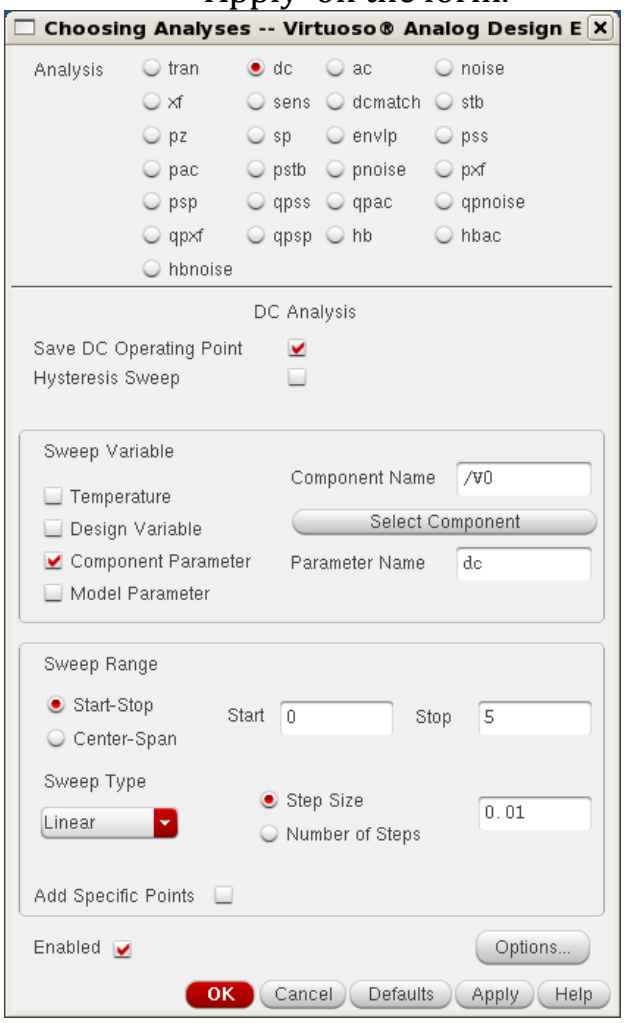


q. After clicking on the "InputNet" and "OutputNet," click the "ESC" key. The Voltage Transfer Curve will appear (that is, the output voltage as a function of the input voltage) in the Virtuoso Visualization & Analysis XL window as shown in the image below. In the image below, the VTC is indicated in red. The increasing input voltage is shown in pink. Note that these colors correspond to the colors of the dashed nets in the inv_test schematic.

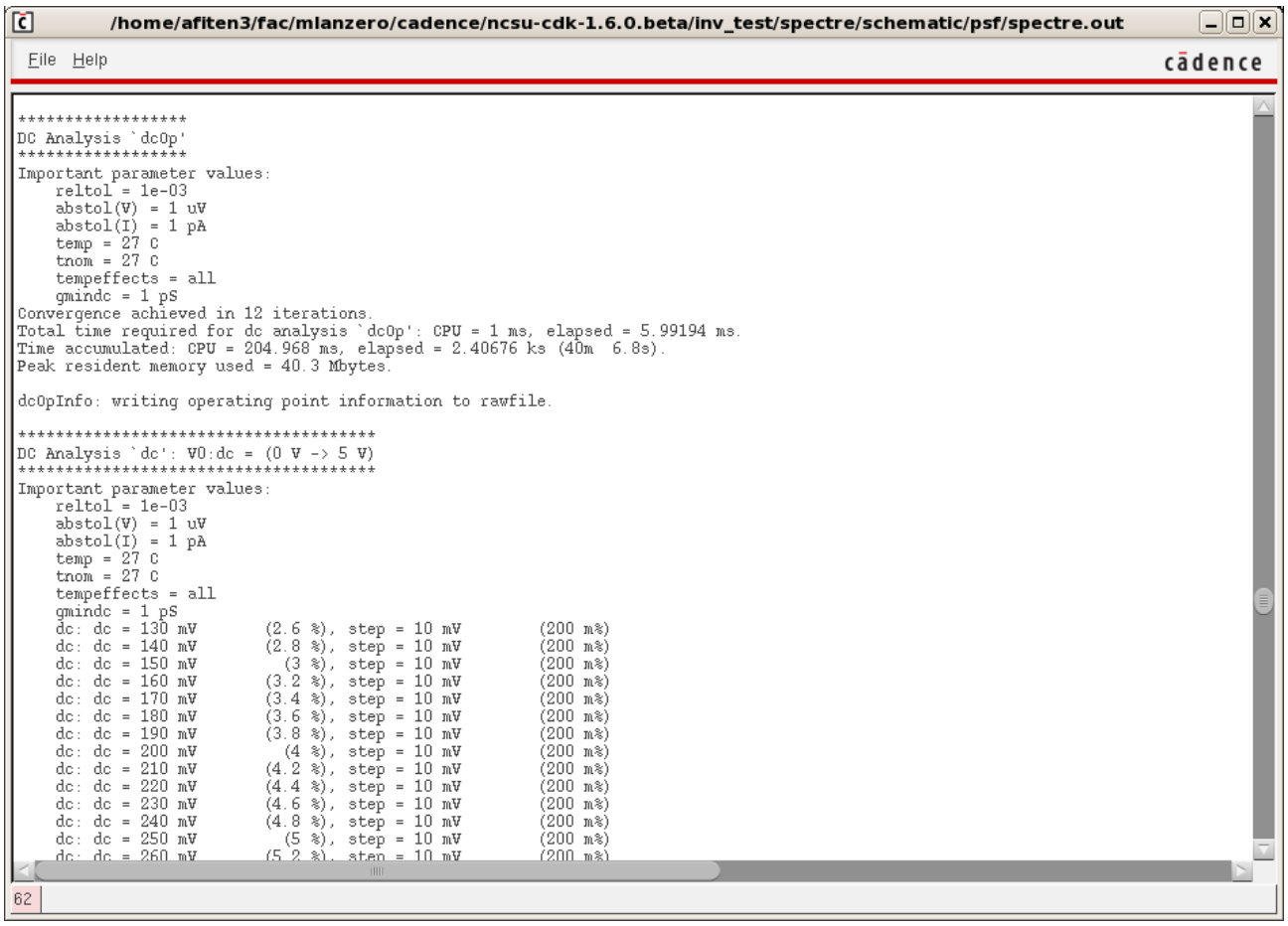


r. Notice that the voltage transfer curve is not smooth; that is, there are points at the locations on the curve where the input voltage has taken a step; recall that you set the step size for this simulation to 0.2 (refer to the "Choosing Analyses" window in a previous step.

s. Now you are going to generate a smooth Voltage Transfer Curve for your inv_test schematic and inverter schematic. Return to the "Choosing Analyses" window and set the "Step Size" to 0.01 (that is, this is equivalent to 0.1 V) as shown in the image below. Click 'Apply' on the form.

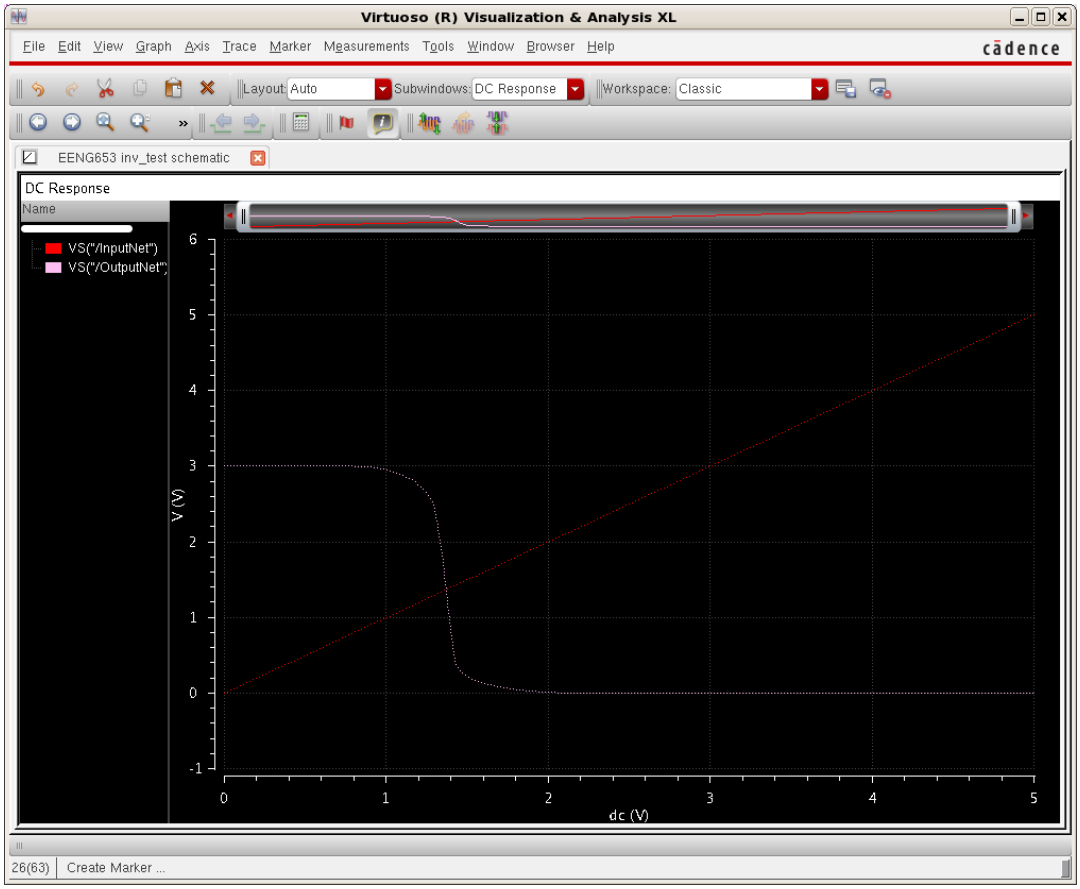


t. In the Virtuoso Analog Design Environment window, select "Simulation → Netlist → Raw." Then select "Simulation → Run." The simulation will look like the results shown in the image below.



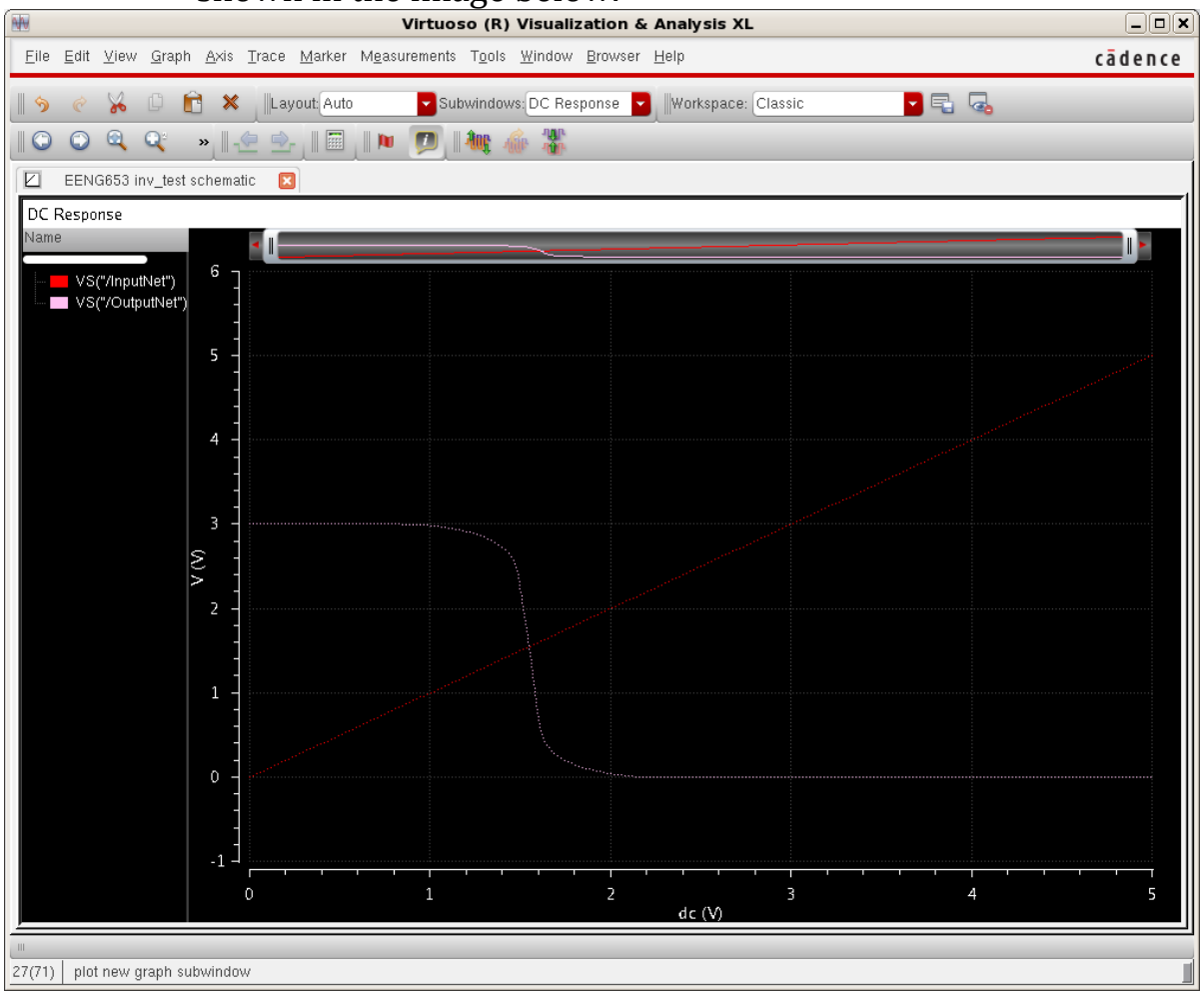
u. Then select "Results → Direct Plot → DC."

v. A blank "Virtuoso Visualization & Analysis XL" window will appear. In the inv_test schematic window, select the "InputNet" and "OutputNet" which will become dashed lines. Then click the "ESC" key. Then the "Virtuoso Visualization & Analysis XL" window will appear with a smooth VTC as shown in the image below.

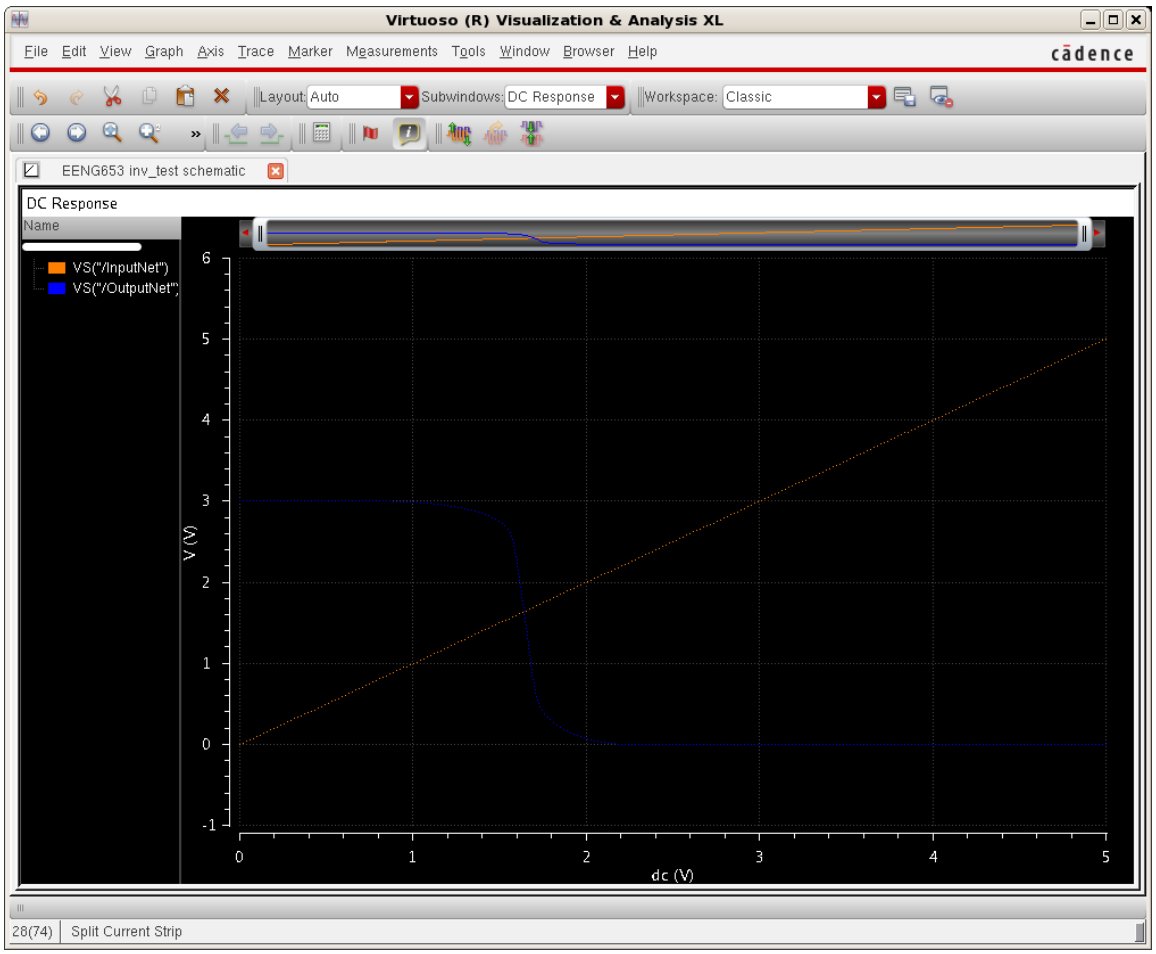


w. Now you will investigate how the response of the Voltage Transfer Curve changes as you change the width of the devices. For example, change the width of the pfet in your inverter schematic to 3microns: w = 3um. Check and Save your inverter schematic and the inv_test schematic.

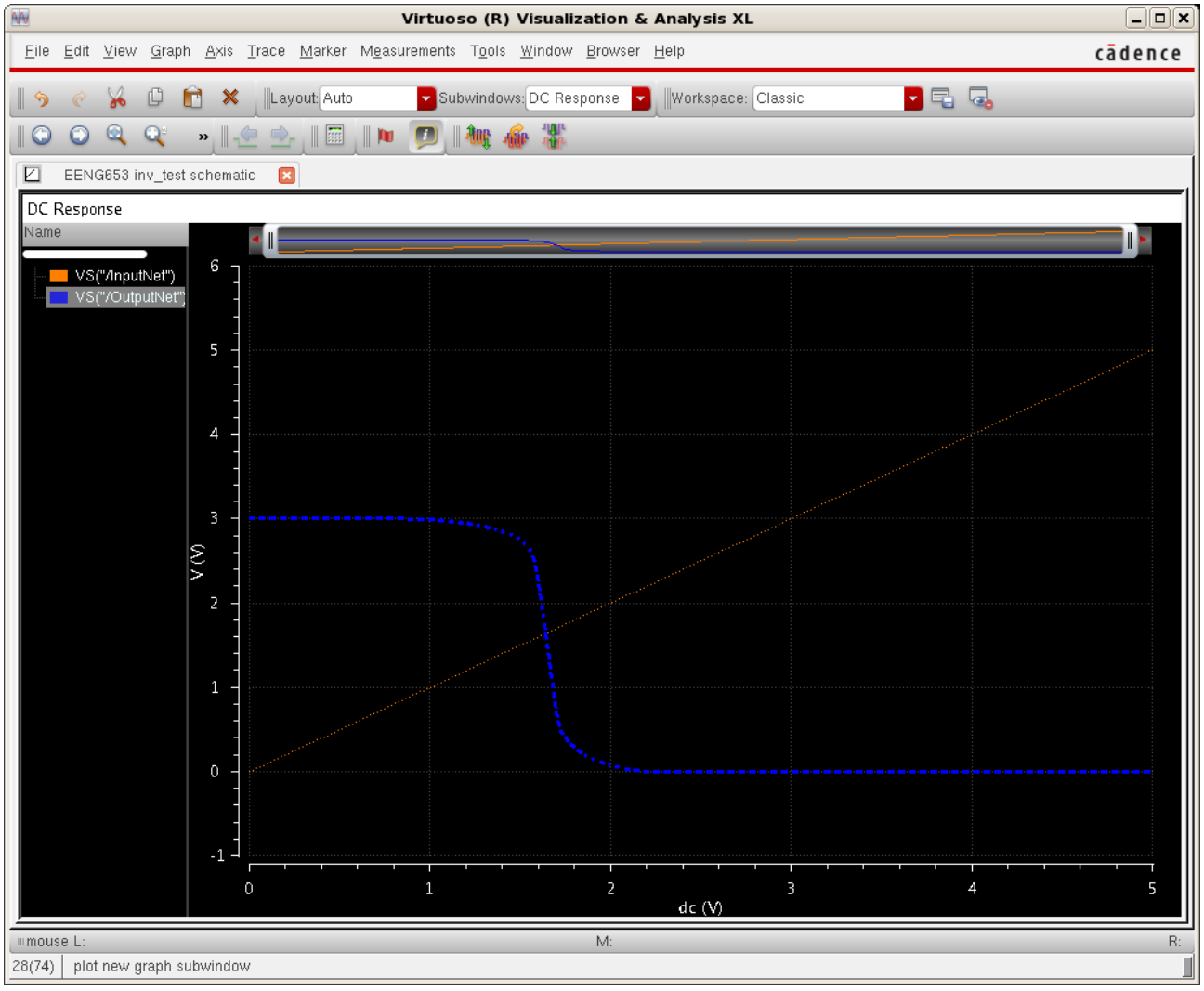
x. Now click on the Virtuoso Analog Design Environment window and select "Simulation → Netlist → Create Raw." Then select "Simulation → Run." Select "Results → Direct Plot → DC," then select "InputNet," "OutputNet," click "ESC." You will obtain an updated VTC in the Virtuoso Visualization & Analysis XL window as shown in the image below.



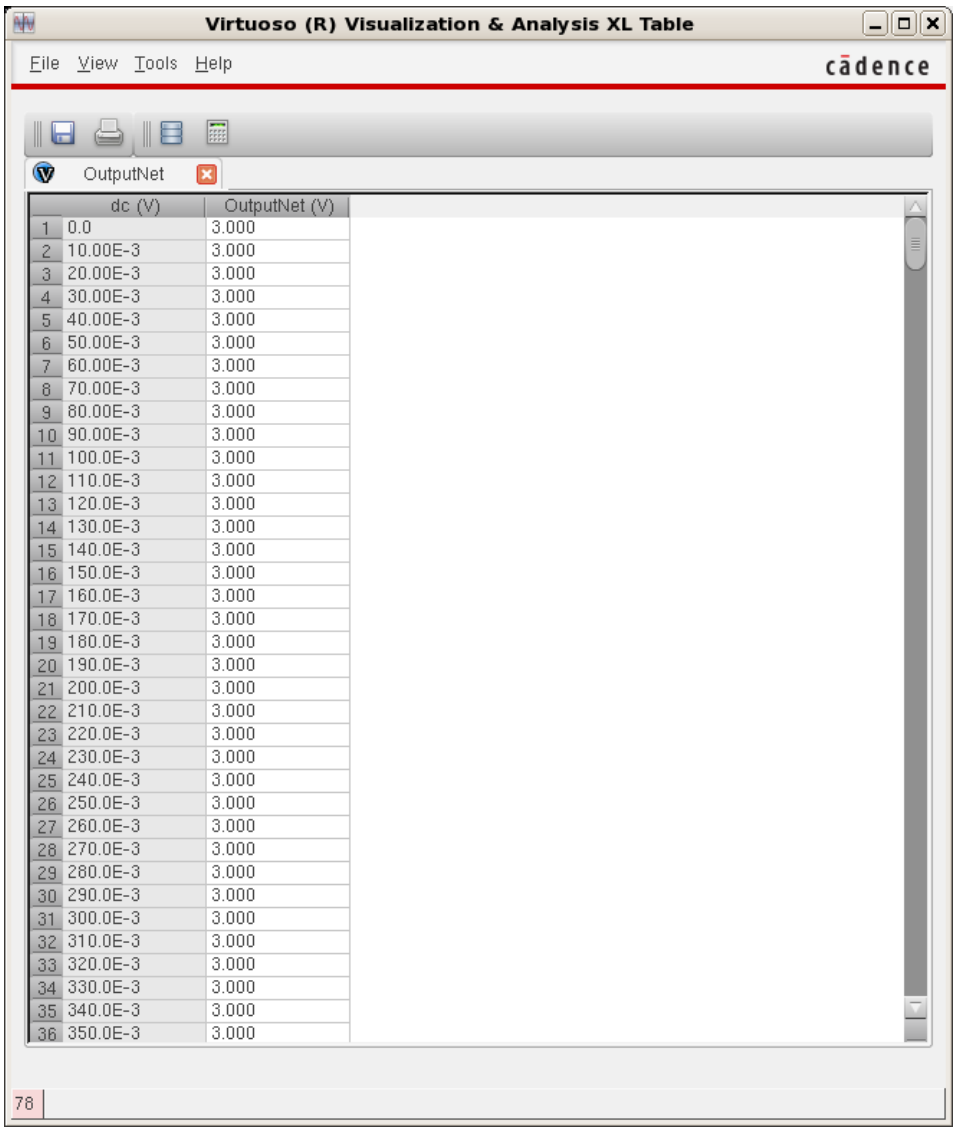
y. Now change the width of the pfet in your inverter schematic to 3*1.5 microns: w = 4.5um. Check and Save your inverter schematic and the inv_test schematic. Now click on the Virtuoso Analog Design Environment window and select "Simulation → Netlist → Create Raw." Then select "Simulation → Run." Select "Results → Direct Plot → DC," then select "InputNet," "OutputNet," click "ESC." You will obtain an updated VTC in the Virtuoso Visualization & Analysis XL window as shown in the image below.



z. Now click on the VTC. It will become bold and dashed as shown in the image below.

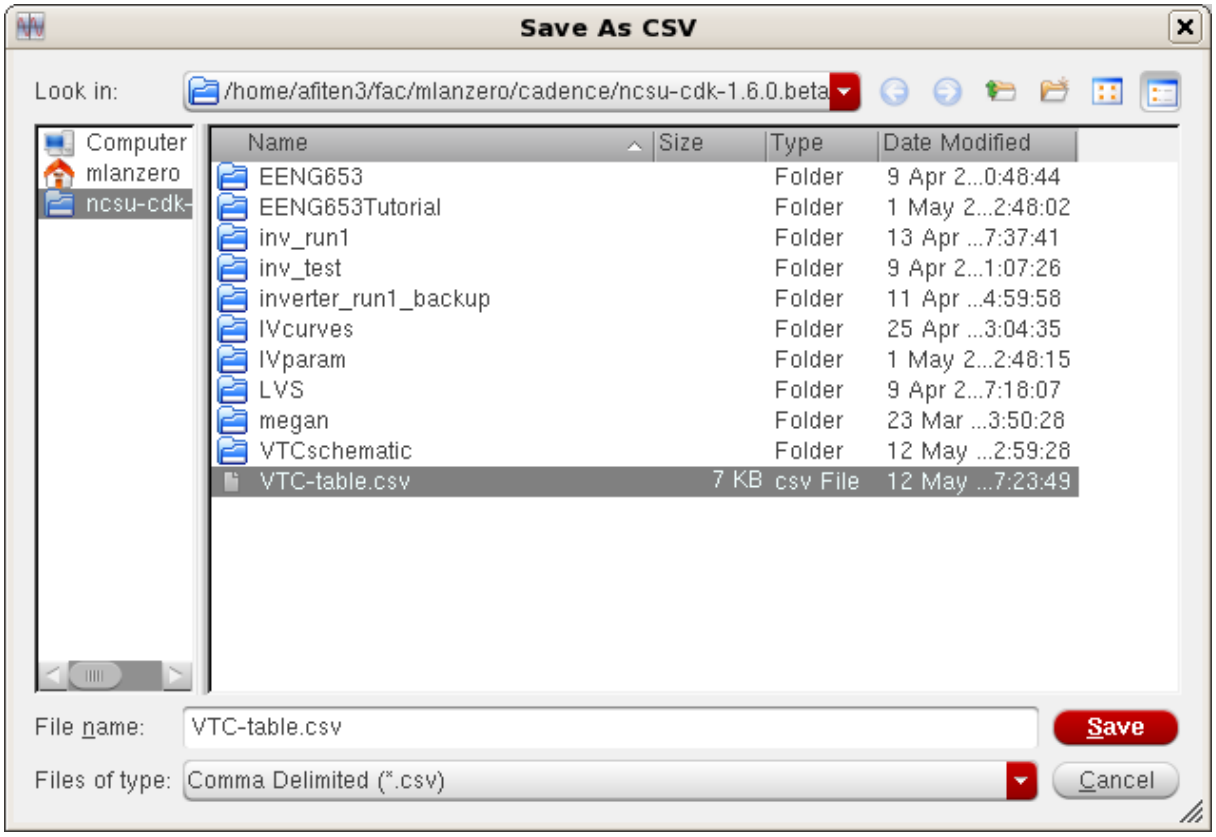


aa. Now right click with your mouse on the curve and select "Table → New Window." A Virtuoso Visualization & Analysis XL Table will appear with the values of the voltage on the InputNet and the values of the voltage on the OutputNet, where the voltage on the InputNet ranges from 0V to 5V as you specified in the simulation. The table looks like the image below.



	dc (V)	OutputNet (V)
1	0.0	3.000
2	10.00E-3	3.000
3	20.00E-3	3.000
4	30.00E-3	3.000
5	40.00E-3	3.000
6	50.00E-3	3.000
7	60.00E-3	3.000
8	70.00E-3	3.000
9	80.00E-3	3.000
10	90.00E-3	3.000
11	100.0E-3	3.000
12	110.0E-3	3.000
13	120.0E-3	3.000
14	130.0E-3	3.000
15	140.0E-3	3.000
16	150.0E-3	3.000
17	160.0E-3	3.000
18	170.0E-3	3.000
19	180.0E-3	3.000
20	190.0E-3	3.000
21	200.0E-3	3.000
22	210.0E-3	3.000
23	220.0E-3	3.000
24	230.0E-3	3.000
25	240.0E-3	3.000
26	250.0E-3	3.000
27	260.0E-3	3.000
28	270.0E-3	3.000
29	280.0E-3	3.000
30	290.0E-3	3.000
31	300.0E-3	3.000
32	310.0E-3	3.000
33	320.0E-3	3.000
34	330.0E-3	3.000
35	340.0E-3	3.000
36	350.0E-3	3.000

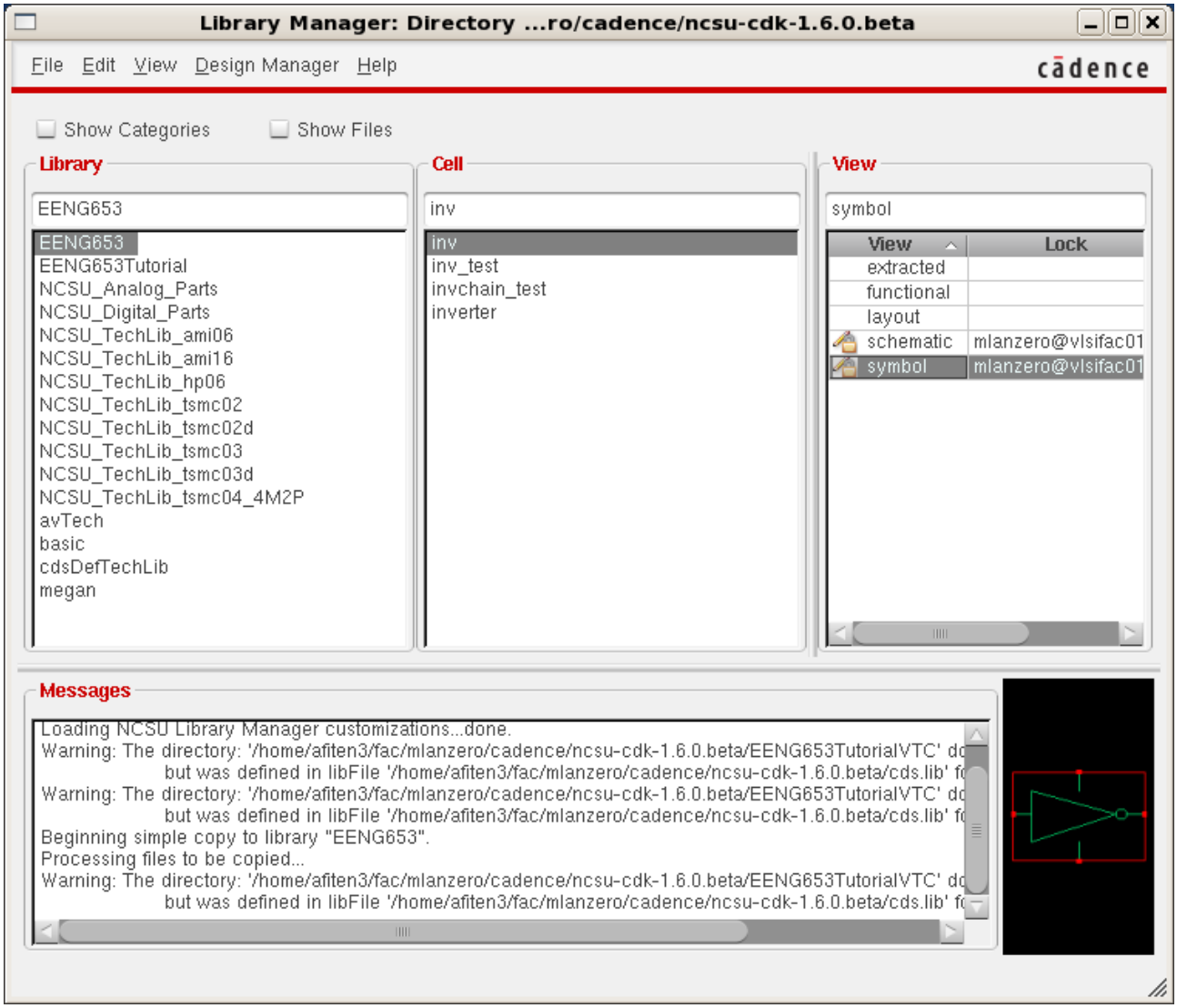
bb. You can export this Table to a CSV file by clicking at the top banner of this window on "File → Save as CSV." The image below shows that this table is saved in the working directory with the name "VTC-table.csv."



cc. You have now completed the voltage transfer curve (VTC) tutorial.

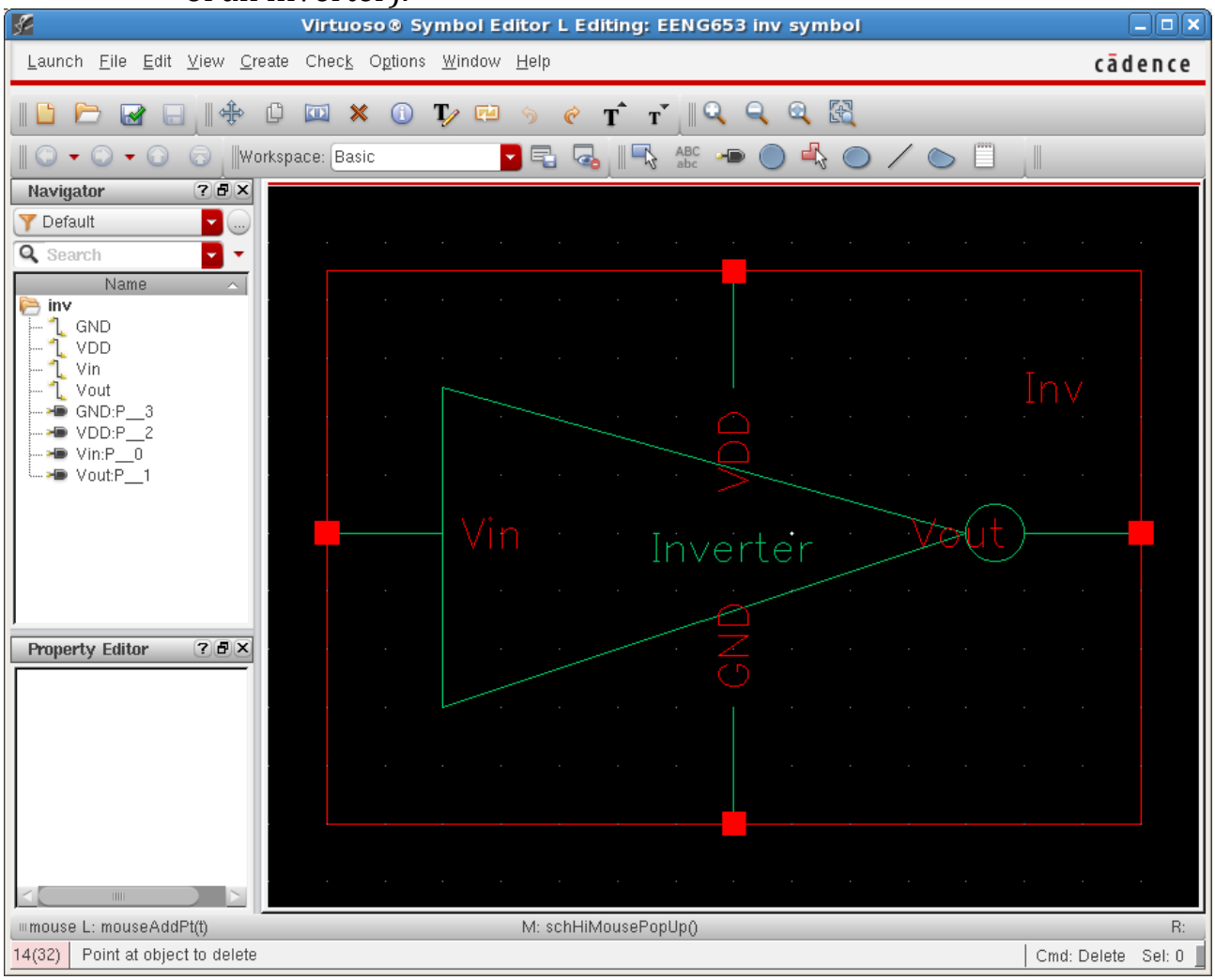
24. Inverter Chain: Creating an Inverter Chain

a. In this section, you will create a chain of 11 inverters. A chain of inverters is referred to as an *inverter chain*. The library 'EENG653' should still be in your library search path, as shown in the library manager below. Copy the 'inv_test' cell to a new cell called 'invchain_test' cell. Copy the 'inverter' cell to a new cell called 'inv'. Change the name of the inverter instantiated in the 'invchain_test' cell to 'inv' from 'inverter.'

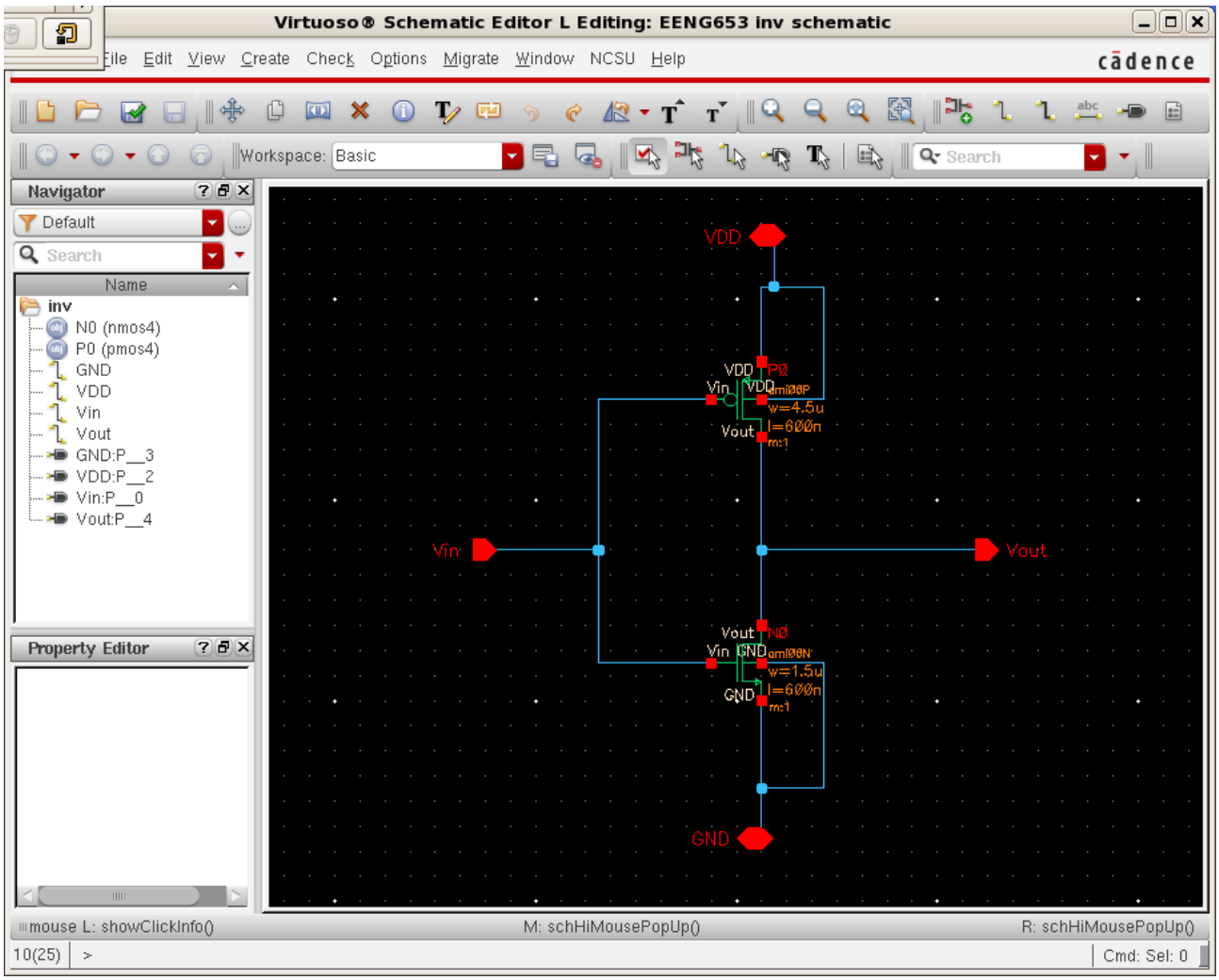


b. Open the 'inv' symbol in the 'EENG653' library and edit it using the editing functions on the bar above the symbol (add green lines, a green circle, delete the green rectangle). You may edit the 'inv' symbol to create an inverter symbol that is similar to the one you are studying in this course.

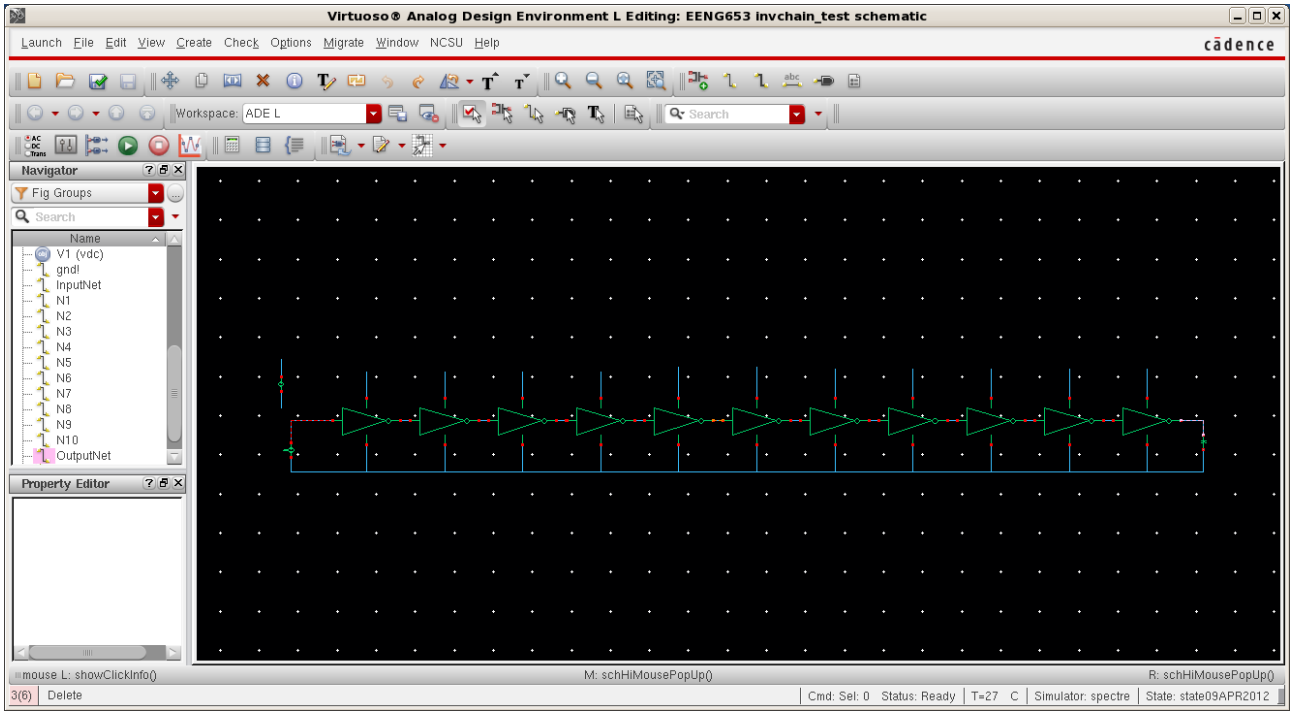
We need this symbol in order to create a hierarchical schematic at the logic (gate) level of an inverter chain. We create a hierarchical schematic using symbols of lower-level schematics (in this case, we create a hierarchical schematic of an inverter chain using the symbol of an inverter).



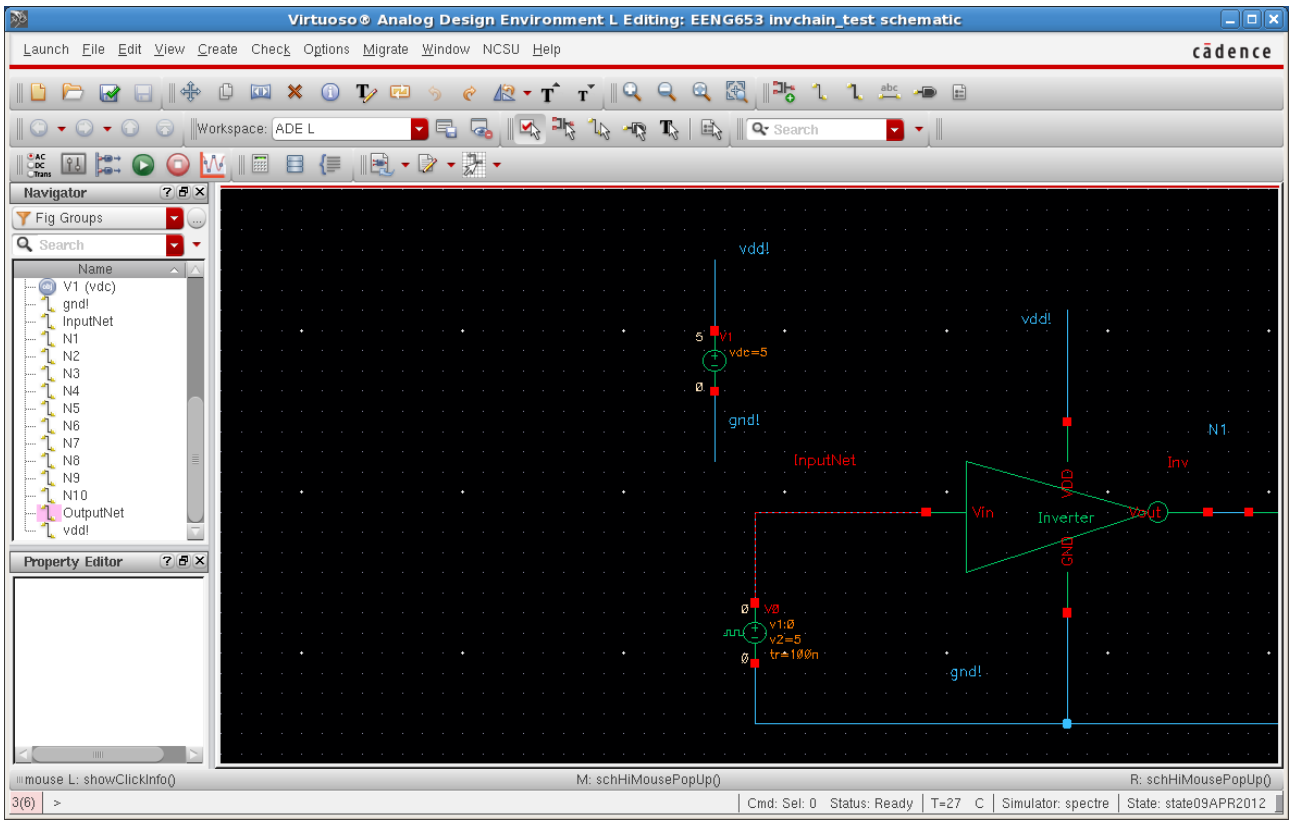
c. The schematic of the 'inv' is shown in the image below. Note that this schematic shows a pfet with a width (4.5 um) that is three times as large as the width of the nfet (1.5 um).



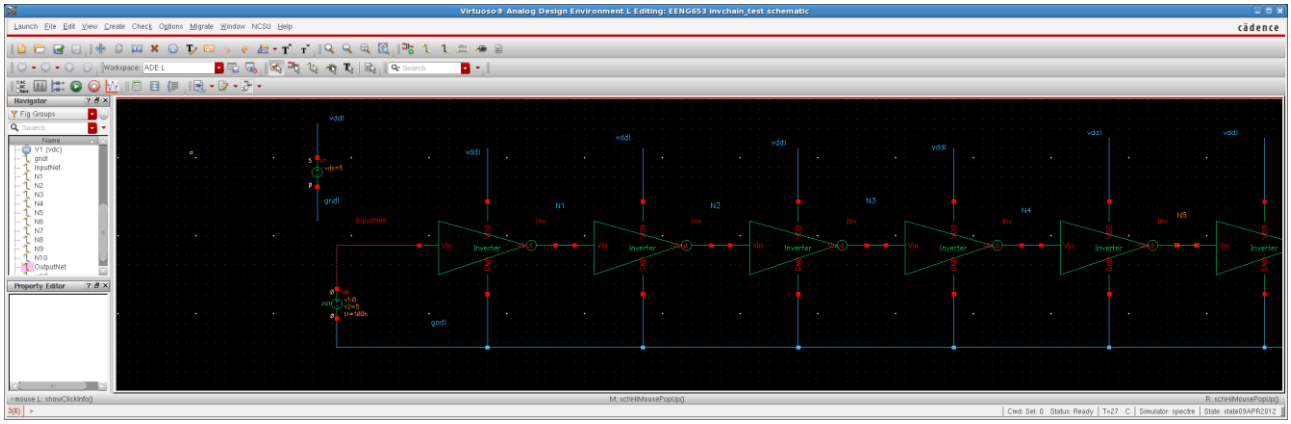
d. We now create a hierarchical schematic that uses the 'inv' symbol that you created. Go to the library manager and open the cell named 'invchain_test'. Edit 'invchain_test' by moving the load capacitor to the right and inserting 10 additional inverters, to create a chain of 11 total inverters. Connect the output of each inverter to the input of the next inverter using wires (review the hotkeys for these functions as reviewed in earlier sections). Connect the output of the last inverter to the load capacitor. Name each net (the nets in this example are called 'InputNet,' 'N1,' 'N2,' … 'OutputNet.') If you make a mistake, you can always do 'Edit → Undo' and try again. Don't be afraid if you make mistakes, just Undo and start over. Connect each inverter to vdd! and gnd! as shown in the image. Check & Save your schematic and inspect the CIW to make sure that it is successful.



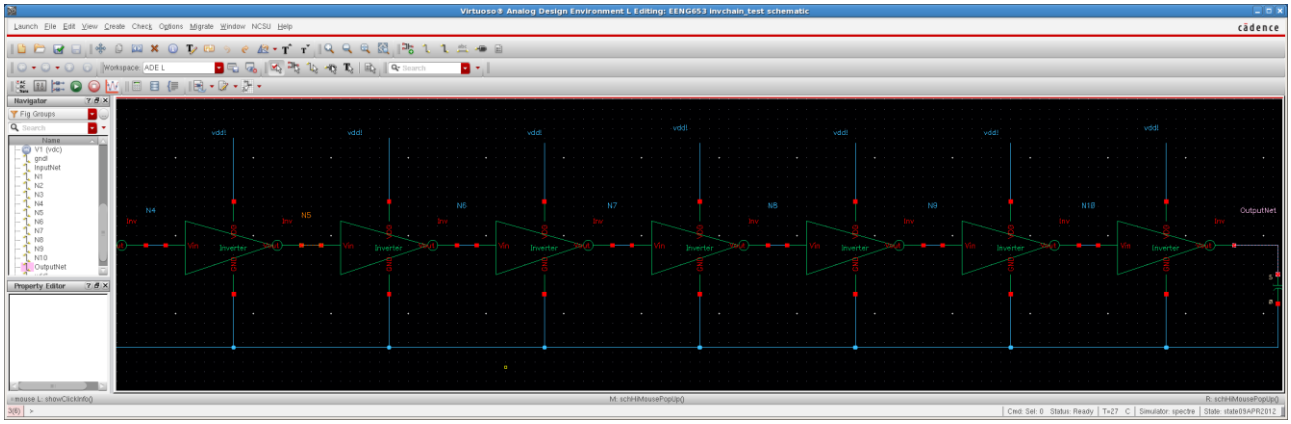
e. Zoom in on the inverter chain and inspect the voltage sources V1 and V2 to make sure they and the first inverter appear as shown in the image below.



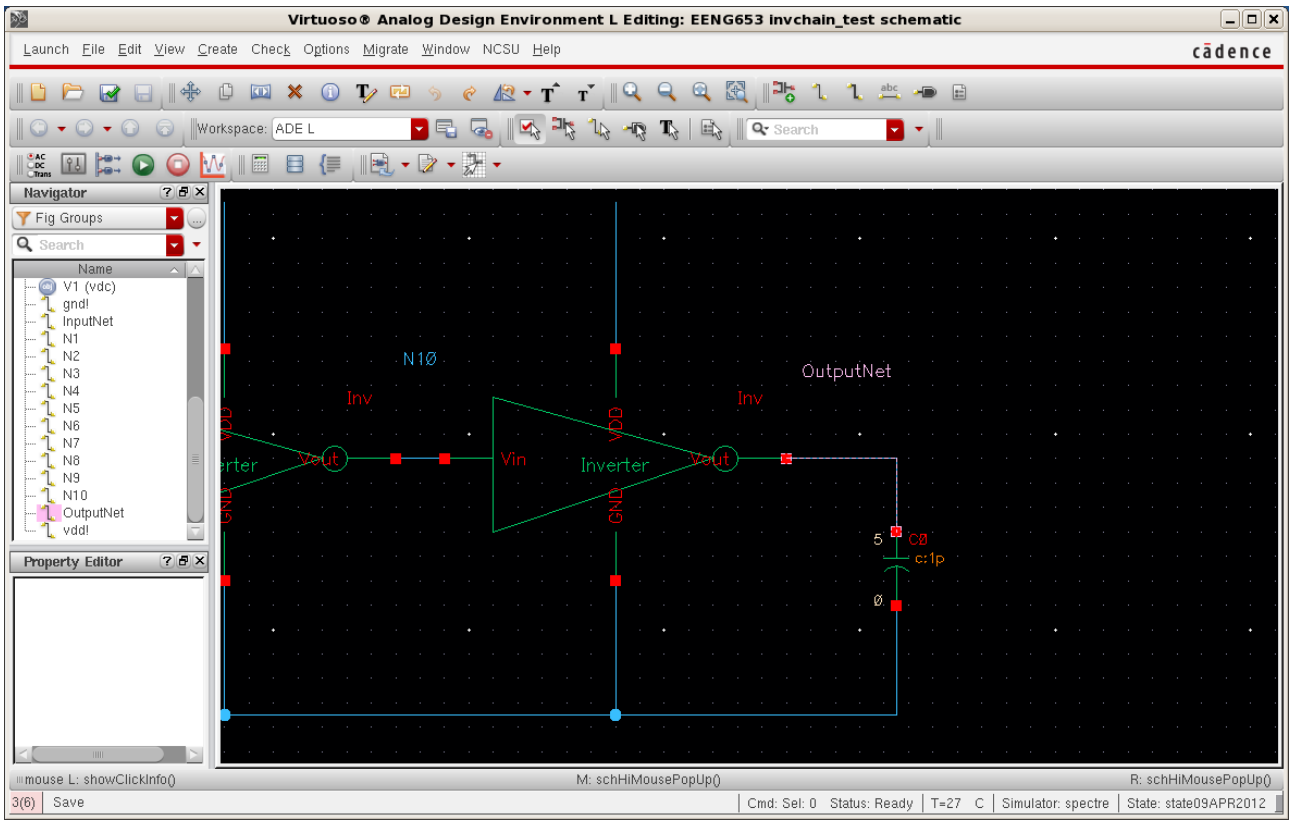
f. Zoom out from the inverter chain, and the first six inverters are shown as in the image below.



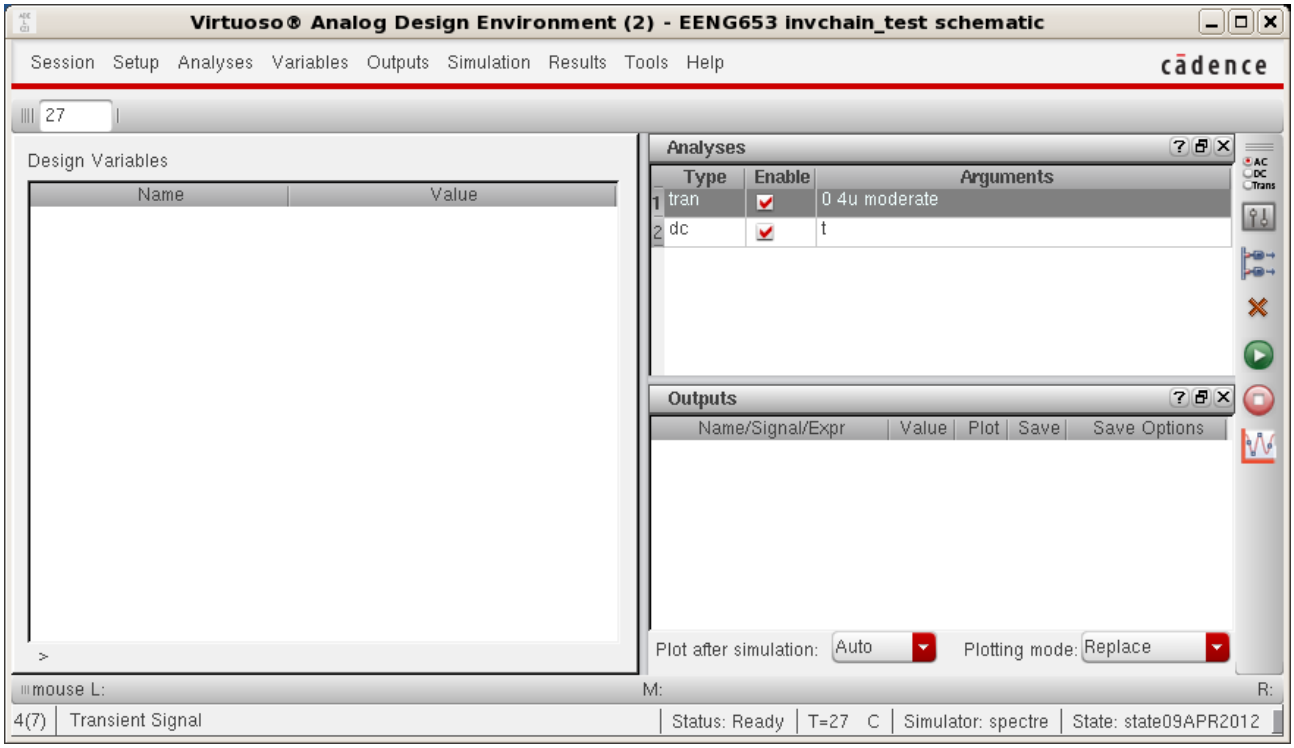
g. The last seven inverters and the load capacitor are shown in the image below.



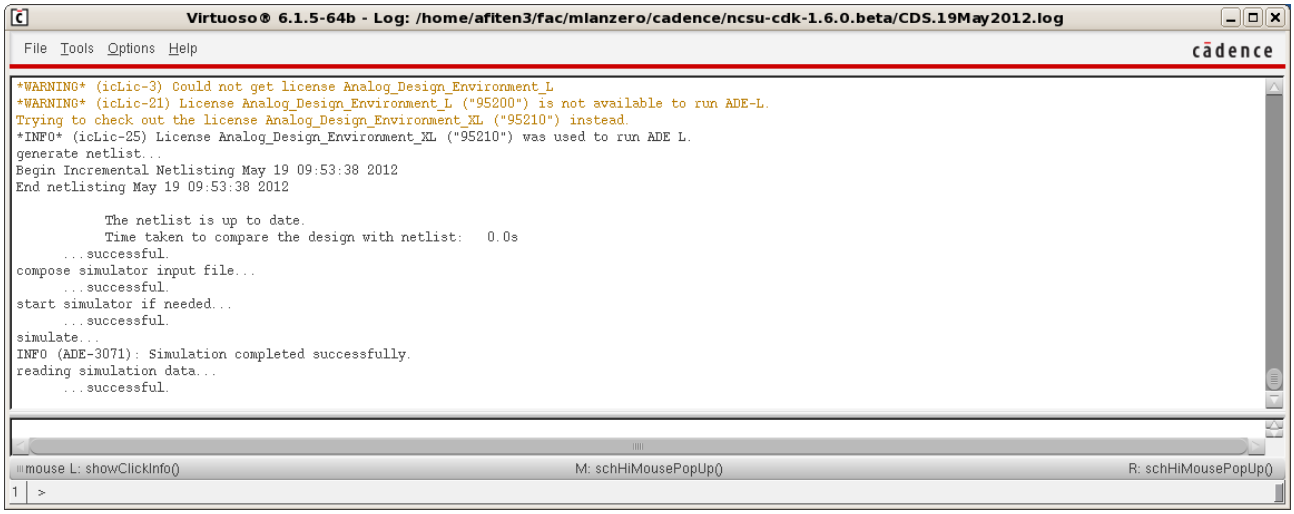
h. Zoom in on the eleventh inverter and the load capacitor in the 'invchain_test' schematic, and it will look as shown in the image below.



i. Set up a transient simulation and a dc simulation using the Virtuoso Analog Design Environment. Use the same series of steps that you used in an earlier section, and refer to it if you forget some of the steps. As a reminder, be sure to point to the device models for the nfet and pfet; point to spectre as the simulator, choose trans and dc analyses; save all the outputs; generate a netlist; run the simulation. The transient simulation is set for 4 microseconds, as shown in the image below.



j. Inspect the CIW to make sure that the simulation completes successfully, as shown in the image below.



k. The netlist for this inverter chain is shown in the image below.

/home/afiten3/fac/mlanzero/cadence/ncsu-cdk-1.6.0.beta/invchain_test/spectre/schematic/netlist/input.scs

File Help cadence

```
// Generated for: spectre
// Generated on: May 19 09:53:33 2012
// Design library name: EENG653
// Design cell name: invchain_test
// Design view name: schematic
simulator lang=spectre
global 0 vdd!
include "/apps/vlsi/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06N.m"
include "/apps/vlsi/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06P.m"

// Library name: EENG653
// Cell name: inv
// View name: schematic
subckt inv GND VDD Vin Vout
    N0 (Vout Vin GND GND) ami06N w=1.5u l=600n as=2.25e-12 ad=2.25e-12 \
        ps=6u pd=6u m=1 region=sat
    P0 (Vout Vin VDD VDD) ami06P w=4.5u l=600n as=6.75e-12 ad=6.75e-12 \
        ps=12.0u pd=12.0u m=1 region=sat
ends inv
// End of subcircuit definition.

// Library name: EENG653
// Cell name: invchain_test
// View name: schematic
V0 (InputNet 0) vsource type=pulse val0=0 val1=5 period=2u rise=100n \
        fall=100n width=1u
V1 (vdd! 0) vsource type=dc dc=5
C0 (OutputNet 0) capacitor c=1p m=1
I10 (0 vdd! N10 OutputNet) inv
I9 (0 vdd! N9 N10) inv
I8 (0 vdd! N8 N9) inv
I7 (0 vdd! N7 N8) inv
I6 (0 vdd! N6 N7) inv
I5 (0 vdd! N5 N6) inv
I4 (0 vdd! N4 N5) inv
I3 (0 vdd! N3 N4) inv
I2 (0 vdd! N2 N3) inv
I1 (0 vdd! N1 N2) inv
I0 (0 vdd! InputNet N1) inv
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12 temp=27 \
    tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5 maxwarns=5 \
    digits=5 cols=80 pivrel=1e-3 sensfile="../psf/sens.output" \
    checklimitdest=psf
tran tran stop=4u errpreset=moderate write="spectre.ic" \
    writefinal="spectre.fc" annotate=status maxiters=5
finalTimeOP info what=oppoint where=rawfile
dcOp dc write="spectre.dc" maxiters=150 maxsteps=10000 annotate=status
dcOpInfo info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts  where=rawfile
saveOptions options save=allpub
```

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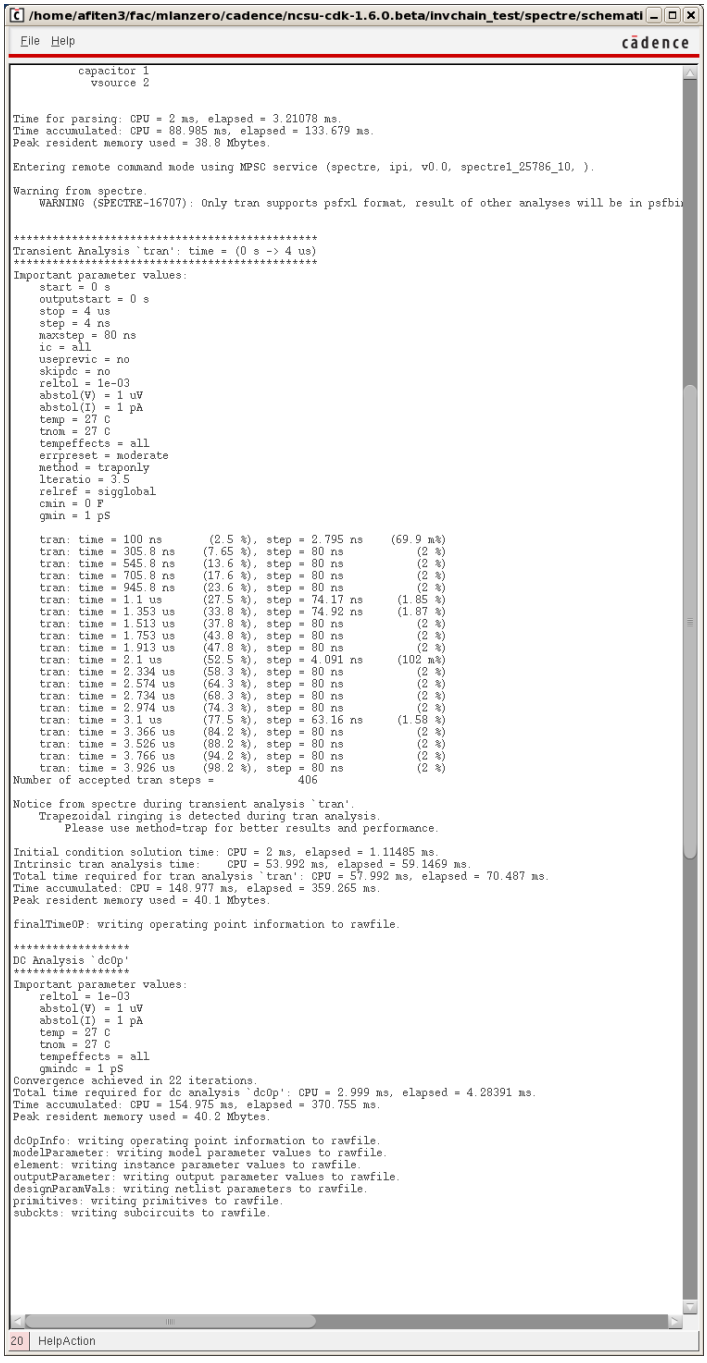
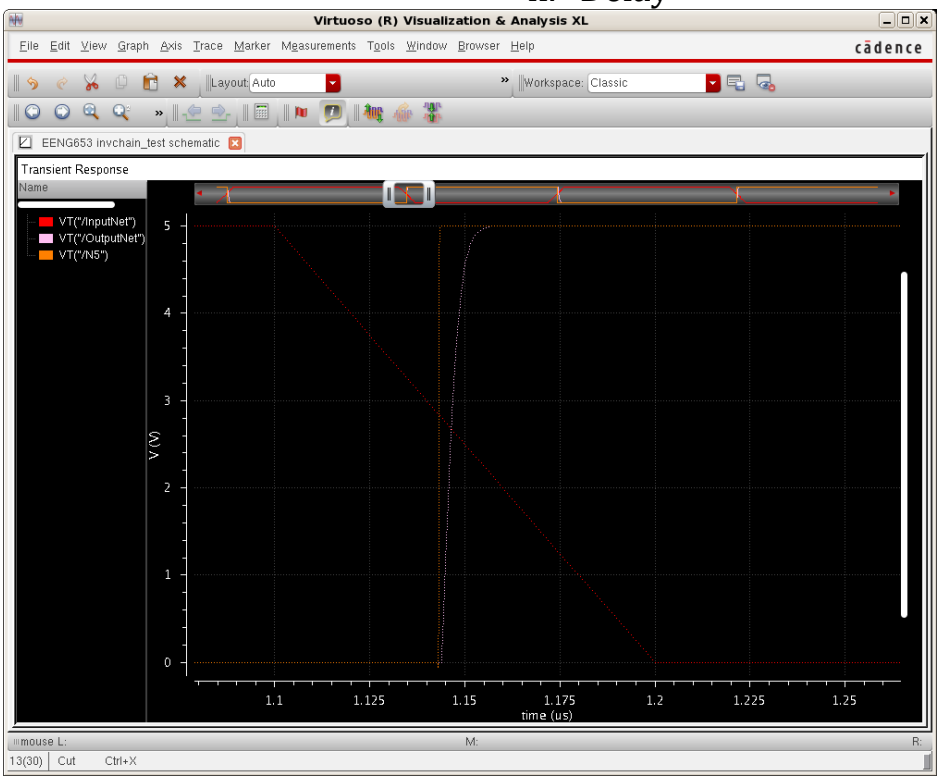
l. The simulation output file (upper half) is shown in the image below.

m. The simulation output file (lower half) is shown in the image below.

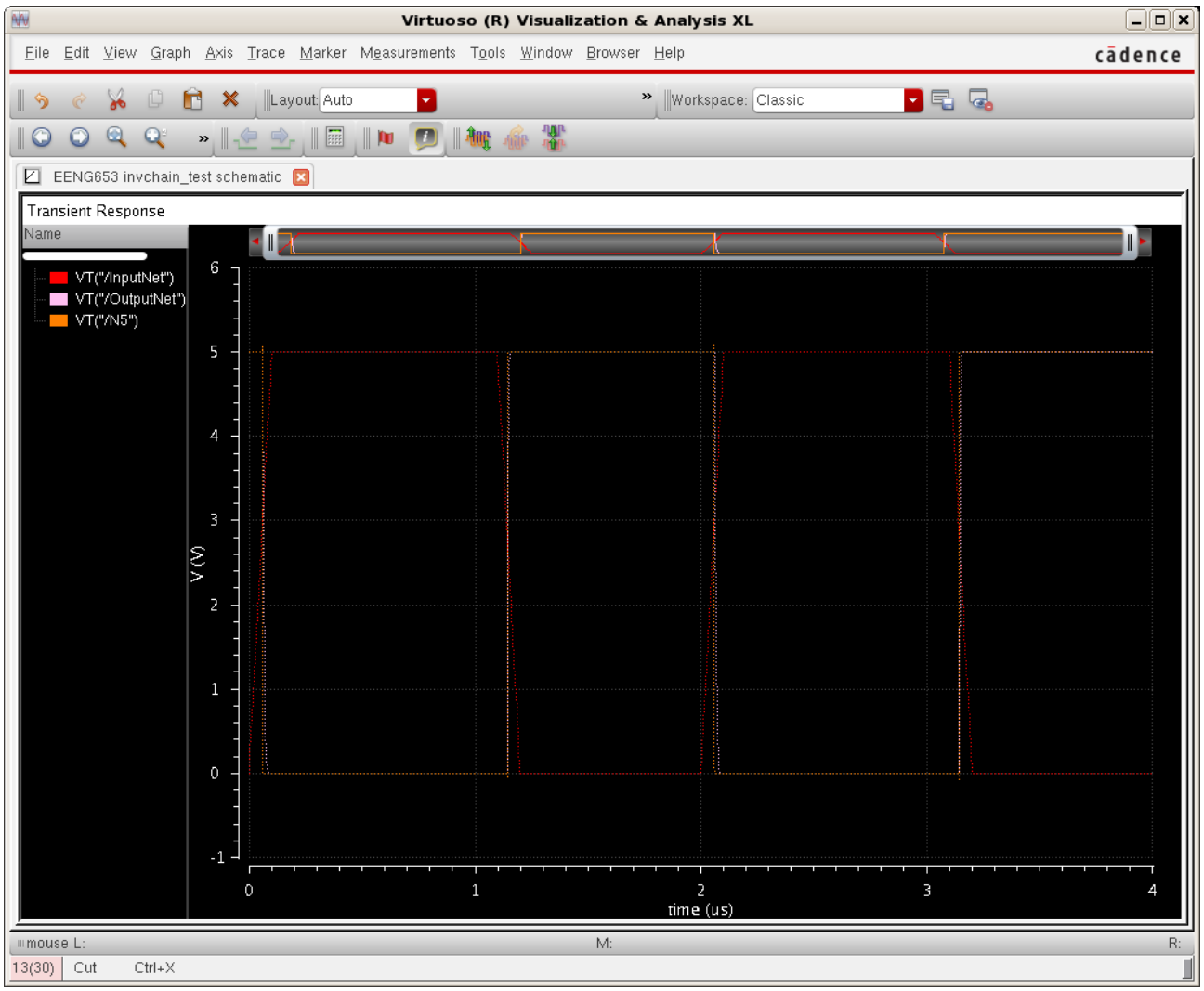


n. After the simulation completes successfully, annotate the results and then perform a direct plot of the transient signals. The image below displays the waveforms of the transient signals 'InputNet,' 'OutputNet,' and 'N5' near the time t = 1.1 microseconds to t = 1.2 microseconds. Values for the following quantities can be obtained for each inverter pair:

a. For the falling transition of the input waveform
   i. Fall time
   ii. Delay
b. For the rising transition of the input waveform
   i. Rise time
   ii. Delay



o. The complete waveforms for 'InputNet,' 'OutputNet,' and 'N5' in the time range t = 0 microseconds to t = 4 microseconds are shown in the image below.



p. You can now save the state for this simulation. Save the state as the name 'state-invchain.' You will load this state in the next section, when you create a ring oscillator. The procedure to save a state was discussed in the previous sections. Refer to the previous sections if you forget how to save the state of your simulation.

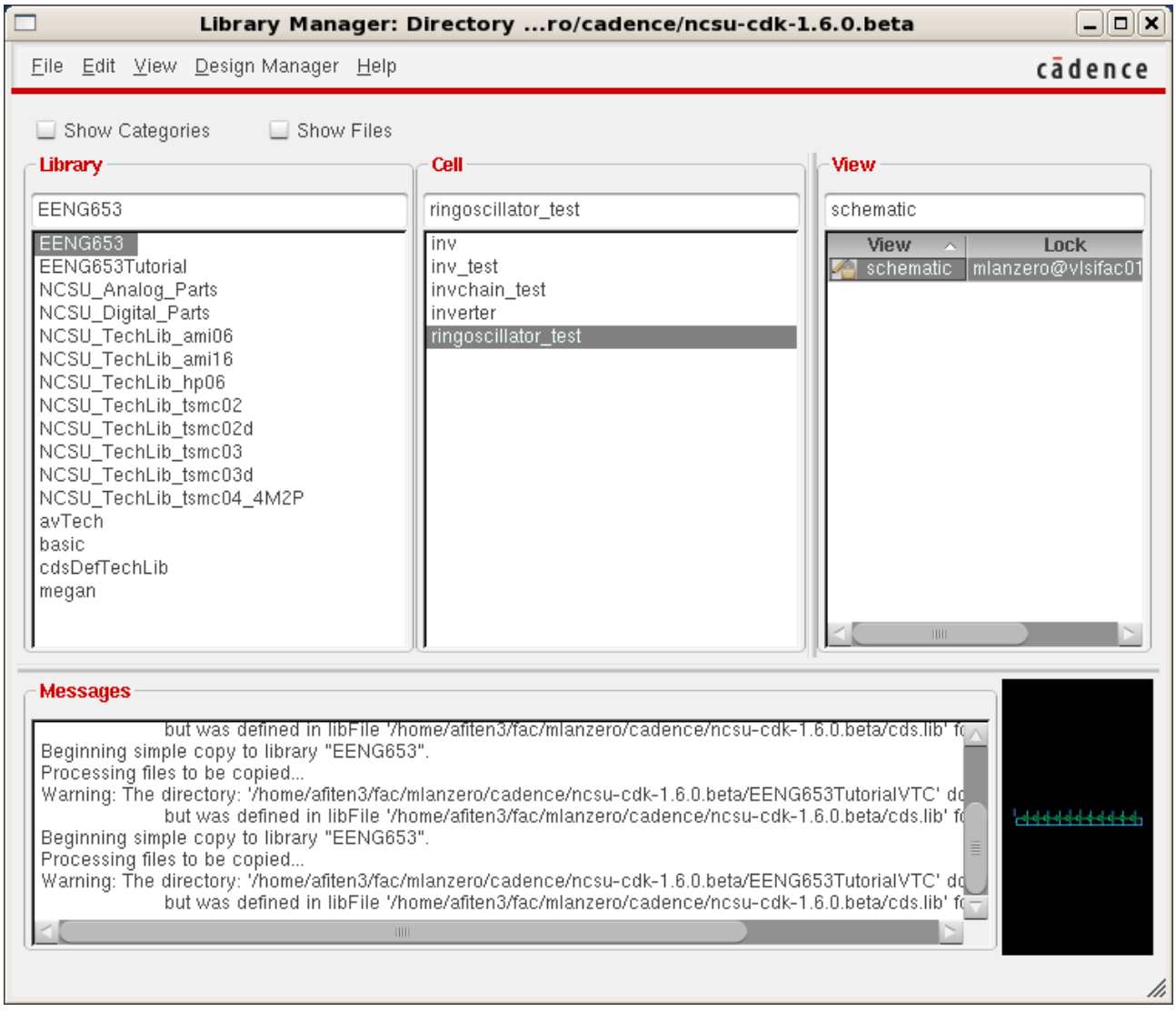
q. You can now increase the value of the load capacitor. Values for the following quantities can be obtained for each value of the load capacitor for each inverter pair. Note that the values of the widths of the successive inverters may need to be increased in order to drive the load capacitor:

a. For the falling transition of the input waveform
    i. Fall time
    ii. Delay
b. For the rising transition of the input waveform
    i. Rise time
    ii. Delay

r. You have now completed this section on the inverter chain.

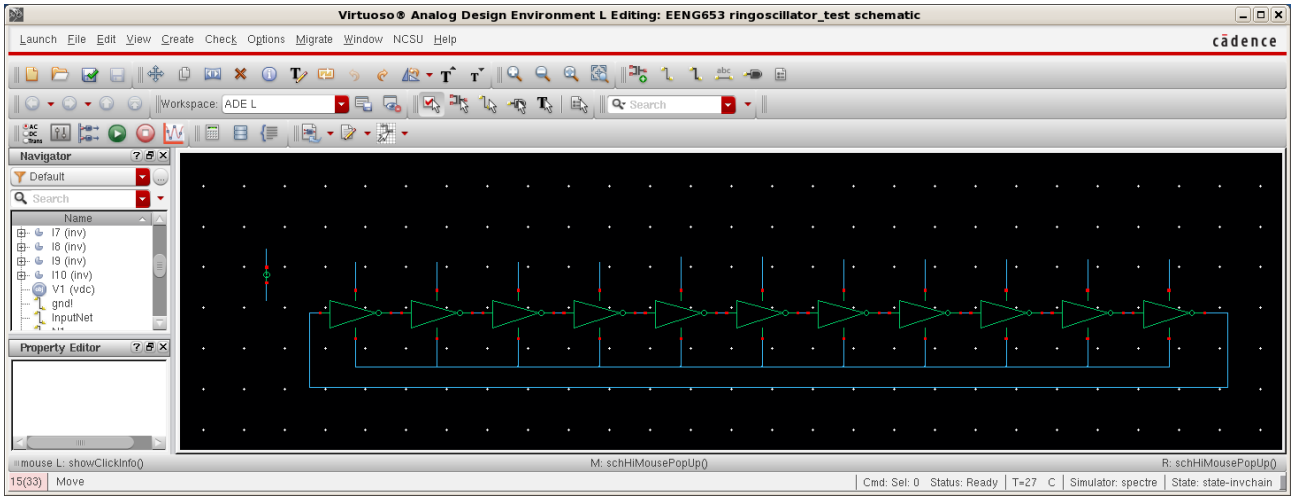
25. Ring Oscillator

a. In this section, you will create and simulate a ring oscillator that is composed of 11 inverters. In the 'EENG653' library, copy the 'invchain_test' cell to a new cell called 'ringoscillator_test' as shown in the image below. Make sure that the 'inv' instantiated in the 'ringoscillator_test' library still points to the 'inv' cell in the 'EENG653' library.



b. Open the 'ringoscillator_test' cell schematic and wire the 11 inverters into a ring as shown in the image below. You will need to delete the load capacitor. Note that the output node of the 11th inverter is connected to the input node of the first inverter as shown in the image.

Check & Save the schematic and make sure the check & save completes successfully by inspecting the CIW. Make sure there are no errors or warnings. If you have errors and/or warnings, go back and fix your schematic. Then, rerun Check & Save your schematic to make sure it completes successfully.

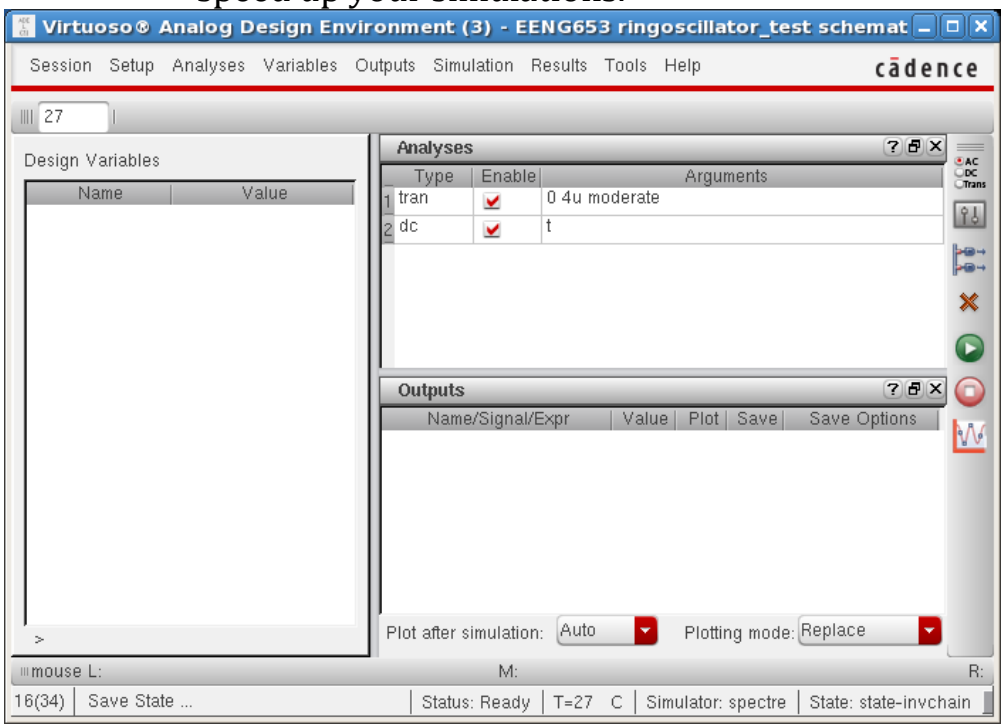


c. When you are creating a hierarchical schematic that contains many levels of hierarchy, you may find it helpful to make modifications on different cells that are instantiated in the schematic without closing and opening different schematics. You can edit or read different cells through a process referred to as *traversing the hierarchy* of the schematic. You can traverse the hierarchy upwards, and you can also traverse the hierarchy downwards. The image below shows how to descend the hierarchy to read a cell in a lower level of the hierarchy (change the radio button to 'edit' if you want to edit the cell in the lower level of the hierarchy.)

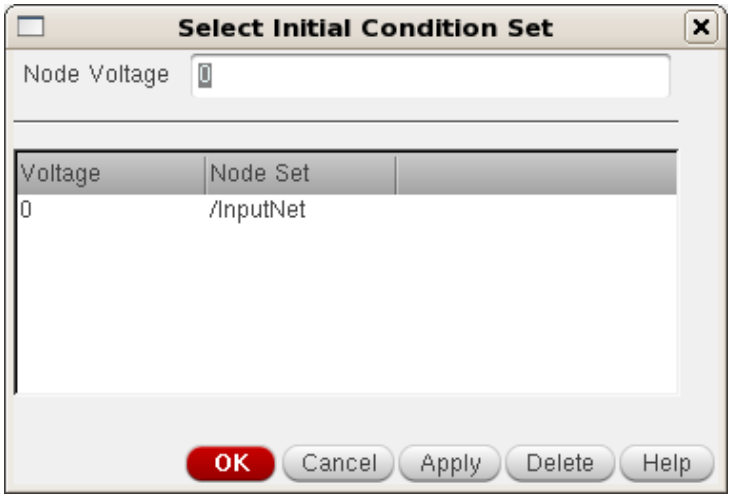
For example, to make modifications to or to read the 'inv' schematic contained in the 'ringoscillator_test' schematic, click on "Edit → Hierarchy → Descend Edit" or "Edit → Hierarchy → Descend Read." The 'Descend' window will appear as shown in the image below. Click OK in the window. The inverter should now appear. You can now edit it if you want; be sure to Check & Save after editing. This will change all instances of 'inv' schematic in your hierarchical schematics.

d. Now you will perform a transient simulation to learn about the operation of the ring oscillator. In the Virtuoso Schematic window, launch the Analog Design Environment (ADE). As in previous sections, you will need to set up the simulation: select the simulator (spectre), load the model files, choose a transient analysis (4 microseconds stop time; moderate accuracy default), choose a dc analysis, print all output signals (allpub), generate the netlist, and run the simulations. You may find it helpful to load the state of the 'state-invchain' that you saved in the previous section. Review the previous sections if you do not recall how to set up these simulations with spectre. Your Analog Design Environment window will appear as shown in the image below.

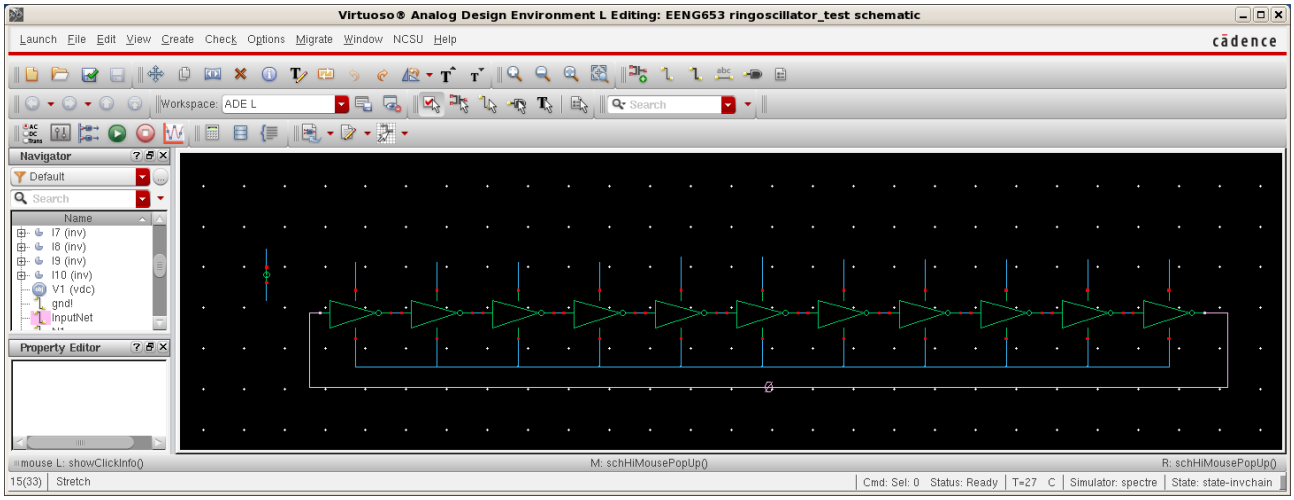
For large schematics, you will want to save only a few signals to speed up your simulations.



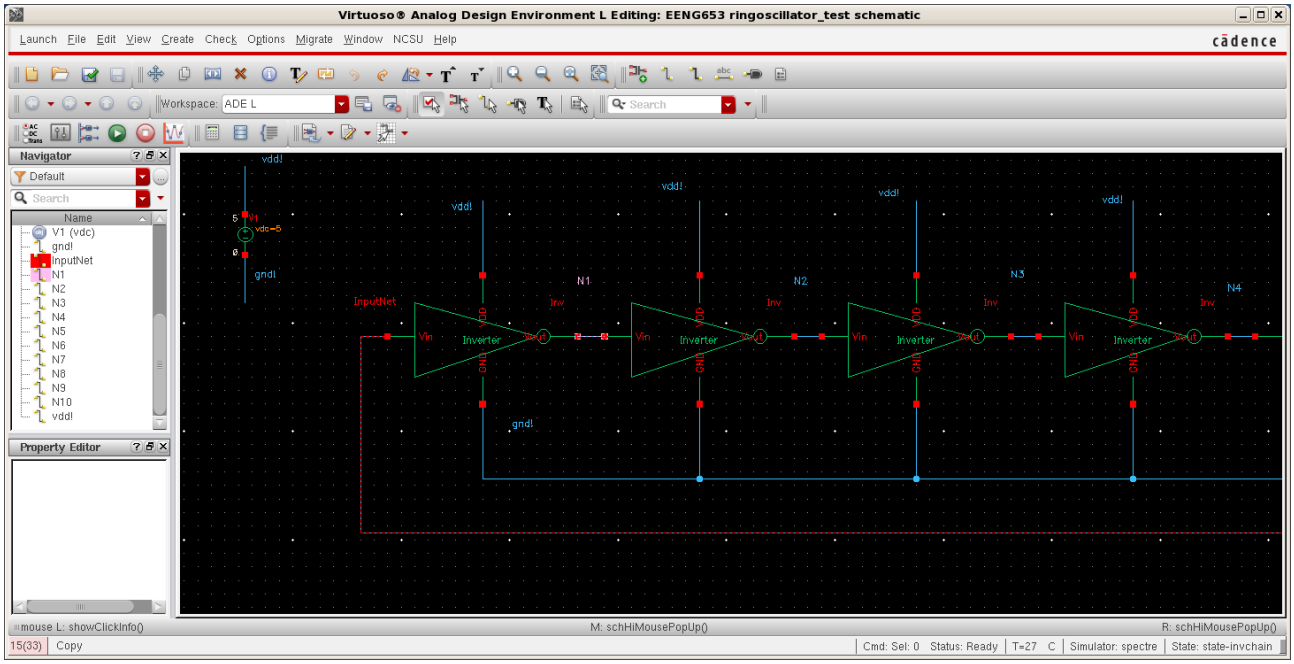
e. To help with convergence of the simulation of the ring oscillator, you will now set up an initial condition which is to initialize the input node to zero (0) at the left-mode inverter. Click on 'Simulation → Convergence Aids → Initial Condition.' A window entitled "Select Initial Condition Set' will appear.



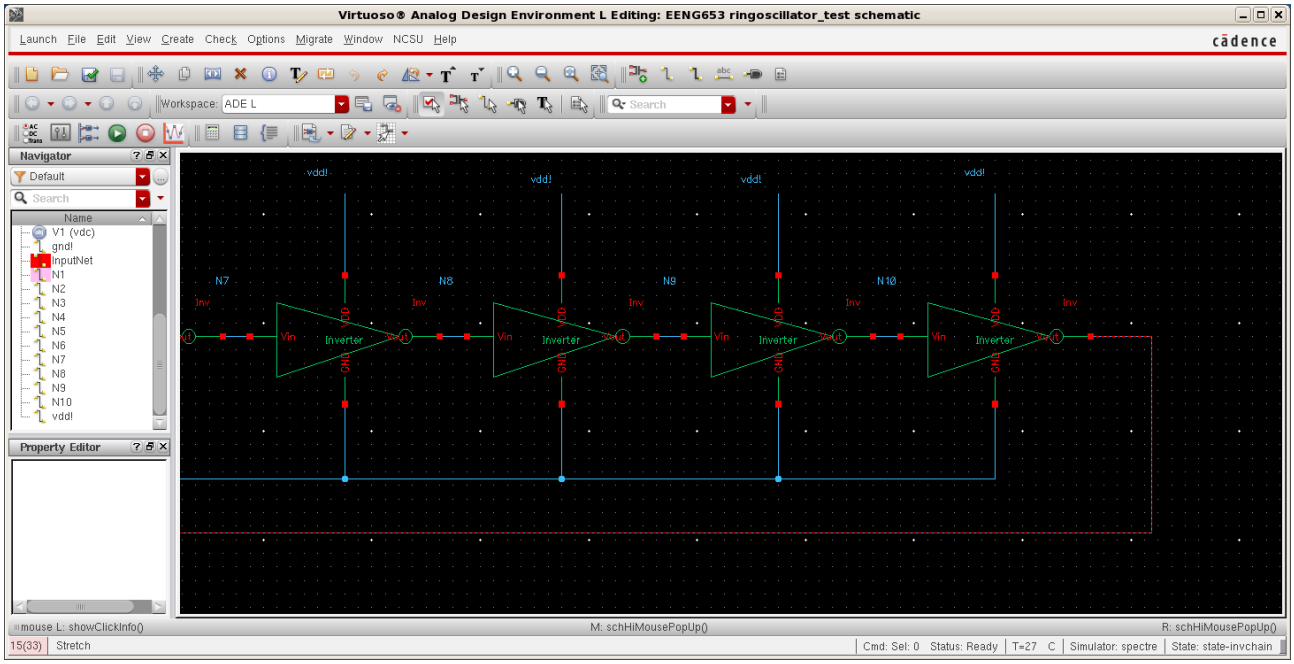
f. Then click on the left-most node in the schematic, as shown in the image below. The 'Select Initial Condition Set' window will show that the 'InputNet' voltage is set to '0.' Note that the net itself becomes highlighted in the 'ringoscillator_test' schematic, and a large '0' is written on top of the net.



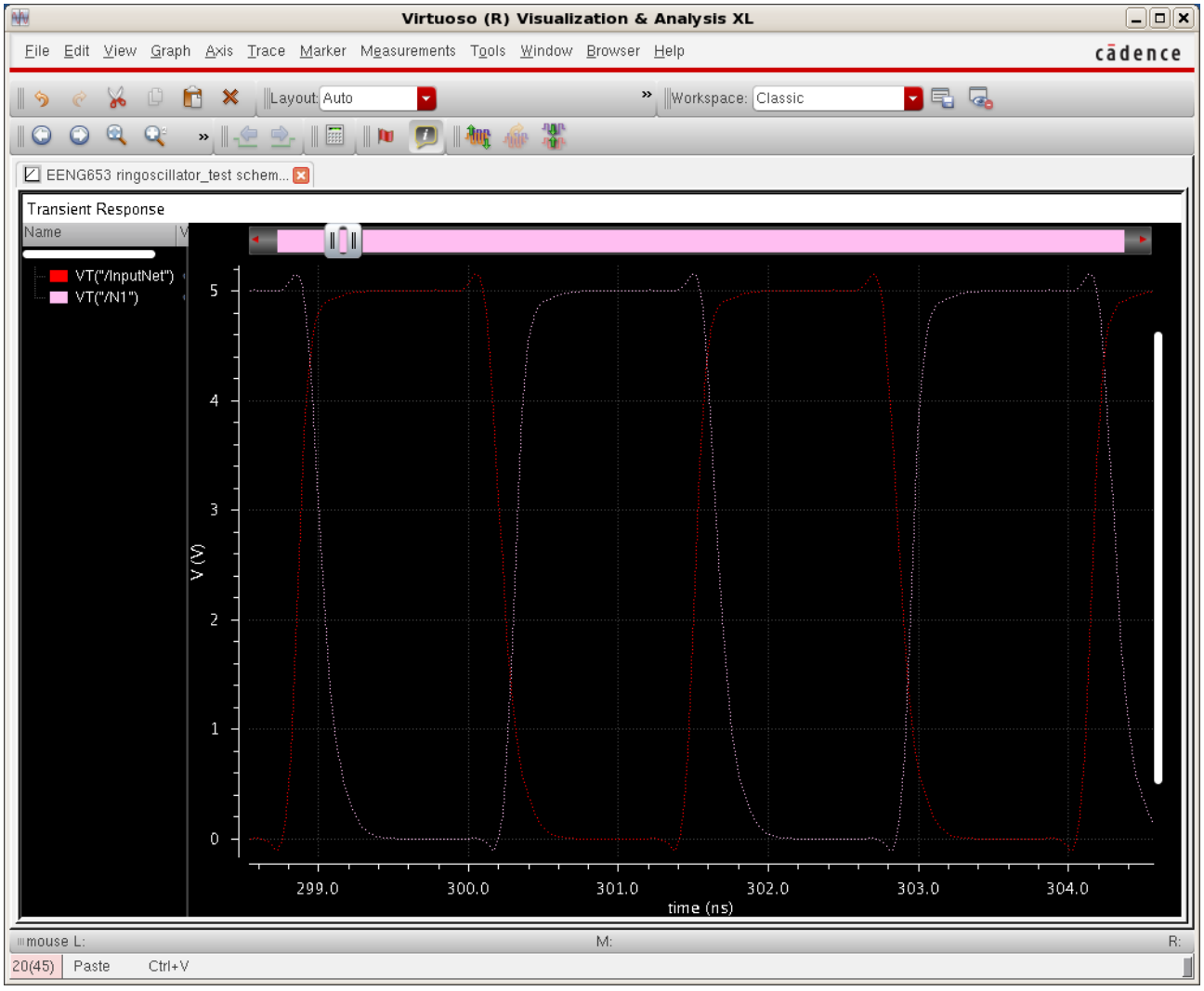
g. The left side of the 'ringoscillator_test' schematic is shown in the image below after zooming in on the initial inverters.



h. The right side of the ring oscillator inverter chain is also shown in the image below after zooming in on the inverters. Notice the output (11th) inverter.



i. You can now generate the netlist and run the simulation. Launch the Visualization & Analysis XL tool and generate plots of the waveforms of the 'InputNet' and the following net (N1, in this case) as shown in the image below. In case there are errors, you will need to go back and correct the errors. You may need to do 'Simulation → Netlist' again if you change the schematic. Remember also that each time you change the schematic, you need to do a 'Check & Save.' You will be able to view the simulation results when there are no errors.



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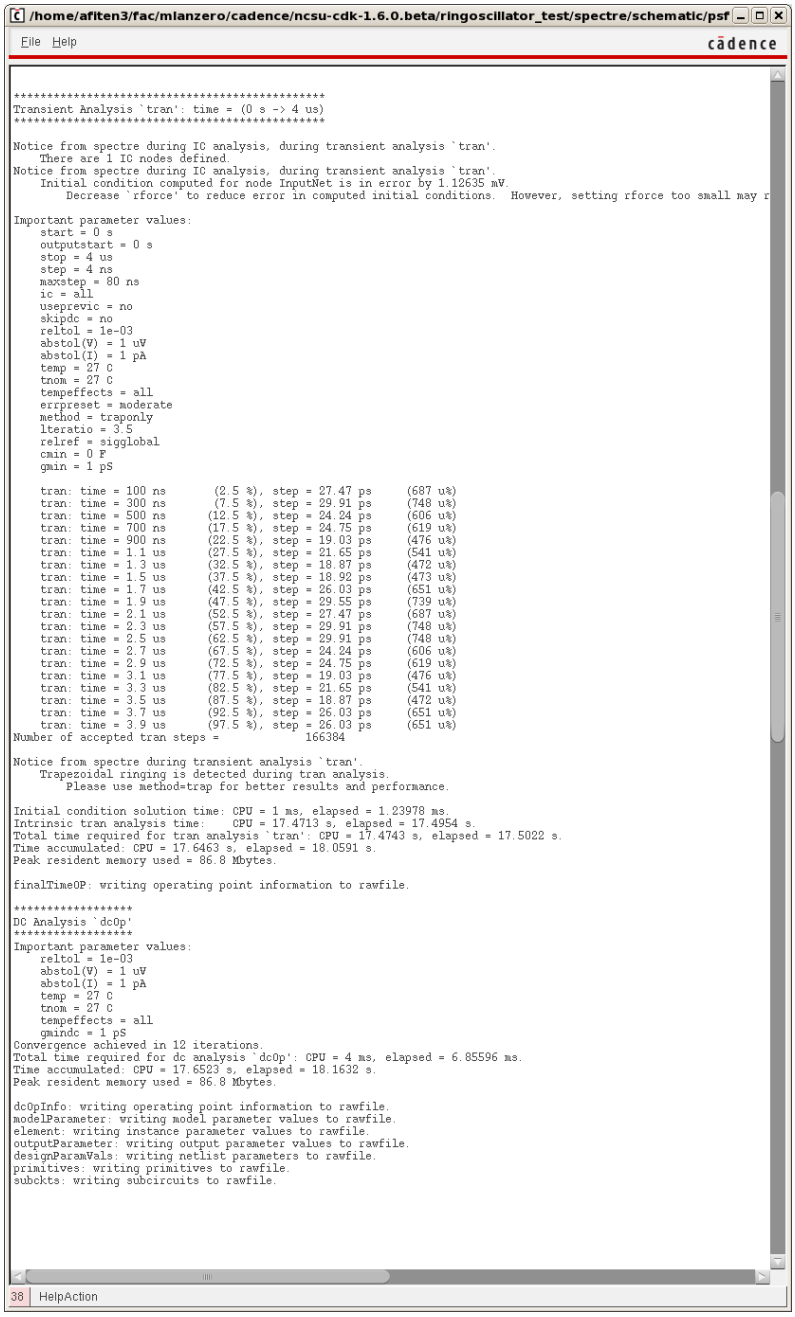
j. The netlist of this ring oscillator is shown in the image below.

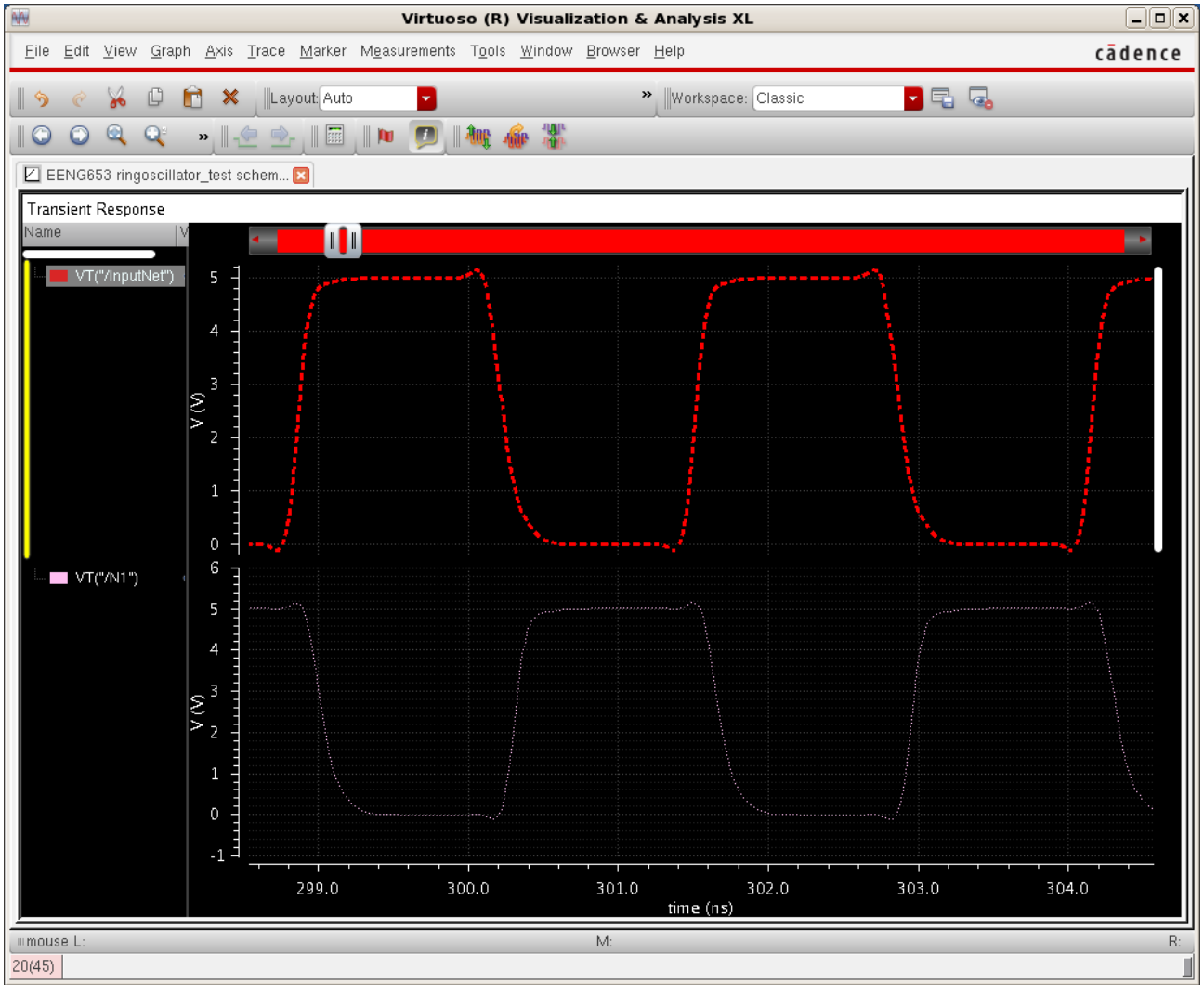
k. The upper part of the file displaying the simulation run is shown in the image below.

l. The lower part of the file displaying the simulation run is shown in the image below.

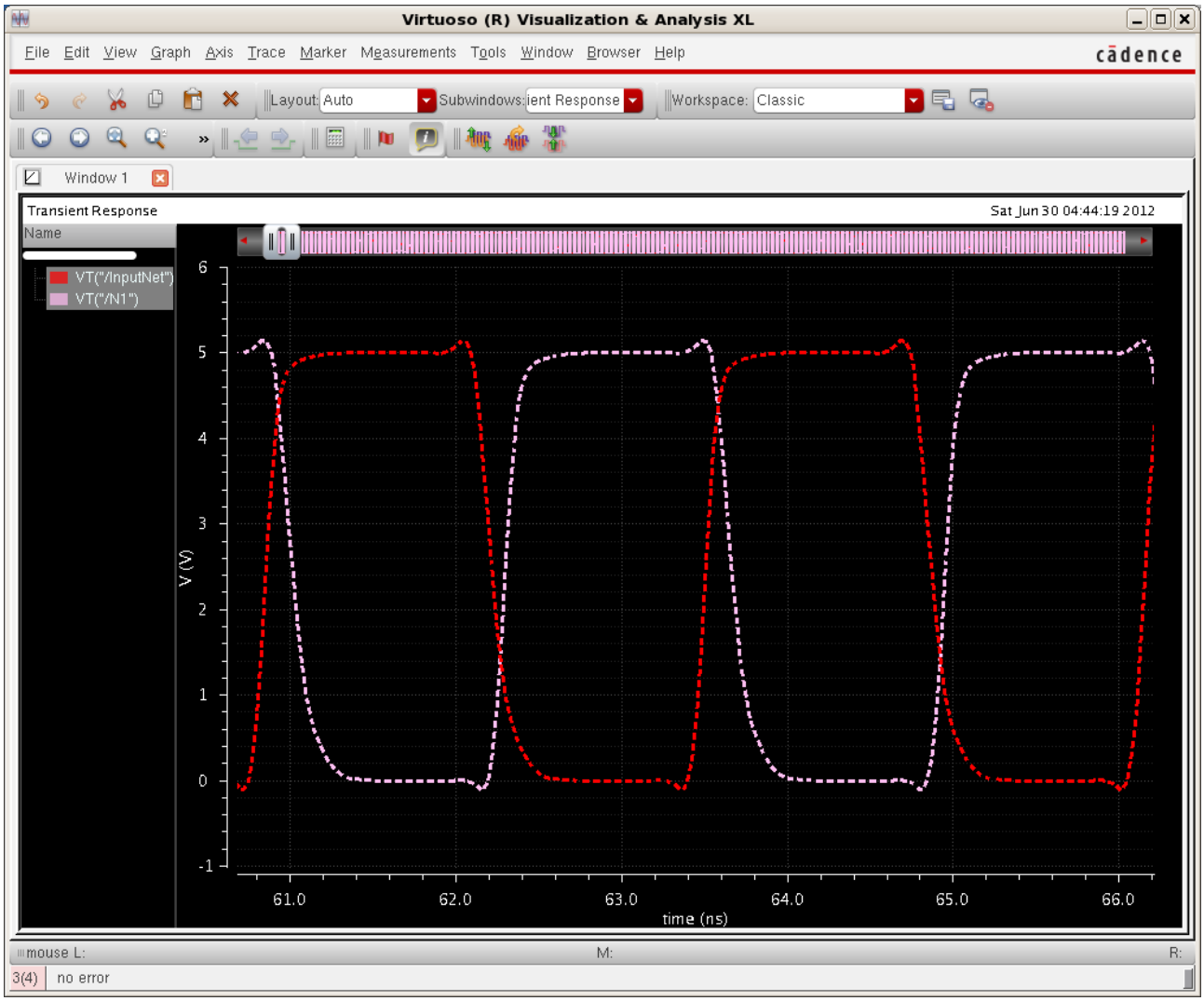


m. You can display the waveforms separately by clicking on the left of the display window and selecting 'Plot to New Strip.'

These waveforms should show the desired results, namely periodic waveforms as we expect for a ring oscillator. You can determine the period of oscillation and measure the inverter delay.



n. You can recombine the waveforms into one set of axes by right clicking in the left section of the Visualization & Analysis window and selecting 'Combine All Analog Traces.' Your Visualization & Analysis XL window will look like the image below. It is a good idea to save your state, such as 'state-ringoscillator,' before exiting the simulator in the event that you would like to redo some of the simulations (then you can load a saved state).



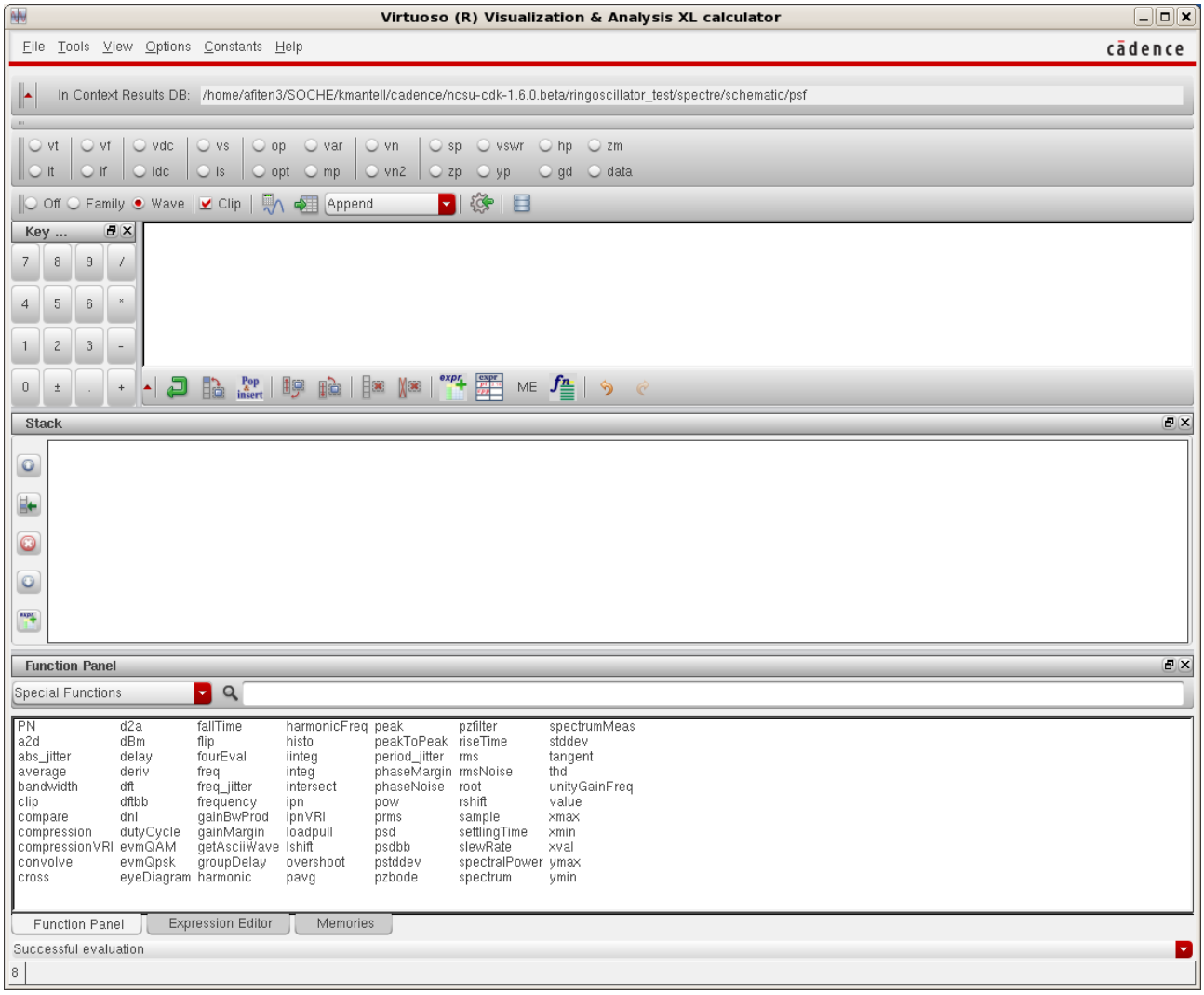
o. Now you have simulated a ring oscillator.

26. Ring Oscillator: Learning to Use the Calculator

a. In this section, you are going to learn how to use the Calculator in Cadence.

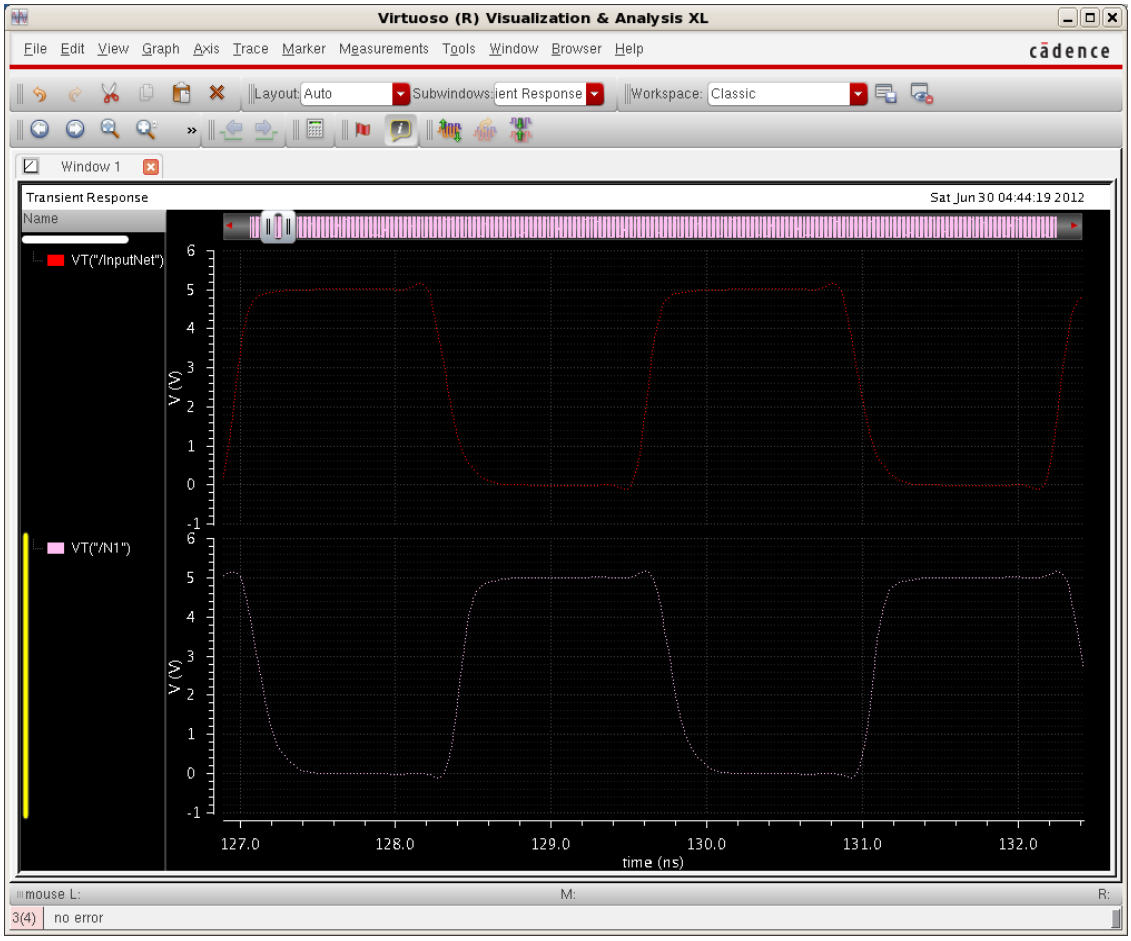
b. The first example will be to show you how to measure the delay in the ring oscillator for the case in which the input waveform has a low-to-high transition (rising transition) and the output waveform therefore has a high-to-low transition (falling transition). You will measure the delay with the Cadence calculator.

c. To open the Cadence Calculator, click on 'Tools → Calculator' in the Analog Environment window, and the 'Calculator' window will appear as shown below. Spend some time to get familiar with the calculator (see Help and the online documents).

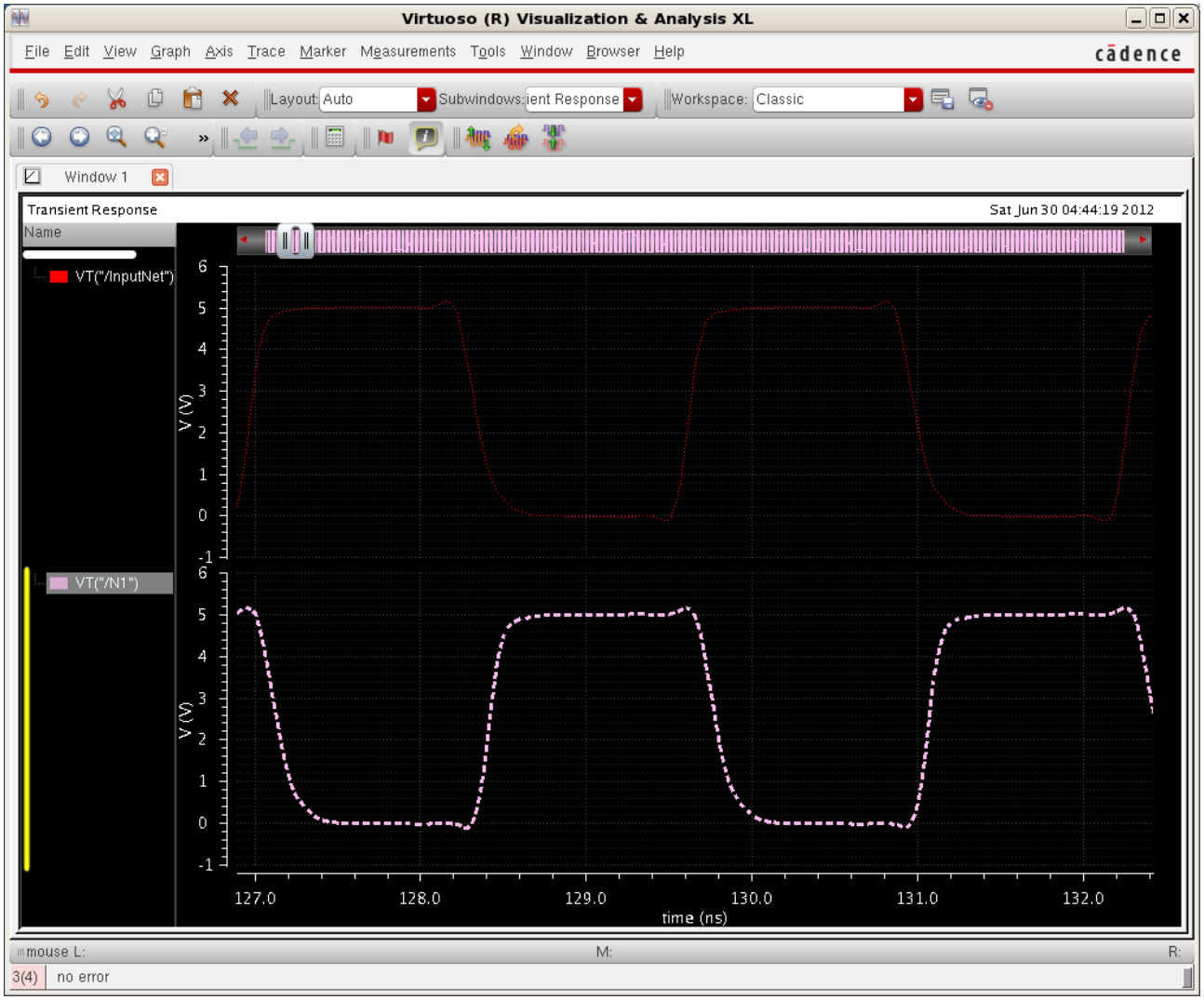


d. The calculator works with a 'stack' (like some HP calculators) in which you first input one or more operands (waveforms), and then you perform an operation on them. After each operation, it is recommended that you clear the stack (clst). To view the stack, you have to enable it (click on the Display Stack).

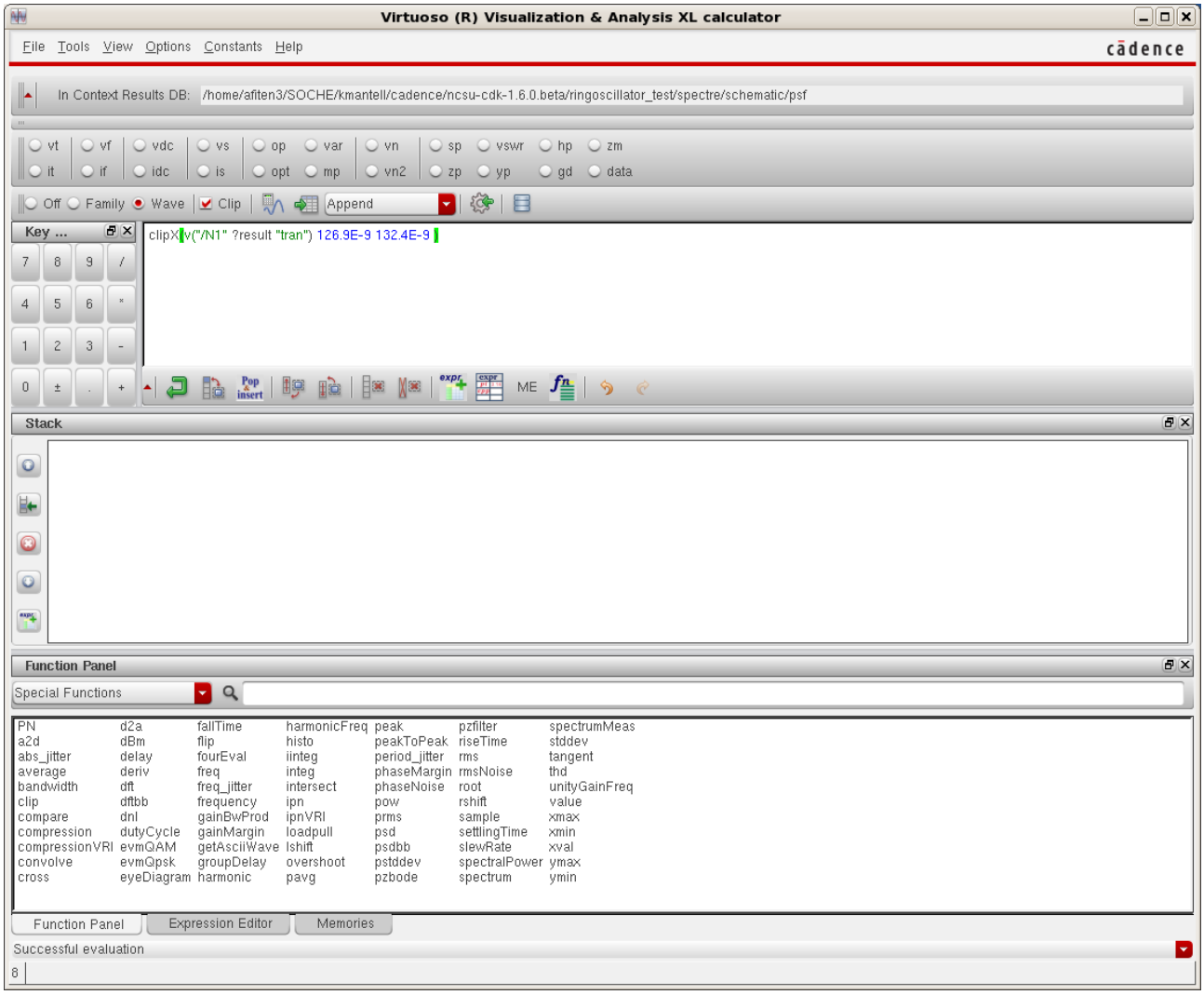
e. Now you will set up your waveforms in the Visualization & Analysis window to look like the ones in the image below. Notice that in this image, the waveform for the InputNet starts low and transitions to Vdd (a low-to-high transition, or rising edge). Notice also that in the image, the waveform for the output net (N1 for the case shown) starts high and transitions to 0 V (a high-to-low transition, or falling edge). This edge is referred to as the first edge, or 'edge 1.'



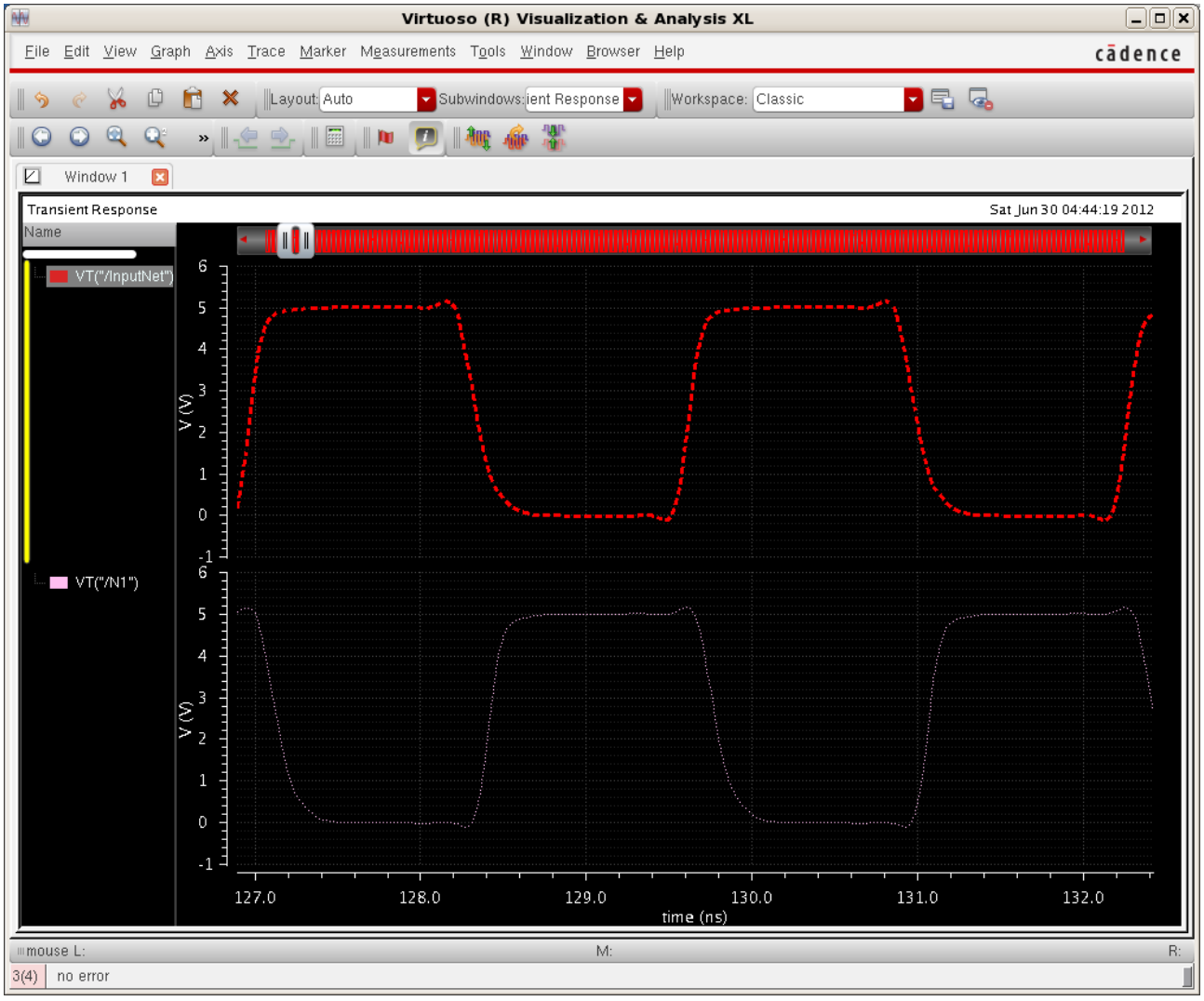
f. Now click on the 'Wave' radio button in the calculator window. Then click on the output waveform (the waveform with the low to high transition, in this case, N1) in the Visualization & Analysis XL window. (Be sure not to click on the wave name on the left-hand side; click instead on the waveform itself).



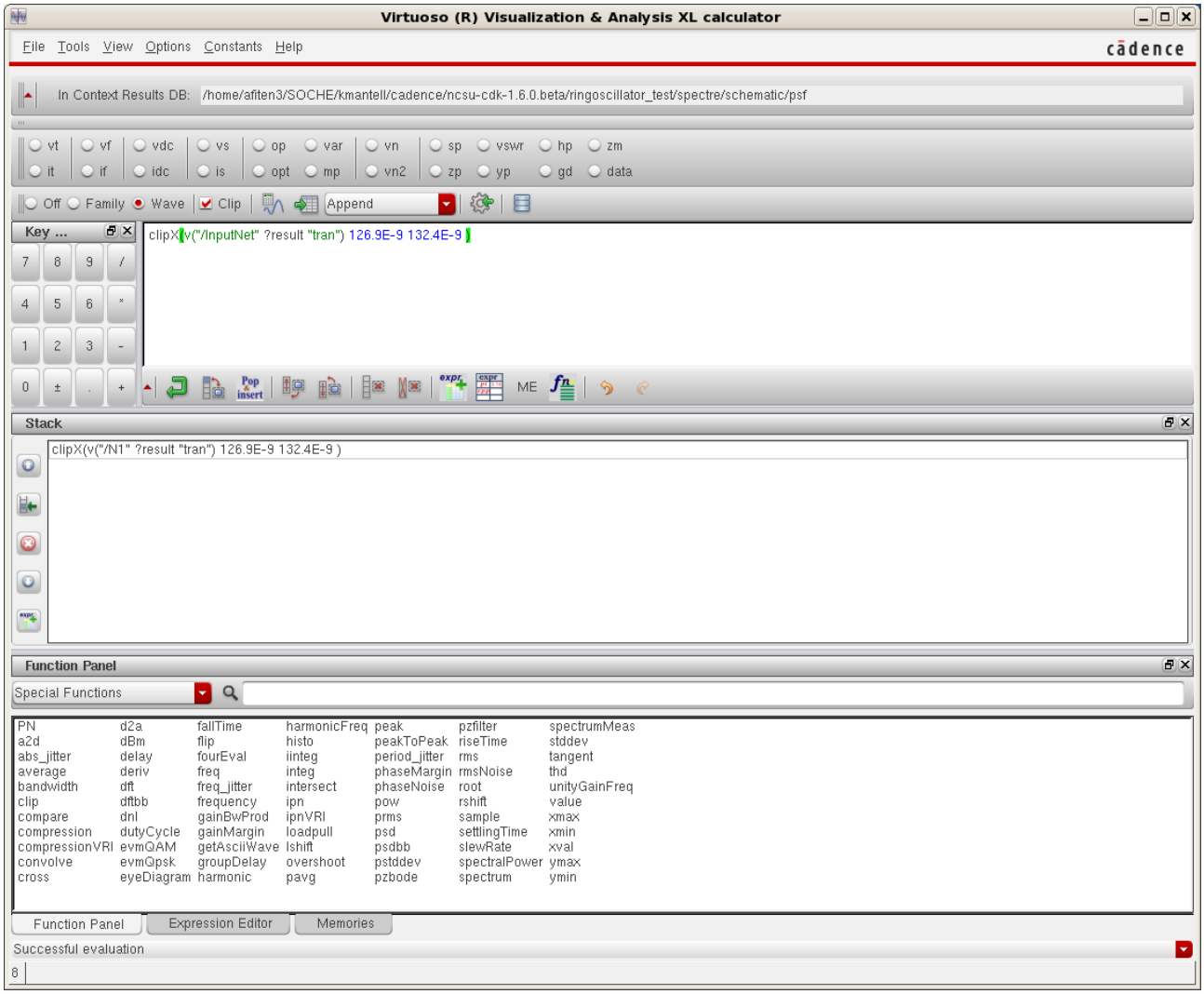
g. A wave name should appear in the calculator window as shown in the image below. This image shows the wave name "N1" in the window. The syntax of the statement in the window, 'clipX,' refers to the zoomed-in portion of the waveform that you are displaying in the waveform window. The syntax of the two values in blue at the end of the statement refer to the start time and to end time of the zoomed-in portion of the viewing window that you selected in the Visualization & Analysis XL window.



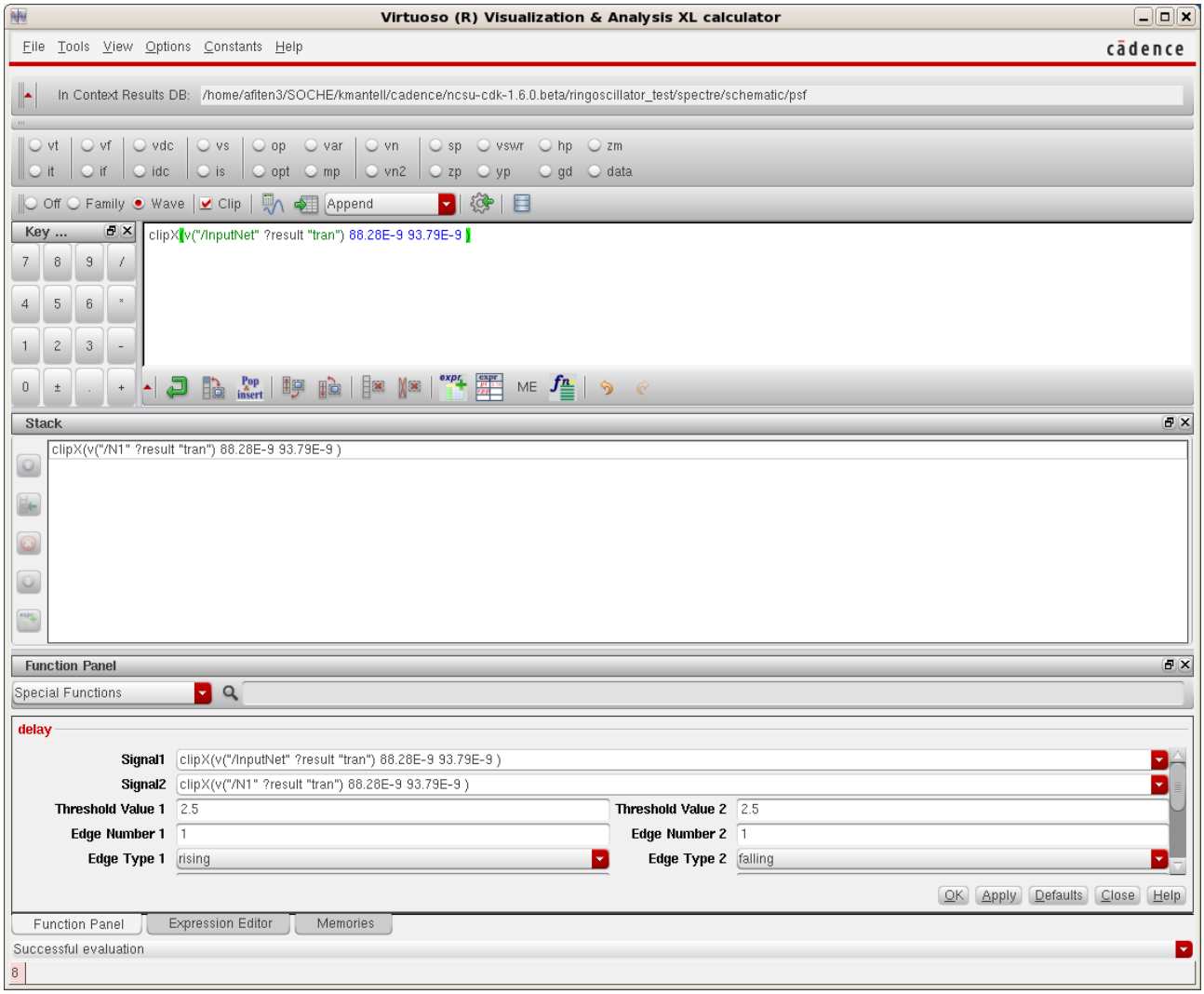
h. Now click on the input waveform wave (it transitions from low to high first). Be sure not to click on the name of the waveform on the left-hand side of the window. You are selecting the rising edge of this waveform, and it is edge 1 (in the zoomed-in portion of the waveform that you display in the window).



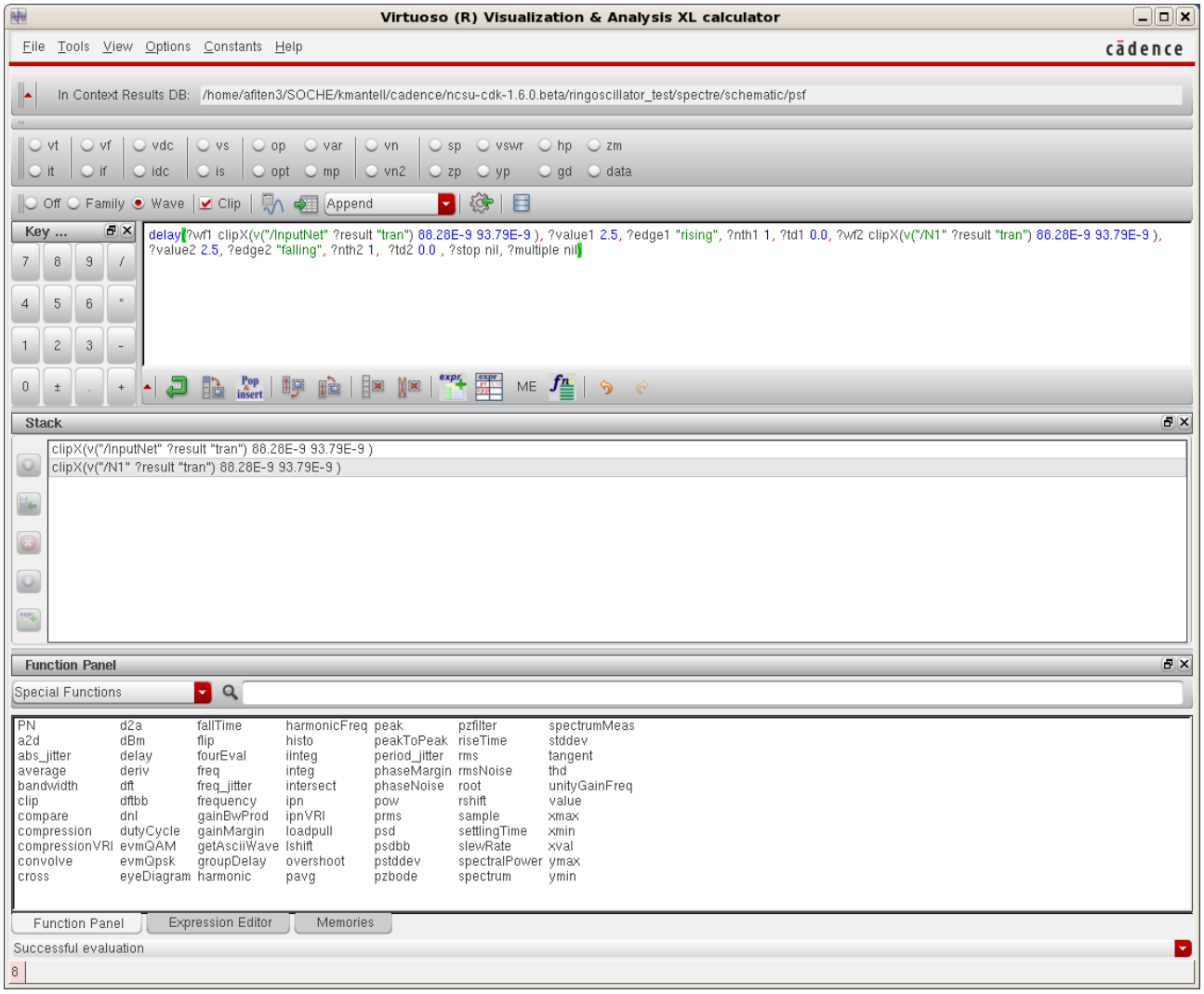
i. Now check in the calculator to verify that the name of the first waveform (N1 in the case shown) has been pushed into the stack and brings the name of the input waveform into the calculator (InputNet in the case shown). Important: Note that the waveforms were entered in reverse order (the late first; then the early one); this is a feature of the stack operation of the calculator.



j. Now move the cursor to 'Special Functions' in the calculator window. Select 'delay'. Fill 2.5 as the threshold values (50% of Vdd = 2.5V since Vdd = 5V). Notice that in the 'delay' section, the name of your first waveform (N1 in this case) is listed as 'Signal2,' and the name of your second waveform (InputNet in this case) is listed as 'Signal1'. For Signal1, set the Edge Number equal to 1. For Signal2, set the Edge Number equal to 1. For Signal 1, set the Edge Type 1 to 'rising.' For Signal 2, set the Edge Type 2 to 'falling.' Then click 'OK'.



k. Notice the change in the calculator window. The entry has now been expanded to show the delay calculation expression.



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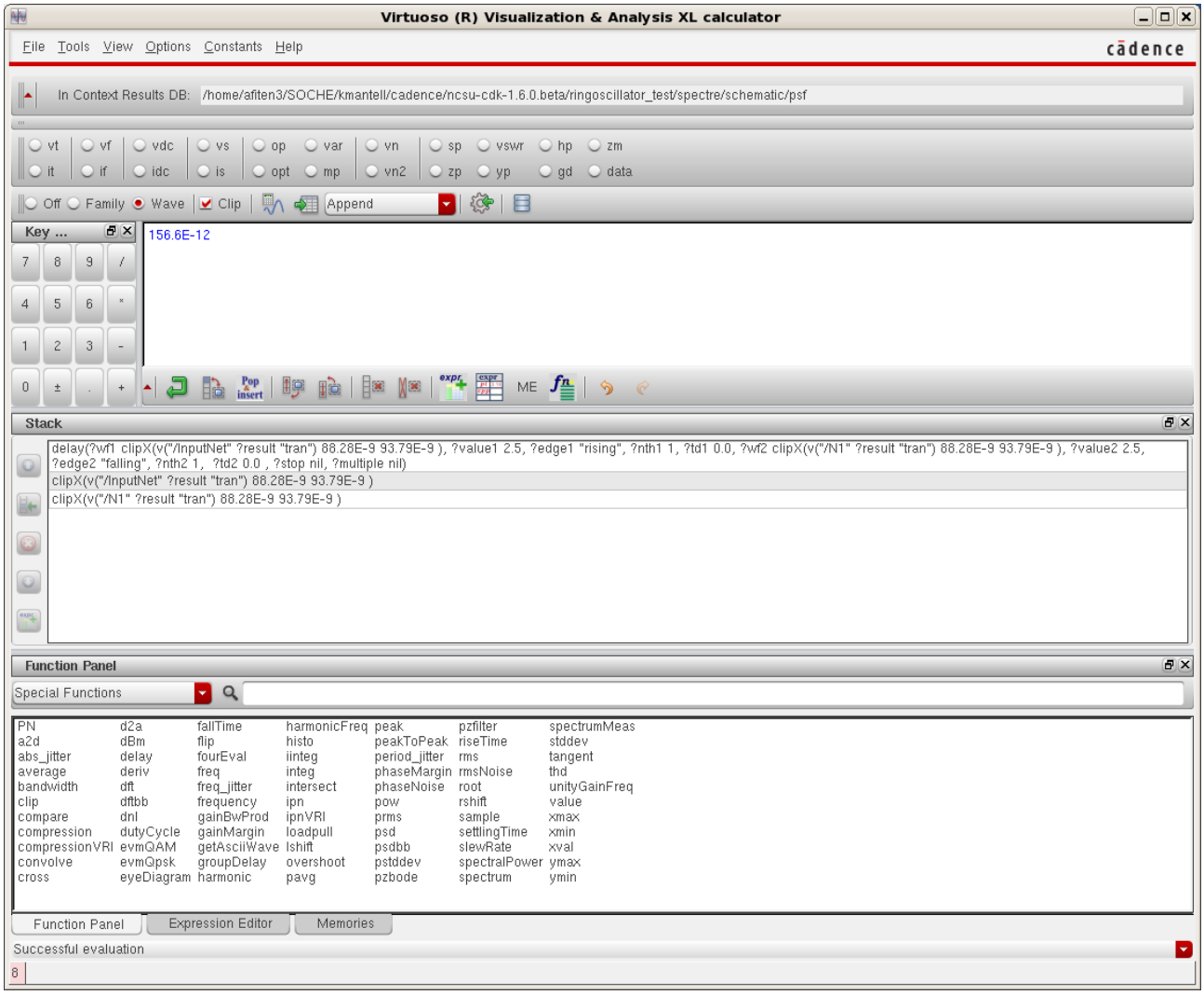
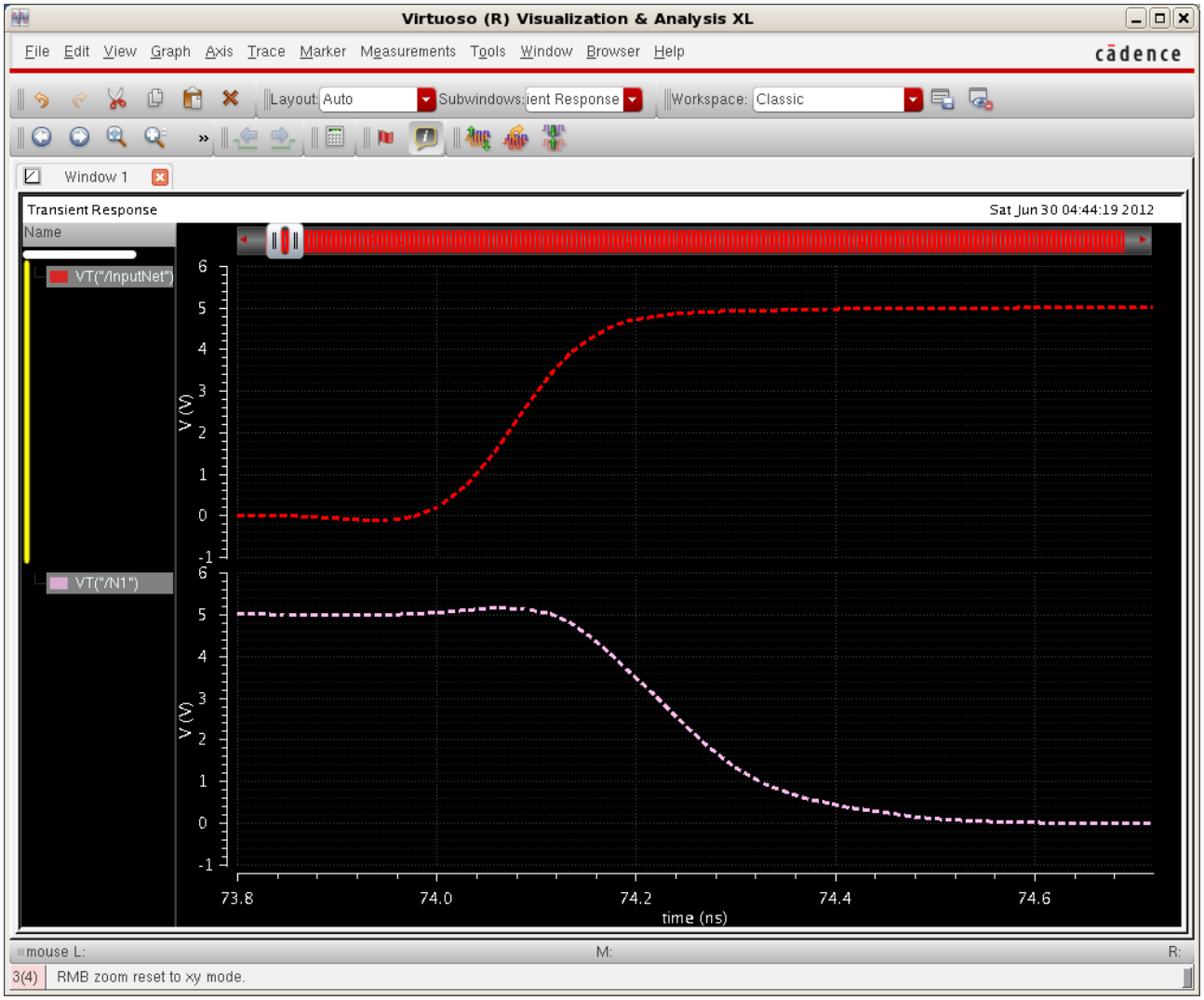
l. Now click on the 'Evaluate' buffer (the icon to the left of 'Append' pulldown), and you will see a value for the rising delay (tpLH) for the inverter (in the ring oscillator). In the image below, the result of the delay calculation shows that the rising delay for edge 1 is 156.6 ps.

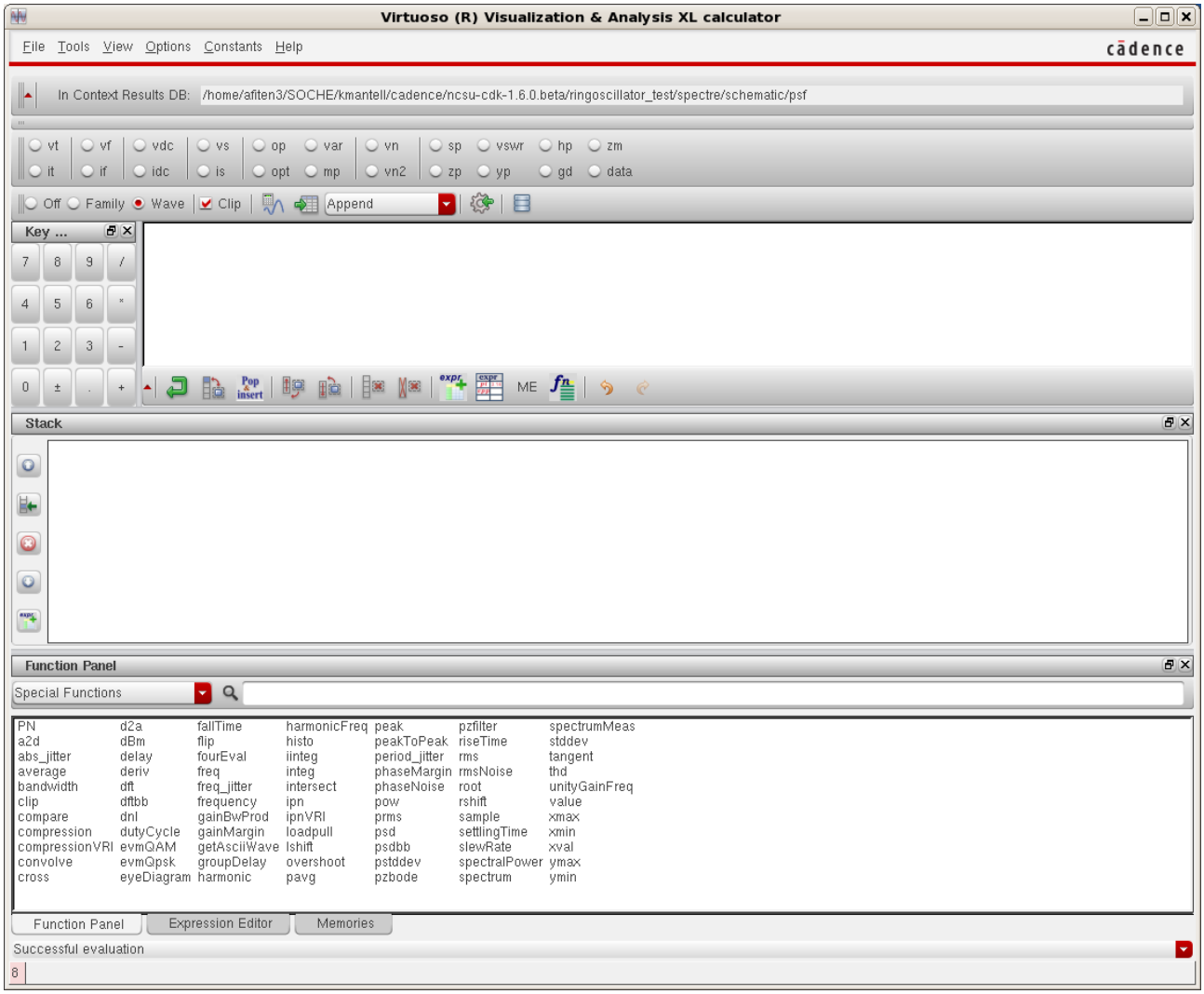


m. The image below shows the zoomed-in section of a single transition. The input waveform is a rising edge (InputNet in this case), and the output waveform is a falling edge (N1 in this case). You can highlight both waveforms by holding the shift key and clicking on the two waveforms. This makes it easier to see whether the rise time of the InputNet is equal to the fall time of the output net (N1 in this case) and thus, the extent to which the inverter is balanced.



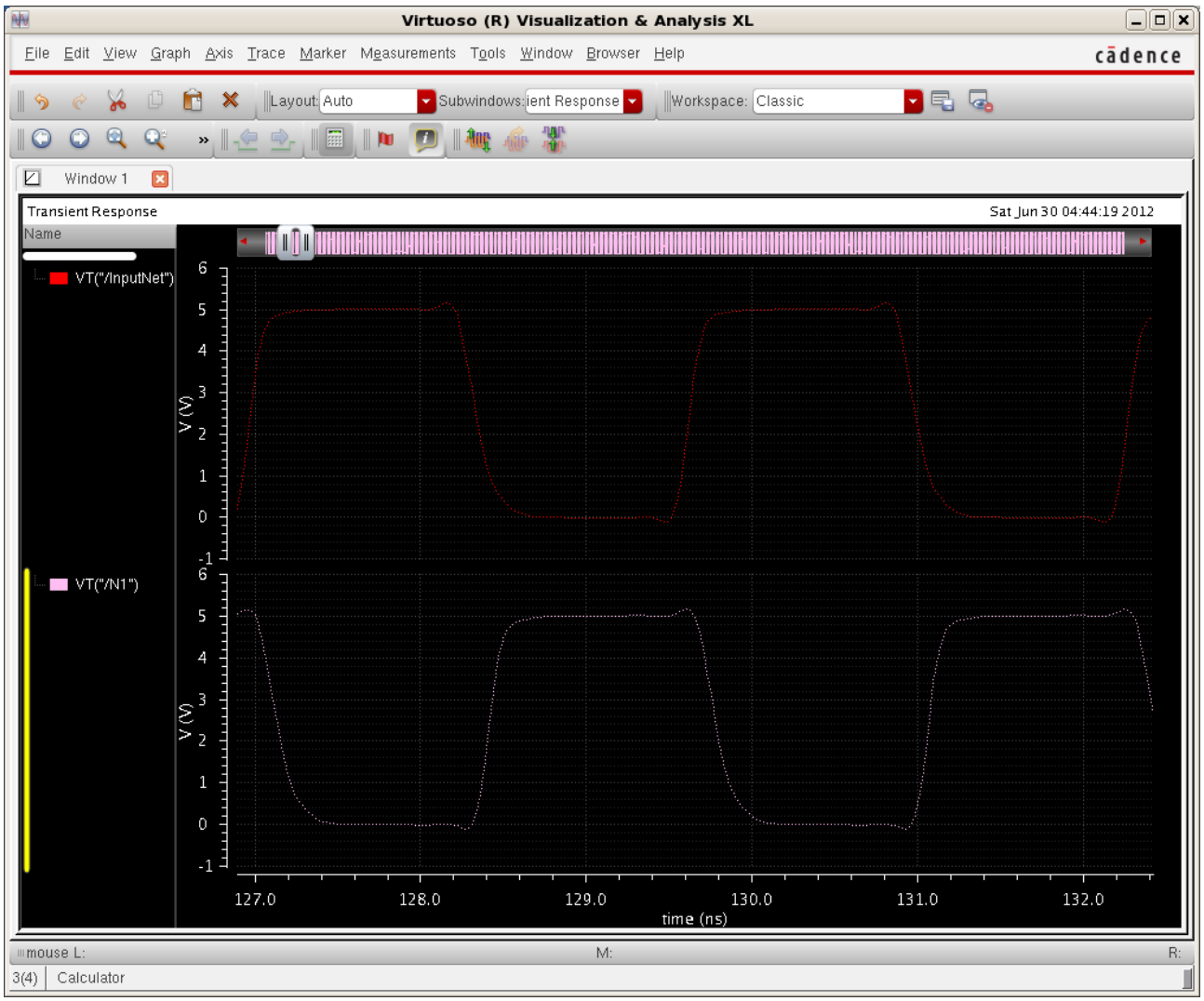
n. Now you are going to measure the delay of the high-to-low transition for these two signals (tpHL).

o. First, you can clear the 'Evaluate' buffer and clear the stack (clst) as shown in the image below.

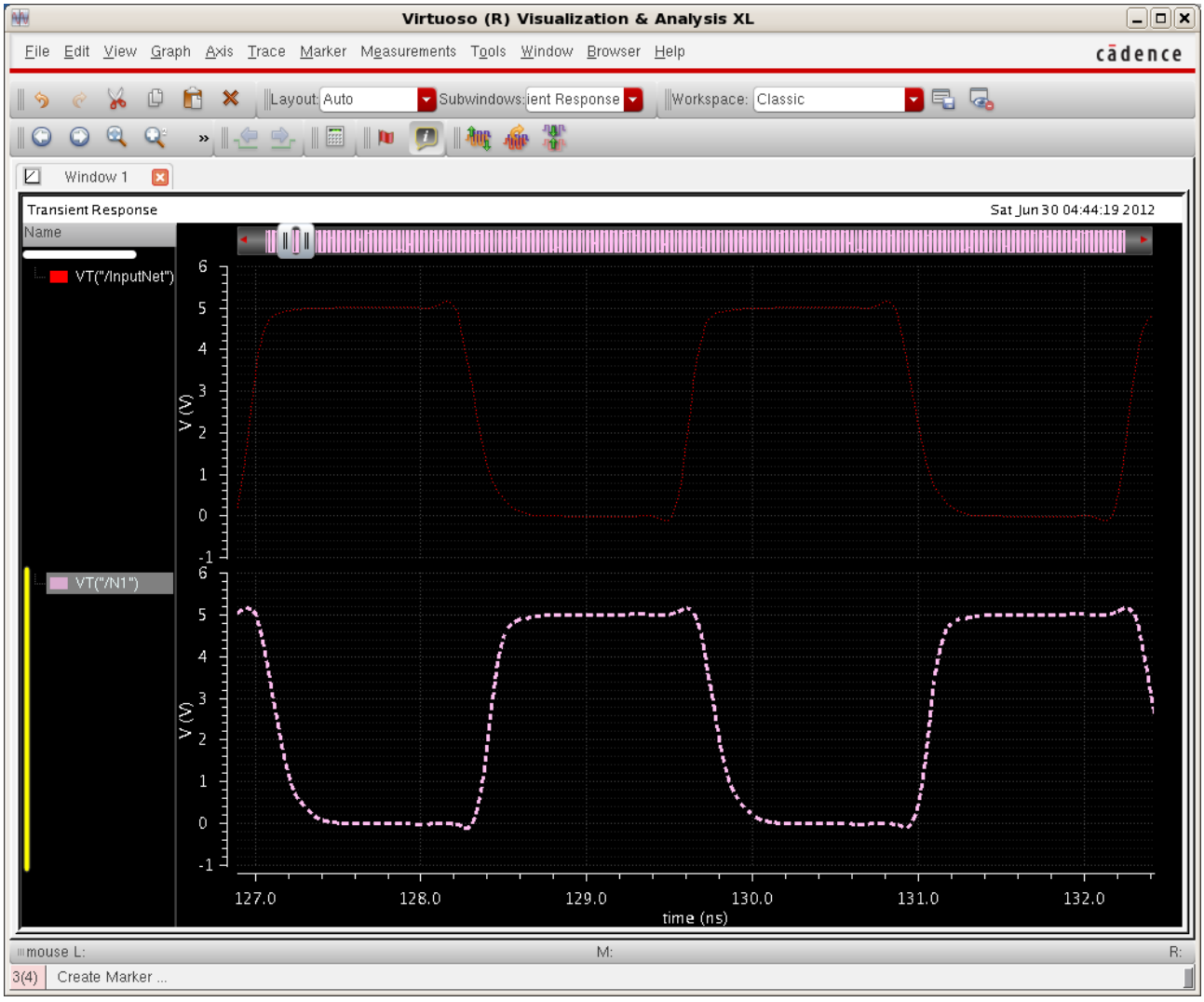


p. You will execute similar steps in this part of the exercise with the calculator.

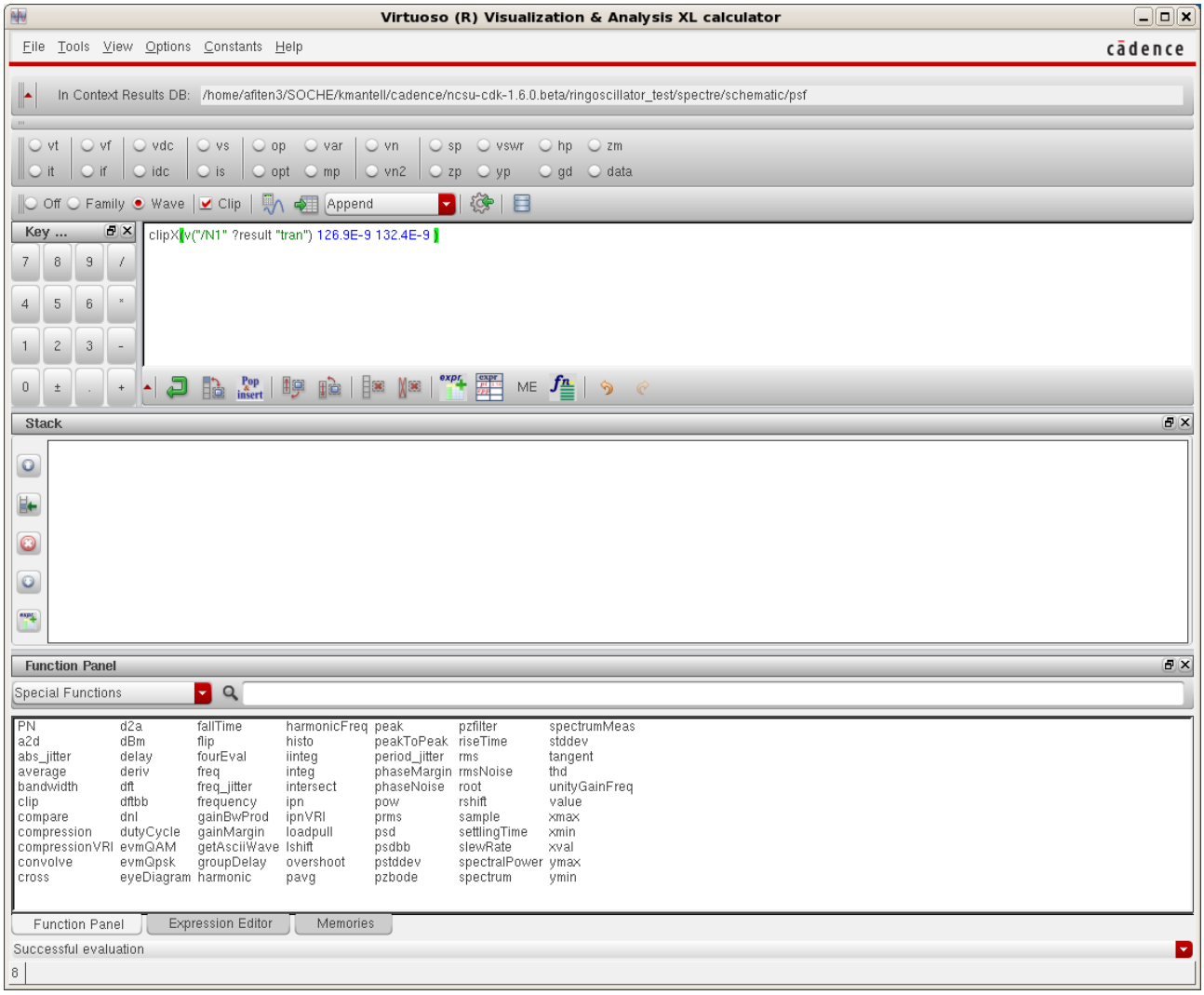
q. First make sure that your waveforms look like the ones shown in the Visualization & Analysis window (the same as for the previous set of steps to obtain the delay tpLH).



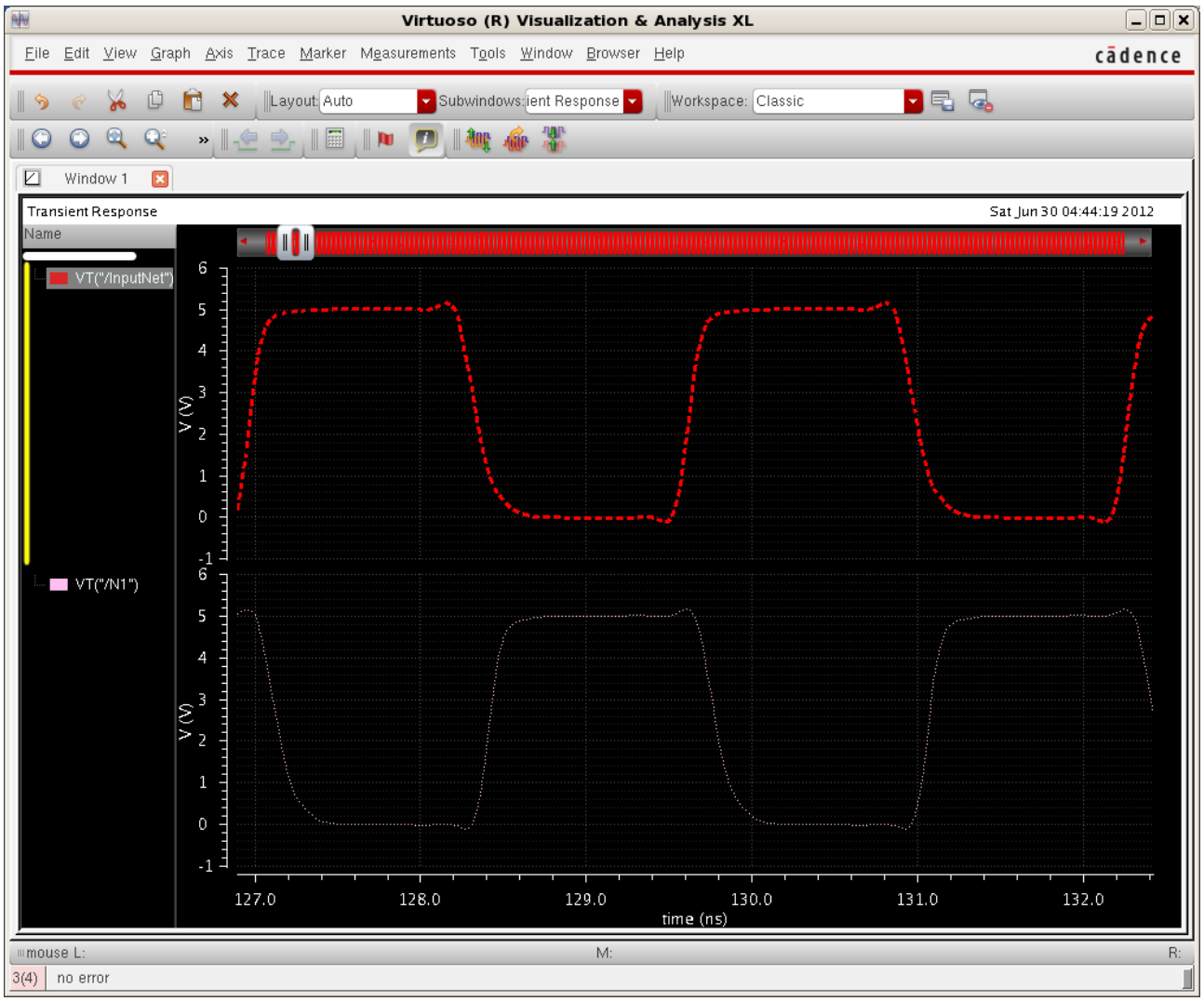
r. Now click on the 'Wave' radio button in the calculator window. Then click on the output waveform (the waveform with the low to high transition, in this case, N1) in the Visualization & Analysis XL window. (Be sure not to click on the wave name on the left-hand side; click instead on the waveform itself).



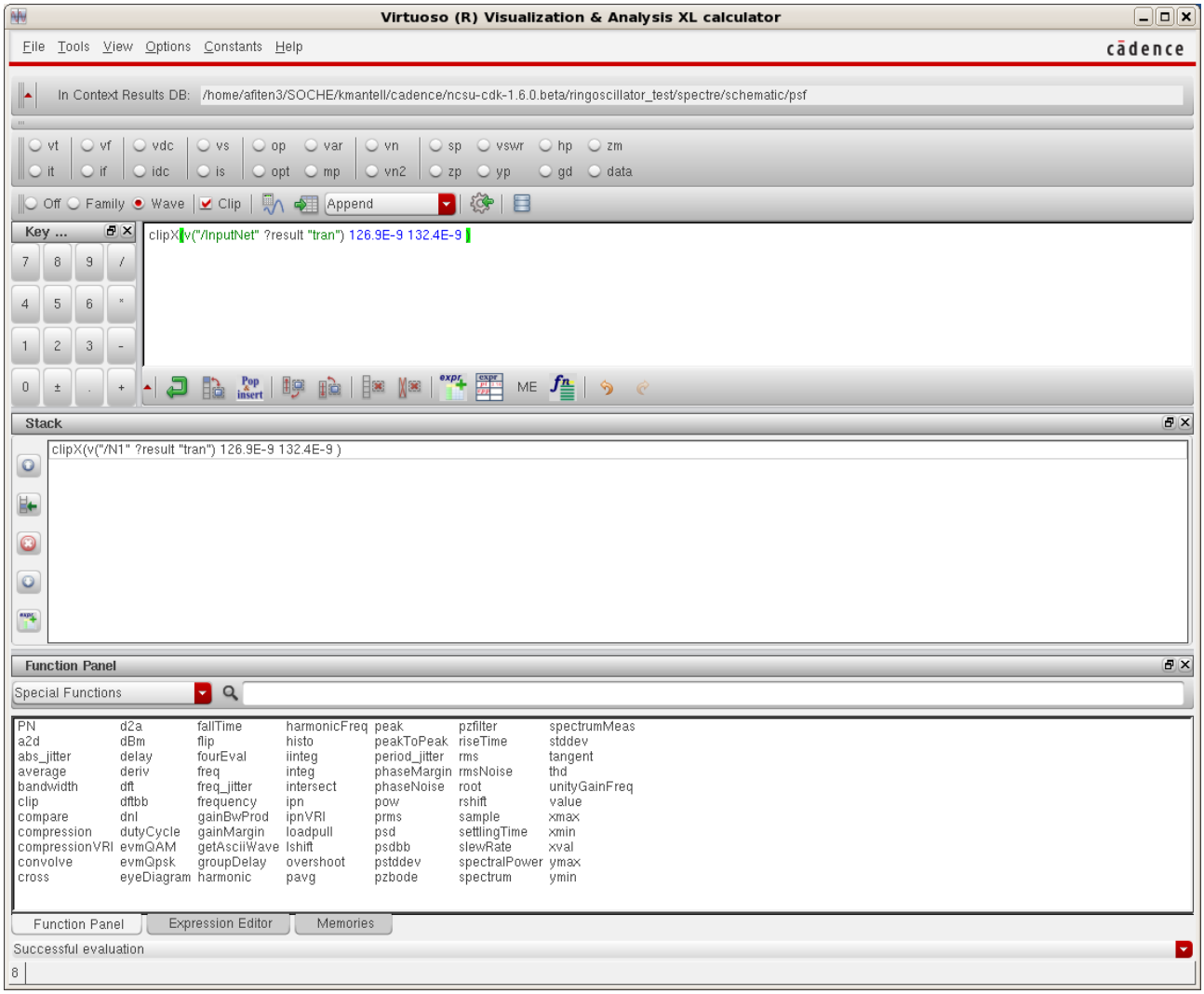
s. A wave name should appear in the calculator window as shown in the image below. As before, this image shows the wave name "N1" in the window. The syntax of the statement in the window, 'clipX,' refers to the zoomed-in portion of the waveform that you are displaying in the waveform window. The syntax of the two values in blue at the end of the statement refer to the start time and to end time of the zoomed-in portion of the viewing window that you selected in the Visualization & Analysis XL window.



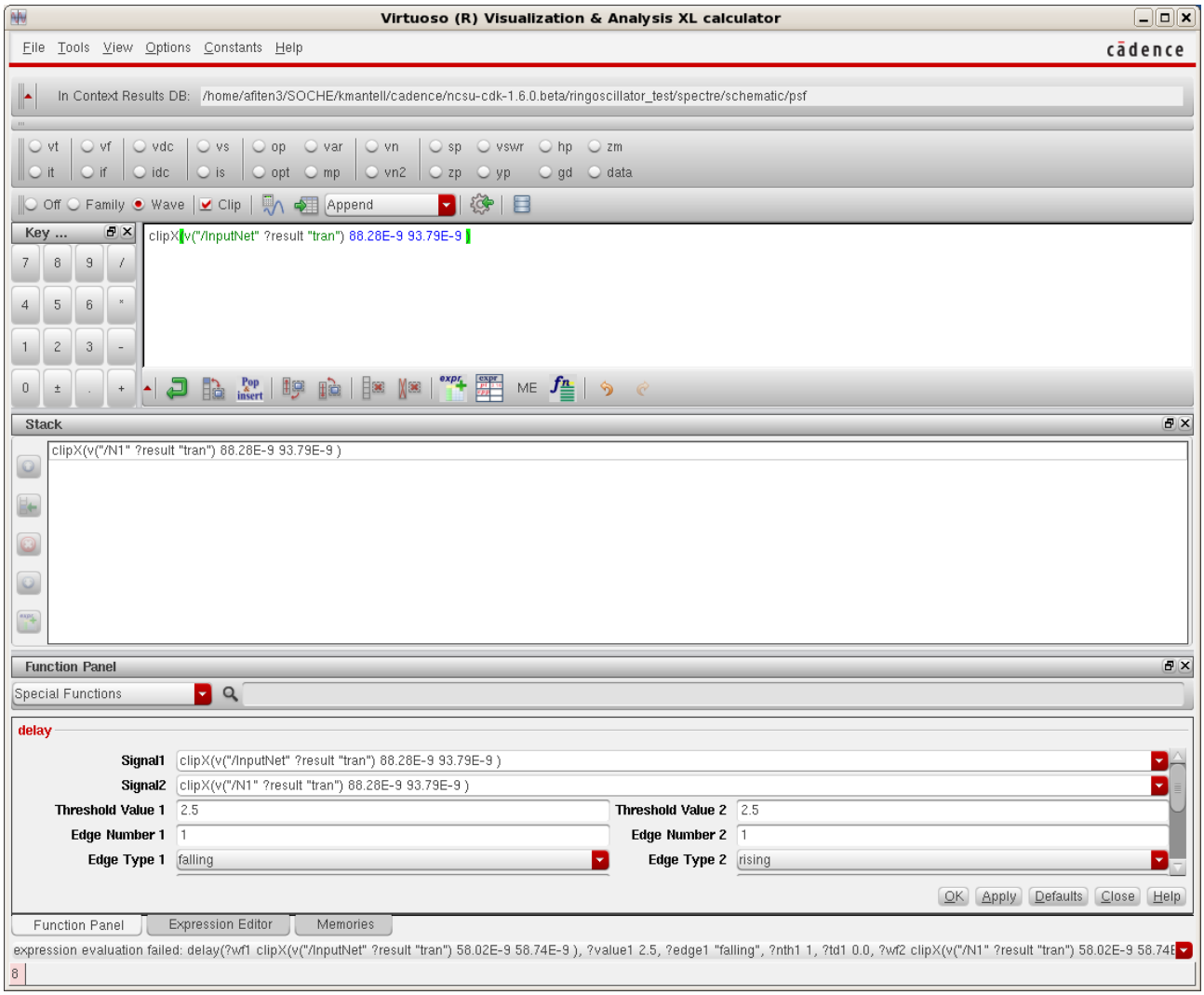
t. Now click on the input waveform. Be sure not to click on the name of the waveform on the left-hand side of the window. You are selecting the first falling edge of this waveform, and it is edge 1 (in the zoomed-in portion of the waveform that you display in the window).



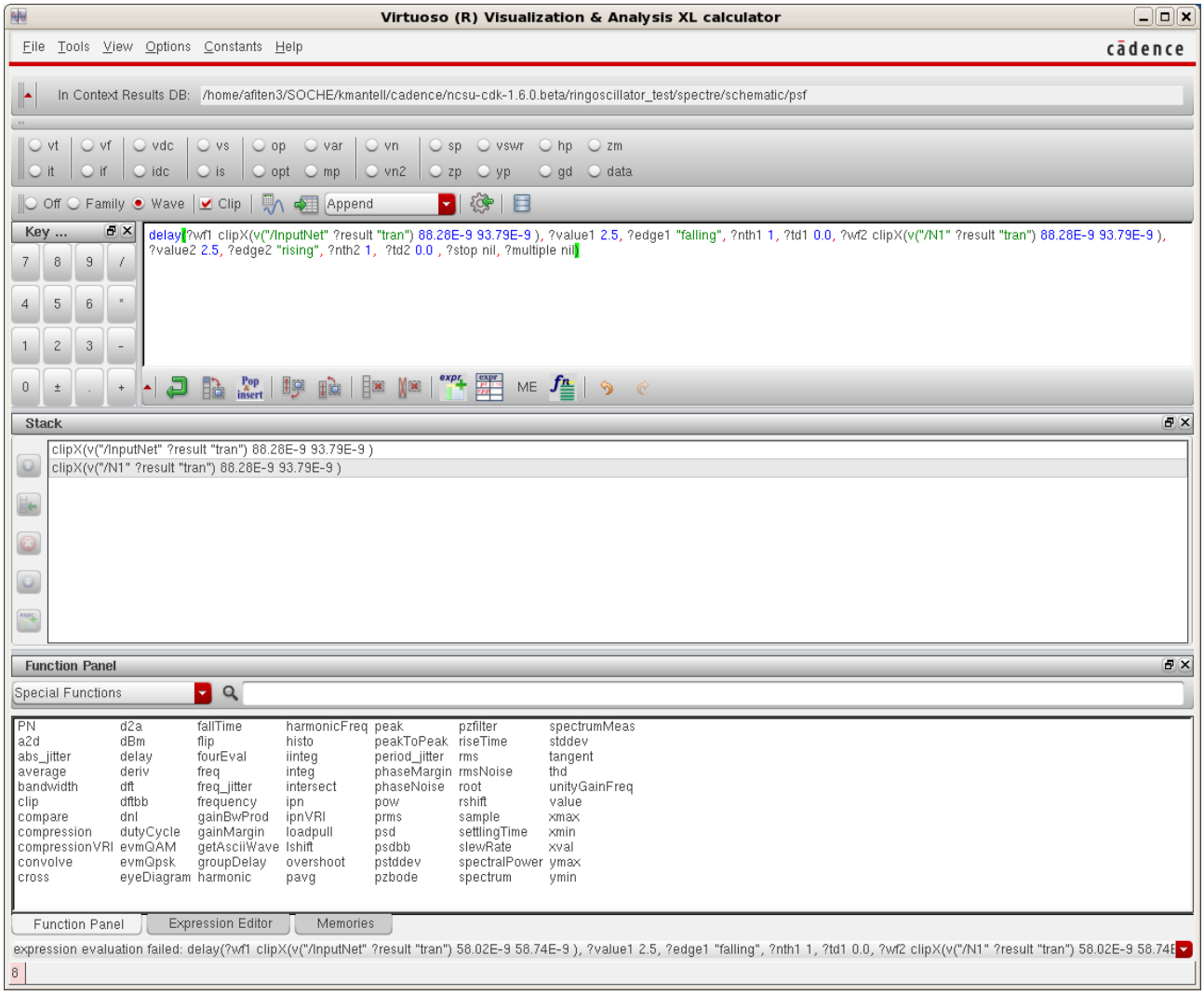
u. Now check in the calculator to verify that the name of the first waveform (N1 in the case shown) has been pushed into the stack and brings the name of the input waveform into the calculator (InputNet in the case shown). Important: Note that the waveforms were entered in reverse order (the late first; then the early one); this is a feature of the stack operation of the calculator.



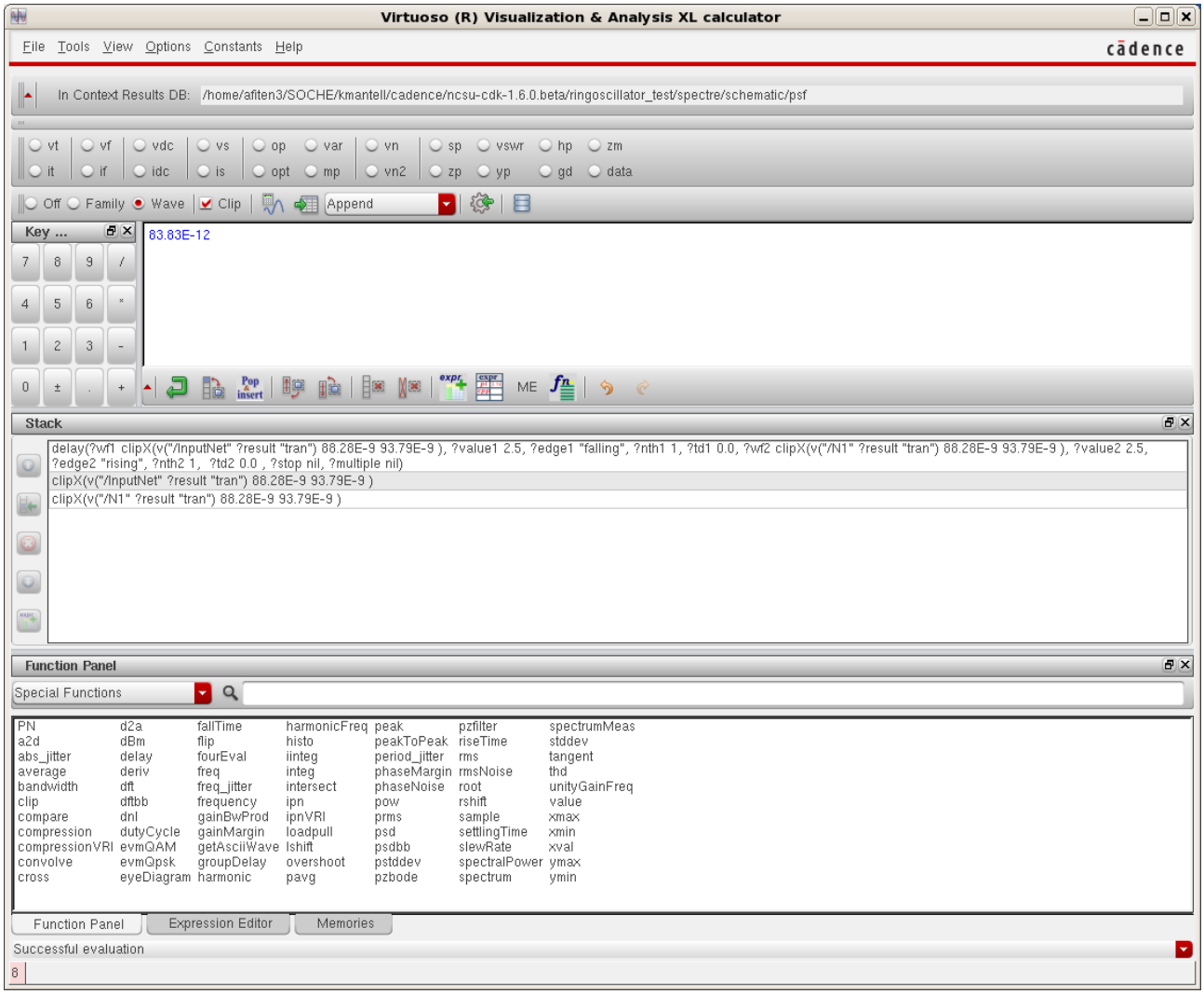
v. Now move the cursor to 'Special Functions' in the calculator window. Select 'delay'. Fill 2.5 as the threshold values (50% of Vdd = 2.5V since Vdd = 5V). Notice that in the 'delay' section, the name of your first waveform (N1 in this case) is listed as 'Signal2,' and the name of your second waveform (InputNet in this case) is listed as 'Signal1'. For Signal1, set the Edge Number equal to 1. For Signal2, set the Edge Number equal to 1. For Signal 1, set the Edge Type 1 to 'falling.' For Signal 2, set the Edge Type 2 to 'rising.' Then click 'OK.'



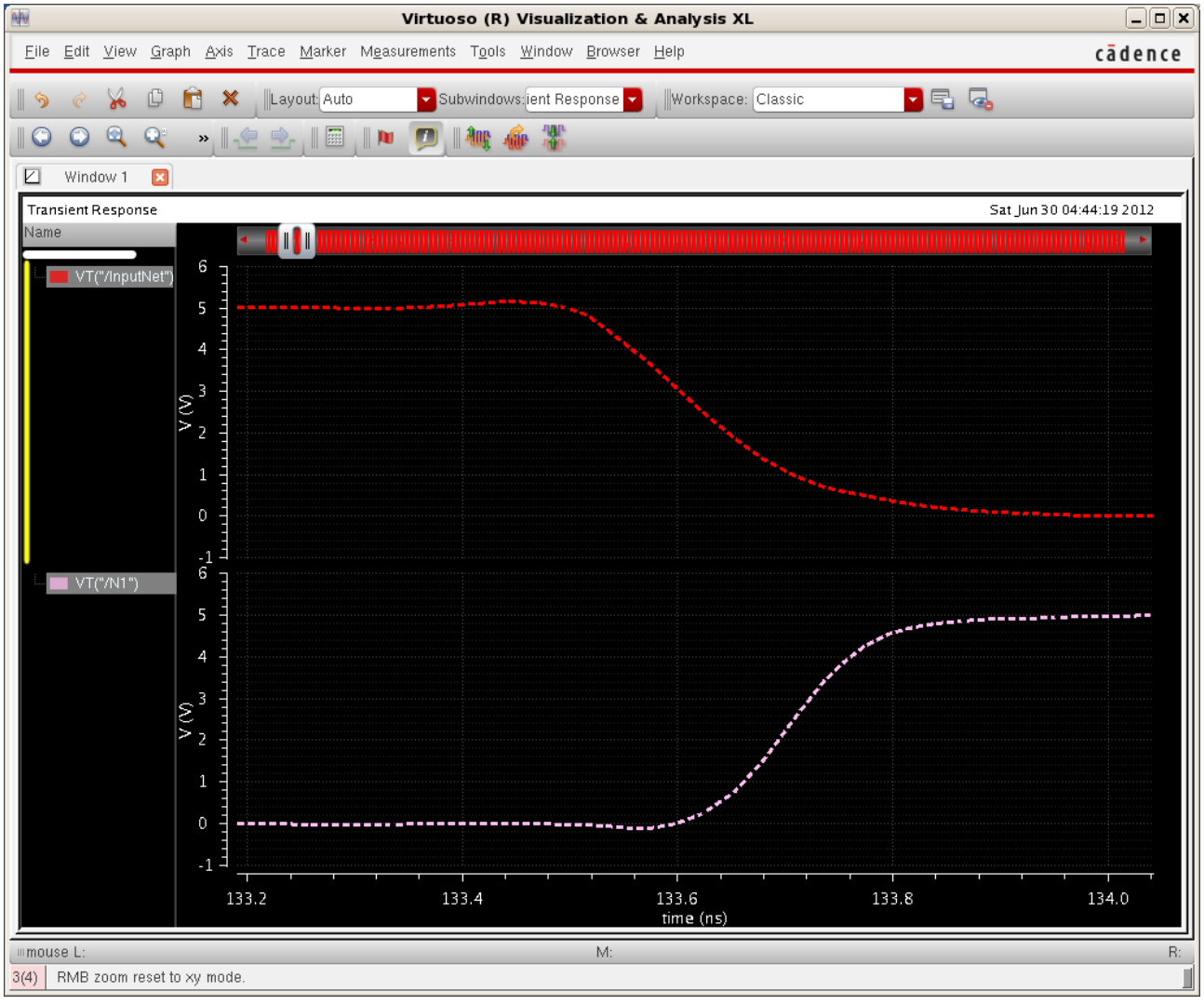
w. Notice the change in the calculator window. The entry has now been expanded to show the delay calculation expression.



x. Now click on the 'Evaluate' buffer (the icon to the left of 'Append' pulldown), and you will see a value for the falling delay (tpHL) for the inverter (in the ring oscillator). In the image below, the result of the delay calculation shows that the rising delay for edge 1 is 83.83 ps.



y. The image below shows the zoomed-in section of a single transition. The input waveform is a falling edge (InputNet in this case), and the output waveform is a rising edge (N1 in this case). You can highlight both waveforms by holding the shift key and clicking on the two waveforms. This makes it easier to see whether the fall time of the InputNet is equal to the rise time of the output net (N1 in this case) and thus, the extent to which the inverter is balanced for this transition.



z. You can also measure the period of this ring oscillator.

aa. You have now learned to use the calculator using your simulation of a ring oscillator.

27. Parameterized Inverter Chain: Delay of Inverter Chain

a. In this section, you are going to create a hierarchical schematic at the logic gate level by using symbols that represent lower-level schematics. When you create a hierarchical schematic, it may be necessary to use different gates that represent the same logic but have different transistor sizes (e.g. a 'weak' inverter and a 'strong' inverter) and different corresponding power levels. It is also desirable at times to be able to move easily from one technology to another (e.g., from 0.6 microns to 0.25 microns). In these cases, it is helpful to parameterize the sizes of the transistors in the schematics.

In this section, you will start with the schematic and symbol for the inverter that you created in a previous section (inv). You may want to review the previous sections and refresh your memory.

First, copy the existing inverter cell to four other cells named invx1, invx4, invx16, and Loadx64, respectively. These cells will be parameterized inverters; specifically, the cells will be a parameterized inverter with minimum size (x1), four times the minimum (x4), 16 times the minimum (x16), and a fixed load 64 times the minimum.

In order to copy the cells, first click on the 'EENG653' library, then on the inverter cell (such that they become highlighted). Then select 'Edit → Copy,' and the 'Copy Cell' form will appear as shown in the image below. Complete the name of the new cell, as shown for the case of the 'invx1' cell. Make sure that 'Copy All Views' is selected. (If your inverter were to have contained additional schematics, then it would be important to select 'Copy Hierarchical' as well).

In this way, you should copy four more inverter cells in the 'EENG653' library (you could have also copied the cell into a different library.)

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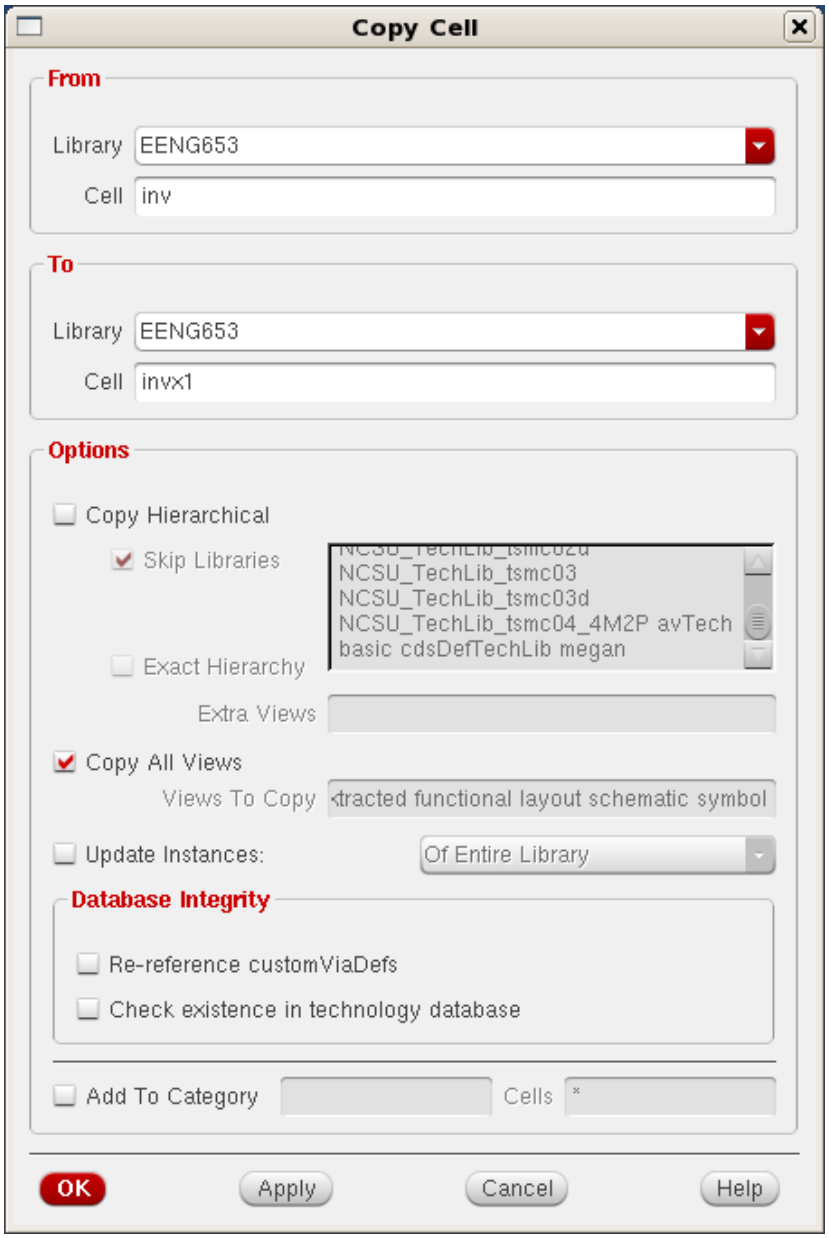

b. Open the EENG653 invx1 schematic (to review, one way to do this is to click on the Library Manager window and then double-click on the schematic view in this window). You will now change the properties of the nmos4 and pmos4 to become *parameterized*. Recall that to change the properties of the nmos4, you click on the device (highlight it), and type 'q' (the hotkey).

Edit the properties for the nmos4:

1. Set the Width to 'Width';
2. Set the Length to 'Length'.

Edit the properties for the pmos4:

1. Set the Width to 'a*Width';
2. Set the Length to 'Length'.

Replace the VDD pin with an instance of the 'vdd' symbol from the 'basic' library. Replace the GND pin with an instance of the 'gnd' symbol from the 'basic' library. You will be setting the values for ground and power at the top level of the hierarchy (this practice is helpful for more complicated schematics).

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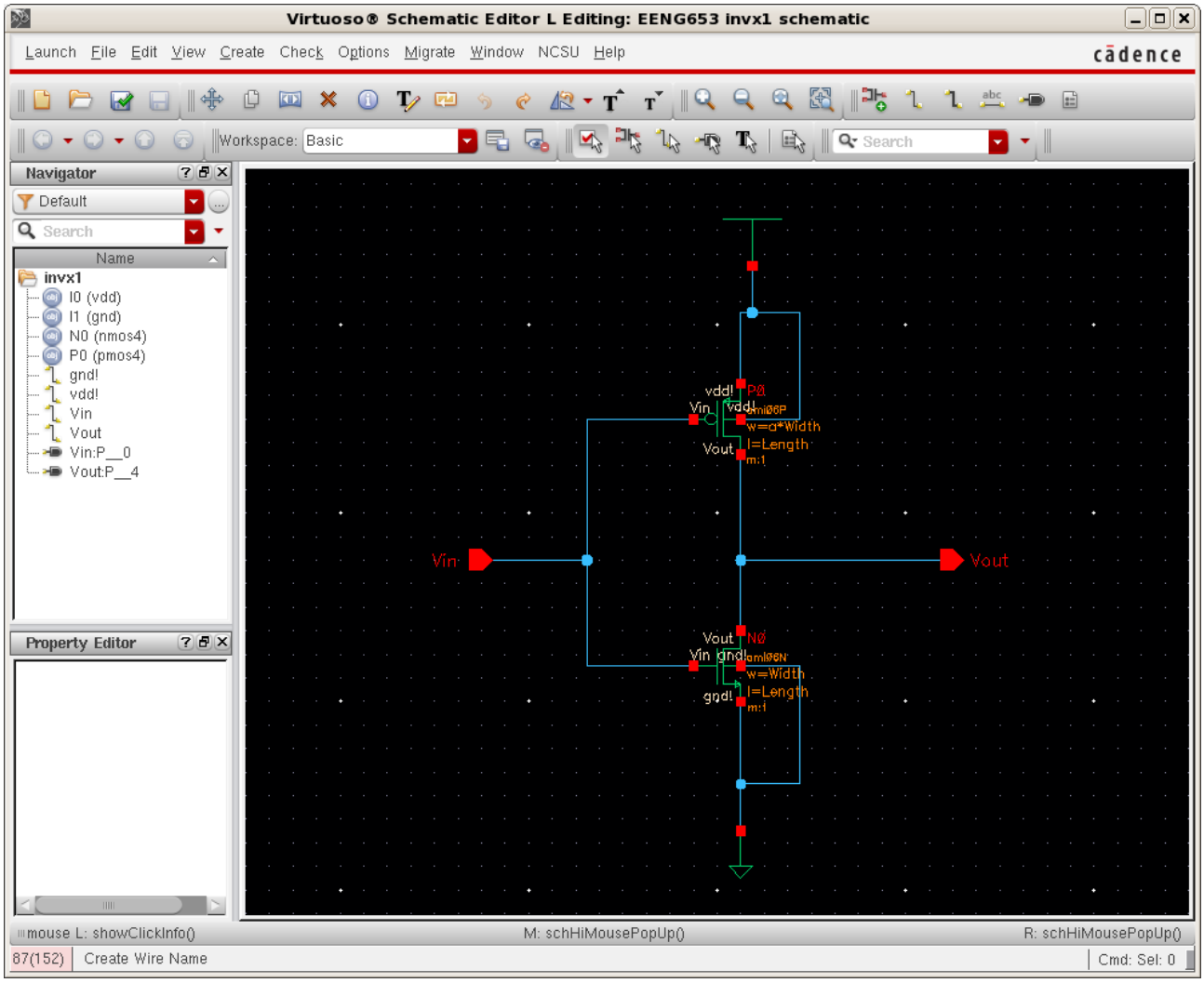
Your schematic will look like the image shown below.



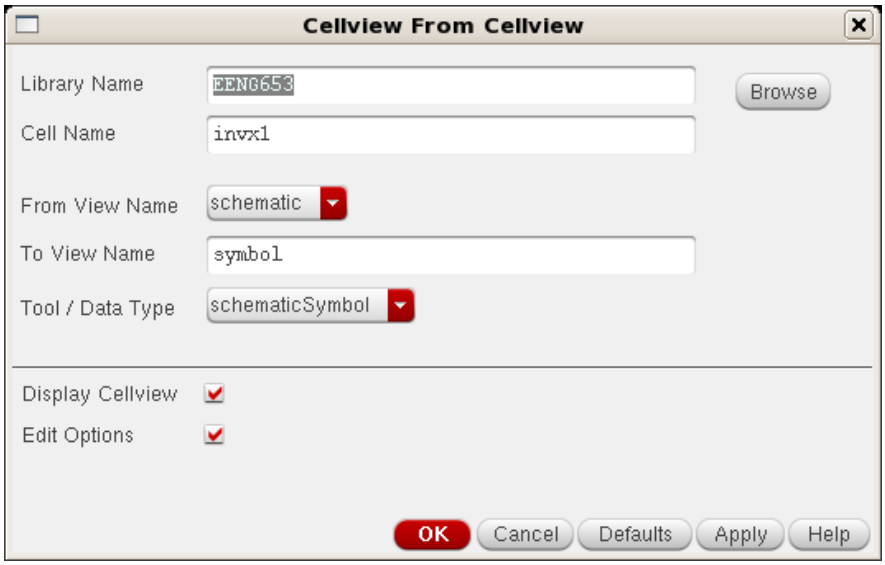
This image shows a parameterized inverter. You have parameterized the width and length of each transistor. In this case, you have parameterized the length of the nmos4 and length of the pmos4 with the parameter 'Length,' (default value is 0.6 microns), the width of the nmos4 with the parameter 'Width,' (e.g., 1.5 microns base size) and the width of the pmos4 with the parameter 'a*Width.' Note that the 'a' is used to change the ratio of the pmos4 width to the nmos4 width: PMOS/NMOS ratio.

When you instantiate this inverter schematic in a hierarchical schematic, you will be able to:

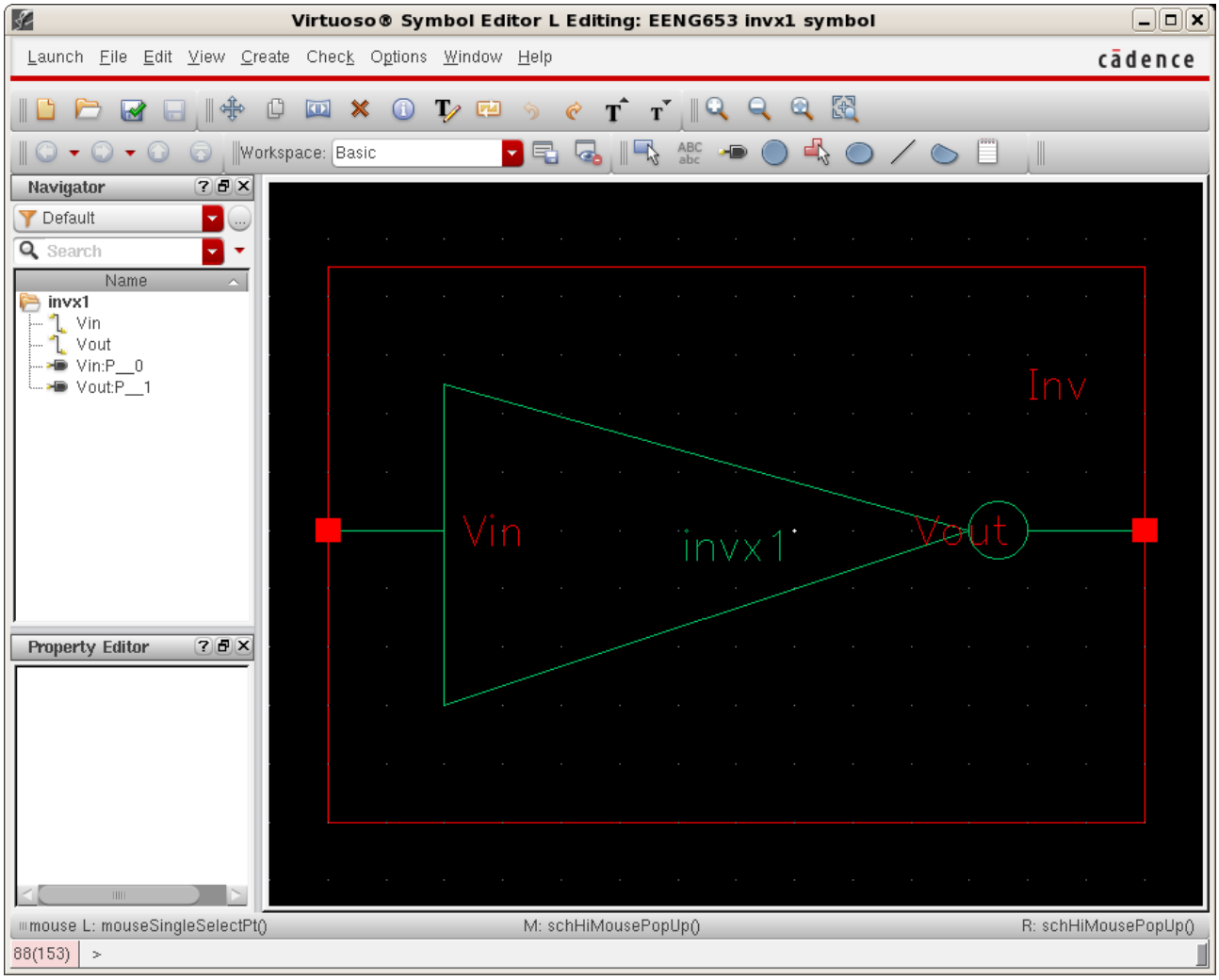
1. Keep the default values;
2. Change the default values to migrate to a new technology (such as changing 'Length' to 0.25 microns for a 0.25 micron CMOS technology);
3. Change the transistor sizes to create different transistor strengths for different inverters.

c. Create a symbol for the invx1 schematic. In the EENG653 invx1 schematic, select "Create → Cellview → From Cellview". The form "Cellview From Cellview" will appear as shown in the image below. Fill in the form with Cell Name 'invx1', From View Name as 'schematic', To View Name as 'symbol'. Then click OK.

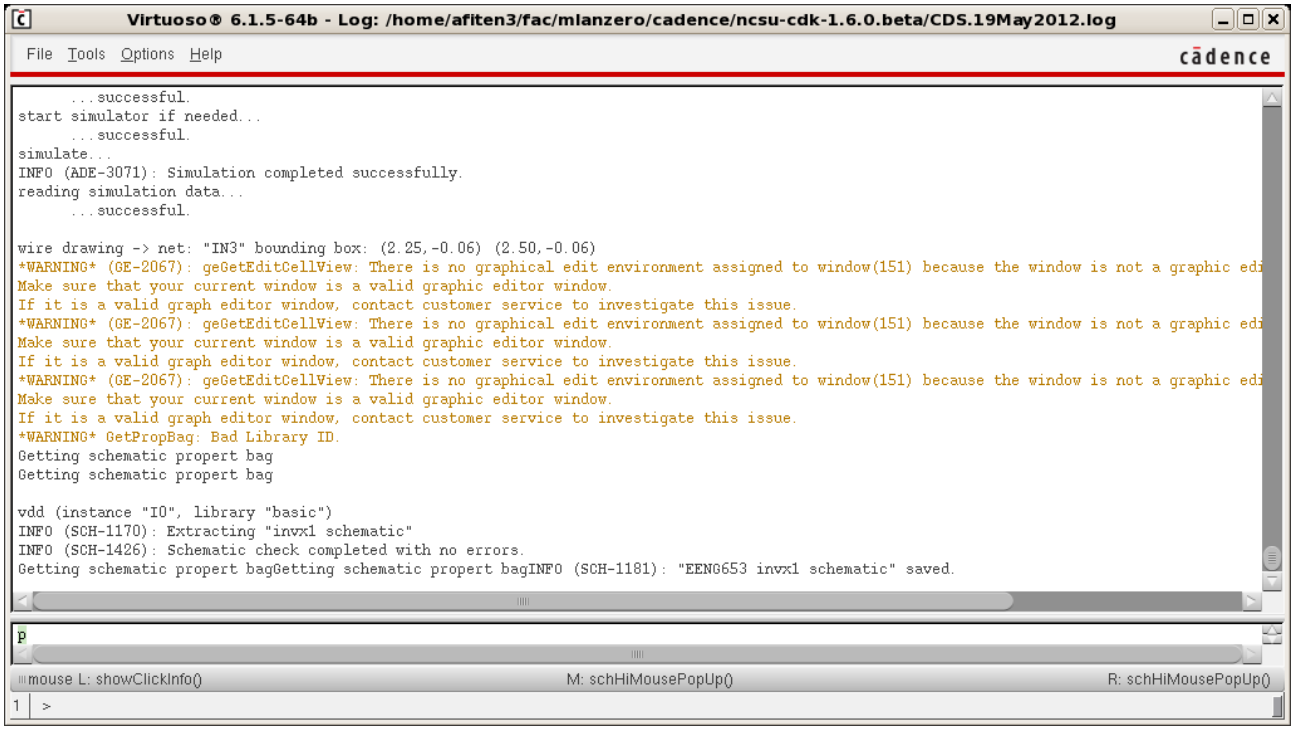
The "Create Cellview" window will appear when the invx1 symbol already exists. You can select 'Modify' to use the previous symbol (where you will delete the VDD and GND pins with green lines) or you can select 'Replace' and start over with a fresh symbol.



d. The invx1 symbol will look like the image shown below.



e. Run Check and Save on the invx1 schematic. When you run Check and Save, the CIW will report that the invx1 "Schematic check completed with no errors." If there are errors, correct the schematic and/or symbol and re-run Check and Save. Be sure that Check and Save completes with no errors, as shown in the image below.



f. Now you will *parameterize* the width and length for your additional inverters: invx4, invx16, and Loadx64.

Parameterizing transistor widths

For each inverter, change the length of each pmos4 and each nmos4 to the parameter 'Length'. Setting the length of each device to 'Length' is standard practice for the case of digital design in which transistor lengths are set to the minimum value (in this case, 0.6 microns) in order to achieve high performance.

Parameterizing transistor lengths

For each inverter, set the widths according to the following:

1. invx4
    a. pmos4 width: 'a*b*Width'
    b. nmos4 width: 'b*Width'
2. invx16
    a. pmos4 width: 'a*b*b*Width'
    b. nmos4 width: 'b*b*Width'
3. Loadx64
    a. pmos4 width: 'a*c*Width'
    b. nmos4 width: 'c*Width'

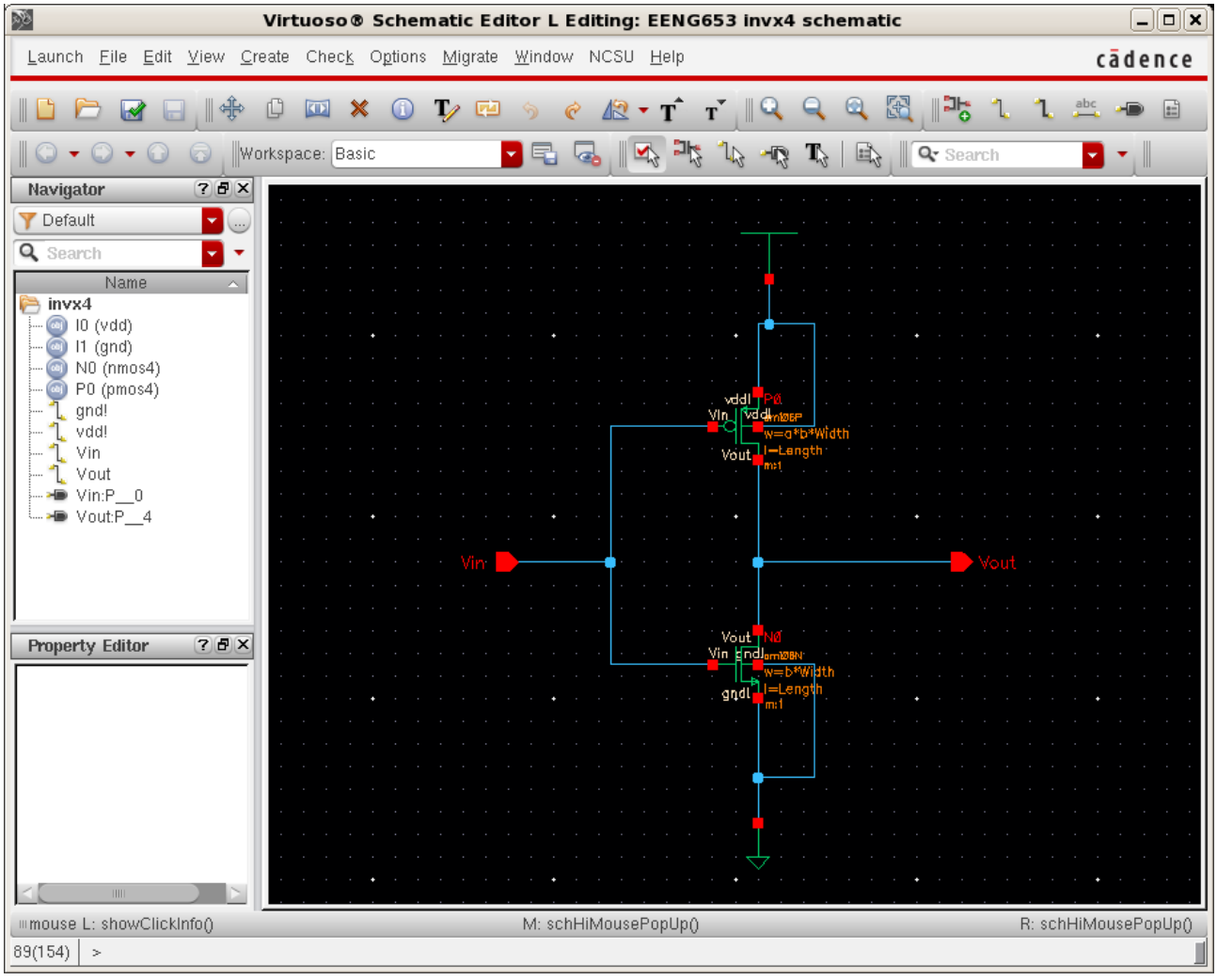
Notice that invx4 and invx16 are parameterized twice (with 'a' and 'b'). Notice that Loadx64 is parameterized twice (with 'a' and 'c') and is kept independent of parameter 'b' in order to compare the results of different choices of sizes for invx4 and invx16 when the inverter chain drives a fixed load (default value for 'c' is c = 64).

For each of these inverters, replace the VDD pin with an instance of the ‘vdd’ symbol from the ‘basic’ library. Replace the GND pin with an instance of the ‘gnd’ symbol from the ‘basic’ library. You will be setting the values for ground and power at the top level of the hierarchy (this practice is helpful for complicated schematics).

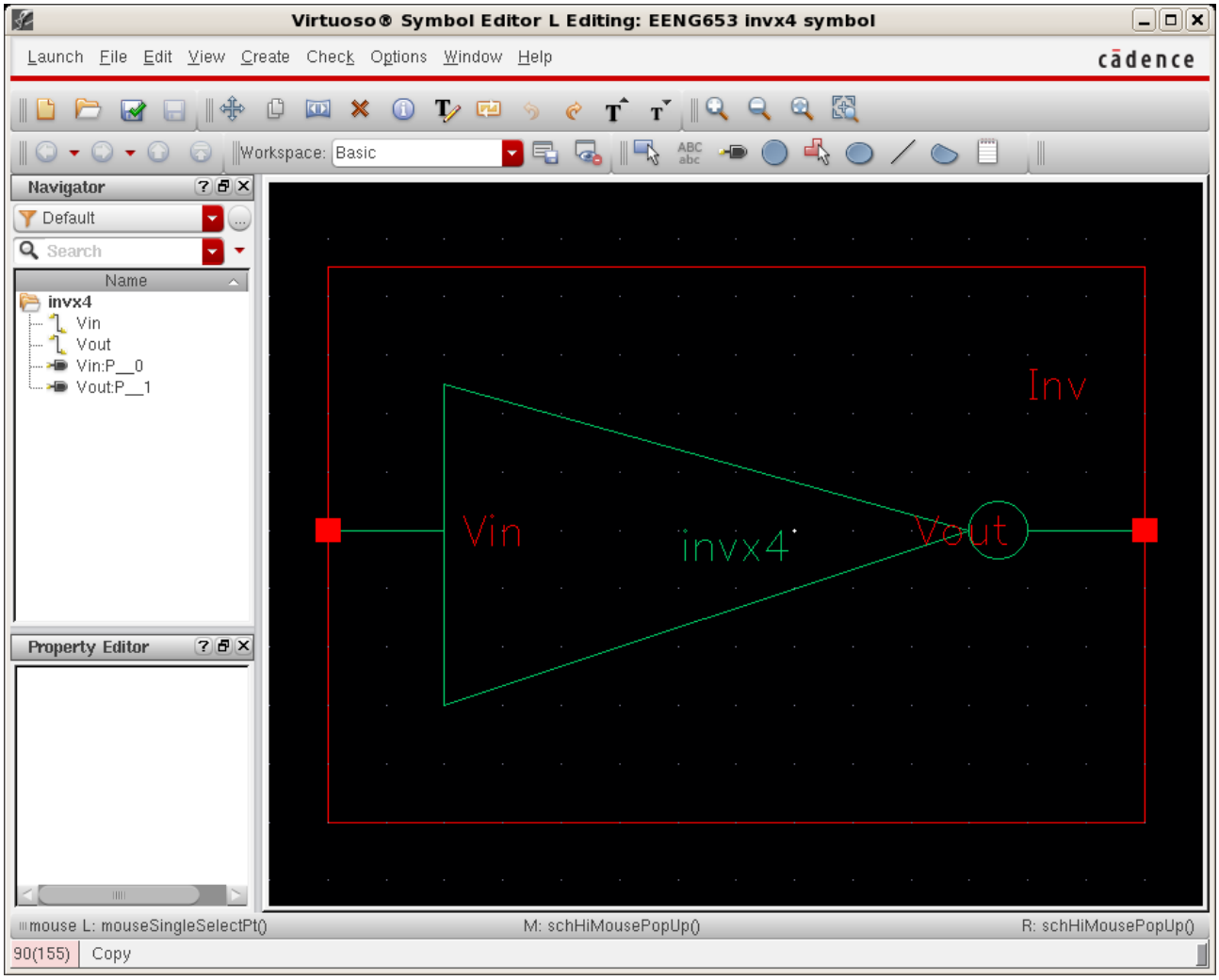
Create a symbol for each inverter. Save the inverter symbol.

Check and Save each inverter. Make sure that the CIW reports that the Check and Save completed successfully.

g. The image below shows the invx4 schematic.



h. The image below shows the invx4 symbol.



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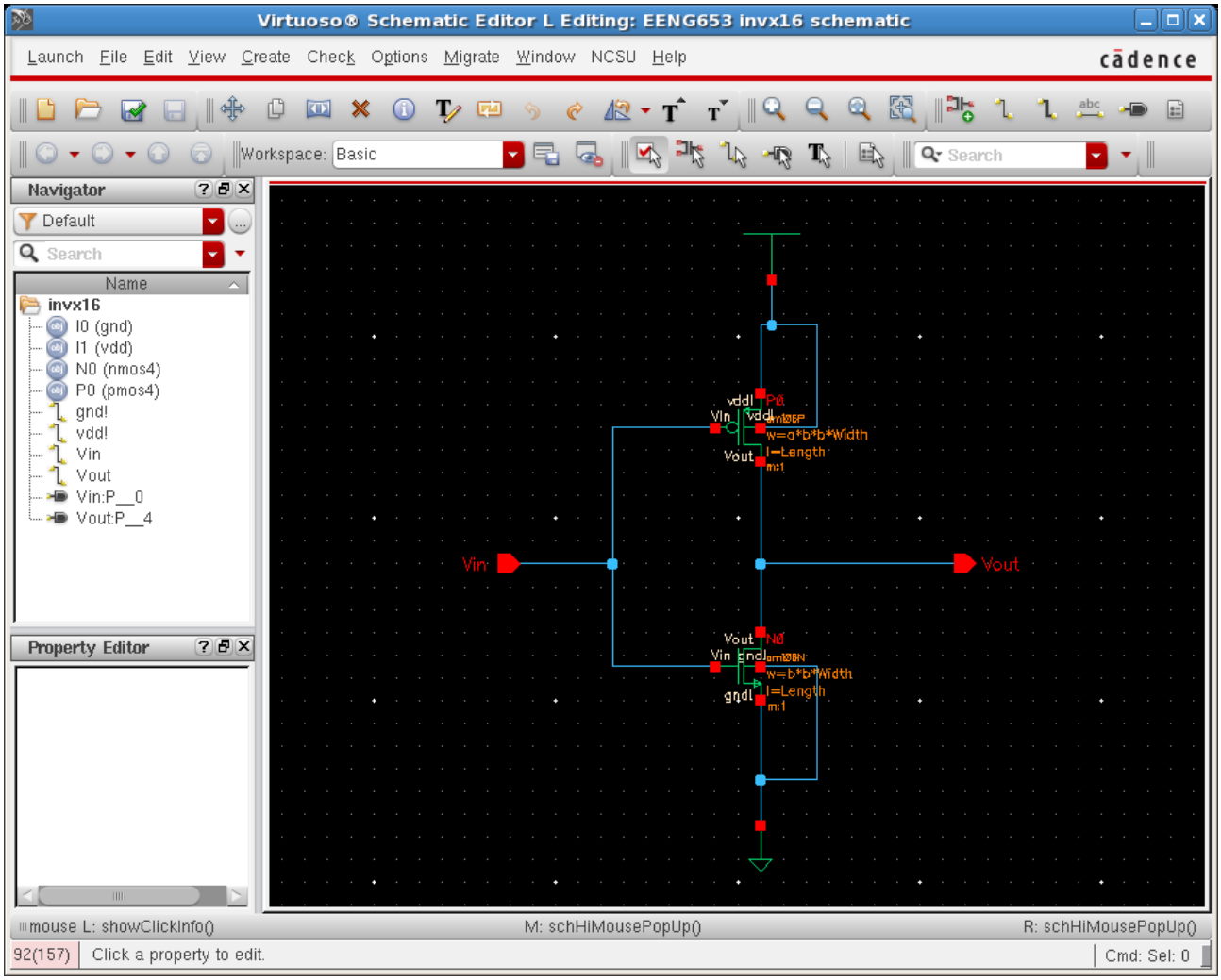
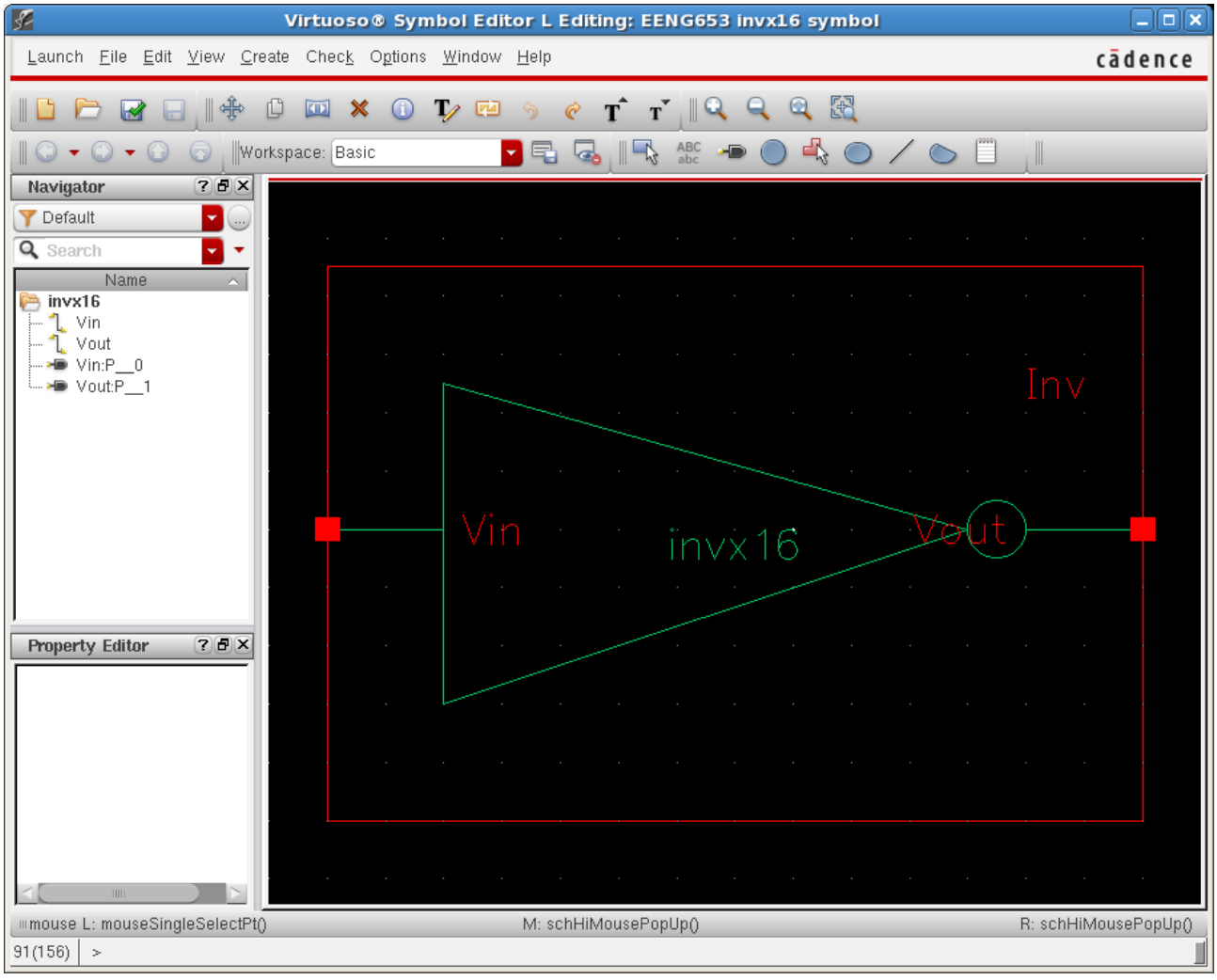
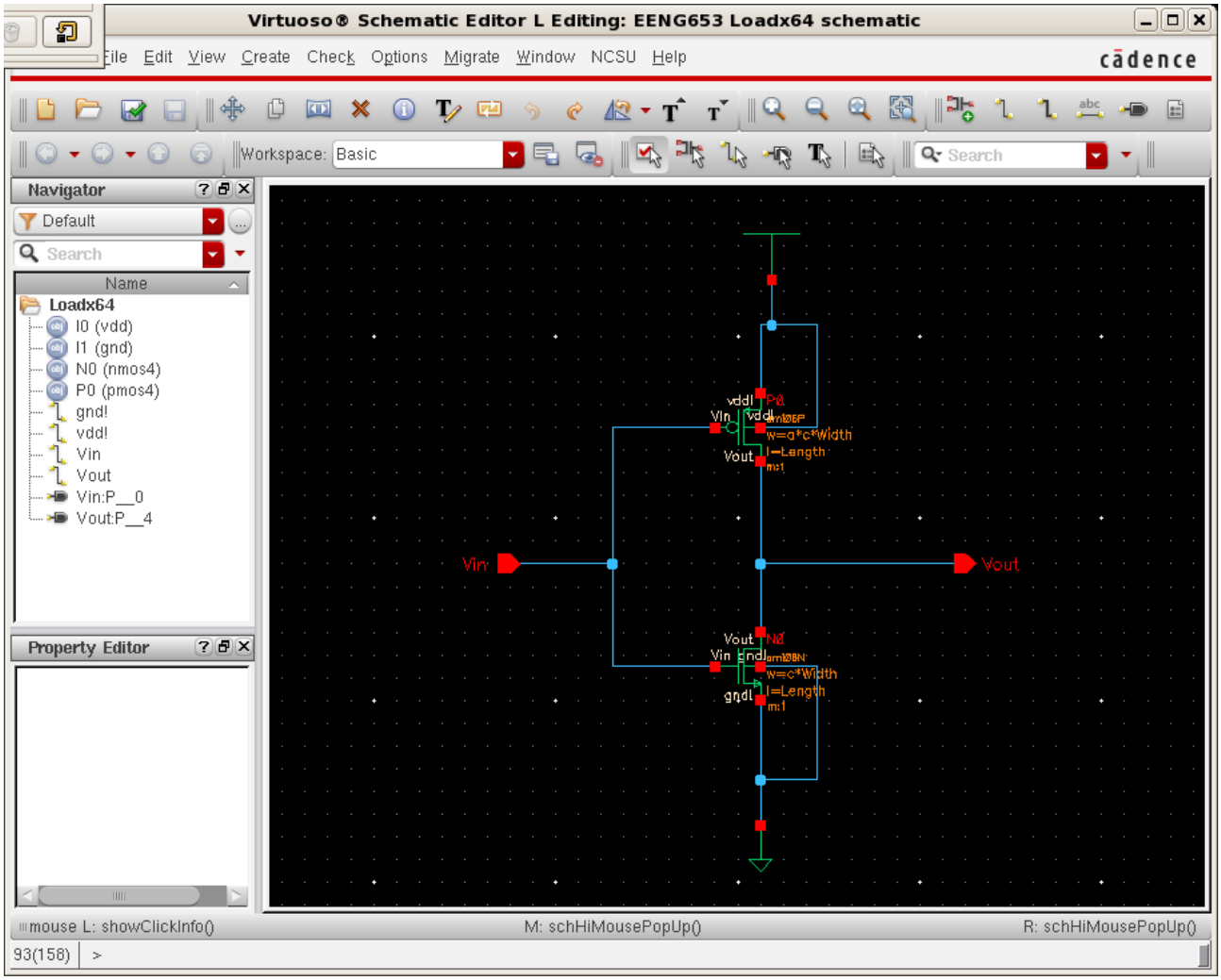
i. The image below shows the invx16 schematic.



j. The image below shows the invx16 symbol.



k. The image below shows the Loadx64 schematic.



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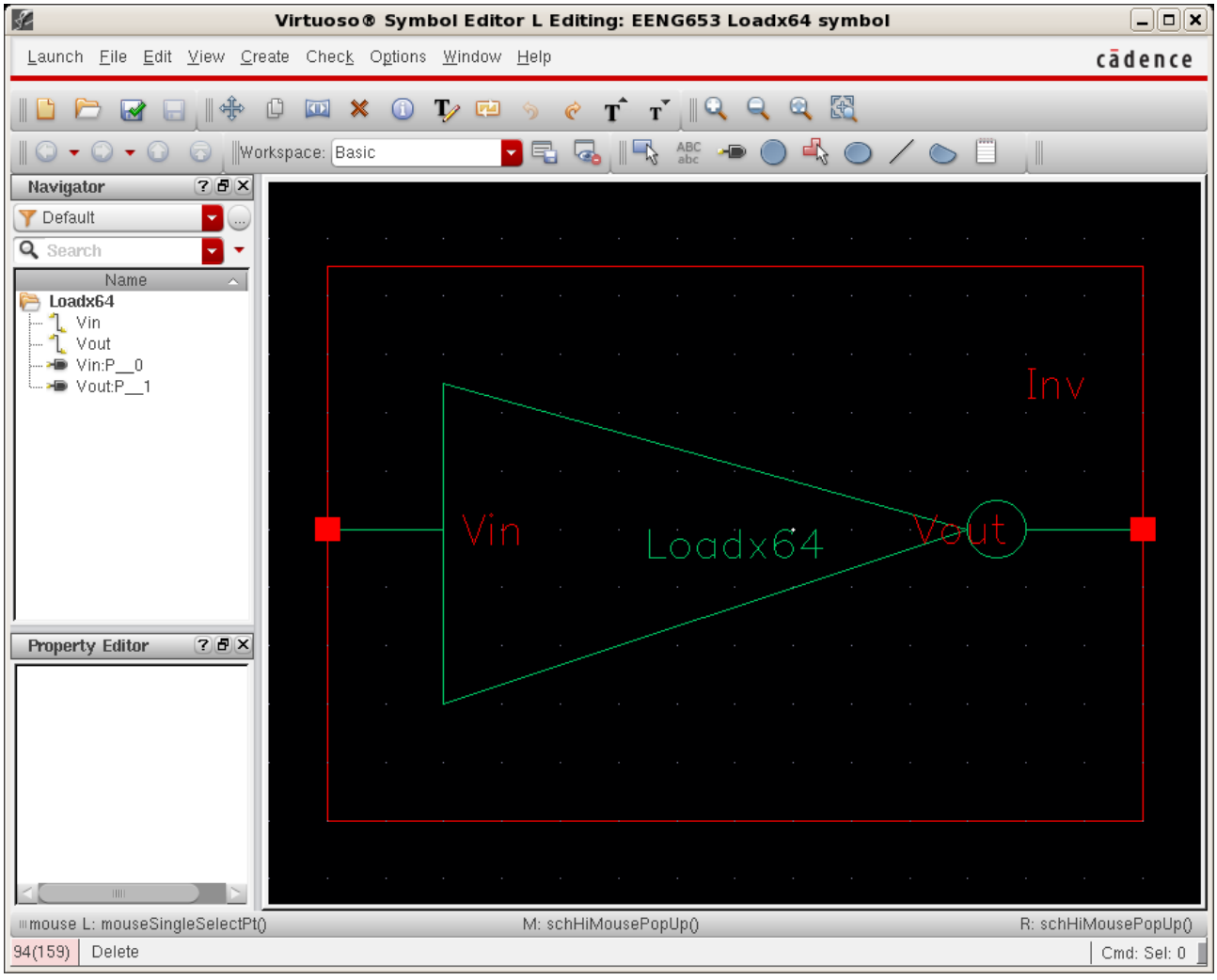
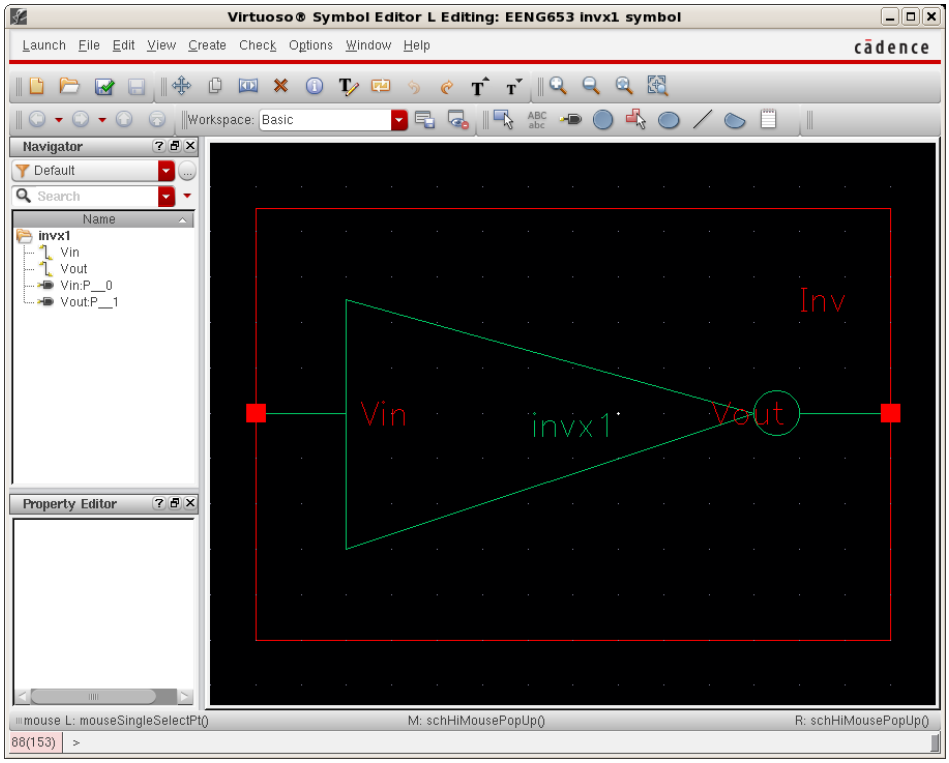
l. The image below shows the Loadx64 symbol.



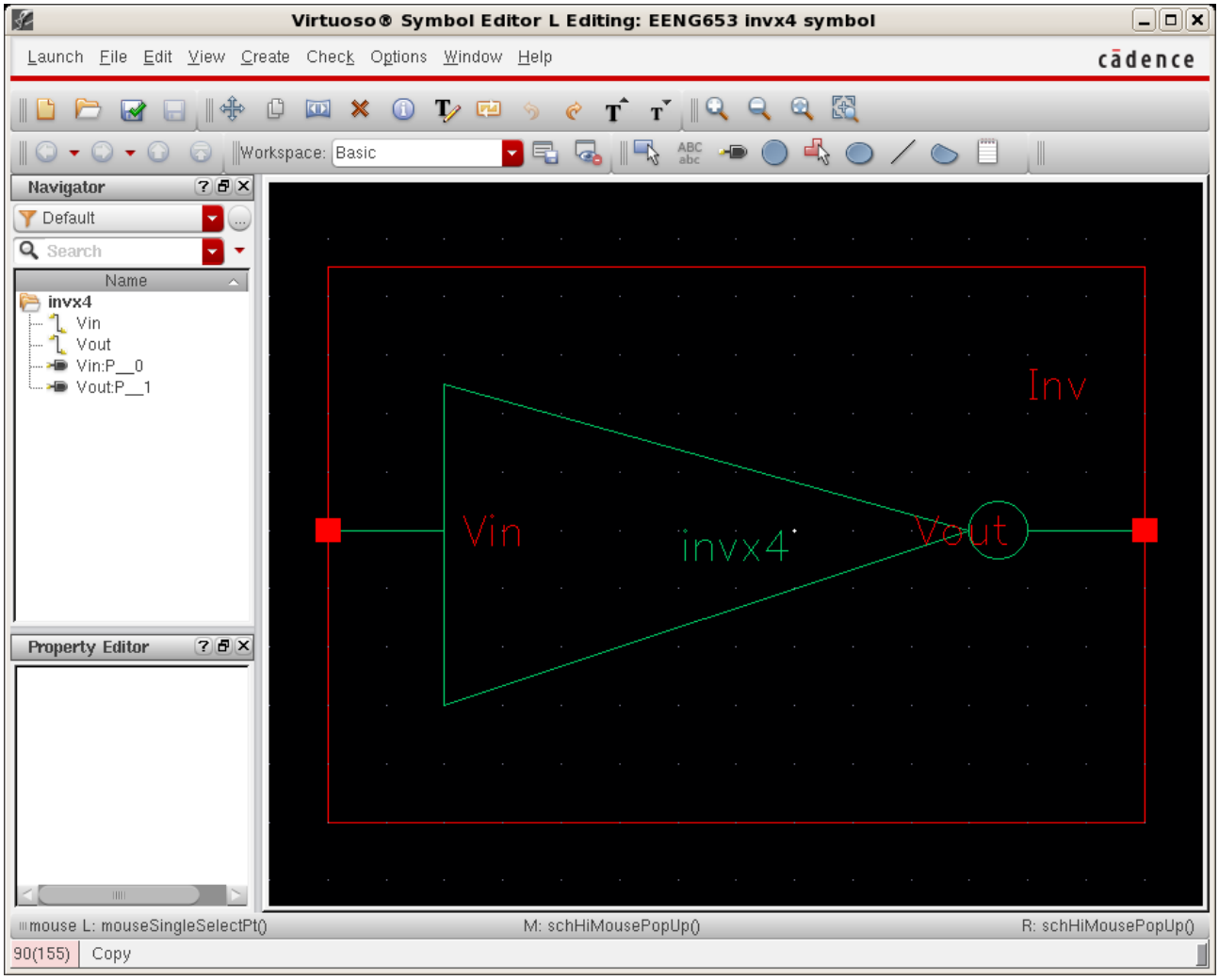
m. Now you will edit each of the symbols that correspond to the four inverter schematics to indicate their different characteristics. This revision is not necessary but it is a good design practice. Recall that to open the symbol, you can click on the Library Manager and then double-click on the symbol view of the invx1 inverter.

Select 'Edit → Properties → Objects' and then click on the green text of the symbol itself. Type the name of the symbol; the symbol should change to reflect the change. Save the symbol.

For the case of the invx1 symbol, change the text to 'invx1'. The image of the invx1 symbol is shown below.



n. Change the names in the symbols of the other inverters. The image below shows the symbol of the invx4 inverter.



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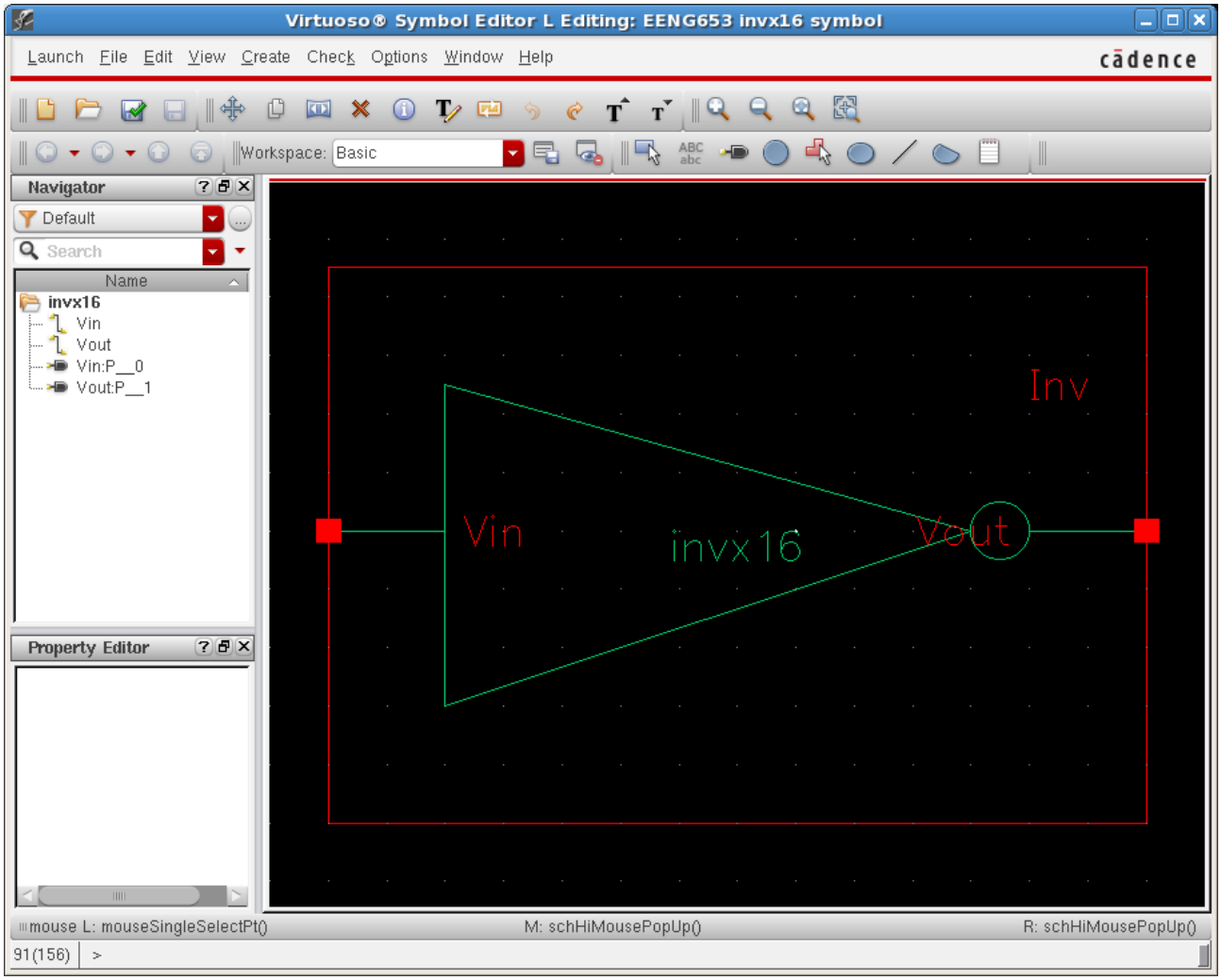
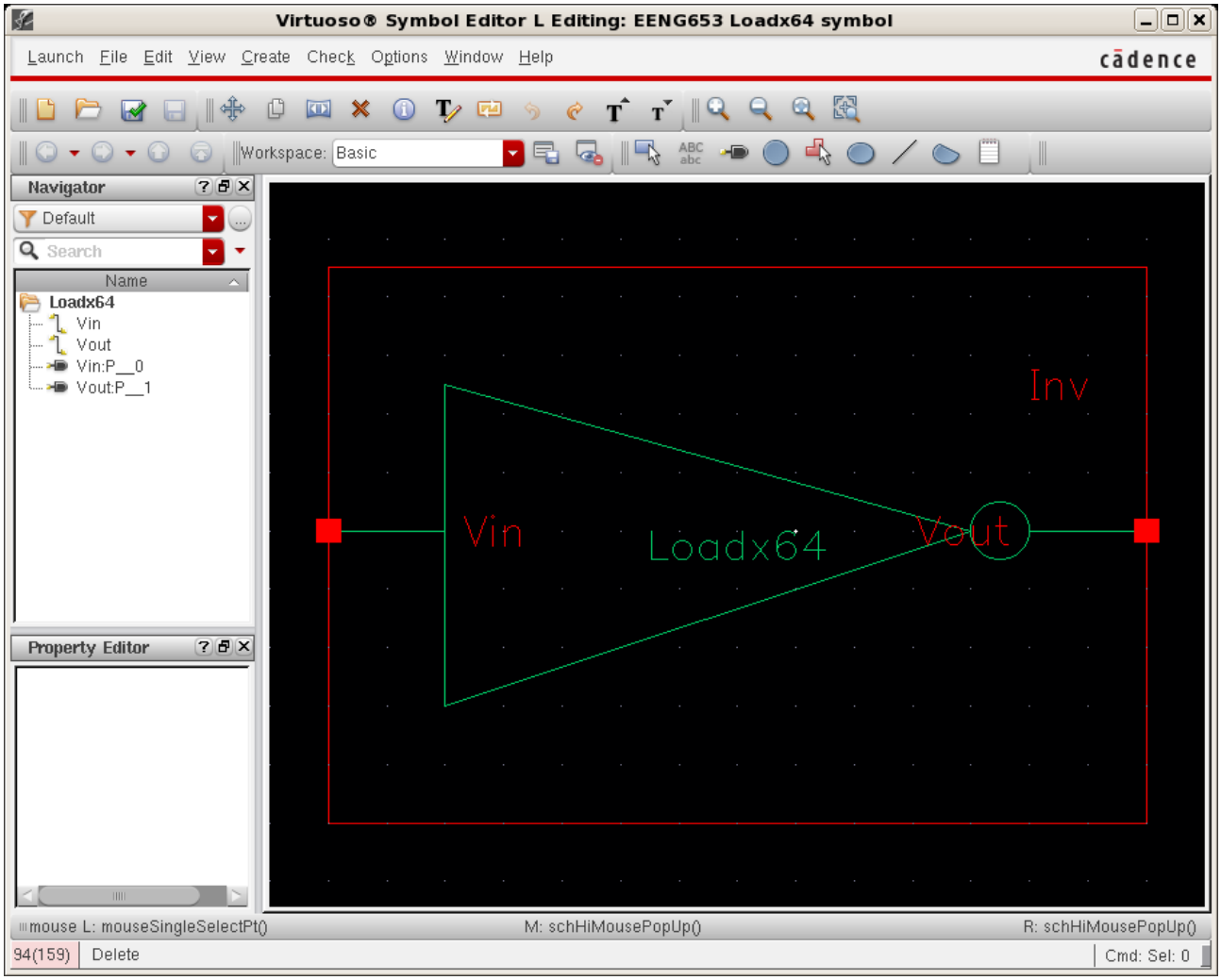
o. The image below shows the symbol of the invx16 inverter.



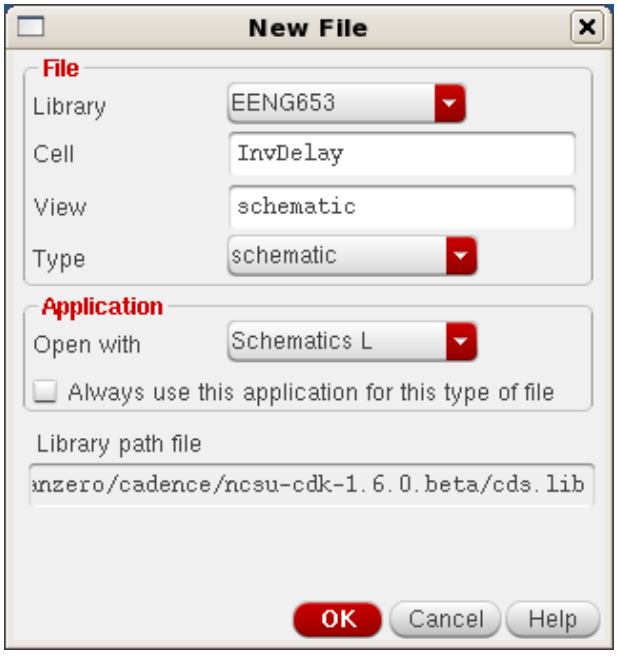
p. The image below shows the symbol of the Loadx64 inverter.



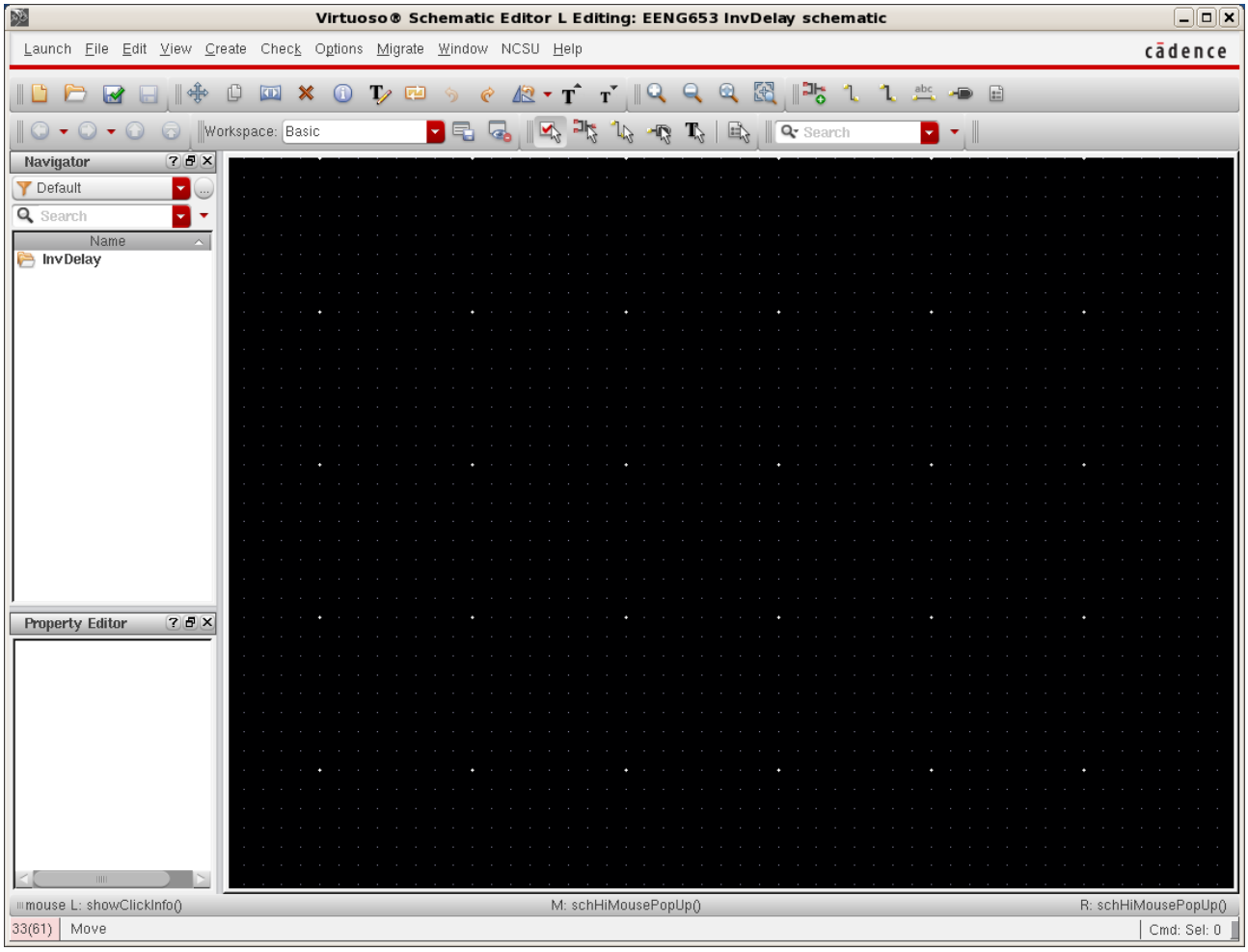
q. Now you are going to create a hierarchical schematic of an inverter chain. In the schematic of the inverter chain, you will instantiate one instance of an invx1, one instance of an invx4, one instance of an invx16, and one instance of a Loadx64 inverter.

You can call the new hierarchical schematic, 'InvDelay.' Open the Library Manager and highlight the 'EENG653' library. Select 'File → New → CellView,' and the 'New File' form will appear as shown in the image below. Complete the form as shown in the image. The Cell name will be 'InvDelay,' and the View name will be 'schematic.'

Then click 'OK' on the form.

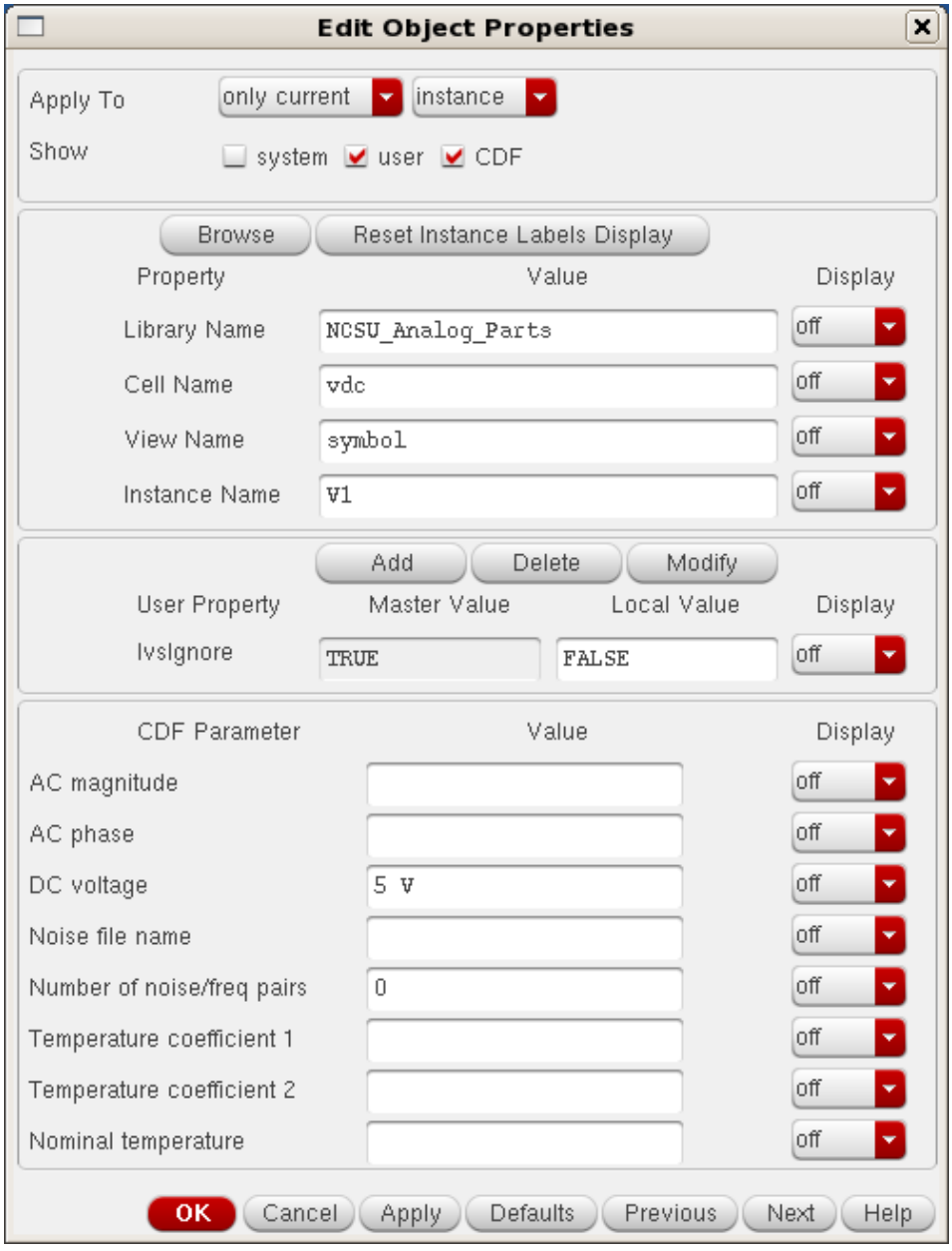


r. After clicking 'OK,' an 'EENG653' 'InvDelay' schematic window will appear as shown in the image below.

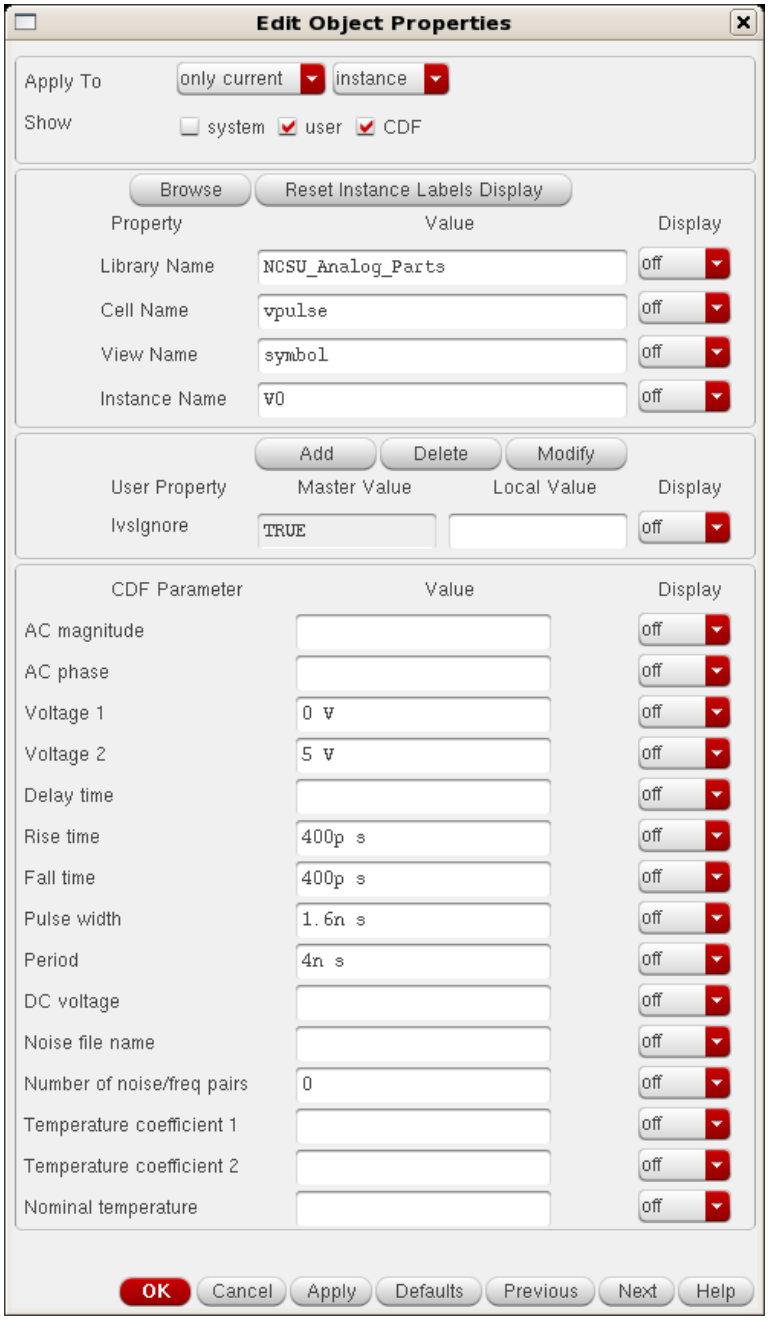


s. In the 'EENG653' 'InvDelay' 'schematic' window, instantiate four cascaded inverters comprised of an invx1 (one instance), invx4 (one instance), invx16 (one instance), and Loadx64 (one instance). Use the Component Browser form as shown in the image below.

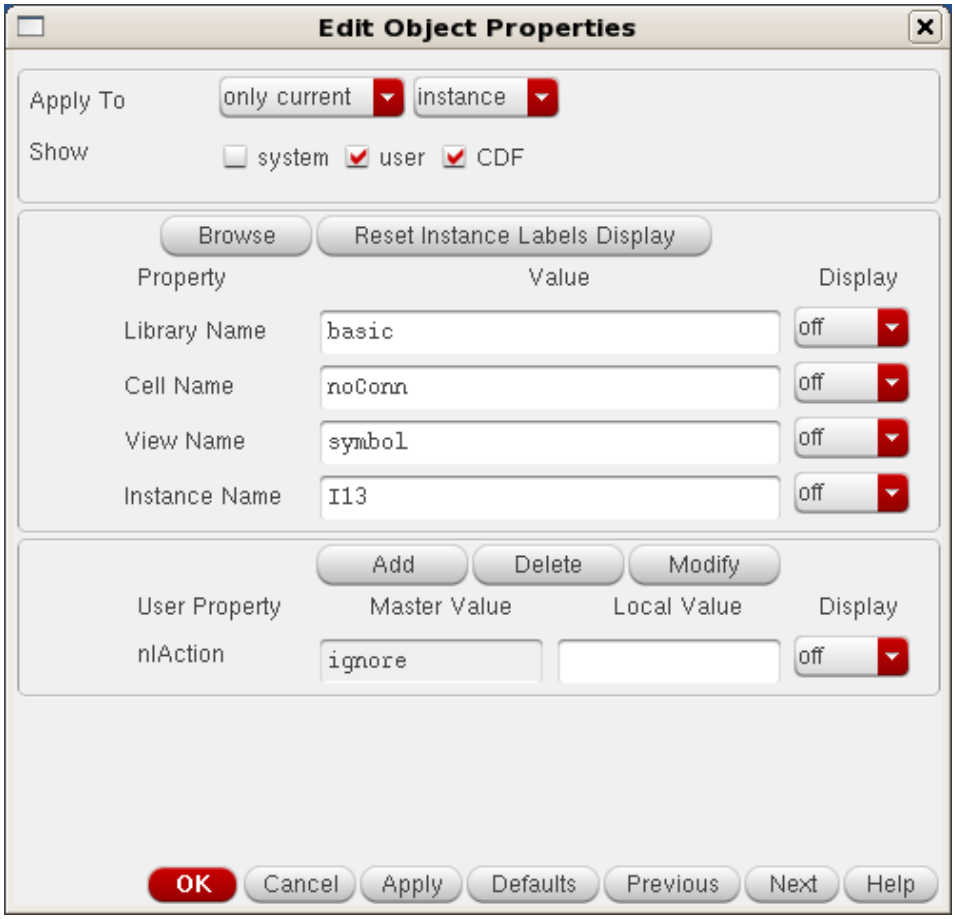
t. Create an instance of the power supply, vdc, and set the values as shown in the image below. Set the DC voltage to 5 V.



u. Create an image of the voltage pulse, vpulse in the schematic. Set the values of the pulse as shown in the image below. Set Voltage 2 = 5 V; Rise time to 400ps; Fall time to 400ps; Pulse width to 1.6ns; and Period to 4ns.



v. Add a noConn symbol to terminate the Loadx64 (final inverter) as shown in the image below.



w. Let's review the creation of this inverter chain.

So far, you have instantiated four inverters, the vpulse symbol, vdc symbol, and the noConn symbol.

Now connect the vdc to vdd (a symbol from the 'basic' library) and gnd (a symbol from the 'basic' library). Connect the terminals with wires (blue).

Connect the vpulse to gnd and to the net "IN1". Use wires and wire labels.

Connect the input port 'IN' to the input of invx1, and label the input net "IN1". Use wires and the labeling tool.

Connect the output of invx1 to the input of invx4 with a wire.

Connect the output of the invx4 to the input of invx16 with a wire.

Connect the output of invx16 to the input of Loadx64 with a wire.

Label the wire between invx1 and invx4 as 'IN2'.

Label the wire between invx4 and invx16 as 'IN3'.

Label the wire between invx16 and Loadx64 as 'OUT'.

Connect the output of invx16 to the output pin labeled "OUT".

Connect the output of the Loadx64 inverter to the noConn.

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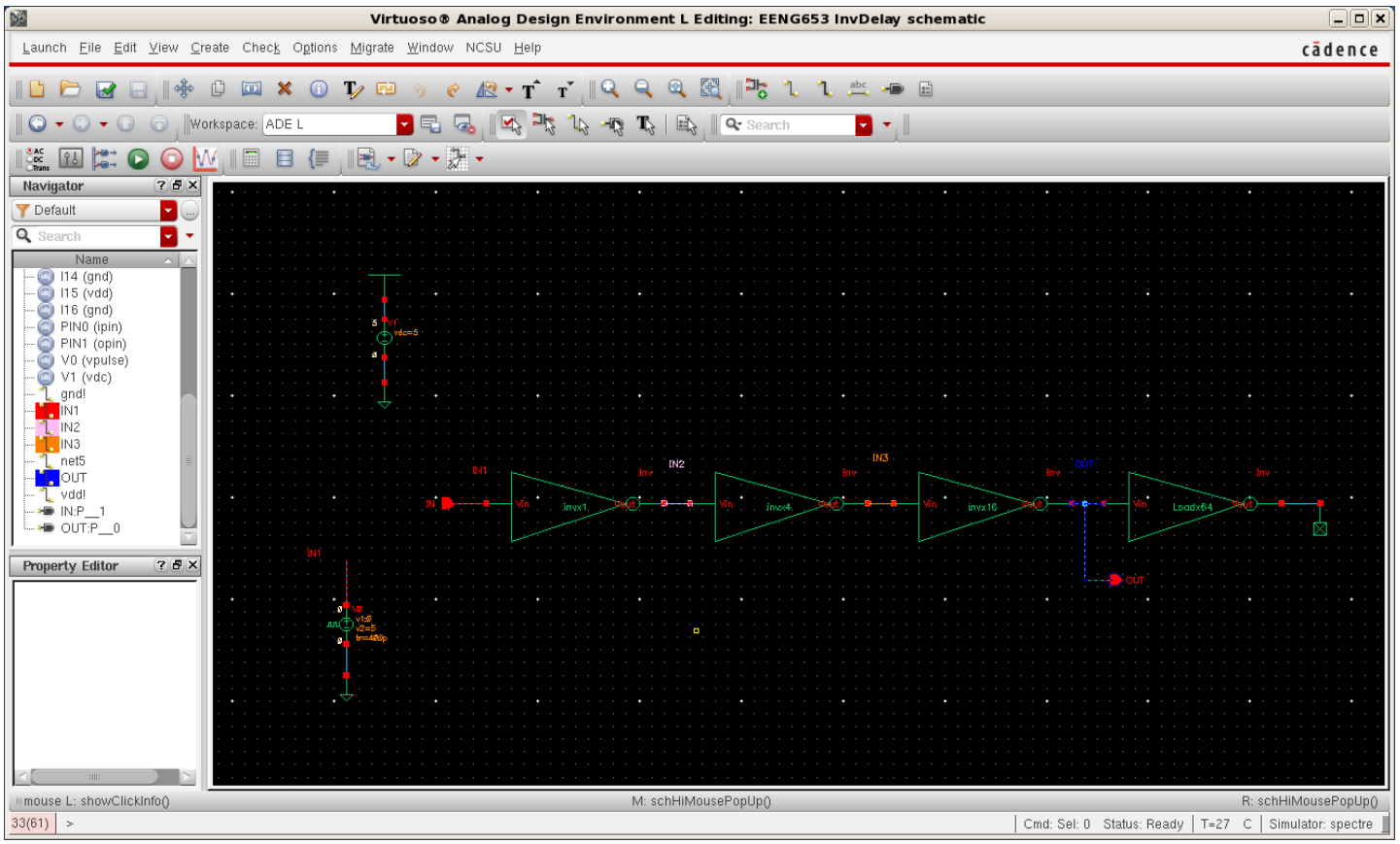
The schematic of the EENG653 InvDelay (inverter chain) will appear as shown in the image below.



x. You have now constructed a schematic of an inverter chain and need to assign values to the widths and lengths of each of the transistors in each inverters (sometimes this process is referred to as *sizing* the transistors).

In this example, you will investigate the delay of the inverter chain for the case in which the fanout is 4 (FO = 4); theoretically, you could have constructed an inverter chain composed entirely of the same inverter, with each inverter driving four different inverters (FO4). In this example, you will use the new parameterized inverters. To achieve an FO4 inverter chain, you will assume that each inverter drives an inverter for which (1) the nfet width is four times the width of the driving nfet, and (2) the pfet width is four times the width of the driving pfet.

This means that you can keep the first inverter at the base *size*, make the second inverter *four times the size* of the first inverter, make the third inverter *16 times larger* than the first inverter, and the fourth inverter *64 times larger* than the first inverter. We can accomplish *this sizing of the inverter chain* by setting the parameter b = 4.

Note that if you want to generate an inverter chain with a different sizing, you just need to change the value of the parameter b. You can do this easily because you have already defined the parameter b in each inverter.

Before setting up the simulation of the inverter chain, you will learn one additional skill that is useful in your work with schematic entry. This skill is the ability to *traverse the schematic hierarchy*.

In order to traverse the schematic hierarchy *in Read mode*, click on the EENG653 InvDelay schematic, and then select "Edit → Hierarchy → Descend Read." Then click on the instance – such as the first inverter - in which you wish to descend (without the ability to edit).

In order to traverse the schematic hierarchy *in Edit mode*, click on the EENG653 InvDelay schematic, and then select "Edit → Hierarchy → Descend Edit." Then click on the instance in which you wish to descend (with the ability to edit).

y. Before you simulate the inverter chain, there are a couple comments about the use of four inverters in the chain. Specifically, you will use the InvDelay schematic to determine the optimum value of the pmos to nmos ratio (that is, the value of the parameter a) for a given value of the parameter b. In this example, you will set the parameter b = 4 (for this FO4 inverter chain).

In this example, the role of the first inverter is to generate an input waveform that is more realistic; that is, the rise time and fall time are more realistic than the rise time and fall time of a waveform that is a simple step or piecewise linear (as for the waveform that is generated by vpulse).

The last inverter (Loadx64) is used only as a load, in this example.

Note that you are strongly recommended to use this type of approach when you estimate delays through simulation; do not drive inputs directly because the results may be unrealistic.

The two remaining inverters (invx4 and invx16) are used in the inverter chain so that you can measure both tpLH and tpHL.

z. Now you will simulate the inverter chain, InvDelay. Click on the EENG653 InvDelay schematic and select "Launch → ADE L". The Virtuoso Analog Design Environment will appear showing the correct library (EENG653), cell name (InvDelay), and view name (schematic).

Setup the simulation for spectre by clicking on the ADE environment window with 'Setup → Simulator/Directory/Host' and select spectre in the "Choosing Simulator/Directory/Host" window that appears.

Select the correct model libraries by clicking on the ADE environment window with 'Setup → Model Libraries" and choosing the following two model libraries in the "spectre6: Model Library Setup" window that appears:

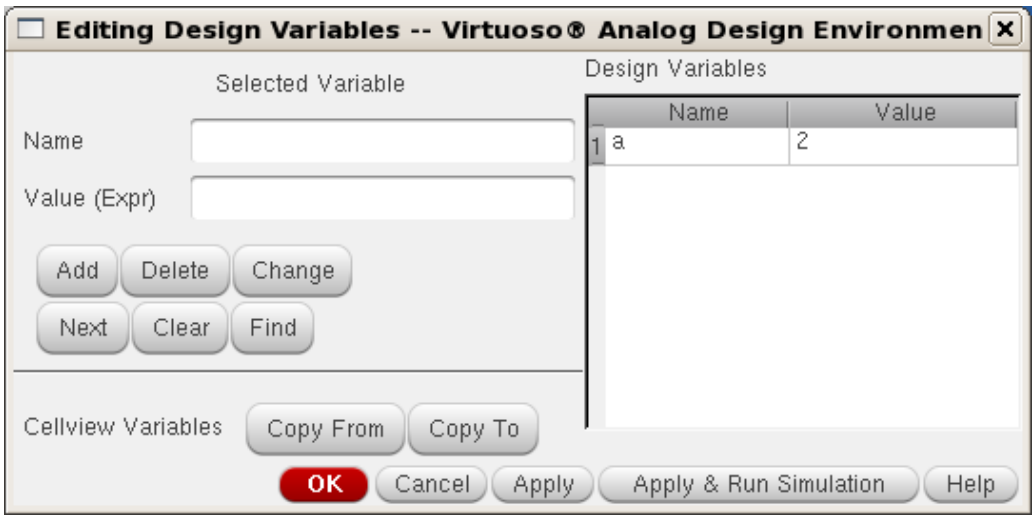
1. /apps/vlsi/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06N.m
2. /apps/vlsi/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06P.m

Select the transient simulation type by clicking on the ADE environment window with 'Analyses → Choose' and selecting 'tran' in the "Choosing Analyses" window. In this window, set the "Stop Time" to 8n (type 8n in the window). Select 'moderate' as the Accuracy default. Make sure there is a 'check mark' in the radio button next to the word 'Enabled.' Then click OK.

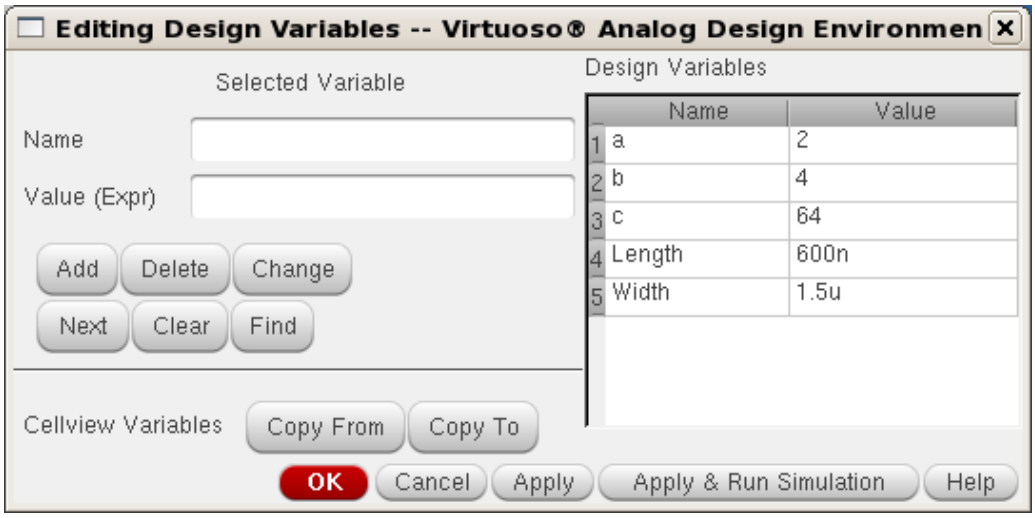
Select all outputs by clicking on the ADE environment window with 'Outputs → Save Options' and select 'allpub', 'Save model parameters info', 'Save elements info', 'Save output parameters info', 'Save primitives parameters info', 'Save subckt parameters info', and set 'Output format' to 'psfxl'. Then click 'OK' on the form.

The next settings you will need to make are to set the values of the parameters a, b, c, Length, and Width.

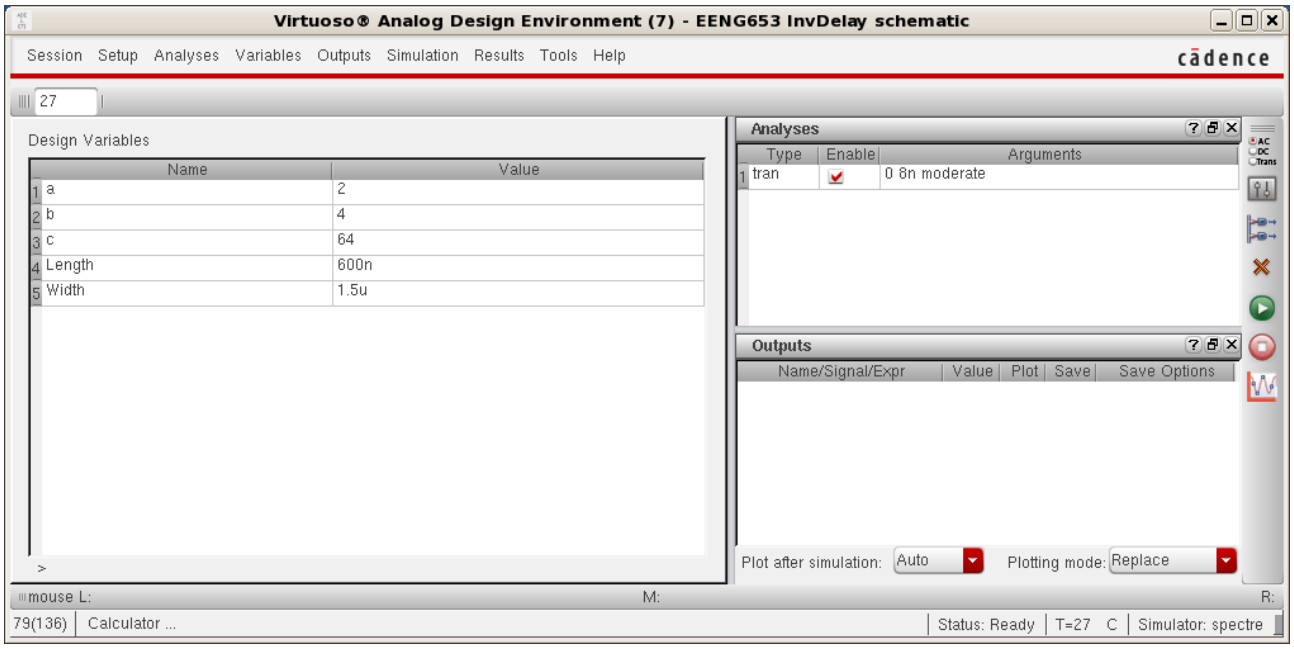
You can set the values of each parameter by clicking on the ADE environment window with 'Variables → Edit', which will produce the 'Editing Design Variables' window as shown in the image below. In the 'Name' dialog box, enter a, and in the 'Value (Expr)' dialog box, enter 2. Then click the 'Add' button. The parameter a with value 2 will move to the right-hand side of the form as shown in the list below under the name 'Design Variables.'



aa. You can now enter the values for the parameters b, c, Length, and Width. Set the value of the parameter b to 4, the value of the parameter c to 64, the value of the parameter Length to 0.6 microns (0.6u), and the value of the parameter Width to 1.5 microns (1.5u). The list of design variables will now appear as shown in the image below.



bb. You are now ready to simulate. Look again at the Virtuoso Analog Design Environment window. The list of design variables will appear on the left-hand side of the window, as shown in the image below. Note that the window also shows that the type of analysis is 'tran' (it is enabled).



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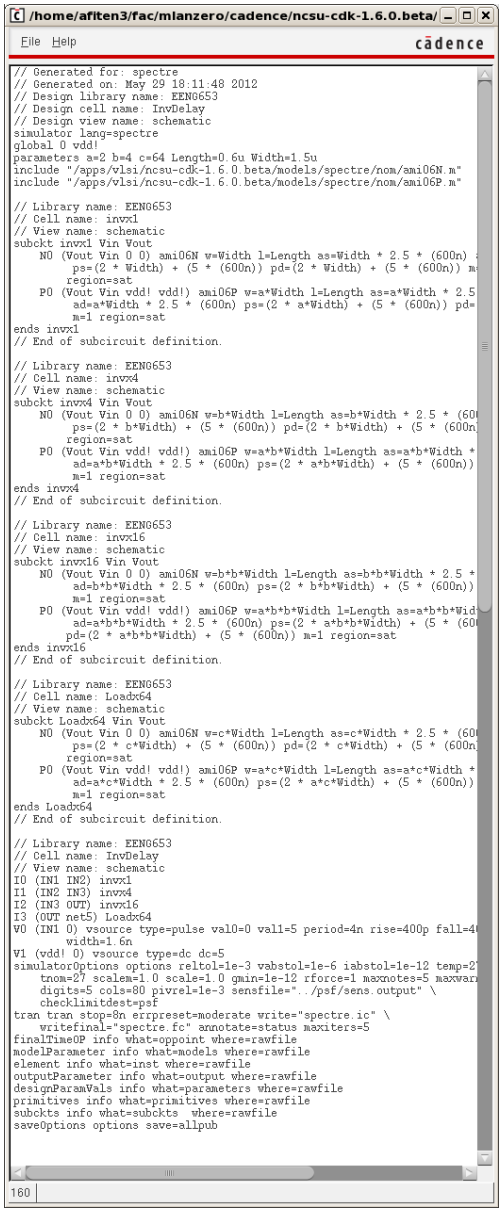
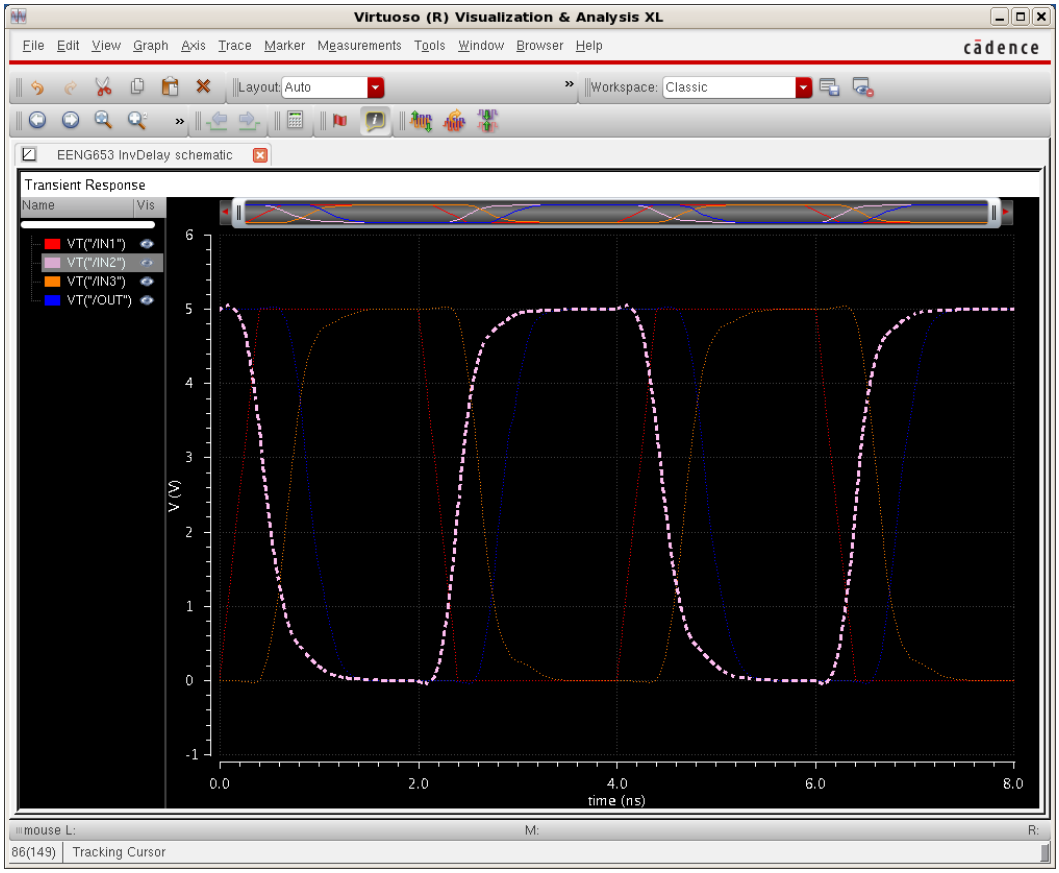
cc. Generate a netlist for your InvDelay inverter chain by clicking on the Virtuoso ADE window and selecting "Simulation → Netlist → Generate Raw.' A netlist window will appear as shown in the image below (the input.scs file).



dd. Now you can run the simulation by clicking on the ADE window and selecting "Simulation → Run." A run window will appear as shown in the image below (spectre.out file).

ee. Remember that each time you change the schematic, you will need to do a Check and Save. If there are no errors in your simulation (look at the CIW to verify that the simulation completed with no errors), you may visualize the simulation results. Since this is a transient analysis, you will inspect voltage waveforms.

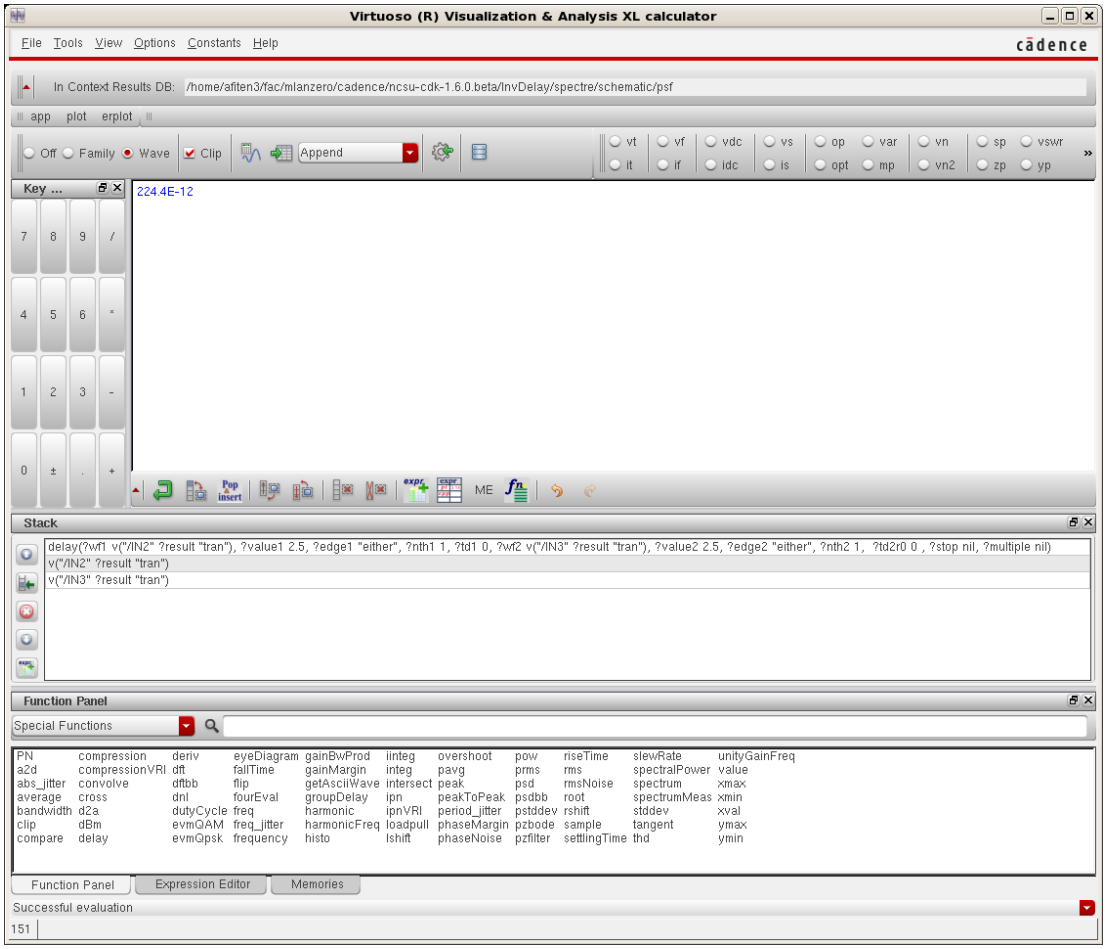
To visualize the simulation results, click on the ADE window and select 'Results → Direct Plot → Transient Signal'. A Virtuoso Visualization & Analysis XL window will appear. Click on the InvDelay schematic and select the signals IN1, IN2, IN3, and OUT. Then type 'ESC'. The waveforms will appear as shown in the image below (select one to highlight it).



28. Parameterized Inverter Chain: More Use of the Calculator

a. You can now measure the tpLH and tpHL for the second and third inverters with signals IN2 and IN3 (recall that the role of the first inverter is to generate the realistic waveform, and the fourth inverter is the load). To do this accurately, you are going to use the waveform calculator (you can also save the waveforms in a table, as explained earlier).

To open the waveform calculator, click on the ADE window. Then select 'Tools → Calculator' which will open the calculator as shown in the image below.



b. Get familiarized with the waveform calculator (also discussed previously). The calculator works with a 'stack' in which you first input a waveform (or more than one waveform) and then perform an operation. After each operation, it is recommended that you clear the stack. To view the stack, you have to enable it (click on the button 'Display Stack').

Now click on 'wave' in the calculator window. The toggle button should be selected next to the word 'wave'.

Now click on the IN3 waveform in the Virtuoso Visualization and Analysis XL window. A wave will be displayed in the calculator window.

Now click on the IN2 waveform in the Virtuoso Visualization & Analysis XL window. The first wave (for IN3) will appear in the stack, and the IN2 wave will appear in the calculator window.

Note that you have entered the waves in reverse order (the later wave first, then the early wave); this is a feature of the stack operation of the calculator.

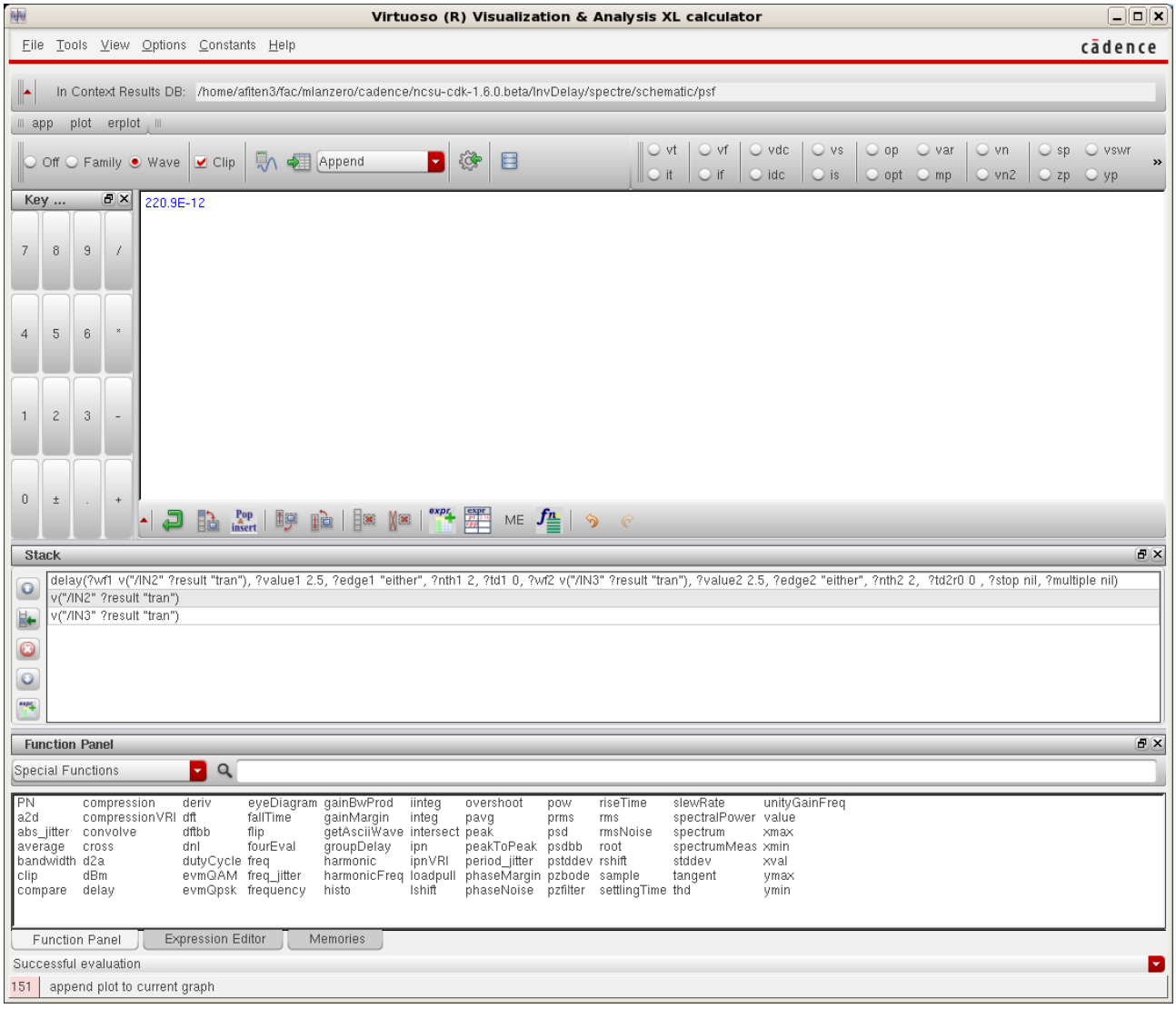
Now click on 'Special Functions' at the bottom of the calculator. Click on 'delay'. In the 'delay' form that appears, fill in 2.5 as the threshold values (since 50% of Vdd = 5 V is 2.5 V); Set 'Edge Number 1' to 1; Set 'Edge Number 2' to 1; Set 'Edge Type 1' to either; Set 'Edge Type 2' to either; Then click OK.

Notice the change in the calculator window. There will be a long expression.

Now click the icon for the 'Evaluate buffer', and you will see the value of approximately 224ps appear in the calculator window, which represents tpLH for the second inverter with a fanout of 4 (you measured the delay from IN2 to IN3 in a transition going from

low to high). Notice that the value in the calculator window shown above is 224.4E-12 which represents 224.4ps.

c. Clear the 'Evaluate buffer' and the stack. Now measure the value of tpHL for the second inverter. You will follow the same steps as for the previous calculation (of tpLH), except that you will set 'Edge Number 1' to 2 and 'Edge Number 2' to 2. The value for tpHL is approximately 221ps; (for the case of the image below, tpHL is 220.9ps.)



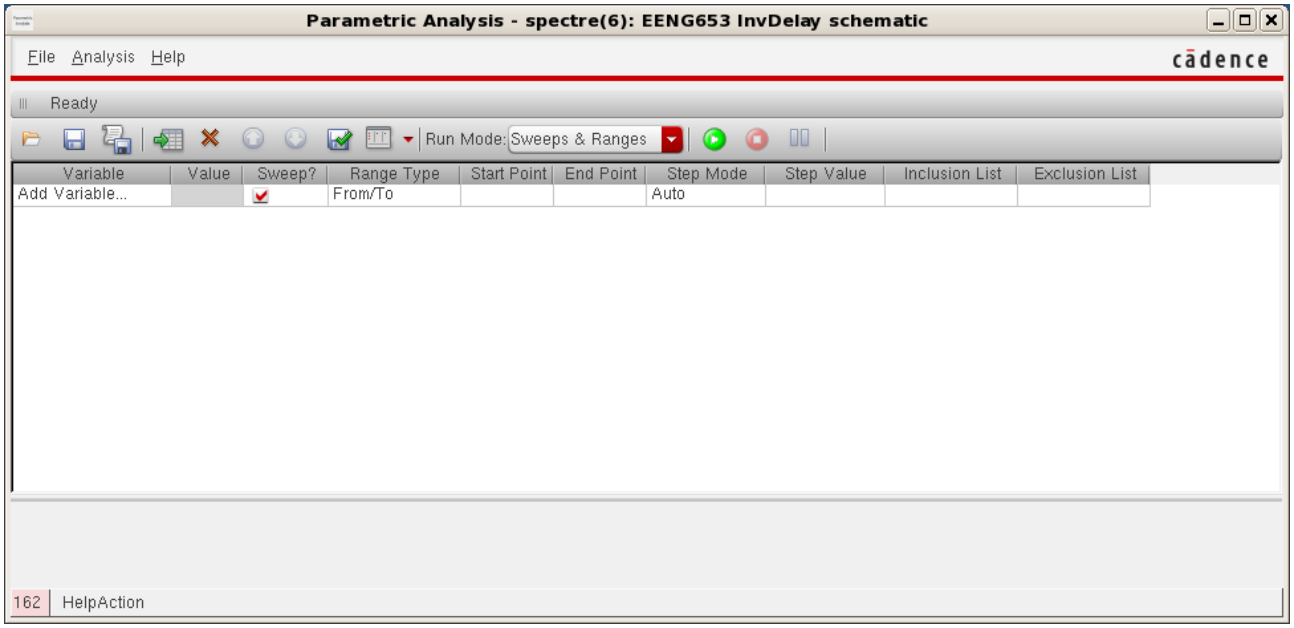
d. The value of tpHL is slightly less than the value of tpLH, as expected because of the difference between the mobility of the electron and the mobility of the hole (the carriers in the nmos and the pmos). What is the ratio of the mobility of the electron and the hole? What is the value of the parameter a? Which is larger? Although the simulation results may suggest that the value of the width of the pmos device may need to be increased even larger (to what value?), you only need to do this (that is, increase the value) if you are mainly interested in producing an inverter with a symmetric voltage transfer curve (VTC) and with equal values of tpHL and tpLH (that is, tpHL = tpLH). If you are interested in propagation delay (the average of tpHL and tpLH), you may actually want to make them less symmetric to gain speed.

e. You have now simulated an inverter chain with FO4.

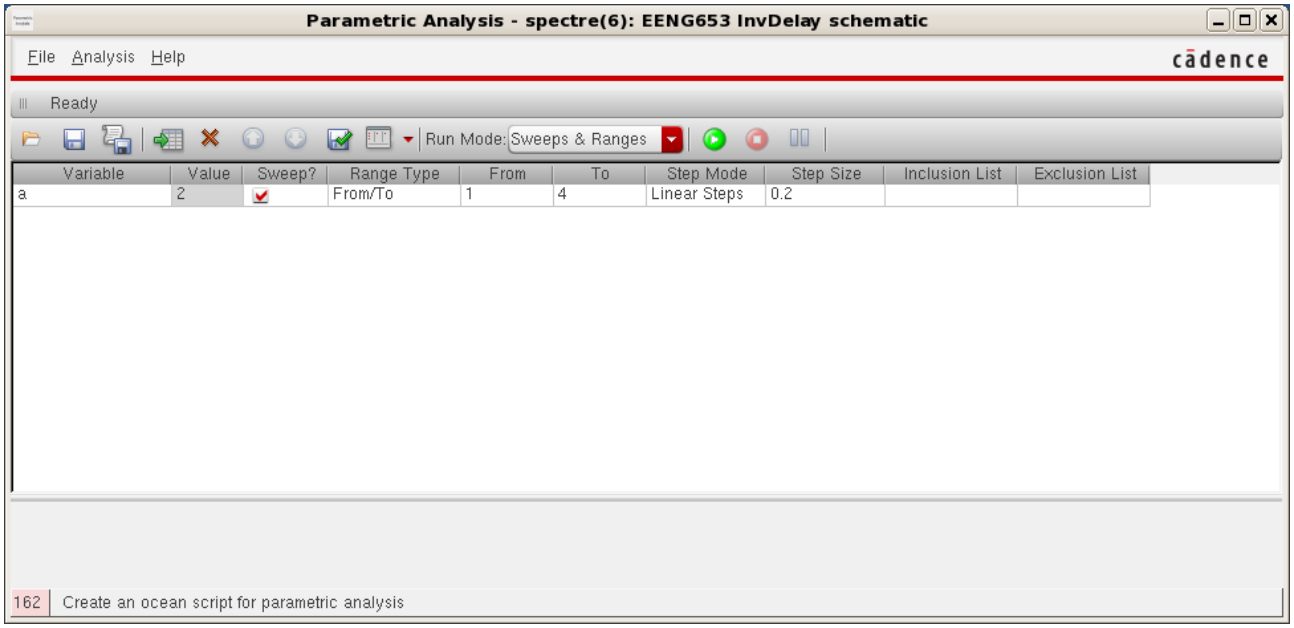
29. Parameterized Inverter Chain: Parametric Analysis of the Delay of an Inverter Chain

a. You will now determine the optimal ratio of the pmos width to the nmos width through simulation. In order to obtain the optimal value of the ratio, you will perform multiple simulations with different values for a, and you will determine the fastest solution. It is possible to perform these simulations manually. In this section you will learn how to perform the simulations automatically in the Cadence software.

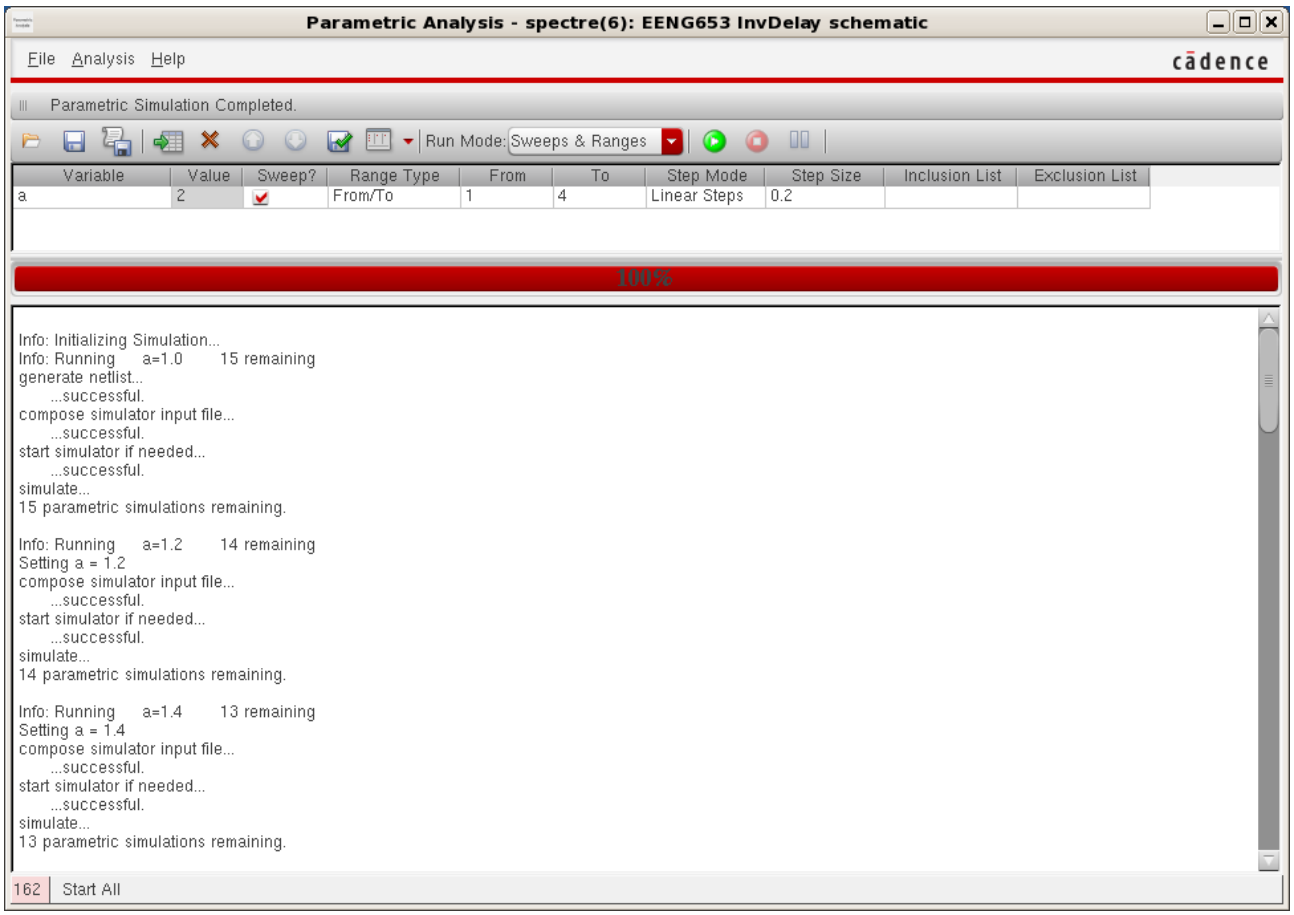
b. Click on the 'Virtuoso Analog Design Environment' window for the EENG653 InvDelay schematic and select 'Tools → Parametric Analysis.' The 'Parametric Analysis' window will appear as shown in the image below.



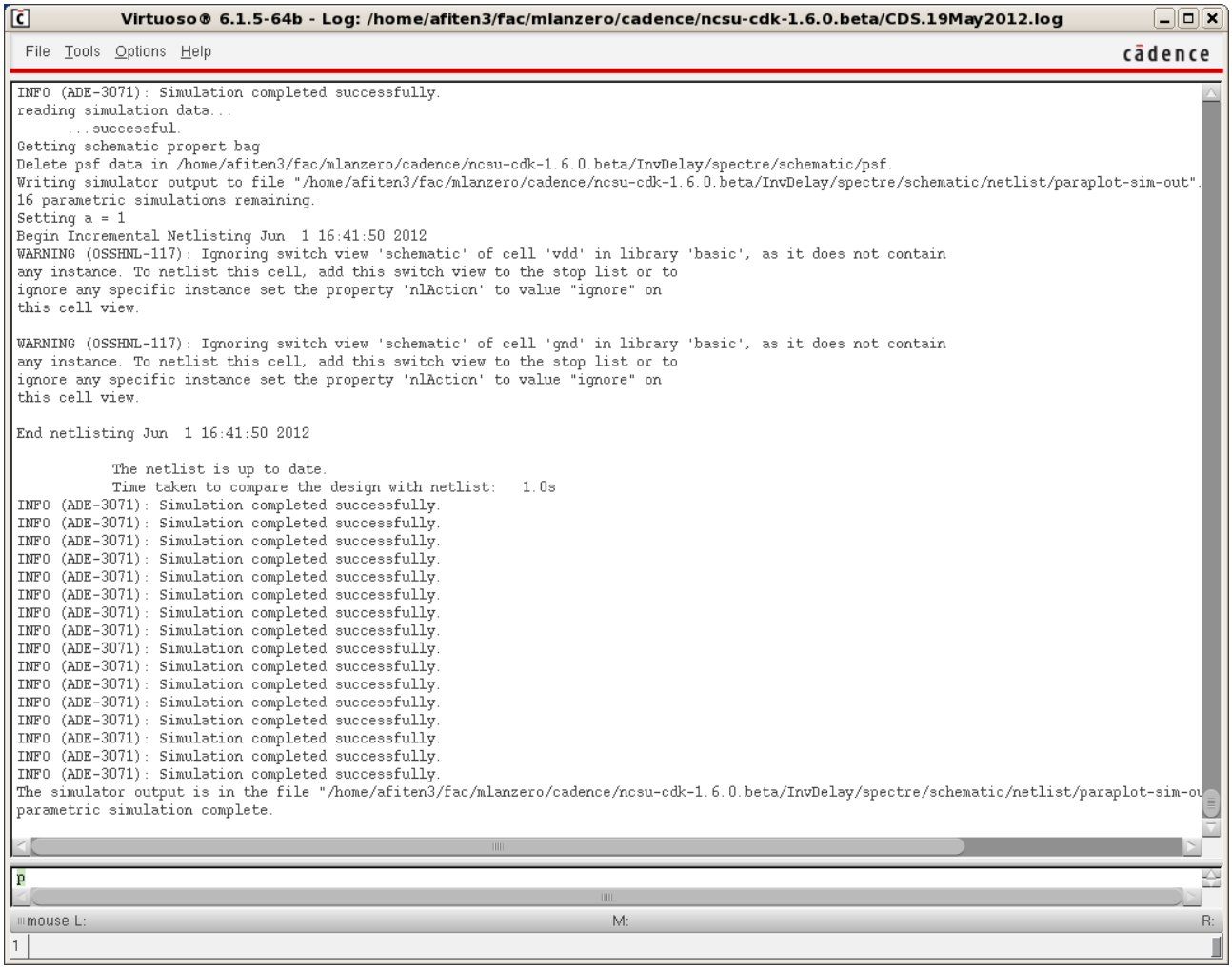
c. In the 'Parametric Analysis' window, type 'a' in the 'Variable' column. Type '1' in the 'From' column; type '4' in the 'To' column; select 'Linear Steps,' and set 'Step Size' to '0.2' as shown in the image below.



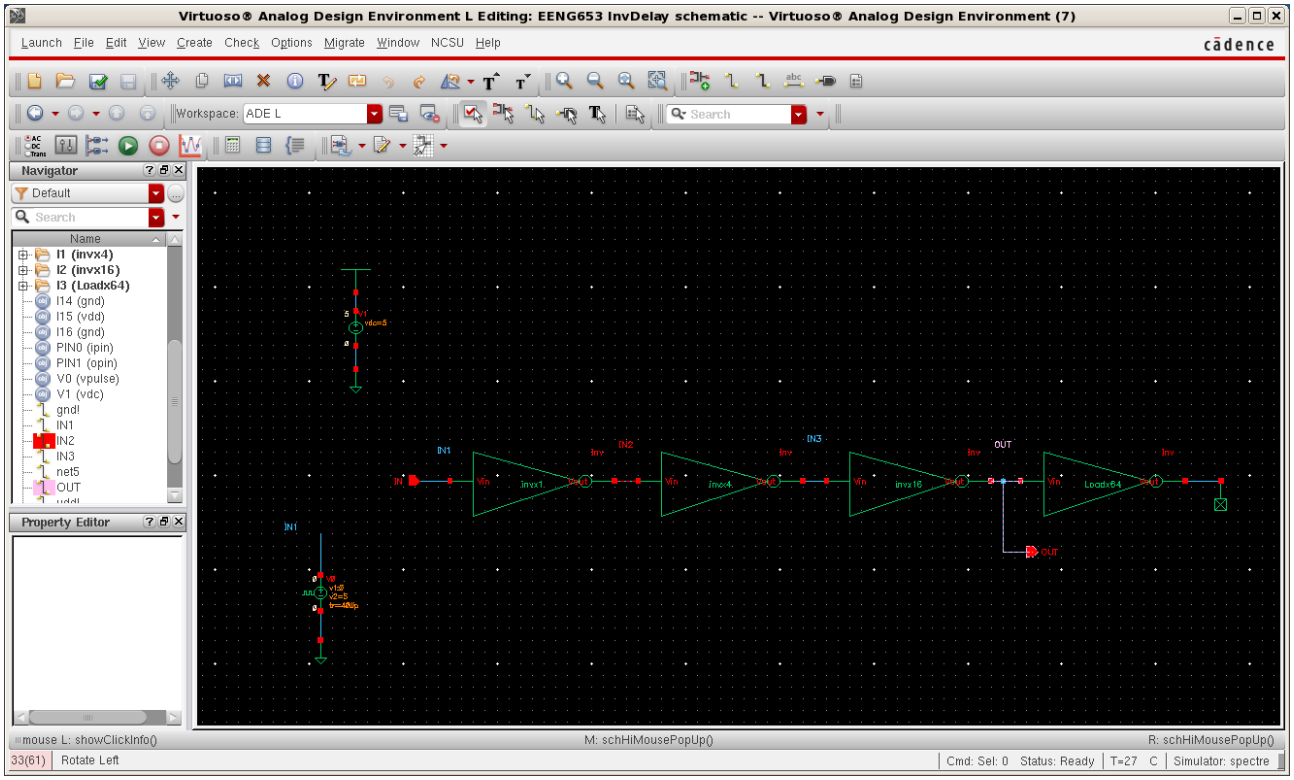
d. In the 'Parametric Analysis' window, select 'Analysis → Start.' The simulations of your inverter chain will start to run, as indicated in the run window of the 'Parametric Analysis' window below.



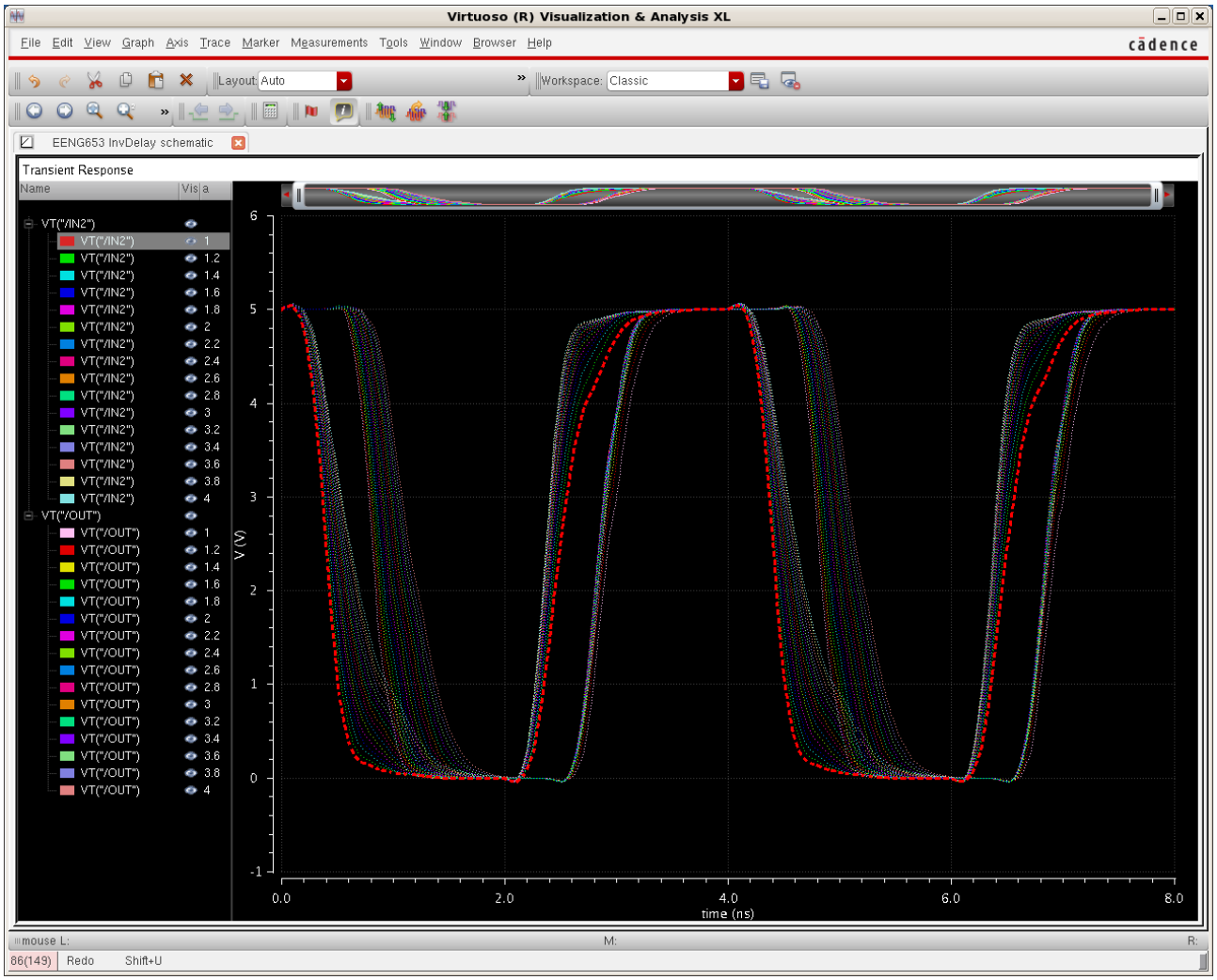
e. The CIW will also report that the simulations are running, as shown in the image below.



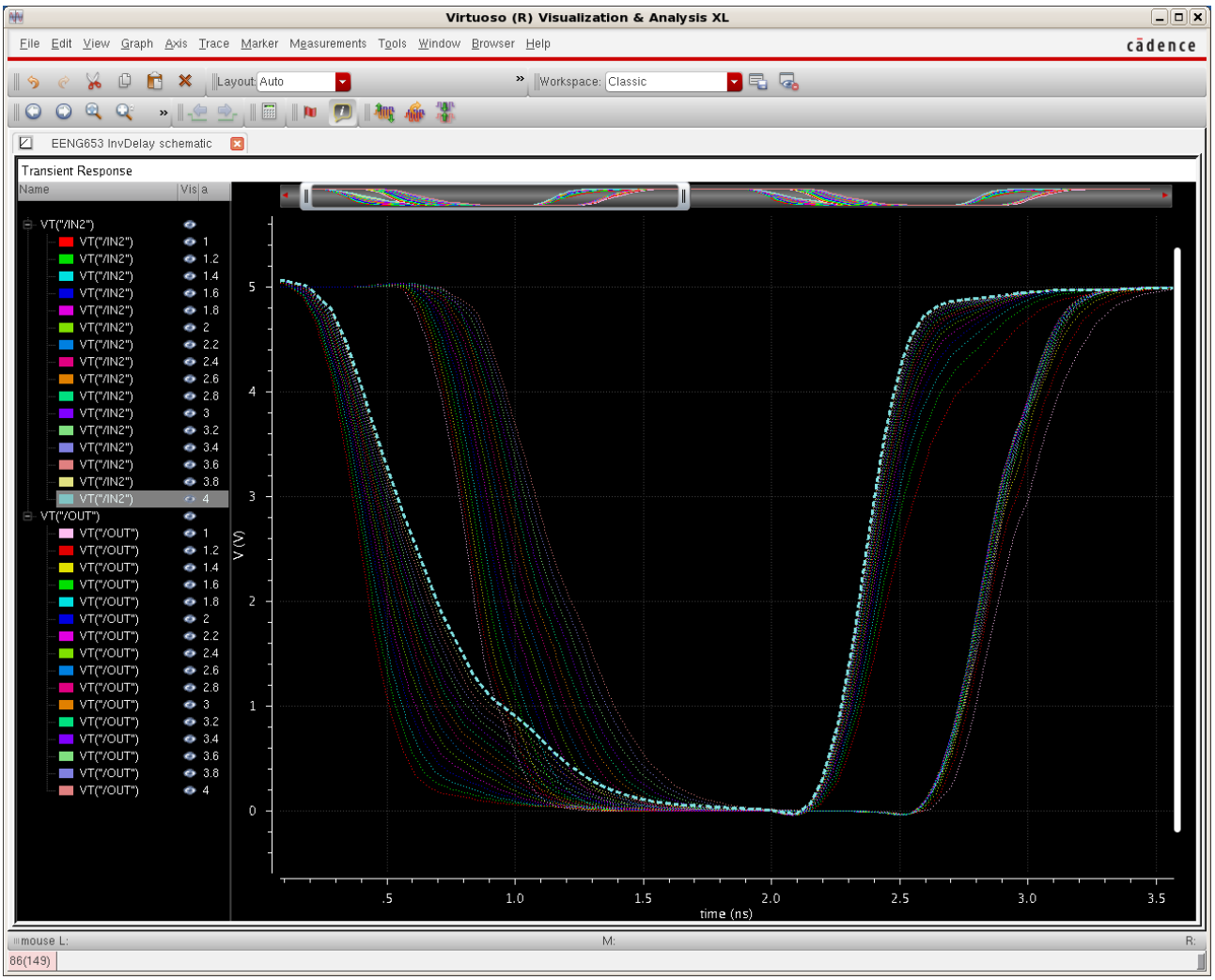
f. When the simulations are completed, you can plot the waveforms. In the Virtuoso Analog Design Environment window, select 'Results → Direct Plot → Transient Signal.' Then move your mouse to the window showing the EENG653 InvDelay schematic and click on the 'IN2' net and the 'OUT' net. These two nets will become dashed lines and will become highlighted, as shown in the image below.



g. Then click 'ESC' in the EENG653 InvDelay schematic, and the Virtuoso Visualization & Analysis XL window will appear showing the 'IN2' waveform and the 'OUT' waveform for the duration of the simulations as shown below (click on the 'IN2' waveform and the 'OUT' waveform to see the left-most keys indicating the simulations with different values of the parameter 'a'). The image below shows the 'IN2' waveform with a = 1.0 highlighted in a red dashed line; this is the fastest high-to-low transition (and slowest low-to-high transition). Note that the values of the delays are similar for a=1 to a=3.



h. The image below shows the 'IN2' waveform with a = 4.0 highlighted in a blue dashed line.



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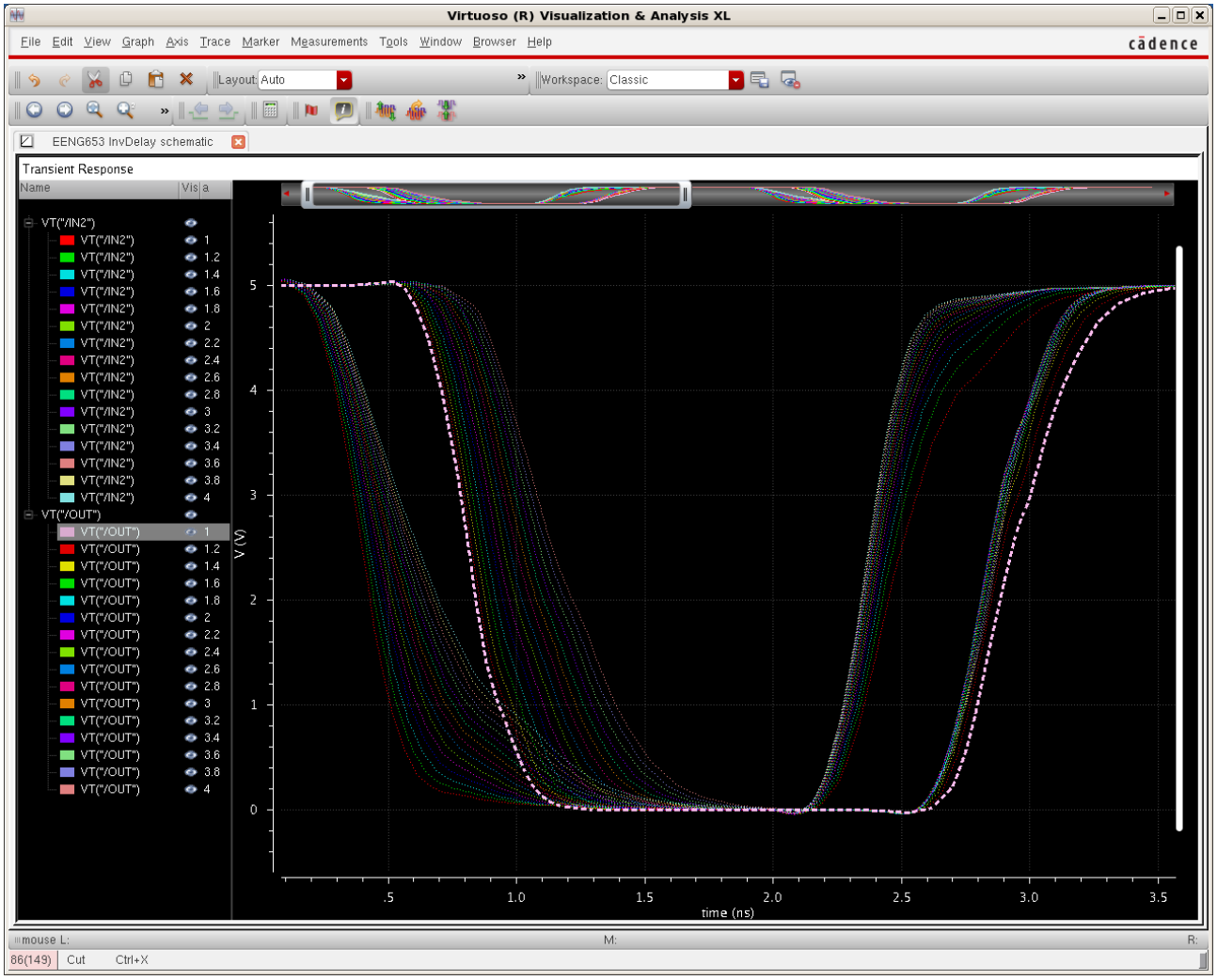
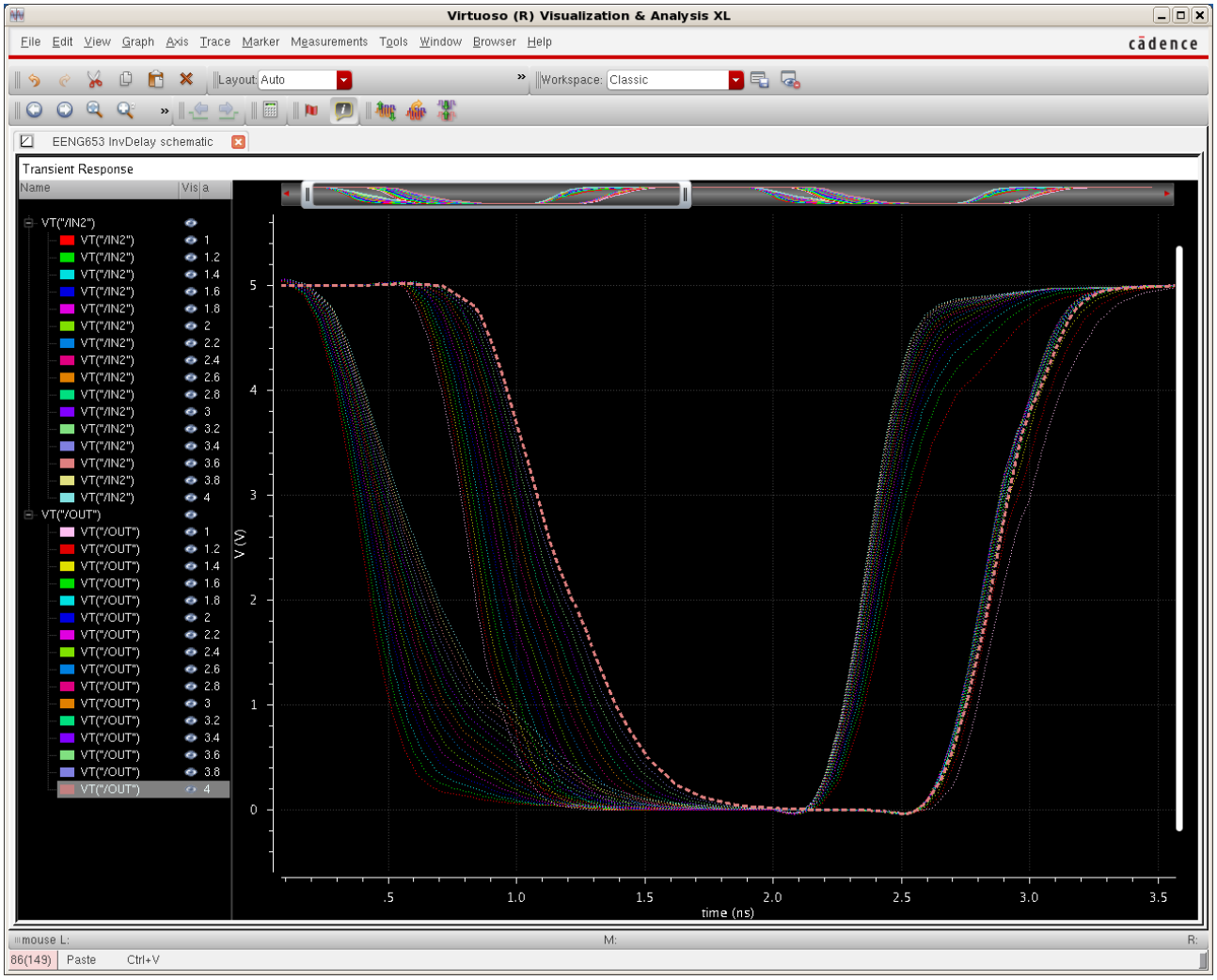
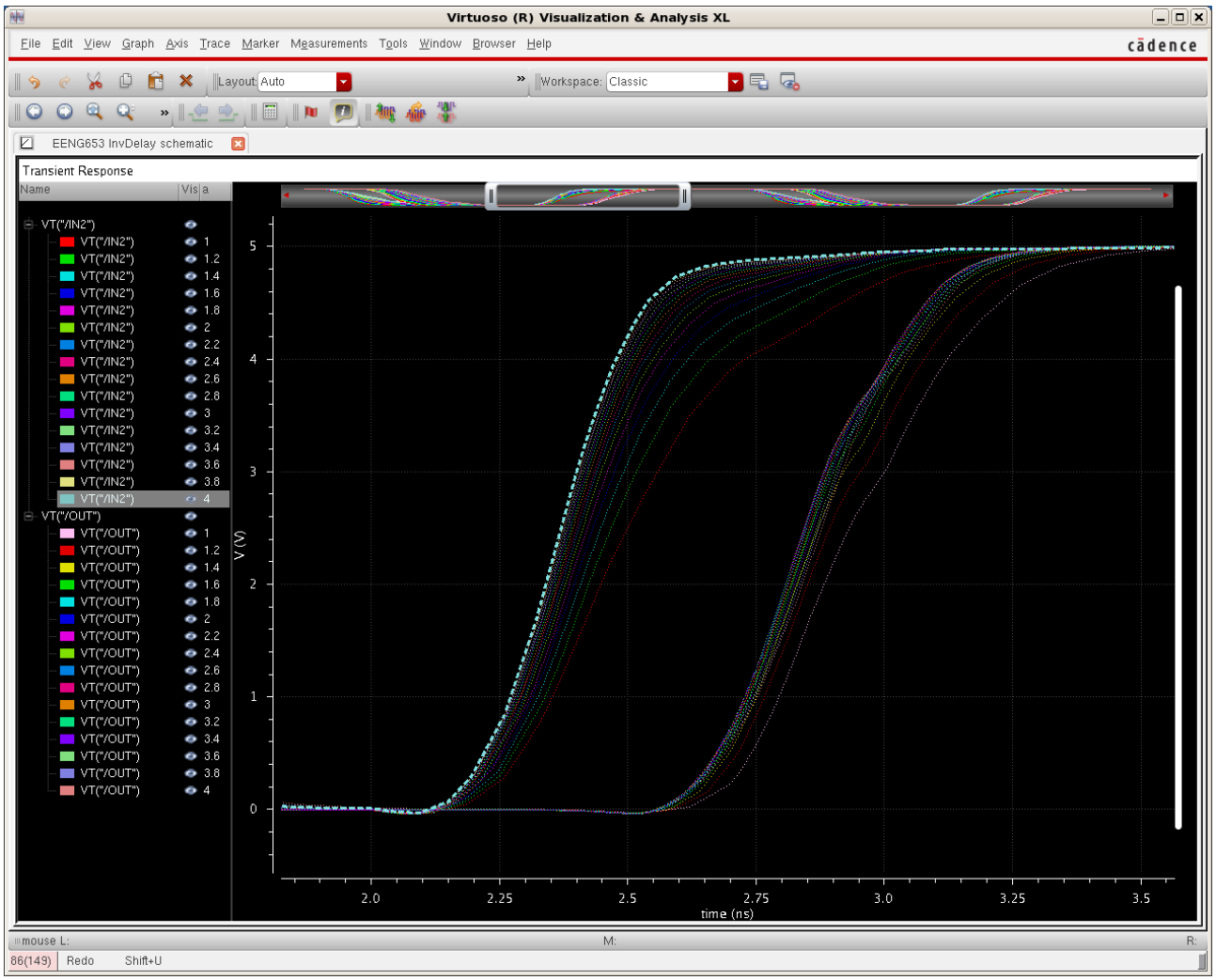
i. The image below shows the 'OUT' waveform with a = 1.0 highlighted in a pink dashed line.



j. The image below shows the 'OUT' waveform with a = 4.0 highlighted in a peach dashed line.



k. If you zoom in on the low-to-high transition of 'IN2', you will see that the fastest transition is the case for which a = 4. The slowest transition is the case for which a = 1 (see the next image).



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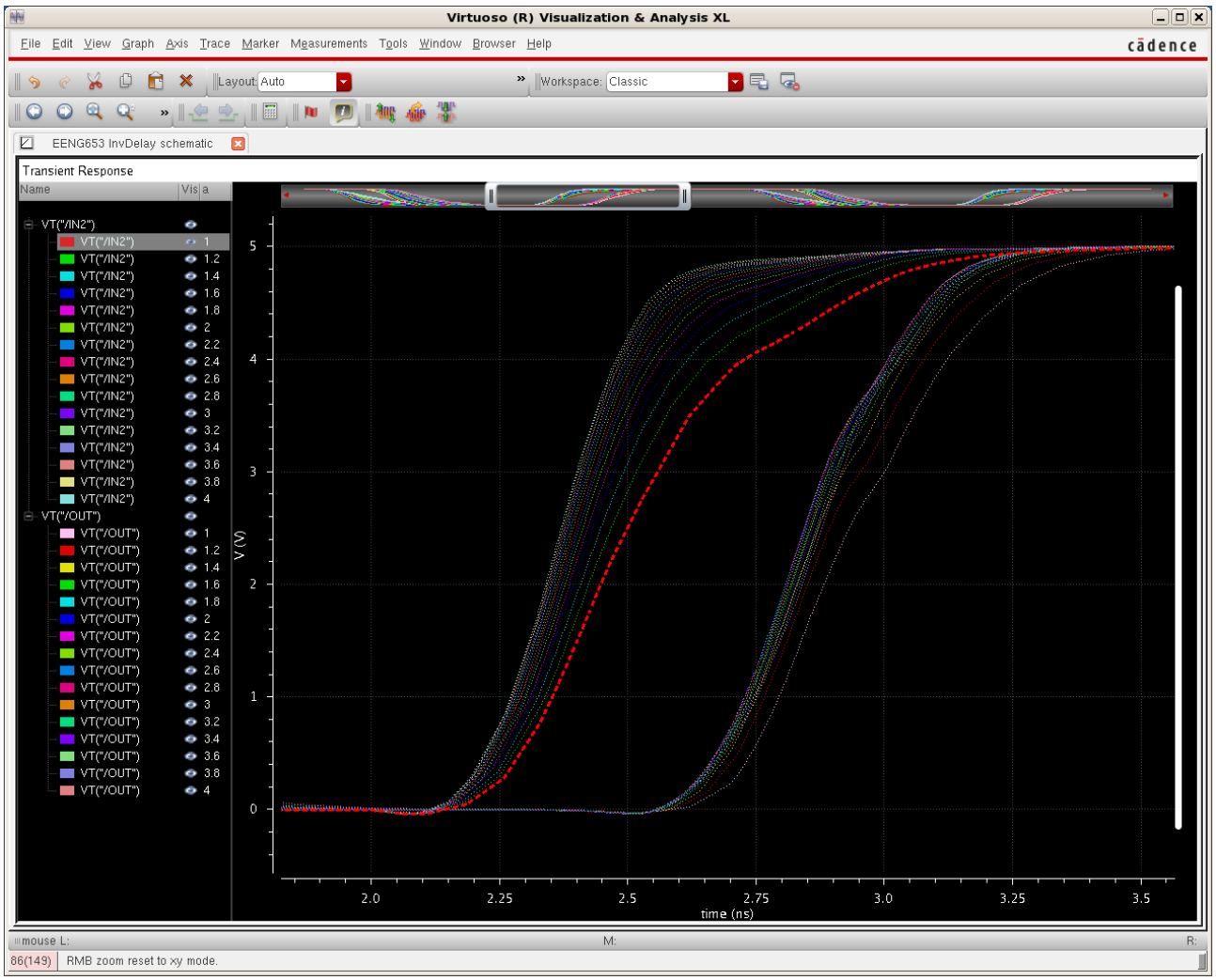
l. The slowest low-to-high transition for 'IN2' is the case for which the width of the pmos device is equal to the width of the nmos device (a = 1).



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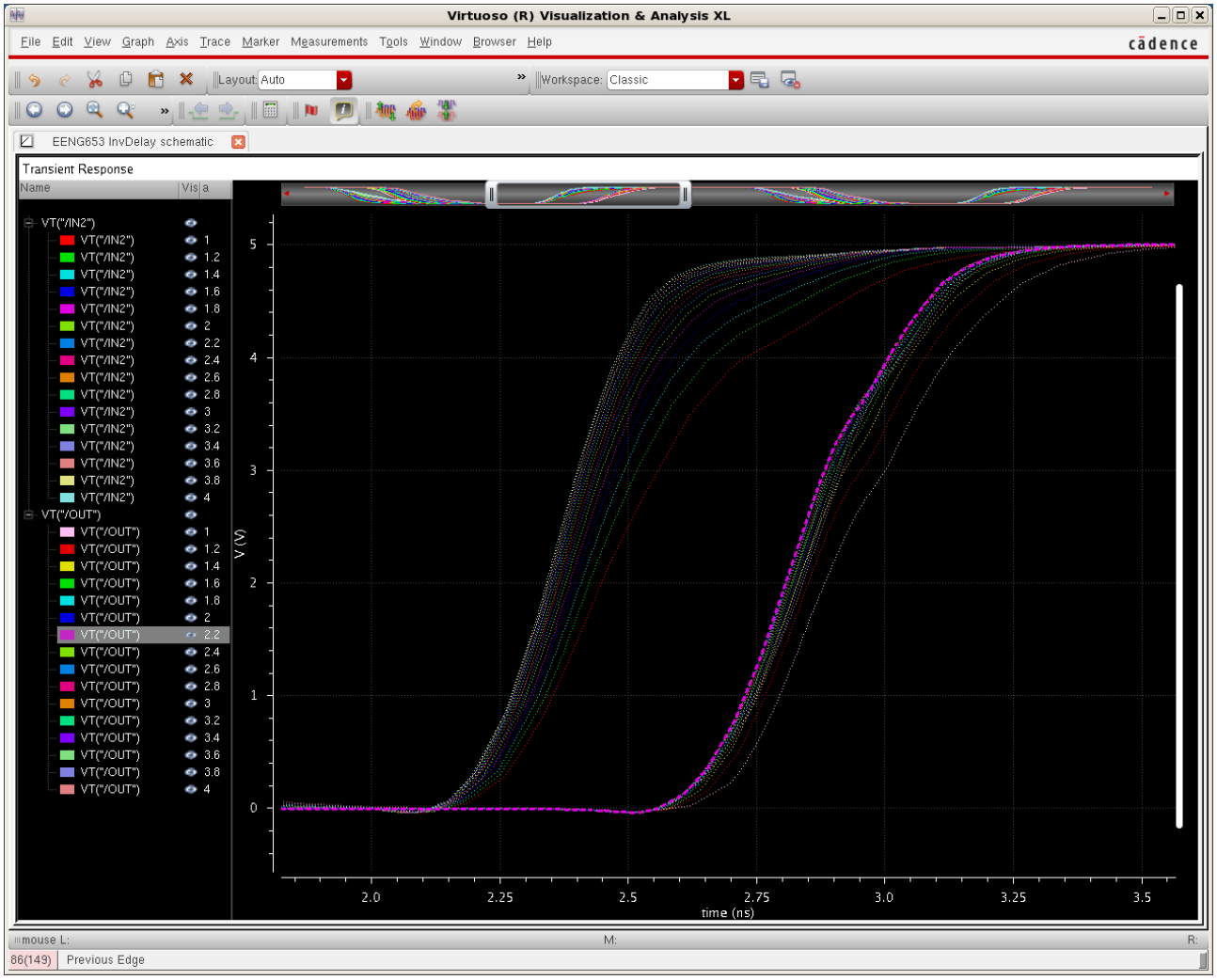
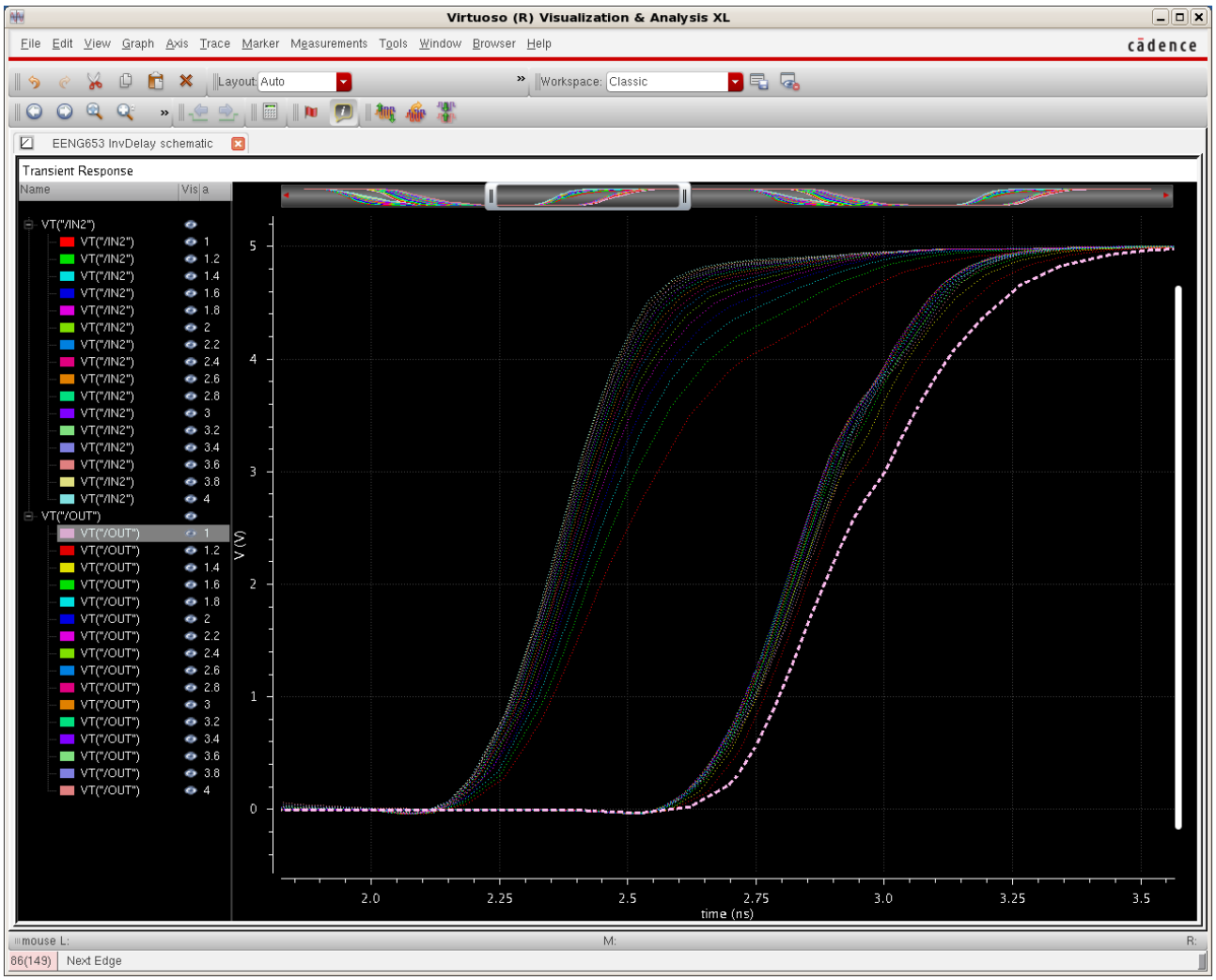
m. The image below shows the 'OUT' waveform with the fastest low-to-high transition, for which a = 2.2 highlighted in a purple dashed line.



n. The image below shows the 'OUT' waveform with the slowest low-to-high transition with a = 1.0 highlighted in a pink dashed line.



o. It is a good idea to save your state before exiting the simulator in case you would like to redo some of the simulations; with a saved state, you can start by loading the state that you saved previously. To save the state, click on the Virtuoso Analog Design Environment window and select 'Session → Save State.' Then input the name that you would like to use for the state and click 'OK' on the form. For example, you can set the 'Save As' field to 'state-InvDelay-schematic.'

30. The End.