Index

A

ABSTOL, 28
Abut, 98, 427, 429-430
AC analysis in SPICE, 19-20, 285
AC small-signal analysis, 280
Accumulation, 132-134, 136, 159, 514
Active area, 83-99
  design rules, 99
Active-PI loop filter, 573-574
Active load, 657, 872
Active pixel sensor, 504-505
Adaptive biasing, 920-923
ADC, see Analog-to-digital converter
Adder, 367-369, 373, 395, 407-410, 412, 419-421
Aliasing, see Analog-to-digital converter
Amplifier,
  adaptive biasing, 920-923
  biasing, 291-292, 297-302, 613, 621, 624-625, 635-652, 699, 863-866
  body effect 691-692, 709
  cascode, 686-689, 696-697
  class A, 672, 688, 691, 697, 701, 727
  class AB, 672, 697-701, 709-710, 727-728, 800, 802-805, 810, 814, 817, 819-820, 865, 878
  common-gate, 671, 689-690, 708-709, 732, 783
  common-source, 657-658, 666-667, 671-673, 698-699, 717, 751, 756, 773-774, 793, 800, 814, 820-823
  current source load, 657, 665, 671-674, 686, 689-691, 698-699, 704, 719, 731-733, 774, 876
  distortion, 701, 704-706, 710, 737-740, 790, 807, 831
  efficiency, 699-702
  feedback, see Ch. 31
  frequency response, 661-666, 674-685, 687, 696-697, 708, 721
  gain, 279, 291, 657-673, 686-692, 719-720
  input capacitance, 693, 1141
  noise, 219-262, 669-670, 686, 688, 694
  noise figure, 233-240
  overshoot, 811, 895, 936
  phase response, 662-665, 675-688
  pole splitting, 676-685
  push-pull, 698-703
  slew rate, 672-673
  source follower, 670, 690-698
Amplifier (continued),
  transimpedance, 666-667
Analog-to-digital converter (ADC), 931, 947-957, 985-1015
  0.5 LSB, 943
  1.5 bits/stage, 1068-1075
  aliasing, 953-955, 1008
  aperture error, 956-957
  architectures, 985-1016
  binary search, 1003-1005
  calibrating, 1079
  charge redistribution, 1005-1007
  comparator placement, 1061, 1070, 1082
  coarse conversion, 991
  cyclic, 1059-1066
  DFT, see discrete Fourier transform
  differences of oversampling and Nyquist rate converters, 1008-1009
  differential nonlinearity (DNL), 950-951, 989-990, 998, 1007
  digital error correction, 1068
  discrete Fourier transform (DFT), 218, 956
  fine conversion, 991
  flash, 985-990
  flash accuracy issues, 988-990
  folding frequency, 955
  gain error, 953, 992-994
  higher-order sigma-delta modulation, 1014
  implementing, 1052-1095
  integral nonlinearity (INL), 951-952, 989, 997-998, 1007
  least significant bit (LSB), 940
  missing codes, 951
  noise shaping, 1011-1012
  Nyquist rate, 1007
  offset, 953, 989-990, 996-998, 1007
  operational amplifier issues, 992-994
  oversampling, 1007-1015
  parallel, feed-forward, 990
  pipeline, 994-998, 1067
  pipeline accuracy issues, 996-998
  pulse-density modulation, 1009
  quantization error, 948-949
  quantization levels, 947-949
  quantization noise, 956
  residue, 994
  resolution versus oversampling, 1014-1015
  sampling function, 954-955
  SAR, 1003-1005
  scale factor error, 953
  sigma-delta modulation, 1009
  signal-to-noise ratio (SNR), 956
  specifications, 947
  successive approximation, 1003-1007
  successive approximation accuracy issues, 1007
  successive approximation register, see SAR, 1003-1005
  transfer curve, 948-953, 987, 994

Analog-to-digital converter (ADC) (continued),
two-step, 990-992
two-step accuracy issues, 992
Analog models, 269-310
body effect transconductance, 287-288
transconductances, 279-280, 288
Analog signal characteristics of, 932
Anisotropic etch, 171
Anode, 43, 757, 760
AOI logic, 364-369
Aperture error, see sample-and- hold
Arbiter, 383
Astronomy, 246
Autozeroing, 1006, 1051, 1053
Avalanche breakdown, 143, 154, 253-254
Averaging noise,
flicker, 246
thermal (white), 240-241
Averaging circuit, 539-540, 873-874, 1078-1079

B

β (transconductance parameter), 142
Back end of the line (BEOL), 90, 177-178, 199-208
Backend processes, 208-211
Bandgap energy of silicon, 759
Bandgap voltage references (BGR), 745, 761-770
Battery, 695, 730
BCD, see binary coded decimal
BEOL, see back end of the line
Beta-multiplier reference (BMR), 624-630, 647, 650, 750-754
compensation, 630
Biasing,
general long channel analog design, 291-293
general short channel design, 297-300
high-speed design, 299-302, 863-866
long-channel circuit, 647
push-pull amplifier, 699
short-channel circuit, 650
Binary coded decimal, 965
Bi-phase, 584-585
Bipolar junction transistor (BJT), 47, 150
lateral, 758
parasitic, 2, 37, 56, 341-342, 757-758
temperature behavior, 758-759
vertical, 757
Bird's beak, 181
BJT, see bipolar junction transistor
Bloats, 35
BMR, see beta-multiplier reference
Body effect, 139, 148-149, 276-277, 691-692, 709
gamma, γ, 139, 276
Body transconductance, 287-288
Bonding pad, 4, 59
layout, 59-62, 100-102
Bootstrapped inverter, 546-547
Bottom plate capacitance, 115, 839-840
Bottom plate sampling, 839-842, 1052
Breakdown,
diode model in SPICE, 58
oxide, 154
voltage, 58, 143
BSIM4, 154-157
Buffers,
class AB output, 672, 697-701, 709-710, 727-728, 800, 802-805, 810, 814, 817, 819-820, 865, 878-891, 900-901
digital, 344-348
fully differential input, 920
input, 534-542
NMOS only, 350, 546-547
op-amp, 793-810, 865, 878-891, 900-901
source follower, 696-698
Bulk CMOS process, 31, 180
Buried channel, 304
Bus, 68, 100-103, 321, 351, 412-419, 427, 527

C

C'_{ox}, 114-115, 123-124, 132-135
Calibration, 1023-1024, 1035-1038, 1049-1050, 1061, 1079
Calma stream format, see GDS, 36
Caltech intermediate format, see CIF, 36
Capacitance, 44, 135
bottom plate capacitance, 115, 839-840
bottom and sidewall, 117
depletion, 43-45, 47-49, 58, 94, 100, 117, 122, 133, 147, 244, 315, 342-343, 398, 478, 546, 618, 844
diffusion, 45-47, 117
metal layer parasitics, 61
MOSFETs 116-118, 132-135
sidewall, 44-45, 117
Capacitive feedthrough, 449, 831-832, 1050
Capacitor
common-centroid layout, 980
depletion, 43
poly-poly, 113-115
layout, 113-115, 851-852
parasitics, 61, 115
temp co, 116
voltage coefficient, 116
Capacitor error averaging, 1068, 1075-1083
Carrier lifetime, τ_T, see diode, minority carrier lifetime
Carrier transit time, τ_T, see diode, minority carrier lifetime
Cascode,
amplifier, 686-689, 696-697
current mirror, 636-652
differential amplifier, 733-735, 793-794, 877-891
origin of the name, 636

Cathode, 43, 757
CGBO, 135
CGDO, 123-124, 135
CGSO, 123-124, 135
Channel hot electron (CHE), 468-469
Channel-length modulation (CLM), 143-147, 273, 277, 280-281, 289, 613-617, 639, 856
Charge injection, 830-840, 856, 863, 937, 1050
Charge pumps, 329, 461, 542-546, 558-561, 578-580, 591-593, 600, 603
CHE, see channel hot electron
Chemical/mechanical polishing (CMP), 163, 170, 173, 182, 185, 187, 201-207, 211
Chemical vapor deposition (CVD), 176-177, 179, 182, 184-185, 187, 190, 193, 196, 199, 202-207
Chip, 3, 32, 36
  cross-sectional view, 4, 32
  design, 1
  IC design flowchart, 2
  packaging, 4, 211
  layout view, 4, 32
  organization, 447
CIF (Caltech Intermediate Format), 36, 53
Class AB, 672, 697-701, 709-710, 727-728, 800, 802-805, 810, 814, 817, 819-820, 865, 878
CLM, see Channel length modulation
Clock feedthrough, 449, 456, 830, 832-834, 838-840, 860, 863, 937
Clock generation, 577, 1082-1084
  nonoverlapping, 401-402, 843, 850, 853-856, 874, 896, 1084
Clock recovery circuit, 551-552, 584, 588-589, 591, 602-607, 608, 611
  self-correcting, 588-594
Clock synchronization, 383, 551, 591, 596
Clocked logic, 397, 403-408
CMOS, 1
  active pixel sensor, 504-505
  IC design process, 1-2
  passive elements, 105-106
  process flow, 91
  process integration, 161
  scaling, 54, 152
  trends, 152
  twin-tub, 31
  unit processes, 161
CMOS fabrication, 161-212
  APCVD, 176
  back end of the line (BEOL), 90, 177-178, 199-208
  backend processes, 208-211
  BEOL, see back end of the line
  boule, 163
  burn-in, 208, 211
  chemical/mechanical polishing (CMP), 163, 170, 173, 182, 185, 187, 201-207, 211
  chemical vapor deposition (CVD), 176-179, 182, 184-187, 190, 193, 196, 199, 201-207
CMOS fabrication (continued),
  critical dimension (CD), 179
  contact module, 202-203
  contaminates, 171, 208
  Czochralski (CZ) growth, 162-163
  degree of anisotropy, 170-171
  deposition, 90, 161, 173-177, 179, 191-192, 196, 200-208, 210-211
  depth of focus (DOF), 168-169, 201, 205
  die seperation, 3, 211
  diffraction effects, 168-169
  diffusion, 117, 163, 165-167, 211
  doping processes, 52-53, 161, 165-167
  dry etching, 170-171, 208
  electrical coupling, 202, 205
  electronic grade silicon (EGS), 162
  electromigration problems, 203
  etching, 33, 90-91, 93, 170-172, 175-176, 183, 190, 192, 200, 202, 208, 211, 444
  etch rate, 170-171
  etch profile, 171
  EGS, see electronic grade silicon
  epitaxial wafers, 31-32, 180
  FEOL, see front end of the line
  field oxide (FOX), 38, 83-84, 86-87, 90-91, 116-117, 181
  front end of the line (FEOL), 90, 177-178, 180-199
  final test, 208, 211
  gate oxides, 163, 191-192
  IMD, see intra-metal (layer) dielectric
  intra-metal dielectric (IMD), 69, 178, 205-208
  ion implantation, 140, 165-167, 170, 184, 211
  ion implanter, 165
  implant profile, 165-166
  isolation, 90-91, 173, 177, 181-183, 205
  lattice damage, 165, 184
  LOCOS, 181
  mask alignment, 84, 86, 94, 170
  masks, 34-35, 53, 69, 84, 86, 163, 167-168, 170, 173, 179
  metallization, 178, 203-205
  metallurgical grade silicon (MGS), 162
  MGS, see metallurgical grade silicon
  n-wall, 184-186
  n-well, 179, 181, 184, 187-190
  numerical aperture, 168
  p-wall, 184-186
  p-well, 179, 181, 184, 187-191
  packaging, 3-5, 59, 208, 211
  passivation, 62, 173, 178-179, 208-210
  pattern transfer, 168
  PECVD, 176-177
  PECVD reactor, 177
  photolithography, 161, 167-171, 173, 182-193, 196, 202-203, 206, 208-211
  physical vapor deposition (PVD), 175-176, 200, 204, 208

CMOS fabrication (continued),
plasma etching, 173-177
polysilicon, 166, 178-179, 191-194
pre-metal dielectric (PMD), 178, 200-204
process description, 89-91, 178-179
process integration, 177-208
rapid thermal annealing, 199-201
rapid thermal processing (RTP), 164
reactive ion etching (RIE), 171-173
registration errors, 170
resolution, 168-169, 171
reticle, see mask
salicide module, 199
scribe lines, 209, 211
selectivity, 170
shallow trench isolation (STI), 90-91, 177-178, 181-188
silica, 161-162
silicide, 83, 88-92, 94, 199-201
SOI wafers, 180
source drain module, 193-199
starting material, 180-181
step coverage, 174
stepper, 34, 167-168
straggle, 165
streets, see scribe, 209, 211
technology computer assisted design (TCAD), 179
thermal oxidation, 34, 161, 163-164, 182, 184, 190, 192, 211
thin film deposition, 173-177
thin film removal, 161, 170-171
trench liner, 184
twin tub (well) module, 187-190
unit processes, 161-177
via 1 module, 205-207
wafer manufacture, 161-163
wafer probe, 208-211
wet etching, 170-171
yield, 152, 209-211
CMOSedu design rules, 53-55, 69
CMFB, see common-mode feedback
CMRR, see common-mode rejection ratio
Common-centroid, 111-113, 618, 724, 851, 916, 980
Common drain amplifier, see source follower
Common gate amplifier, 671, 689-690, 708, 732, 783
Common-mode feedback (CMFB), 836-837, 863, 869-875, 881-885, 888-904, 906-908, 1057-1058
compensating, 871-873
dynamic, 1089-1091
settling time, 895
switched-capacitor, 874-875, 896-904, 907-908, 1089-1091
Common-mode rejection ratio (CMRR), 721-724, 742, 773, 789-790, 823, 825, 833
Common-mode voltage (V_{CM}), 837
Common source amplifier, 657-658, 666-667, 671-673, 698-699, 717, 751, 756, 773-774, 793, 800, 814, 820-823
Communication system, 582-583
Comparators, 909-930
block diagram, 910
characterizing, 915-918
clamped input stage, 917
clocked, 918-919
dc performance, 915-916
decision circuit, 910-914
dynamic, 854-856
gain and offset, 916, 1061-1062, 1068, 1075
hysteresis, 912-914
input slew rate, 918
inverter based, 854-856
kickback noise, 448-449, 456, 910, 918, 930
operation, 909
output buffer, 913-915
placement, 1061, 1082-1084
pre-amp, 910-913
propagation delay, 918
self-biased, 920
sensitivity, 909-910, 930
transient response, 916
Compensation, 773-792, 794, 814-815, 819-820, 892, 895
beta-multiplier reference, 630
common mode feedback (CMFB), 871-873
constant-g_m, 738-740
high-speed, 783-787
indirect, 783-787, 825
gain enhancement, 809-812
lead, 782
Miller, 774, 788
nested Miller, 820
pole splitting, 674-679, 685, 780, 783, 814, 821
slew-rate limitations, 787-789
Conductivity, 39-41
silicon-dioxide, 468
Constant-g_m,
bias circuit, 625
diff-amp, 738-740
Contact resistance, 47, 64, 70-71, 80, 147, 209, 962
Contact potentials, 42-43, 124, 137-138
Convergence help in SPICE, 28, 401
Complementary to absolute temperature (CTAT), 745, 759, 761-762, 765, 768
Counter, 329, 485-486, 506, 998-1002
as a digital filter, 506-507
Counter-doped, 52-53
Coupled noise, 1092-1093
rejection, 838
Critical dimension (CD), 179
Cross-sectional view, 3-5
Crosstalk, 59, 71-72, 427

CTAT, see complementary to absolute temperature
Current differential amplifier, 737, 921-922
Current mirrors, 273-274, 510, 512, 563, 613-656
  biasing, 621-626, 647, 650, 863-866
  cascode, 273-274, 636-646
  design, 615
  dynamic, 856-858
  floating, 647, 651-652, 698-699, 703-704, 710, 804-805, 808, 820, 865
  layout, 616-620, 642
  low-voltage, wide-swing, 639-651
  matching, 616-620
  output resistance, 288, 298, 613, 622, 636-644
  regulated drain, 645-646
  SPICE statement, 620
  subthreshold operation, 635
  supply independant biasing, 624
  temperature coefficient, 632
  V_{THN} mismatch, 616
  KP mismatch, 616-617
  wide swing, 639-651
Current mirror load, 715-717, 731
Current-mode DAC, 1018, 1024-1030, 1042
Current steering DAC, 1042-1044
Current starved VCO, 329, 561-565, 571, 574
CVSL logic, 369-370
Cyclic ADC, 1058-1066
Czochralski (CZ) growth, 162-163

D

DAC, see Digital-to-analog converter
Damascene process, 90, 207
Data conversion
  signal characteristics, 931-935
DC analysis in SPICE, 13-15
DC sweep convergence in SPICE, 29
Decades, 20
Decoder, 329, 430, 433, 447, 449, 457-462, 480, 966, 985-987
Decoupling capacitor, 73-74, 81, 417, 419
Decibels, 20
Delay time, 49-52, 65, 89, 317-318, 348, 358-359, 362, 526-527, 531-533
  NAND gate, 392
  phase shift, 665
  TG, 376
  word line, 443
Delay elements, 408, 595-596
Delay locked loop (DLL), 592-602
Delay & transition times 317-320
Delta-sigma modulation, see Sensing using delta-sigma modulation (DSM), see also Sigma-delta modulation
Depletion capacitance, 43-45, 47-49, 58, 94, 100, 117, 122, 133, 147, 244, 315, 342-343, 398, 478, 618, 844
Depletion device, 140
Depletion region, 43
Depth of focus (DOF), 168-169, 201, 205
Design rules, 53-54, 69, 75, 98-99
  active and poly, 98-99
  CMOSedu, 53-55, 69
  n-well, 36-37, 53-54
  metal layers, 69
DFT, see discrete Fourier transform
DIBL, see drain induced barrier lowering
Dickson's charge pump, 544
Dielectric constants, 114
Die, 3-4, 32, 59-60, 62, 68, 75, 110, 116, 209, 211, 411-412, 427, 429, 443, 746, 958, 960, 998
Die seperation, 3, 211
Differential amplifier, 711-744
  ac operation, 718-721
  adaptive biasing, 920-922
  body effect, 730, 742
  cascode, 733-735
  class AB, 727-733
  common-centroid layout, 724
  common mode range (CMR), 713-716, 732-733, 735
  common mode rejection ratio (CMRR), 721-723
  constant transconductance, 738-740
  current, 737, 921-922
  current mirror load, 715-717, 731-733
  dc operation, 711
  gain, 719, 722, 733, 736
  low voltage, 736
  matching, 724-726
  minimum power supply voltage, 717
  noise, 726-727
  output resistance, 719, 733-734
  self-biased, 534-538, 920
  slew rate, 727
  source cross coupled pair, 727-733
  wide swing, 736-740, 918-919
Differential nonlinearity (DNL), 941-943, 950-951, 963, 967-971, 976-980, 989-990, 998, 1007, 1029-1034, 1040-1041
  improving using segmentation, 1032-1034, 1043
Differential output op-amp, 836-842, 863-908
  benefits, 838
  simulating, 841, 878-904, 927
Diffusion,
  capacitance, 45-47, 117
  process, 117, 163, 165-167, 211
Digital error correction, 1068 , *see also* Analog-to-digital converter (ADC), 1.5 bits/stage
Digital-to-analog converter (DAC), 931, 938-947, 965-985
  0.5 LSB, 943
  accuracy, 941
  binary switch array, 966-967
  binary weighted, 971, 974-975, 977-980
  calibration, 1035-1038
  charge scaling, 978-982, 1005-1007

Digital-to-analog converter (DAC) (continued),
current source mismatch, 976-977
current steering, 973-975, 1042-1044
cyclic, 982-983, 1019
decoder, 966
differential nonlinearity (DNL), 941-943, 963, 967-971, 976-980
dynamic range, 947, 963
full scale voltage, 939, 941, 963
gain error, 945-946, 953, 1019
input combinations, 938
integral nonlinearity (INL), 943-945, 967-971, 976-977, 979, 980
ladder, 967, 971
latency, 945
least significant bit (LSB), 940-941
LSB, see least significant bit
monotonicity, 943
most significant bit (MSB), 940
MSB, see most significant bit
nonmonotonic, 943
offset, 943-946
op-amp issues, 992-994
pipeline, 984-985, 1098
R-2*R*, 971-973, 1024-1035, 1038-1040
reference voltage, 938-941, 956
resistor string, 966-971
resistor string mismatch, 967-970
resolution, 933-934, 937-938, 940-943, 946-947
settling time, 945
segmentation, 1032-1034
signal-to-noise ratio (SNR), 945-946, 956
specifications, 938-947
split-array, 980-981, 1019
transfer curve, 940
W-2*W*, 1043-1044
wide-swing, 1026-1032
without an op-amp, 1038-1044
Digital models, 311-319
Digital phase-locked loop (DPLL), 551-612
active-PI loop filter, 573-574, 581, 588, 591
block diagram, 552
charge pump, 558-561, 578-580, 591-593, 600, 603
dead zone, 577, 600, 609
delay elements, 595-596
examples, 596-607
jitter, 557, 564, 571, 579, 582, 591-592, 594, 597, 600
lock range, 567, 569-570, 573-574, 576-577, 579-580, 592
loop filter, 552, 554-557, 559-561, 567-582
PFD, 552-553, 557-561, 575-580, 591, 600-603, 608
pull-in range, 567-569, 571, 574, 576-577, 579, 592
static phase error, 572-573, 577, 579, 600, 604, 610
Digital phase-locked loop (DPLL) (continued),
system concerns, 582
tristate output, 559-560, 575-579, 581
XOR DPLL, 568-574
XOR Phase Detector, 552-557, 559, 561
Diode,
anode, 43, 757, 760
breakdown voltage, 58, 253
carrier transit time, τ_T, see minority carrier lifetime
cathode, 43, 757
depletion capacitance, 43-45, 117
diffusion capacitance, 45-46, 117
drain or source to substrate, 117, 143, 398, 403, 543, 618
electrostatic discharge, 100-102
ESD, see diode, electrostatic discharge
long base, 45
minority carrier lifetime, τ_T, 45-48, 242-243
n-well/p-substrate, 31-32, 39-45, 53, 57-58, 94, 96, 543
noise, 242-244, 249, 252-253
parasitic BJT, 757-759
photodiode, 249, 504
reverse recovery time, 46-49
saturation (scale) current, I_S, 39, 47, 181, 398
Schottky, 92, 760
short base, 45
SPICE modeling, 14-15, 47-49
storage capacitance, see diffusion capacitance
storage time, 46-49
temperature behavior, 759
t_{rr}, see reverse recovery time
t_s, see storage time
τ_T, see minority carrier lifetime
Zener, 253-254
Discrete Fourier transform (DFT), 218, 956
Distortion,
amplifier, 701, 704-706, 710, 737-740, 807, 993-994
common-mode level variation, 740, 790, 807
multiplier, 923
pulse width, 531
signal-to-noise plus distortion ratio (SNDR), 956
SPICE modeling, 705-706
switches, 831
total harmonic distortion (THD), 704-706, 923
Distortionless transmission, 582
DLL, see Delay-locked loop
DNL, see Differential nonlinearity
Dominant pole, 680
Domino logic, 405-407, 409
Doping processes, 52-53, 161, 165-167
Doublet, 810
DPLL, see Digital phase-locked loop
Drain induced barrier lowering (DIBL), 154
DRAM, see memory, DRAM

Drawn length, 87, 116-117, 132, 144
Drawn width, 68, 87, 116-117, 132, 315
DRC (design rule check), 36
Drive current, see on current
Drivers, 344, 449, 459-463, 481, 546
  distributed, 347-348
DSL logic, 370-372
DSM, see Sensing using delta-sigma modulation (DSM)
Dummy elements, 113, 618, 851
Dynamic circuits, 829-862
  amplifiers, 858
  capacitive feedthrough, 67, 830-832
  charge injection, 830, 856, 830-833
  clock feedthrough, see capacitive feedthrough
  comparator, 854-856
  current mirrors, 856-858
  dummy switch, 832
  IOS, 856-857
  kT/*C* noise, 833-834, 856
  logic, 397-410
  OOS, 856-857
  op-amp settling time, 852-853
  reducing charge injection & clock feed-through, 832
  reducing op-amp offset-voltage, 853-854
  sample-and-hold, 838-840
  simulating, 401
  storage capacitors, 852-853, 856
  switch, 829-834
  switched capacitor integrator, 845-850
  switched capacitor resistor, 843-845
Dynamic logic, 397-410
  charge leakage, 399-400
  clocked CMOS, 403-408
  domino logic, 405-406
  PE logic, 405
  NP logic, 407
  shift register, 402
  simulating, 401
  zipper logic, 407
Dynamic power dissipation, 339-340
Dynamic range, 490, 506, 833, 839, 947, 963, 1009, 1014

E

Edge detector, 374, 587
Effective channel length, 132
Effective switching resistance, 312-315, 317, 320, 335, 344, 390, 392
Electrode layer, 115
Electrical length, 144
Electromigration, 59, 68, 70
Electrostatic discharge (ESD),
  diode, 59, 100-103, 530-531, 549
Energy,
  bands in silicon, 39-43
Energy (continued),
  electrical, 213-215, 217
  implant, 166
  thermal, 225-226, 236
Energy spectral density (ESD), 217
Enhancement device, 140
Epi layer, 31
Epitaxial wafers, 31-32, 180
ESD, see electrostatic discharge, see also energy spectral density
Etching, 33, 90-91, 93, 170-172, 175-176, 183, 190, 192, 200, 202, 208, 211, 444
Equalizer, 539, 582-583, 610
Excess gate voltage, see overdrive voltage, 271
Excess phase shift, 665

F

Fall time, 317-318
Feature size, *F*, 444
Feedback, 1099
  amplifier, 1106
  beta network, 1107
  bandwidth extension, 1101-1103
  closed-loop impedances, 1112
  closed-loop parameters, 1112
  determining signal path, 1107
  equivalent transconductance, 1121-1123
  factor β, 776, 1100
  forward path, 1107
  gain desensitivity, 1101
  gain margin, 781, 1138
  input/output impedance control, 1104
  input mixing, 1106
  inversions around the loop, 1107-1108
  open-loop impedances, 1110
  open-loop parameters, 1110
  output sampling, 1106
  phase margin, 781, 1138
  properties, 1104-1105
  recognizing topologies, 1105
  reduction in nonlinear distortion, 1103
  rules for output sampling, 1107
  series-series, 1109-1110, 1128-1132,
  series-shunt, 1141-1143
  series mixing, 1105
  series sampling, 1105
  shunt-series, 1108-1109, 1132-1135
  shunt-shunt, 1109-1110, 1119-1128, 1145
  shunt mixing, 1105
  shunt sampling, 1105
  stability, 777
  using a gate-drain resistor, 1125-1128
FEOL (front end of the line), 90, 177-178, 180-199
Fermi energy level, 42-43
Field device, 38, 181, 184-185
Field implant, 38-39
Field oxide, see FOX (field oxide)

Flash memory, 113, 463, 469-476, 481-482, 487-489
Flatband voltage, 139
Flicker noise, see noise
Flip-flops, 380-389
  data (D), 386-388
  hold time, 388-389
  metastability, 383-385, 396
  setup time, 388-389
Floating current source, 647, 651-652, 698-699, 703-704, 710, 804-805, 808, 820, 865
Floating gate, 113, 466
Floor plan, 412, 958
FNT, see Fowler-Nordheim tunneling
Folded-cascode, 641, 648-649, 714-715, 802-810, 827-828, 872
Fowler-Nordheim tunneling (FNT), 469-474, 487
FOX (field oxide), 38-39, 83-87, 181
FPGA (field programmable gate arrays), 1, 412
Frequency response,
  amplifier, 661-666, 674-688, 696-697
  doublet, 810
  noise, 220-223
  op-amp, 680, 792-793
  pole splitting, 674-679, 685, 780, 783, 814, 821
  transmission channel, 538-541
Frequency synthesis, 577, 591
f_T, unity current gain frequency, 290-292, 297-302, 309, 316, 863, 903, 906
Fully-differential circuits, 833, 836-842, 863-930
  benefits, 833, 838
  bottom plate sampling, 839-842
  common-mode feedback, 836-837, 863, 869-875, 881-885, 888-895, 896-904, 906-908
  delay elements, 595-602
  gain, 836
  noise rejection, 838
  sample and hold, 838-842, 880-881, 901-904
  SPICE model, 841-842
f_{un}, op-amp unity-gain frequency, 260-261, 680-685, 740, 779-781, 785-786, 792-793, 797-799, 852-853, 993
  gain-enhancment, 808-812
  plot (general), 680

G

Gain-enhancement (GE), 808-812, 889-890
Gain-f_T product (GFT), see MOSFET, GFT (gain-f_T product)
Gain margin, 781
Gamma, γ, 139, 276
Gaussian probability distribution function, 248-249
Gate current, see Tunneling, gate current
GDS, 36, 53, 78
Generation, 40
GFT, see MOSFET, GFT (gain-f_T product)
GIDL, Gate-Induced Drain Leakage, 154
g_m, 279-280
  long-channel equation, 280
  short-channel, 293, 297-299
  subthreshold, 292-293
Glitch area, 1041-1042
GM, see Operational amplifier, gain margin
g_{mb}, 289-290
GMIN, 29, 401
GOX (gate oxide), 86-87, 114
Gradual channel approximation, 140, 151
Graphical design format, see GDS, 36
Gray code, 965-966
Ground bounce, 71-74, 81
Guard rings, 110, 343, 757, 851, 957, 960

H

Harmonic distortion, see Distortion, 704-706, 831, 923, 993-994
Hi-Z, 321-322, 350-351, 370, see also Tri-state outputs
High-speed op-amp, 783-787, 891
High impedance node, 397, 629-630, 673, 696, 721, 796, 819
Hold time, 388-389
Hot-carrier effect, 151
Hysteresis, 523-529, 537-538, 547-548, 910-916, 918

I

I_{drive}, see on current
$I_{D,sat}$, 144-145, 158, 271-272
INL, see Integral nonlinearity
Imaging, 504-505
  noise, 246
  sensing, 504-519, 1145-1148
Impact ionization, 153
Inductance, 72
Incomplete settling, 496, 502-503, 520
Input buffers, 531-542, 920
Input offset storage (IOS), 856-857
Input-referred offset, see Offset voltage
Instanced (or placed), 429
Integral nonlinearity (INL), 943-945, 951-952, 967-971, 976-977, 979-980, 989, 997-998, 1007, 1029-1032, 1034-1038, 1040-1041
Integrator,
  ADC, 998-1002
  delta-sigma, 492, 1010-1014
  noise, 245, 267
  offset, 846
  PLL, 573, 575
  switched capacitor, 845-850, 861, 901, 907-908
Inter layer dielectric (ILD), 69, 81
Interconnect burden, 429
Interdigitated layout, 110-113, 960
Intrinsic,
  carriers, 40-41

Intrinsic (continued),
propagation delay, 65-66, 81
silicon, 40-42, 52-53
Inverter, 331-352
buffer design, 344-347
dynamic power dissipation, 339-340
layout, 341-343, 413, 422-425
noise margins, 333
other configurations, 349-351
power delay product, 340
switching characteristics, 337-338
sizing, 344
transfer characteristics, 332-336
tri-state output, 351
VTC, see transfer characteristics
I_{off}, see off current
I_{on}, see on current
Ion implantation, 165
I_S, see Diode, saturation current
Isotropic etch, 171

J

Jagged plots, 29
Jitter, 557, 564, 571, 579, 582, 591-592, 594, 597, 600, 1000
peaking, 582
J_s, scale current density, 57
Junction capacitance, see depletion capacitance, 43

K

Keeper MOSFET, 406-407, 461
Kickback noise, 448-449, 456, 910, 918, 930, 1061
KP, 142
kT/*C* noise, 229, 240, 244, 250-251, 517, 833-834, 846, 856, 896

L

Lambda, λ,
channel-length modulation (CLM), 144, 147, 289, 298, 617, 620
layout (in the MOSIS rules), 54
wavelength, 168
LASI, see http://CMOSedu.com
Latch, 380-386, 400, 403-404
Latch-up, 2, 46, 180, 341-343, 349-350
Lateral diffusion,
MOSFET source/drain, 116-117, 124, 144, 315, 616, 620
n-well fabrication, 35-36, 56
SPICE, 147
Layout,
active, 83-85
adder, 420-421
binary-weighted capacitor array, 980
bipolar junction transistor, 757-758
bonding pad, 59-60, 62, 75-77
capacitor, 113-116, 419, 851,
capacitor bottom plate, 115, 840
common-centroid, 111-113, 724
corners, 38
design rules, 37, 68, 99
diff-pair, 724
diode, 757-760
DRAM cell, 443-446
drawing order, 4
dummy elements, 113, 618, 851
electrode, 115
flash memory cell, 466-471
guard rings, 110, 343, 757, 851, 957, 960
inverter, 341-343, 413, 422-425
large-width MOSFETs, 121
lateral bipolar, 757-758
long-length MOSFETs, 120
matching (to improve), 617-620, 724
MOSFET, 86-87, 95 (NMOS), 96 (PMOS) 116-124, 617
MUX/DEMUX, 422
n-well, 32, 36-37, 94
NAND and NOR gates, 358, 415
pad, 60, 75, 102
parasitic pnp, 757
power and ground, 417
resistor, 32, 94, 109-113
Schottky diode, 760
serpentine pattern, 57
SR latch, 416-417
SRAM, 463-464
standard-cell, 97-98, 343, 413, 427-431
standard cell frame, 97, 343
stick diagram, 422
TG (transmission gate), 415
unit cell, 109, 851-852
view, 3-5
VLSI, 1, 411
Layout view, 3-5
LDD, see lightly-doped drain
L_{diff}, see lateral diffusion
L_{drawn}, see drawn length
L_{elec}, see electrical length
L_{eff}, see effective channel length
Leakage current, 93, 181, 184, 200, 244, 249, 397-403, 547
Level shifting, 547-548, 692
pumped output voltage driver, 546
Lifetime of a minority carrier, τ_T, see diode, minority carrier lifetime
Lightly-doped drain (LDD), 90-91, 116, 151-152, 179, 193-196
Linear region, see Triode region
LOCOS, 181
Long-channel,
analog models, 269-296

Long-channel (continued),
digital models, 312-316
MOSFETs, xxxi, 132-150
tables, 292, 317, 320
Low impedance node, 673
Low power, 149, 299, 451, 476, 563, 635, 727, 729, 737
Low voltage, 476
current mirror, 637-639
differential amplifiers, 727, 729, 736-740
reference, 760, 768-770
LTspice, see http://CMOSedu.com

M

Manchester NRZ, 584
Masks, 34-35, 53, 69, 84, 86, 163, 167-170, 170, 173, 179, 851
aligning, 84, 86, 94, 170
CMOS fabrication, 182-209
Matching, 8
capacitor, 116, 1075-1081
common-centroid, 111-113, 618, 724, 851, 916, 980
current mirror, 615-618, 636, 642
diff-pair, 724-726
interdigitated layout, 110
layout, 105, 617-620
NMOS vs PMOS, 440-441
resistors, 110-113, 1040-1041
R-2*R* DAC, 1029-1030
threshold voltage, 616, 726, 856, 867
transconductance, 616
Measurements, 246, 267
currents in SPICE, 10, 274-275
noise, 213, 219-224
probe, 326-327
Memory circuits, 433-482
array architectures, 434-447
buried capacitor cell, 446
chip organization, 447
decoders, 457-461
DRAM, 348, 438-446
EEPROM, 469
efficiency, 447
EPROM, 468
erased, 466, 471
F, feature size, 443-445
flash, 113, 463, 469-476, 481-482, 487-489
folded bit line, 441-446
floating gate, 466-474
global decoders, 458
local decoders, 458
memory cells, 463
NAND flash, 471
NSA, 435-439
open array, 436
organization, 457
Memory circuits (continued),
peripheral circuits, 448
PE decoder, 461
PROM, 464-465
programmed, 466, 471
PSA, 440-441
RAM block diagram, 433, 457
refresh operation, 441
ROM, 464
row drivers, 461
sense-amp design, 448-456
sensing basics, 435-441
SRAM, 463-464
trench capacitor cell, 444-445
Metal layers, 59-74
bond pad, 4, 59
capacitive feedthrough, 66
cross-sectional view, 64
delays, 65
design rules, 69
electromigration, 59, 68, 70
inter layer dielectric (ILD), 69
intrinsic propagation delay, 65
parasitics, 61, 64-65
sizing, 68-74
Metallurgical grade silicon (MGS), 162
Metastability, 383-385, 396, 450, 452, 478, 918
Miller,
capacitance, 311-312, 661-662, 664, 674, 684
compensation, 774, 788
effect, 311, 687, 693
eliminating, 686
neglected zero, 662-665
nested, 820
theorem, 660-661, 676
Minority carrier lifetime, τ_T, see diode, minority carrier lifetime
Mixed signal, 706, 842, 957, 960
Mobility, 40, 106, 144, 153
Monotonic, 943, 966, 1041
Moore's law, xxxi
MOSFET, 131
accumulation, 132-134, 136, 159, 514
adjusting threshold voltage, 140
capacitances, 117,123, 135
capacitors, 544
C_{gs} calculation, 145
channel-length modulation, 144
depletion, 133
depletion device, 140
diode-connected, 272, 534, 542, 545, 579, 624, 627, 629, 639, 648, 673, 708, 719, 737, 819-820, 872
dummy poly strips, 618
effective width, 116
enhancement device, 140
excess gate voltage, see overdrive voltage
field device, 38, 181, 184-185

MOSFET (continued),
flatband voltage, 139
flicker noise, 302-303, 833
f_T, unity current gain frequency, 290-292, 297-302, 309, 316, 863, 903, 906
gain-f_T product (GFT), 300-302
gate tunnel current, 154, 242, 403, 474-475
$I_{D,sat}$, 144-145, 271
I_{off}, 150, 294, 398, 408
I_{on}, 150, 152-153, 157-158, 297, 314, 316
IV characteristics, 140, 157
lateral diffusion, 116-117, 124, 144, 315, 616, 620
layout and cross-sectional views, 86-87, 95-96, 118-122
linear region, see MOSFET, triode region
long channel, xxxi, 132-150, 269-296, 312-317, 320
NMOS layout, 95
ohmic region, see MOSFET, triode region
output resistance, 288
overdrive voltage, 271, 297-302, 616, 800, 802, 804, 863-864, 884, 892, 896, 903, 906
overlap capacitances, 132
oxide encroachment, 116-117, 132, 181-182
pad oxide, 182
parallel connection, 358
parasitic resistances, 118
pinch-off, 143
PMOS layout, 96
punch-through, 143
saturation region, 143-145, 271
scaling, 152
series connection, 359
short channel, xxxi, 151-158, 297-302, 314-317, 320
SPICE statement, 119-120
source/drain depletion capacitances, 117
subthreshold slope, 150
symbols, 96-97, 131
temperature effects, 293-295
threshold voltage, 135-140, 293
triode region, 141, 271, 278
$V_{DS,sat}$, 144-145, 271
MOSIS, 3, 53-55
multiproject wafer, 3
web address, 3
Multipliers, 923-929
multiply-by-2, 992, 994, 1060, 1062-1064, 1071, 1080
multiplying quad, 924
simulating, 926-928
squaring circuits, 928-929
Multivibrator circuits, 529-531, 565-567
MUX/DEMUX, 378-381, 422

N

N-well, 31-58
cross-section, 32, 36, 39
design rules, 36, 54
patterning, 35
resistor, 32, 38, 94
n-well substrate diode, 39
N-select (n+ implant), 84-85, 179
NAND gate, 353-356
layout, 358, 414-415
switching characteristics, 358-363
switching point voltage, 354-355
NBTI, Negative Bias Temperature Instability, 153
Negative frequency, 218
Netlists, downloadable at CMOSedu.com
n_i, see Intrinsic, carrier
NMOS, 95-97, see also MOSFET
NMOS clock driver, 546-547
NMOS inverter, 349, 546-547
Noise, 213-268
1/f, see flicker
amplifier, 220-223
analysis, 235
avalanche, 252-254, 268
averaging thermal (white) noise, 240-241
averaging flicker noise, 246
burst (popcorn), 252-253
correlation, 256-258
differential amplifier, 726-727
diode, 242-244, 249, 252-254
equivalent bandwidth, 220-223
estimating RMS value from the time-domain amplitude, 249
excess, 253
feedback, 259-261
figure, 233-240
flicker, 213, 244-253, 261-262, 267, 302-303, 833
gate tunnel current, 220, 242
Gaussian probability distribution function, 248-249
generator, 253-254
imaging chip, 245-246
input-referred, 220-224, 226-240, 247, 249, 251, 256-261
integrator, 245, 267
kT/*C*, 229, 240, 244, 250-251, 517, 833-834, 846, 856, 896
margins, 333
mean squared, 214-215, 262
MOSFET, 302-304
modeling, 219
noiseless resistor model in SPICE, 236-238
op-amp, 247-252, 259-261
phase noise, 592
photodiode, 249-250

Noise (continued),
pink, 244
popcorn, 252
power spectral density, 215-218
random telegraph signal, 252-253
red, 245
resistors, 225-229
RMS, 215, 217, 219-224, 248-249
root mean squared, see RMS
shot, 242-244, 268
signal-to-noise ratio, 230-234, 246, 266-267, 945-946, 956, 964
spectrum analyzer, 216-218
SPICE modeling, 227-228, 237-238, 243-244, 251-252, 302-304
noiseless resistor model, 236-238
standard deviation, 248-249
substrate, 851
temperature, 239-240
thermal, 225
transimpedance amplifier, 249-251
variance, see Noise, mean squared
white, 219-221, 225, 240-242, 253-254
Zener, 253-254
Nonoverlapping clocks, 401-402, 843, 850, 853-856, 874, 896, 1082-1085
NOR gate, 353-357
layout, 358, 414-415
switching characteristics, 358-363
switching point voltage, 356-357
NRD and NRS, 118-120, 813
Nyquist criterion, 934

O

Octave, 20
Off currrent (I_{off}), 150, 294, 398, 408
Offset binary, 965
Offset voltage,
ADC, 953, 1000, 1005-1007, 1014
adding to a sense amp, 498
charge injection, 831, 836, 841
CMRR, 723, 789-790
common-mode voltage, 792
constant-g_m, 740, 792
DAC, 945-946
delta-sigma ADC, 1014
diff-amp, 725-726, 867-868, 875
flash ADC, 988-990
gain error, 936
integrator, 846
modeling in an op-amp, 776, 827, 867-888
modeling with SPICE, 654, 867-868, 870-871
multiplier, 923
op-amp, 775-776, 804, 813, 818, 825, 853-857, 863, 867-868, 870-871, 892-895, 902-903
pipeline, 996-998
random, 775
Offset voltage (continued),
removal, 518-519, 853-857
sensing, 497-500, 502
systematic, 775, 818, 916, 930
Ohmic contact, 83
Ohmic region, see Triode region
On current (I_{on}), 150, 152-153, 157-158, 297, 314, 316
One shot, 529
Open circuit gain, 298, 300-302, 668, 673, 678, 876
Operating point analysis in SPICE, 282-283
Operational amplifiers, 773-828, 863-908
biasing, 865-866, 876
CMFB, see common mode feedback
CMRR, see common mode rejection ratio
common-mode output voltage, 838
common mode feedback (CMFB), 836-837, 863, 869-875, 881-885, 888-895, 896-904, 906-908
common mode rejection ratio (CMRR), 721-724, 742, 773, 789-790, 823, 825, 833
folded-cascode, 641, 648-649, 714-715, 802-810, 827-828, 872
fully-differential, 836-842, 863-904
f_{un}, op-amp unity-gain frequency, 260-261, 680-685, 740, 779-781, 785-786, 792-793, 797-799, 808-812, 852-853, 993
gain-enhancement, 808-812, 889-890
gain margin (GM), 781
high-speed design, 783-785, 806-812, 863
input common-mode range (CMR), 476, 730, 732, 741, 743, 774, 787, 701-702, 802, 807, 870, 872, 889
layout of differential op-amps, 865
offset-voltage, 775, 853, 867, 893
open-loop response, 780, 781, 795, 799, 801,804, 805, 806, 811, 812, 822, 823
OTA with buffer, 800-808
output voltage swing, 775, 880, 884, 886, 891
phase margin (PM), 781
power amplifier, 807-808
power dissipation, 775
PSRR, 790-791, 838
offsets, 775, 892
RHP zero, 662, 782
settling time, 852, 895, see also Settling time
simulation results, 886, 902
single-ended to differential, 894
slew-rate limitations, 787, 800
SPICE (ideal) model, 628, 841
start-up problems, 887
switched capacitor CMFB, 874-875, 896-897
voltage regulator, 812-817
Operational transconductance amplifier (OTA), 796-808
Optical Proximity Correction (OPC), 79

Oscillator,
astable, 530-531
ring, 339-341, 547
Schmitt trigger, 527-529
Voltage controlled, 561-567
OTA, see operation transconductance amplifier
Output buffer, see Buffers
Output Offset Storage (OOS), 856-857
Overdrive voltage, 271, 297-302, 616, 800, 802, 804, 863-864, 884, 892, 896, 903, 906
Overglass layer, 62-63, 75-77, 80, 83
Overlap capacitance, 123-124, 132
Oxide,
breakdown, 154
capacitance, 114-115, 132
encroachment, 116-117, 132, 181-182
growth, 34, 163-164

P

P-select (p+ implant), 84-85, 179
P-wall, 184-186
P-well, 31, 52-54, 179, 181, 184, 187-191, 469-474
Packaging, 3-5, 59, 208, 211
Pad layer, 62
Parasitics, 1-2
Pass gate (PG), 321-326, 357
Pass transistor, see Pass gate (PG)
Passivation, 62, 178-179, 208-210
Path selector, 378
Patterning, 32-35
PCE, see power conversion efficiency
PE logic, 404-405
Peak detector, 539-540
PECVD (plasma enhanced CVD), 176-177
PG, see Pass gate (PG)
Phase-locked loops, see Digital phase-locked loop (DPLL)
Phase margin, 781
Phase shift, 665
Photodiode, 249, 1145
Photolithography, 161, 167-171, 173, 182-193, 196, 202-203, 206, 208-211
Pinch-off, 143
Pipelining, 407
Pitch, 443
Plasma etching, 173-177
PLL, see Digital phase-locked loops
PM, see Operational amplifier, phase margin
PMD, see pre-metal dielectric
PMOS, 96-97, see also MOSFET
PN junction physics, 39-43
PNP, lateral, 757
model, 758
Pole splitting, 674-679, 685, 780, 783, 814, 821
Poly (polysilicon), 83, 166, 178-179, 191-194
design rules, 99
poly2, 113-115
Polycide, 88
Power and ground, 72-74, 417
Power conversion efficiency (PCE), 699-702
Power delay product (PDP), 340
Power dissipation,
inverter, 339-340
Pre-metal dielectric (PMD), 178, 200-204
Probe, 326-327
Process characteristic time constant, 316
Process description, 89-91, 178-179
Process flow, 89-91, 161
Process integration, 177-208
Process, voltage, and temperature (PVT), 299, 531, 745, 867
Proportional to absolute temperature (PTAT), 745, 762
PSRR, 790-791, 838
PTAT, see proportional to absolute temperature
Pulse density modulation, 1008
Pulse statement, 21
Pumps, 542-550
driver, 546
Punch-through, 143
Push-pull amplifier, 698-704
PVT, see process, voltage, and temperature

R

Rail, 698
Random offsets, 775
RC circuit, 17-20, 50
distributed, 49-52, 65, 89, 348
Reactive ion etching (RIE), 171-173
Recombination, 40, 252
References, 745-772
bandgap, 757-772
CTAT, 745, 761-762
diode based, 757-772
low voltage, 760, 770
PTAT, 745, 762-765
thermal voltage, 762-764
Registration errors, 170
Regularity, 412
Regulated drain CM, 645
RELTOL, 28
Resistance, 37
calculation, 37
looking into the drain, 668
looking into the source, 669
resistivity, 37
sheet, 37
Resistor,
common-centroid layout, 111-113
delay through, 49-52
dummy elements, 113
guard rings, 110
interdigitated layout, 110
layout, 38, 56-57, 109-113

Resistor (continued),
layout of corners, 38
n-well, 32, 38-39, 94
properties, 88
sheet resistance, 37
switched-capacitor, 843
temp co, 88, 106, 116, 631,
unit elements, 109
Reticle, see mask
Return Ratio, 1139-1141
Reverse recovery time, 46-49
RHP zero, 662, 685
Ring oscillator, 339, 547
Ringing, 695
Rise time, 50, 317-320
Routing, 430
ROX (recessed oxide), see FOX (field oxide)
RSHUNT, 29, 401

S

Saturation current, see Diode, saturation (scale) current, I_S
Salicide, 199-200
Saturation region, 143-145, 271
S/H, see Sample-and-hold
Sample-and-hold, 834-836, 838-842, 880-881, 901-904, 935-938, 1052-1058
acquisition time, 936
aperture error, 937
aperture jitter, 937
aperture uncertainty, 937
droop, 937
gain error, 936
hold mode, 937
linearity, 936
offset, 936
overshoot, 936
sampling error, 937
settling time, 936
single-to-differential, 1054-1058
Scale current, see Diode, saturation (scale) current, I_S
Scale factor, 36-37, 44, 53-56, 60-62, 75, 89, 114, 117, 119-120, 132, 134, 146-147, 154, 157-158
Scaling theory, 152
Scanning Electron Microscope (SEM), 55, 79, 124
Scattering, 52, 106
Schmitt Trigger, 523-529
applications, 527-529
Schottky diode, 92, 760, 772
Scope probe, 326-327
Scribe, 75, 209, 211
Select, 84-85, 179
Self-aligned gate, 86-88
Self-biased diff-amp, 534-538, 914, 920
Self-biasing, 624-626, 750-770
start-up circuit, 625, 629, 752-754
Self-correcting phase detector, 588-590
Sense amplifier design, 448-456
clock feedthrough, 449
contention current, 450
creating an imbalance, 451-455
kickback noise, 449-451, 456
increasing input range, 454, 918-919
removing sense-amp memory, 451
reducing power, 453
simulation examples, 454
Sensing using delta-sigma modulation (DSM), 483-519
dynamic range, 490
examples, 484-486
feedback signal, 492-496
Flash memory, 487-496
incomplete settling, 496
imagers, 504-519
low pass filter, 507
mismatches, 517-519
noise issues, 506-507, 517
offset, 497, 517-519
parasitic capacitance, 492
pixel, 504
precision of sense, 485
programmed state, 487
resistive memory, 497-504
sampling, 505
sensing circuit, 488, 499, 511
sigma-delta modulation, 484
voltage to current conversion, 508-510
Sensitivity analysis, 623, 626
Series connection of MOSFETs, 322
delay, 325-326
Series-shunt feedback, 1045, 1113, 1141-1145
Series-series feedback, 1128
Settling time, 663, 782, 788-789, 800, 802, 804, 810, 819, 840, 852-853, 880, 892, 895, 901-904, 936, 945, 990, 993, 1000
incomplete, 496, 502-503, 520
Setup time, 388-389
Shallow trench isolation (STI), 90-91, 177-178, 180-188
Sheet resistance, 37
Shielding, 961
Shift register, 402
Shotgun shell, 242
Short-channel,
analog models, 297-302
digital models, 314-316
effects, 153-154
MOSFETs, xxxi, 151-158
tables, 300, 317, 320
Short circuit protection, 826-827
Shot noise, 242-244
Shunt-series feedback, 1132
Shunt-shunt feedback, 1046-1047, 1119, 1145-1148

Sigma-delta modulation, 1007-1015, see also
Sensing using delta-sigma modulation
first-order, 1010-1014
higher order, 1014
noise shaping, 1014-1015
resolution verses oversampling, 1015
Signal to noise ratio (SNR), 230-234, 246, 266-267, 945-946, 956, 964
Signal to noise and distortion ratio (SNDR), 956
Silicide, 83, 88-92, 94, 199-201
Silicide block, 89
Silicon bandgap energy, 759
Silicon on insulator (SOI), 180
SIN SPICE source, 16-17, 282-287
Single-ended to differential conversion, 894
Single-ended to differential converter,
Skew, 531-537
Slew rate, 727, 787, 800, 853, 918, 922
Small-signal,
AC analysis, 280
models, 279-288
signal parameters, 280, 287-289
SNDR, see signal to noise and distortion ratio
SNR, see signal to noise ratio
SOI, see silicon on insulator
Source-coupled multivibrators, 565
Source-coupled pair, see differential amplifier
Source-coupled VCO, 565
Source degeneration, 667
Source follower, 670, 690-698
body-effect, 691
input capacitance, 693, 1141
output stage, 696-698
Space-charge region, see depletion region
Spectral density of noise, 216-217
Spectrum Analyzer, 216
SPICE, 1, 8-29, 67, 78, 145
ABSTOL, 28
AC analysis, 19-20, 285
bipolar junction transistor, 15
breakdown, 58
common mistakes, 29
convergence, 28, 401
DC analysis, 13-15
diode breakdown voltage, 58
diode model, 14, 47-49, 758
distortion, 705-706
generating netlist, 8
GMIN, 29, 401
initial conditions, 24-25, see also UIC
integrator, 26-28
jagged plots, 29
level, 145
measuring currents, 274-275
mistakes, 29
models, parameters for long channel CMOS process, 145-147
SPICE (continued),
models, parameters for short channel CMOS process, 154, 158
MOSFET models, 302-304
noise analysis, 227-228, 237-238, 243-244, 251-252, 302-304
noiseless resistor model, 236-238
op-amp, 12, 841
opening a netlist, 8
operating point analysis, 9-10, 282-283
piece-wise linear (PWL) source, 23
problems, 29
pulse statement, 21
Q of an LC circuit, 25-26
RELTOL, 28
RSHUNT, 29, 401
Schottky diode, 772
simulating dynamic circuits, 401
SIN source, 16-17, 282-287
subcircuit (subckt), 13
switches, 24
.tran statement, 15, 286, 665-666, 705-706
transient analysis, 15-19, 21-25, 27-28, 286
transfer function analysis, 10-11
UIC, 24-25, 29
Voltage-Controlled Voltage Source (VCVS), 11-12, 628, 841
Voltage-Controlled Current Source (VCCS), 12
VNTOL, 27
Squaring circuits, 928
Square-law equations, 142-144, 271-272
Stability, 776-777
Standard-cell, 97
Standard deviation, 248-249
Start-up circuit, 625, 629, 752-754
Static logic, 353
Stepper, 34, 167-168
STI, see shallow trench isolation
Stick diagram, 422
Storage node, 397
Storage capacitance, 45-46
Storage time, 46-49
Streaming out, 36
Streets, see scribe, 209, 211
Strong inversion, 133
Student projects, 329
Substrate, 31
Substrate pump, 547
Subthreshold,
current, 149, 278
current source/sink, 635
g_m, 292-293
output resistance, 278
slope, 150
transconductance, 292
Switch logic, 369-370
Switched capacitor circuits, 492-494, 843-853
capacitor layout, 851-852

Switched capacitor circuits (continued),
filter, 848-849
integrator, 845-848
resistor, 488-489, 843-848
slew-rate requirements, 862
Switches, 311-317, 829-834
Symmetry, 618
Synchronization, 383, 551, 591, 596
Systematic offsets, 775

T

Tail current, 712, 720-722, 798, 803, 865, 868, 873, 882, 894, 898, 903-904, 907, 920-923
Technology computer assisted design (TCAD), 179
Telescopic diff-amp, see Cascode diff-amp
Temperature coefficient,
bandgap references, 761-770
diode, 759
diode self-biasing, 761-762
MOSFET-only, 633-635
MOSFET voltage divider, 749-750
positive, 106-107
resistors, 88, 105-107
resistor-MOSFET divider, 631-632, 746-749
thermal voltage self-biasing, 762-765
threshold voltage, 293-296, 750
transconductance multiplier, 634-635, 754-755
Temp co, see Temperature coefficient
Temperature effects,
bandgap of silicon, 293
capacitor, 116
KP (transconductance parameter), 295, 633
MOSFETs, 293-296
thermal voltage, 294
threshold voltage, 293-296
TG (transmission gate), 324, 375, 829-832
THD, see Total harmonic distortion
Thermal (white) noise, 225-229
Thermal oxidation, 34, 161, 163-164, 182, 184, 190, 192, 211
Thermal voltage, V_T (kT/q), 39, 758
change with temperature, 294
Thermometer code, 965-966, 974-975, 985-986, 988, 992
Threshold voltage, 135-140, 276, 467
adjusting, 140, 190-192
determining, 293
matching, 616
NMOS, 292, 300
PMOS, 292, 300
temperature behavior, 293-296
Timing errors, 583
Total harmonic distortion, 704-706
t_{ox}, 86-87, 114, 292, 300
.Tran statement, 15-16, 286
Transient SPICE analysis, 48, 52, 66-67, 79, 286, 705-706
Transconductance, 280, 297
parameter, β, 142
variation with frequency, 695
Transconductance amplifier, 796-798, 835-836
Transimpedance amplifier, 249-250, 261, 267, 666-667, 688-689, 1145-1148
Transmission channel, 538-541
Transmission gate, 324, 375, 402
applications, 378
delay through, 376
layout, 415
series connection, 377
static gates, 379
Transit time, 45-47
Transition frequency, f_T, 290-292, 297-302, 309, 316, 863, 903, 906
Tri-state outputs, 351, 370
buffer, 372-373
phase detector output, 559
Trimming, 476, 753-755, 766, 769-770, 1007
Triode region, 141, 271, 278
channel resistance, 278
t_{rr}, see diode, reverse recovery time
True-single phase clocked logic (TSPC), 409-410
t_s, see Diode, storage time
TSPC, see true-single phase clocked logic
τ_T, see Diode, minority carrier lifetime
Tub, 52
Tunneling,
Fowler-Nordheim, 469-470, 487
gate current (direct), 153-154, 220, 242, 300, 403, 468-476, 1146-1148
zener diode, 253
Two's complement, 965-966
Twin well, 31, 52-55
(well) module, 187-190

U

UIC (SPICE use intital conditions), 24-25, 28
Unbalanced input signals, 894-895
Unity-gain frequency, see f_{un} op-amp unity-gain frequency
Unit processes, 161-177

V

V_{CM}, see common-mode voltage
VCO, see voltage controlled oscillator
$V_{DS,sat}$, 144-145, 271
Velocity,
carriers, 106-107, 142, 151, 153
overshoot, 151, 153, 297, 302
saturation, 151, 291, 299, 634
speed of light, 65
VLSI, 1, 411
VNTOL, 27

Voltage coefficient, 107, 116
Voltage-controlled oscillator (VCO), 552, 561, 595
  characteristics, 561
  current starved, 561
  for use with the PFD, 561
  logic based, 567
  source coupled, 565
  use with XOR phase detector, 557
Voltage dividers, 746-756
Voltage follower, 1143
Voltage generators (charge pumps), 542-548
  example, 547-549
  higher voltages (Dickson), 544-545
Voltage references, 745-772
Voltage regulator, 812-819
V_{ov}, see Overdrive voltage
V_T, see Thermal voltage, kT/q
VTC, see Inverter, transfer characteristics
V_{THN}, see Threshold voltage, NMOS
V_{THP}, see Threshold voltage, PMOS

W

Wafer, 3, 32, 161, 180
  manufacture, 161-163
  probe, 208-211
  production, 162
Waterfowl, 242
W_{drawn}, see drawn width
Weak inversion, 132-133, 149-150, 301
Well, 31-58, 53
  contact, 96
  triple, 53, 187, 278
White noise, 219-221, 225, 240-242, 253-254
Wide swing diff-amp, 736-740
Workfunction,
  gates, 191, 304
W-2W current mirror, 1043-1044

X

X_d, 136-137
X_{dl}, 144
XOR gate, 366, 380
  phase detector, 553, 555-556

Y

Yield, 152, 209, 412

Z

Zener diode, 253-254, 268
Zero-nulling resistor, 685, 774-782
Zipper Logic, 407